

3-Phase Brushless Motor Pre-driver

BD63002AMUV

General Description

BD63002AMUV is pre-driver of 3-phase brushless motor. It generates a driving signal from the Hall sensor and drives PWM through the input control signal. Since there is a built-in booster circuit, Nch-Nch MOS transistors can be used on the external power transistor. In addition, the power supply can use 12V or 24V and it has various controls and protection functions built-in, making it useful for a variety of purposes. Because it adopts small packages, it can also be used on small diameter motors.

Features

- Built-in 120° Commutation Logic Circuit
- Driving with Nch-Nch MOS Transistors
- PWM Control Mode (Low Side Arm Switching)
- Built-in Power-saving Circuit
- Direction of Rotation Change Function
- Short Brake Function
- FG Output (Open drain)
- Built-in Protection Circuit for Current Limit, Thermal Shutdown, Under Voltage Lockout, Over Voltage Lockout, Motor Lock Protection

Applications

- OA Machines
- Other General Civil Equipment

Key Specifications

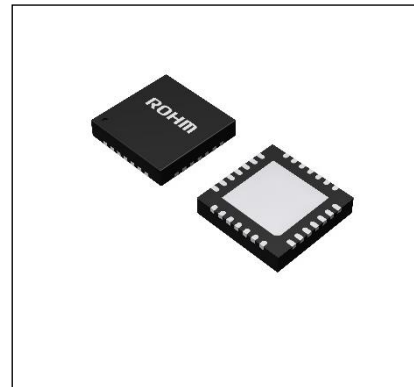
| | |
|--|-----------------------------|
| ■ Power Supply Voltage Rating | 33V |
| ■ Operating Temperature Range | -40°C to +85°C |
| ■ Stand-by Current | 1.2mA(Max) |
| ■ Range of In-phase Input Voltage for Hall Input | V _{REG} -1.7V(Max) |
| ■ Current Limit Detect Voltage | 0.2V±10% |
| ■ UVLO Lockout Voltage | 6.0V(Typ) |
| ■ OVLO Lockout Voltage 1 | 16.0V(Typ) |
| ■ OVLO Lockout Voltage 2 | 28.5V(Typ) |

Package

VQFN028V5050

W(Typ) x D(Typ) x H(Max)

5.00mm x 5.00mm x 1.00mm



VQFN028V5050

Typical Application Circuit

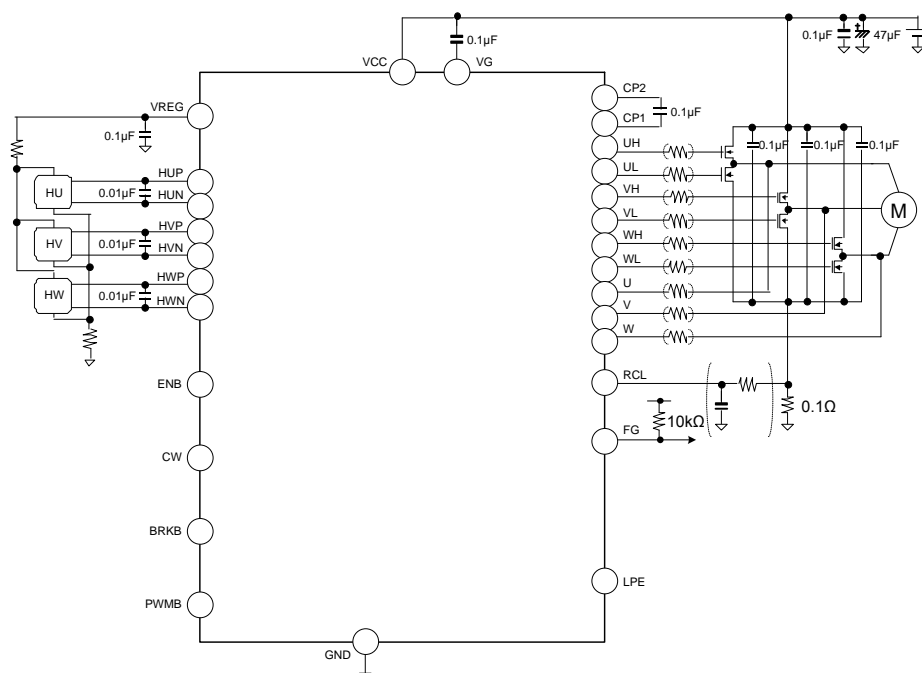


Figure 1. Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

Pin Configuration

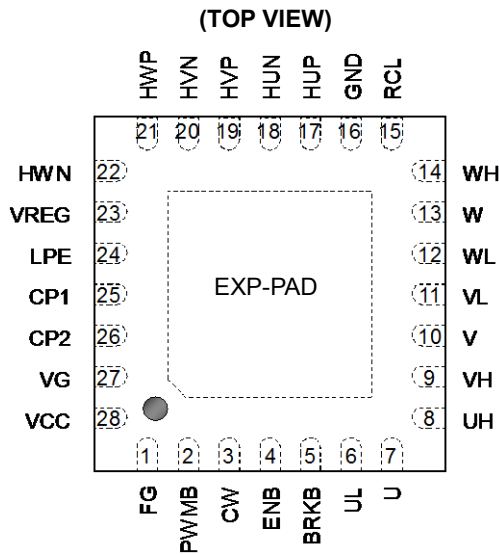


Figure 2. Pin Configuration

Block Diagram

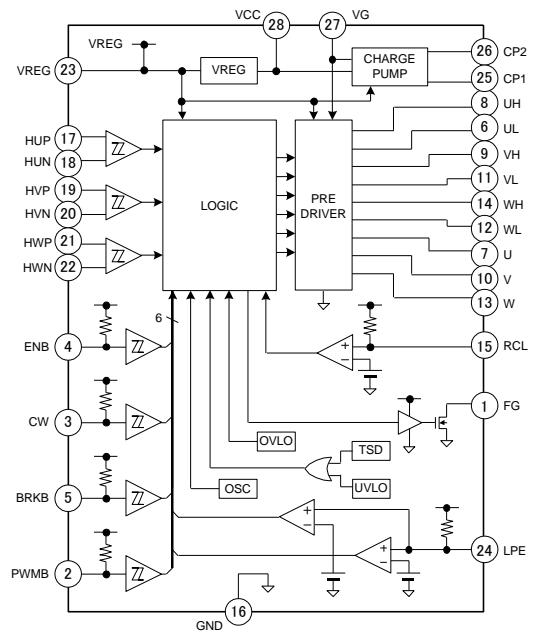


Figure 3. Block Diagram

Pin Description

| Pin No. | Pin Name | Function | Pin No. | Pin Name | Function |
|---------|----------|---|---------|----------|--|
| 1 | FG | FG output | 15 | RCL | Detect voltage input for over current |
| 2 | PWMB | PWM input (negative logic) | 16 | GND | GND |
| 3 | CW | Changing Direction of rotation (H: CW, L: CCW) | 17 | HUP | U phase Hall input+ |
| 4 | ENB | Enable (negative logic) | 18 | HUN | U phase Hall input- |
| 5 | BRKB | Brake input (negative logic) | 19 | HVP | V phase Hall input+ |
| 6 | UL | U phase lower output | 20 | HVN | V phase Hall input- |
| 7 | U | U phase output feedback | 21 | HWP | W phase Hall input+ |
| 8 | UH | U phase upper output | 22 | HWN | W phase Hall input- |
| 9 | VH | V phase upper output | 23 | VREG | VREG output (turn off at stand-by) |
| 10 | V | V phase output feedback | 24 | LPE | Setting about motor lock protection and OVLO (H/M/L input) |
| 11 | VL | V phase lower output | 25 | CP1 | Charge pump setting 1 |
| 12 | WL | W phase lower output | 26 | CP2 | Charge pump setting 2 |
| 13 | W | W phase output feedback | 27 | VG | Charge pump output |
| 14 | WH | W phase upper output | 28 | VCC | Power supply |
| - | EXP-PAD | The EXP-PAD of the center of product connects to GND. | | | |

Description of Operation

Commutation logic (120° commutation)

Truth table

| HU | HV | HW | CW (CW=H or OPEN) | | | | | | FG |
|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|-----|-------------------------|------|
| | | | UH | UL | VH | VL | WH | WL | |
| H | L | H | PWM | PWM ^(Note 1) | H | L | L | L | L |
| H | L | L | $\overline{\text{PWM}}$ | PWM ^(Note 1) | L | L | H | L | L |
| H | H | L | L | L | $\overline{\text{PWM}}$ | PWM ^(Note 1) | H | L | L |
| L | H | L | H | L | $\overline{\text{PWM}}$ | PWM ^(Note 1) | L | L | Hi-z |
| L | H | H | H | L | L | L | PWM | PWM ^(Note 1) | Hi-z |
| L | L | H | L | L | H | L | PWM | PWM ^(Note 1) | Hi-z |
| H | H | H | L | L | L | L | L | L | L |
| L | L | L | L | L | L | L | L | L | Hi-z |

| HU | HV | HW | CCW (CW=L) | | | | | | FG |
|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
| | | | UH | UL | VH | VL | WH | WL | |
| H | L | H | H | L | PWM | PWM ^(Note 1) | L | L | L |
| H | L | L | H | L | L | L | $\overline{\text{PWM}}$ | PWM ^(Note 1) | L |
| H | H | L | L | L | H | L | $\overline{\text{PWM}}$ | PWM ^(Note 1) | L |
| L | H | L | $\overline{\text{PWM}}$ | PWM ^(Note 1) | H | L | L | L | Hi-z |
| L | H | H | $\overline{\text{PWM}}$ | PWM ^(Note 1) | L | L | H | L | Hi-z |
| L | L | H | L | L | $\overline{\text{PWM}}$ | PWM ^(Note 1) | H | L | Hi-z |
| H | H | H | L | L | L | L | L | L | L |
| L | L | L | L | L | L | L | L | L | Hi-z |

(Note 1) When PWMB=L, PWM="H". When PWMB=H, PWM="L"

Enable input pin (ENB)

Output of each phase can be set to ON/OFF (negative logic) through the ENB pin. When applied voltage is V_{ENB} or less, the motor is driven (enable). When applied voltage is V_{STBY} or more or the ENB pin is open, the motor stops (stand-by). Stand-by mode has precedence to other control input signal, VREG output will be OFF. In addition, the ENB pin is pulled up by internal power supply through a resistance of 100kΩ(Typ)±30kΩ.

| ENB | Operation |
|-----------|-----------|
| H or OPEN | Stand-by |
| L | Enable |

PWM input pin (PWMB)

Speed can be controlled by inputting PWM signal into the PWMB pin (negative logic). Synchronous rectifier PWM can be realized through lower switching. When PWMB="L", lower output that belongs to Hall input logic is "H". When PWMB="H" or OPEN, lower output is "L". When PWMB="H" or OPEN status is detected 104μs(Typ), the synchronous rectifier will be OFF. Synchronous rectifier will be ON through falling edges of subsequent PWMB. Additionally, the PWMB pin is pulled up by VREG through a resistance of 100kΩ(Typ)±30kΩ.

| PWMB | Low side output |
|-----------|-----------------|
| H or OPEN | L |
| L | H |

Description of Operation – continued

Brake input pin (BRKB)

Motor rotation can be quickly stopped by the BRKB pin (negative logic). When BRKB="L", lower output become all "H" and operates short brake "H". When BRKB="H" or OPEN, then short brake operation will be released. What is more, the BRKB pin is pulled up by VREG through a resistance of $100\text{k}\Omega(\text{Typ})\pm 30\text{k}\Omega$.

| BRKB | Operation |
|-----------|-------------|
| H or OPEN | Normal |
| L | Short brake |

CW/CCW input pin (CW)

Rotation direction can be switched with the CW pin. When CW="H" or OPEN, the direction is CW. When CW="L", the direction will be CCW. Though we do not recommend switching rotation direction when motor is rotating. If rotation direction is switched when rotating, after the short brake operation until the hall frequency is 40Hz or less, the direction of rotation is switched. And the CW pin is pulled up by VREG through a resistance of $100\text{k}\Omega(\text{Typ})\pm 30\text{k}\Omega$.

| CW | Direction |
|-----------|-----------|
| H or OPEN | CW |
| L | CCW |

FG output

FG output is shaped Hall U phase signal and output through the FG pin. It is not output in stand-by mode. In addition, because the FG pin is output from open drain, use resistance of about $10\text{k}\Omega$ to $100\text{k}\Omega$ to pulled up from outside.

Hall input

Hall input amplifier is designed with hysteresis ($\pm 15\text{mV}(\text{Typ})$) in order to prevent incorrect action due to noise inside. So set bias current for Hall element to make amplitude of Hall input voltage of minimum input voltage (V_{HALLMIN}) or more. Here, we recommend you to connect the ceramic capacitor with about 100pF to $0.01\mu\text{F}$ between differential input pins of Hall amplifier. What is more, because the in-phase input voltage range (V_{HALLCM} , 0V to $V_{\text{REG}}-1.7\text{V}(\text{Typ})$) is designed for Hall input amplifier, so when bias to Hall element, set within this range. When all Hall inputs become "H" or "L", all driver outputs will be "L" by the hall input abnormal detection circuit.

Booster circuit

There is built-in booster circuit used to drive upper Nch MOS transistor. The VG pins can produce a boost voltage (the VCC voltage + $7\text{V}(\text{Typ})$) through connecting capacitors between CP1-CP2 and between VG-VCC. We recommend connected condensers to be $0.1\mu\text{F}$ or more. In addition, because there is built-in protection circuit for insufficient booster, when VG voltage is $V_{\text{GUVON}} (V_{\text{CC}}+4\text{V} (\text{Typ}))$ or less, all driver outputs will be "L".

Current limit circuit (CL circuit)

Output current limit (Current Limit: CL) circuit can be formed by connecting a low resistor used for detecting current between the RCL pin and the GND pin. When RCL voltage is detected $0.2\text{V}(\text{Typ})$ or more, all lower output will be "L". It returns by itself after a set amount of time ($32\mu\text{s}(\text{Typ})$). This operation does not synchronize with the operation that PWM signal is input into the PWMB pin. In addition, in order to avoid misdetection of output current due to RCL noise, the IC sets up the noise-masking period ($1\mu\text{s}$ to $2\mu\text{s}(\text{Typ})$). During noise-masking period, the current detection is disabled.

Thermal Shutdown circuit (TSD circuit)

When chip temperature of driver IC rises and exceeds the set temperature ($175^\circ\text{C}(\text{Typ})$), the thermal Shutdown circuit (Thermal Shutdown: TSD) begins working. At this time, all driver outputs will be "L". In addition, the TSD circuit is designed with hysteresis ($25^\circ\text{C}(\text{Typ})$), therefore, when the chip temperature drops, it will return to normal working condition. Moreover, the purpose of the TSD circuit is to protect driver IC from thermal breakdown, therefore, temperature of this circuit will be over working temperature when it is started up. Thus, thermal design should have sufficient margin, so do not take continuous use and operation of the circuit as precondition.

Under voltage lockout circuit (UVLO circuit)

There is a built-in under voltage lockout circuit (Under Voltage Lockout: UVLO circuit) used to ensure the lowest power supply voltage for drive IC to work and to prevent error operation of IC. When VCC voltage declined to $V_{\text{UVL}} (6\text{V} (\text{Typ}))$, all of the driver outputs should be "L". At the same time, UVLO circuit is designed with hysteresis ($1\text{V}(\text{Typ})$), so when VCC voltage reaches $V_{\text{UVH}} (7\text{V}(\text{Typ}))$ or more, it will enter normal working condition.

Description of Operation – continued

Over voltage lockout circuit (OVLO circuit)

There is built-in over voltage lockout circuit (Over Voltage Lockout: OVLO circuit) used to restrain rise of VCC voltage when motor decelerating. When the LPE pin is at "M" and VCC voltage is V_{OVH1} (16V(Typ)) or more, and when the LPE pin is at "H" or "M" and VCC voltage is V_{OVH2} (28.5V(Typ)) or more, a certain time (4ms(Typ)) of short brake action will be conducted. What is more, because OVLO circuit is designed with hysteresis (1V(Typ)), therefore, when V_{OVH1} is V_{OVL1} (15V(Typ)) or less and when V_{OVH2} is V_{OVL2} (27.5V(Typ)) or less, it can return to normal working condition after a certain time of short brake action.

Motor Lock Protection circuit (MLP circuit)

There is built-in motor lock protection circuit (Motor Lock Protection: MLP), ON/OFF of MLP circuit and OVLO threshold can be set by the LPE pin. Monitor Hall signals, when the LPE = "H" or "M", if Hall signal logic does not change 1.1s(Typ) or more, driver outputs will all be latched as "L". Latch can be released via standby status or through switching BRKB/CW logic. Moreover, when PWMB = "H" or OPEN state is detected for about 15ms, latch can be released by falling edges of subsequent PWMB. However, in case of LPE = "L", and when short brake action (including switching rotation direction) enables or TSD circuit works, MLP circuit does not work. And the LPE pin is pulled up by VREG through a resistance of $30k\Omega(Typ)\pm 9k\Omega$.

| LPE | Monitoring time | OVLO threshold |
|-----------|----------------------|-------------------------|
| H or OPEN | 1.1s(Typ) $\pm 30\%$ | V_{OVH2} , V_{OVL2} |
| M | 1.1s(Typ) $\pm 30\%$ | V_{OVH1} , V_{OVL1} |
| L | Disable | V_{OVH2} , V_{OVL2} |

Pre-driver output

Driving signal is output to external output power transistor through drive signal generated from internal logic. Driving voltage of upper gate is VG voltage ($V_{CC}+7V(Typ)$) and driving voltage of lower gate is VREG voltage (5V(Typ)). In addition, a dead time ($1\mu s(Typ)\pm 30\%$) is designed between driving signals of upper gate and lower gate in order to prevent upper and lower FET from being set to ON synchronously when PWM is rectified synchronously. Due to the influence of the motor's counter electromotive force, the output feedback pin (U, V, W) might swing under GND potential. By this swing, malfunctions and destruction can be caused by application. When negative potential exceeds -1.5V (Typ), 510 Ω or less of resistance can be inserted to prevent malfunction and destruction.

Control signal sequence

Though we recommend you input control signals of the ENB, CW, PWMB, BRKB and LPE pins after inputting VCC, if input control signals before inputting VCC, there won't be any problem. If the LPE pin is set to "H" or "M" when being started, be informed that if motor rotation cannot be detected (edge of FG signal cannot be input) within the set time, then the MLP circuit starts and motor fails to start. Moreover, the order of priority is set to control signal and IC internal signal. Refer to the following table.

Priority of control signal

| Priority | Input / Internal signals |
|-----------------|--|
| 1 st | ENB, UVLO |
| 2 nd | BRKB $\uparrow\downarrow$ (Note 2), CW $\uparrow\downarrow$ (Note 2), PWMB \downarrow (Note 2) |
| 3 rd | TSD, MLP, HALLERR |
| 4 th | OVLO |
| 5 th | VG_UVLO |
| 6 th | BRKB |
| 7 th | CL |
| 8 th | PWMB, CW |

(Note 2) $\uparrow\downarrow$ means rising and falling edges of signal.
For signal name, see [State Transition Diagram](#).

Description of Operation – continued

IC back metal

The back side metal is shorted with IC chip's back side and becomes the GND potential, so there is the danger of malfunction and destruction if shorted with potentials other than GND. Therefore, please absolutely do not design patterns other than GND through the IC's back side.

Operation Under Strong Electromagnetic Field

The IC is not designed for using in the presence of strong electromagnetic field. Be sure to confirm that no malfunction is found when using the IC in a strong electromagnetic field.

Absolute Maximum Ratings (Ta=25°C)

| Item | Symbol | Limit | Unit |
|---|---------------------------|-----------------------------------|------|
| Power Supply Voltage | V _{CC} | -0.3 to +33.0 ^(Note 3) | V |
| VG Voltage | V _G | -0.3 to +38.0 ^(Note 4) | V |
| Output Voltage of Pre-driver | V _(UH, VH, WH) | -0.3 to +38.0 | V |
| | V _(UL, VL, WL) | -0.3 to +7.0 | V |
| FG Voltage | V _{FG} | -0.3 to +7.0 | V |
| RCL Voltage | V _{RCL} | -0.3 to +5.5 | V |
| Voltage of Input of Control and Hall pins | V _{I/O} | -0.3 to +5.5 | V |
| Output Current of Pre-driver(DC) | I _{OMAX(OUT)} | ±15 ^(Note 4) | mA |
| FG Output Current | I _{FG} | 5 ^(Note 4) | mA |
| VREG Output Current | I _{VREG} | -30 ^(Note 4) | mA |
| Storage Temperature Range | T _{stg} | -55 to +150 | °C |
| Maximum Junction Temperature | T _{jmax} | 150 | °C |

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 3) Do not exceed T_{jmax}=150°C. VCC range is -0.3V to +30.0V, when the boost circuit is operating.

(Note 4) Do not exceed T_{jmax}=150°C.

Thermal Resistance^(Note 5)

| Parameter | Symbol | Thermal Resistance (Typ) | | Unit |
|--|---------------|--------------------------|--------------------------|------|
| | | 1s ^(Note 7) | 2s2p ^(Note 8) | |
| VQFN028V5050 | | | | |
| Junction to Ambient | θ_{JA} | 128.5 | 31.5 | °C/W |
| Junction to Top Characterization Parameter ^(Note 6) | Ψ_{JT} | 12 | 9 | °C/W |

(Note 5) Based on JESD51-2A(Still-Air).

(Note 6) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 7) Using a PCB board based on JESD51-3.

(Note 8) Using a PCB board based on JESD51-5, 7.

| Layer Number of Measurement Board | Material | Board Size |
|-----------------------------------|----------|----------------------------|
| Single | FR-4 | 114.3mm x 76.2mm x 1.57mmt |

| Top | |
|-----------------------|------------|
| Copper Pattern | Thickness |
| Footprints and Traces | 70 μ m |

| Layer Number of Measurement Board | Material | Board Size | Thermal Via ^(Note 9) | |
|-----------------------------------|----------|---------------------------|---------------------------------|---------------|
| | | | Pitch | Diameter |
| 4 Layers | FR-4 | 114.3mm x 76.2mm x 1.6mmt | 1.20mm | Φ 0.30mm |

| Top | | 2 Internal Layers | | Bottom | |
|-----------------------|------------|-------------------|------------|-----------------|------------|
| Copper Pattern | Thickness | Copper Pattern | Thickness | Copper Pattern | Thickness |
| Footprints and Traces | 70 μ m | 74.2mm x 74.2mm | 35 μ m | 74.2mm x 74.2mm | 70 μ m |

(Note 9) This thermal via connects with the copper pattern of all layers.

Recommended Operating Condition

| Item | Symbol | Range | | | Unit |
|-----------------------|------------------|-------|------|------|------|
| | | Min | Typ | Max | |
| Power Supply Voltage | V _{CC} | 8.0 | 24.0 | 26.4 | V |
| Operating Temperature | T _{opr} | -40 | +25 | +85 | °C |

Electrical Characteristic (Unless otherwise specified Ta=25°C, V_{CC}=24V)

| Item | Symbol | Limit | | | Unit | Condition |
|--|----------------------|------------------------|-----------------------|------------------------|-------|---------------------------------------|
| | | Min | Typ | Max | | |
| [Whole] | | | | | | |
| Circuit Current | I _{CC} | - | 2.5 | 5.0 | mA | V _{ENB} =0V |
| Stand-by Current | I _{STBY} | - | 0.6 | 1.2 | mA | ENB=OPEN |
| VREG Voltage | V _{REG} | 4.5 | 5.0 | 5.5 | V | I _{VREG} =-10mA |
| [Booster circuit] | | | | | | |
| VG Voltage | V _G | V _{CC} +6 | V _{CC} +7 | V _{CC} +8 | V | |
| VG UVLO Voltage | V _{GUVON} | V _{CC} +3 | V _{CC} +4 | V _{CC} +5 | V | |
| [Driver output] | | | | | | |
| High Side Output Voltage H | V _{OHH} | V _G -0.6 | V _G -0.2 | V _G | V | I _{HSOURCE} =-5mA |
| High Side Output Voltage L | V _{OHL} | 0 | 0.2 | 0.6 | V | I _{HSINK} =5mA |
| Low Side Output Voltage H | V _{OLH} | V _{REG} -0.4 | V _{REG} -0.2 | V _{REG} | V | I _{LSOURCE} =-5mA |
| Low Side Output Voltage L | V _{OLL} | 0 | 0.2 | 0.6 | V | I _{LSINK} =5mA |
| Source Current of High Side | I _{HSOURCE} | 100 | 130 | - | mA | I _{HSOURCE} pulse width ≤1μs |
| Sink Current of High Side | I _{HSINK} | 50 | 65 | - | mA | I _{HSINK} pulse width ≤1μs |
| Source Current of Low Side | I _{LSOURCE} | 50 | 65 | - | mA | I _{LSOURCE} pulse width ≤1μs |
| Sink Current of Low Side | I _{LSINK} | 100 | 130 | - | mA | I _{LSINK} pulse width ≤1μs |
| Dead Time | t _{DT} | 0.7 | 1.0 | 1.3 | μs | |
| [Hall input] | | | | | | |
| Input Bias Current | I _{HALL} | -2.0 | -0.1 | +2.0 | μA | V _{IN} =0V |
| Range of In-phase Input Voltage | V _{HALLCM} | 0 | - | V _{REG} -1.7 | V | |
| Minimum Input Voltage | V _{HALLMIN} | 50 | - | - | mVp-p | |
| HYS Level + | V _{HALLHY+} | 5 | 15 | 25 | mV | |
| HYS Level - | V _{HALLHY-} | -25 | -15 | -5 | mV | |
| [Input of control:ENB] | | | | | | |
| Input Current | I _{ENB} | -75 | -45 | -25 | μA | V _{ENB} =0V |
| Standby Voltage | V _{STBY} | 2.0 | - | 5.5 | V | |
| Enable Voltage | V _{ENB} | 0 | - | 0.8 | V | |
| [Input of control:PWMB, CW, BRKB] | | | | | | |
| Input Current | I _{IN} | -80 | -50 | -30 | μA | V _{IN} =0V |
| Input Voltage H | V _{INH} | 2.0 | - | 5.5 | V | |
| Input Voltage L | V _{INL} | 0 | - | 0.8 | V | |
| Minimum Input Pulse Width | t _{PLSMIN} | 1 | - | - | ms | CW, BRKB |
| Range of Input Frequency | f _{PWM} | 10 | - | 50 | kHz | PWMB |
| [Input of control:LPE] | | | | | | |
| Input Current | I _{LPE} | -267 | -167 | -100 | μA | V _{LPE} =0V |
| Input Voltage H | V _{LPH} | 0.8 x V _{REG} | - | V _{REG} | V | |
| Input Voltage M | V _{LPM} | 0.4 x V _{REG} | - | 0.6 x V _{REG} | V | |
| Input Voltage L | V _{LPL} | 0 | - | 0.2 x V _{REG} | V | |
| [FG output] | | | | | | |
| Output Voltage L | V _{FGOL} | 0 | 0.1 | 0.3 | V | I _{FG} =2mA |
| Leak Current | I _{FGLEAK} | - | 0 | 1 | μA | V _{FG} =5V |
| [Current limit] | | | | | | |
| Detect Voltage | V _{CL} | 0.18 | 0.20 | 0.22 | V | |
| Input Bias Current | I _{RCL} | -32 | -20 | -12 | μA | V _{RCL} =0V |
| Range of Input Voltage | V _{RCL} | -0.3 | - | +1.0 | V | |

Electrical Characteristic (Unless otherwise specified Ta=25°C, V_{CC}=24V) - continued

| Item | Symbol | Limit | | | Unit | Condition |
|-----------------------------------|-------------------|-------|------|------|------|----------------|
| | | Min | Typ | Max | | |
| [UVLO] | | | | | | |
| Release Voltage | V _{UVH} | 6.5 | 7.0 | 7.5 | V | |
| Lockout Voltage | V _{UVL} | 5.5 | 6.0 | 6.5 | V | |
| [OVLO] | | | | | | |
| Release Voltage1 | V _{OVL1} | 14.0 | 15.0 | 16.0 | V | LPE="M" |
| Lockout Voltage1 | V _{OVH1} | 15.0 | 16.0 | 17.0 | V | LPE="M" |
| Release Voltage2 | V _{OVL2} | 26.5 | 27.5 | 28.5 | V | LPE="H" or "L" |
| Lockout Voltage2 | V _{OVH2} | 27.5 | 28.5 | 29.5 | V | LPE="H" or "L" |
| [MLP] | | | | | | |
| Motor Lock Protection Detect Time | t _{LPE} | 0.77 | 1.10 | 1.43 | s | LPE="H" or "M" |

Reference Data ^(Note 10) (Unless otherwise specified V_{CC}=24V)

| Item | Symbol | Reference | | | Unit | Condition |
|------------------------|---------------------|-----------|-----|-----|------|---------------------------|
| | | Min | Typ | Max | | |
| [Current limit] | | | | | | |
| Mask Time | t _{CLMASK} | 0.7 | - | 2.6 | μs | Ta=25°C |
| [Protect] | | | | | | |
| TSD ON Temperature | T _{TSDON} | 150 | 175 | 200 | °C | Junction temperature (Tj) |
| TSD Hysteresis | T _{TSDHYS} | 15 | 25 | 35 | °C | Junction temperature (Tj) |

(Note 10) Not 100% tested.

Typical Performance Curves (Reference Data)

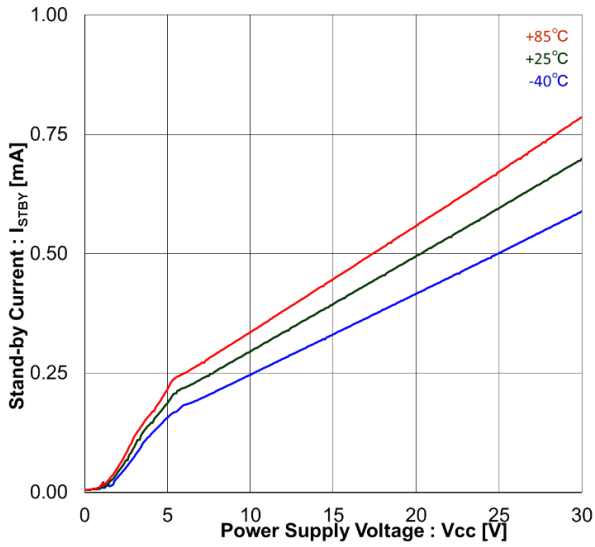


Figure 4. Stand-by Current vs Power Supply Voltage

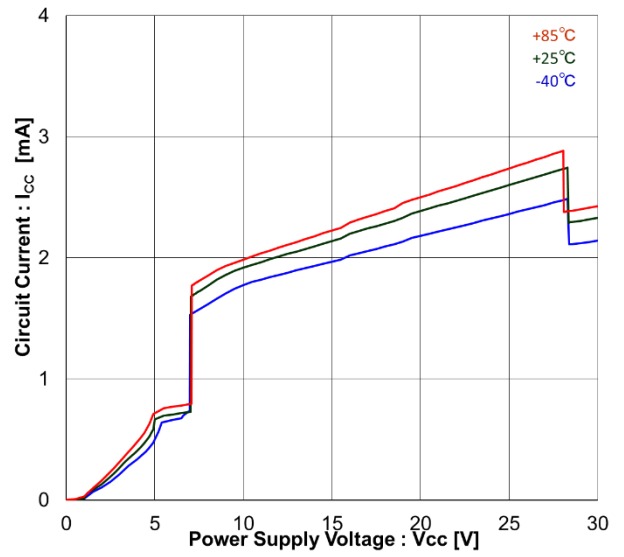


Figure 5. Circuit Current vs Power Supply Voltage

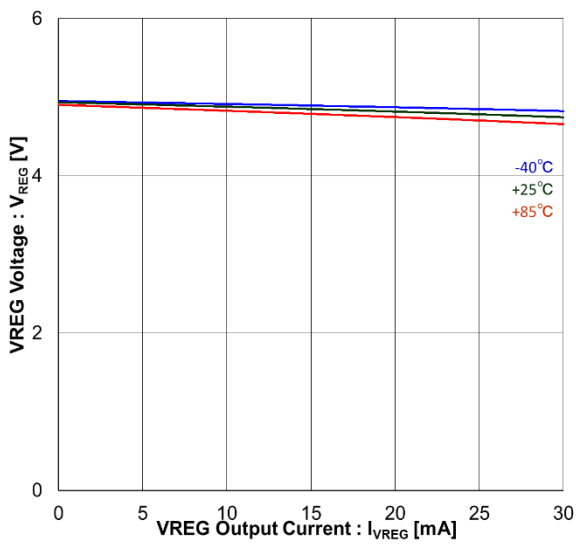


Figure 6. VREG Voltage vs VREG Output Current

Typical Performance Curves (Reference Data) – continued

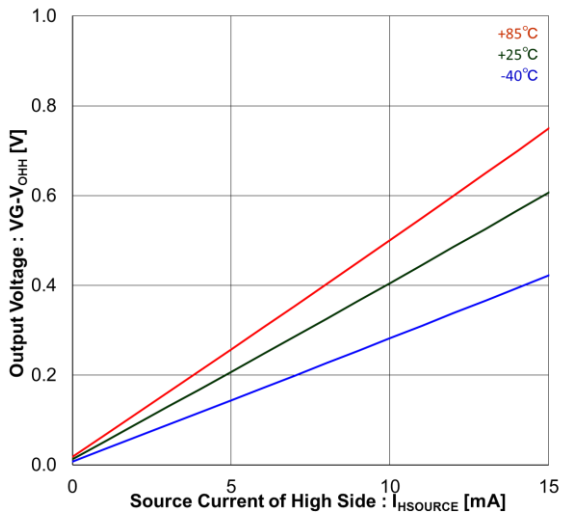


Figure 7. Output Voltage vs Source Current of High Side (High side Output voltage H)

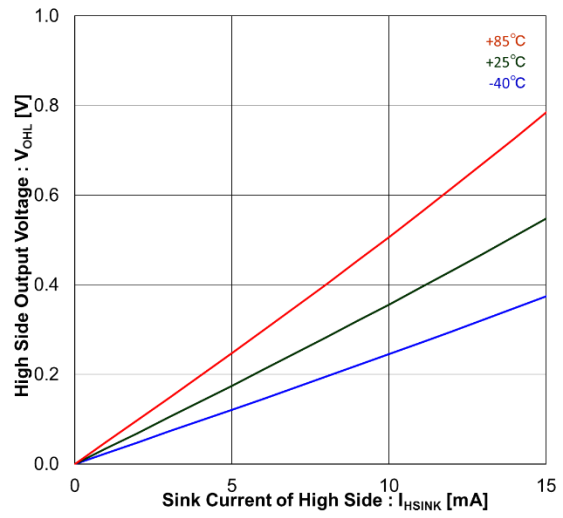


Figure 8. High Side Output Voltage L vs Sink Current of High Side (High side Output voltage L)

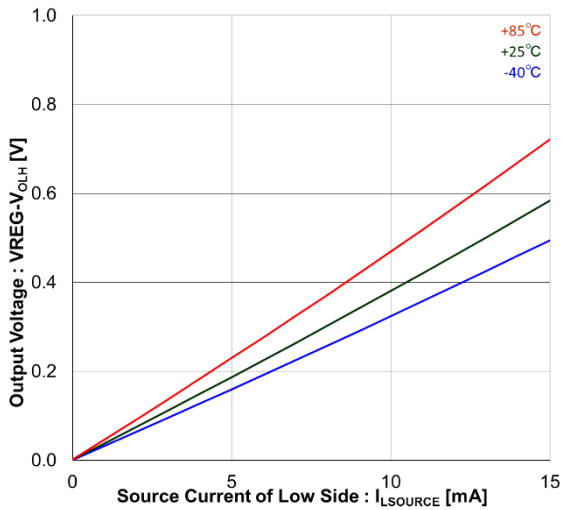


Figure 9. Output Voltage vs Source Current of Low Side (Low side Output voltage H)

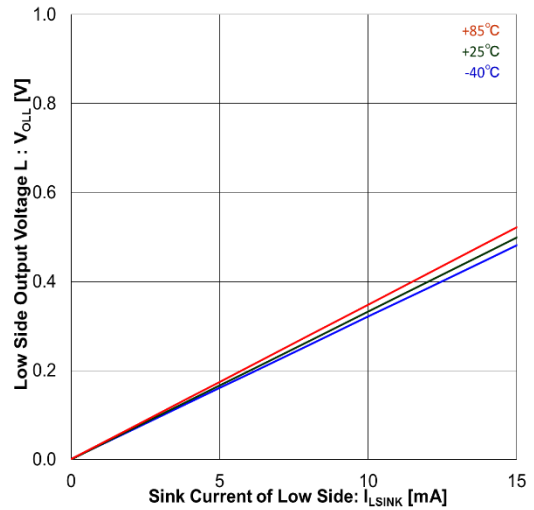


Figure 10. Low Side Output Voltage L vs Sink Current of Low Side (Low side Output voltage L)

Typical Performance Curves (Reference Data) – continued

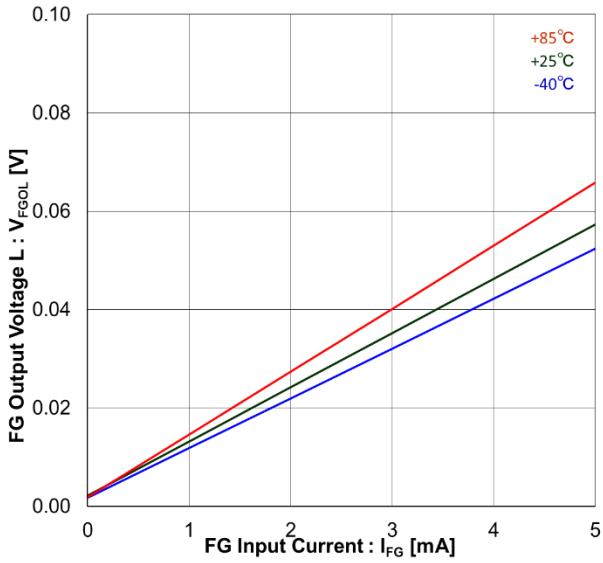


Figure 11. FG Output Voltage L vs FG Input Current

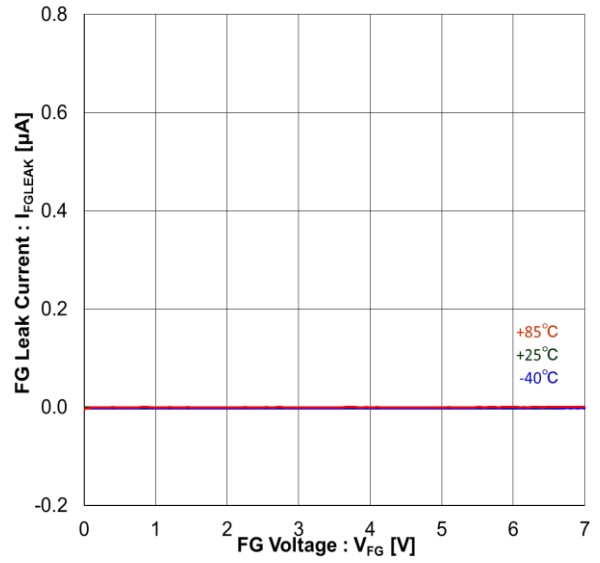


Figure 12. FG Leak Current vs FG Voltage

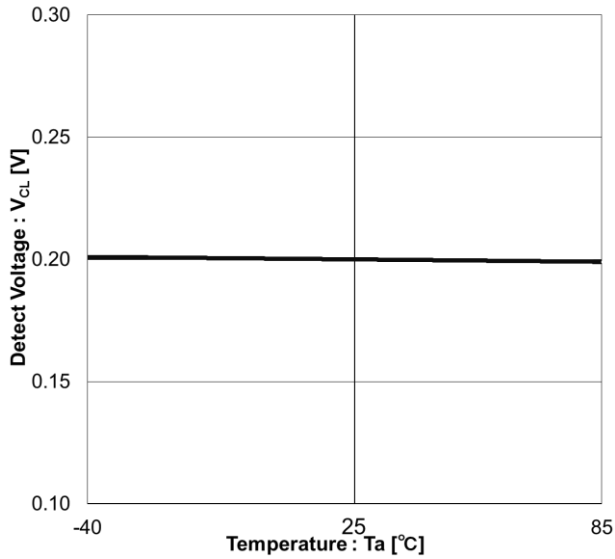


Figure 13. Detect Voltage vs Temperature

Typical Performance Curves (Reference Data) – continued

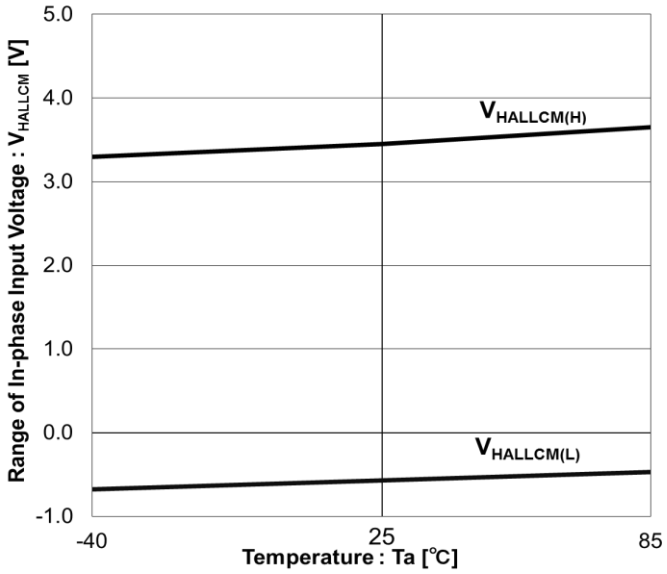


Figure 14. Range of In-phase Input Voltage vs Temperature

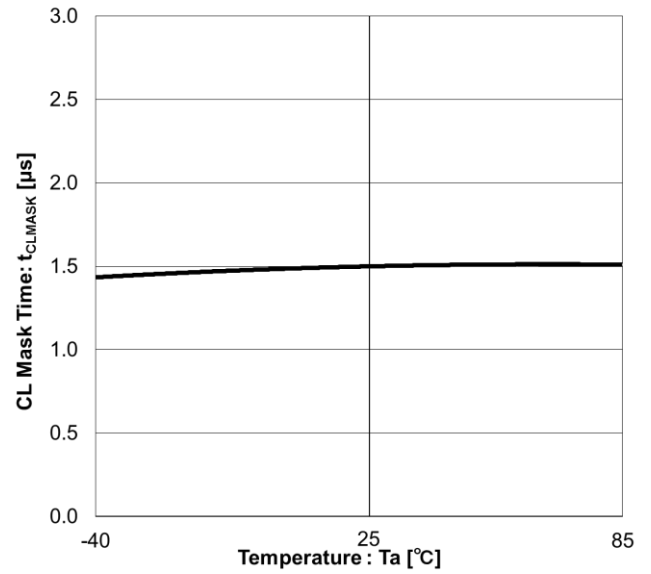


Figure 15. CL Mask Time vs Temperature

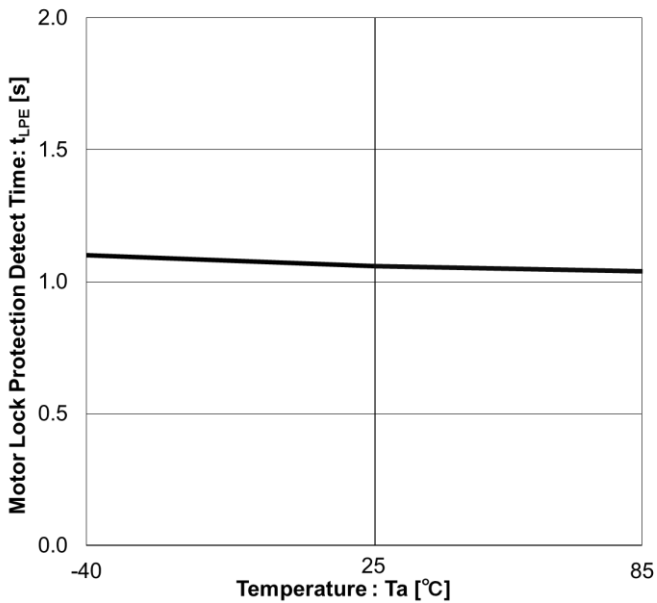
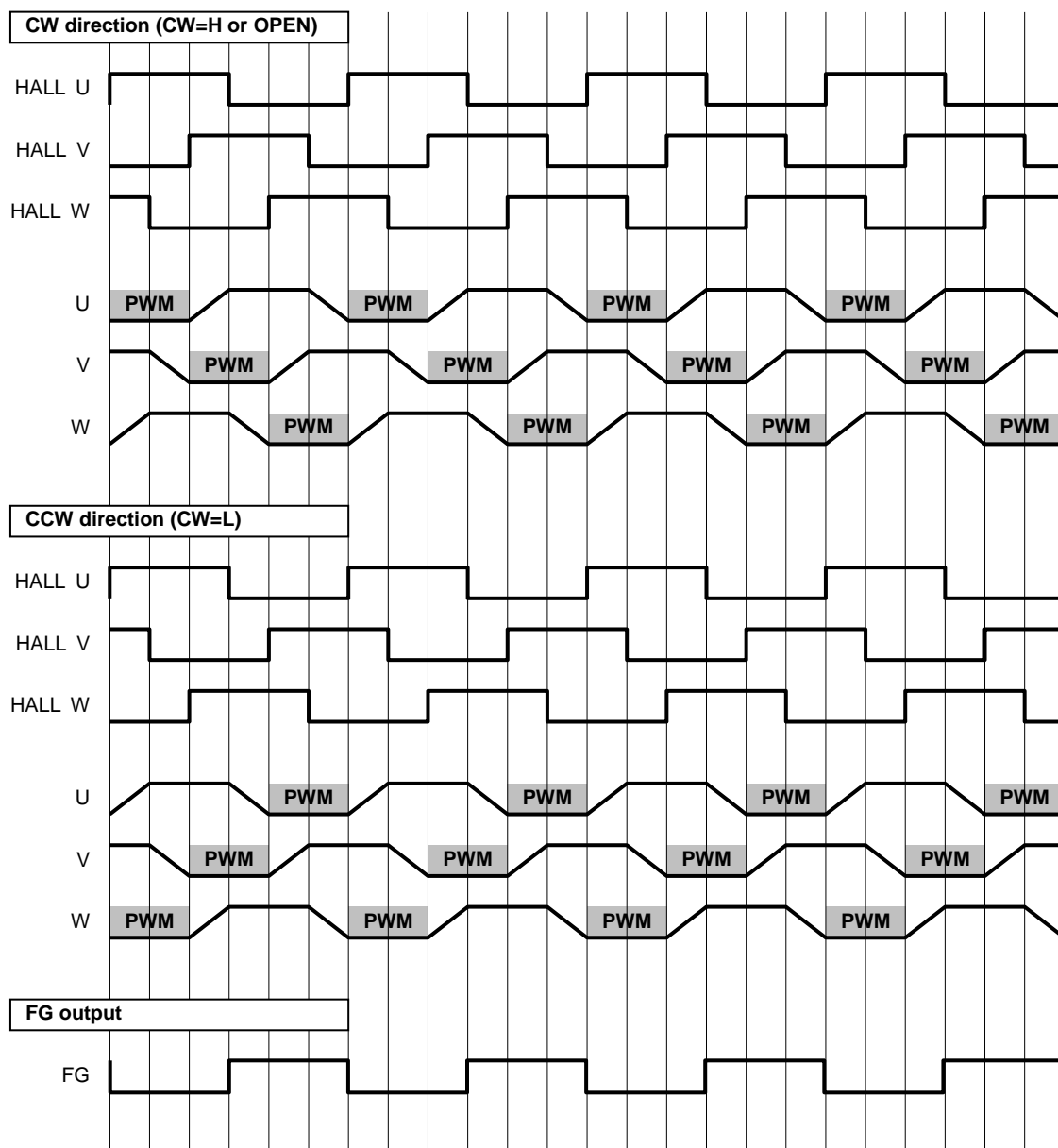
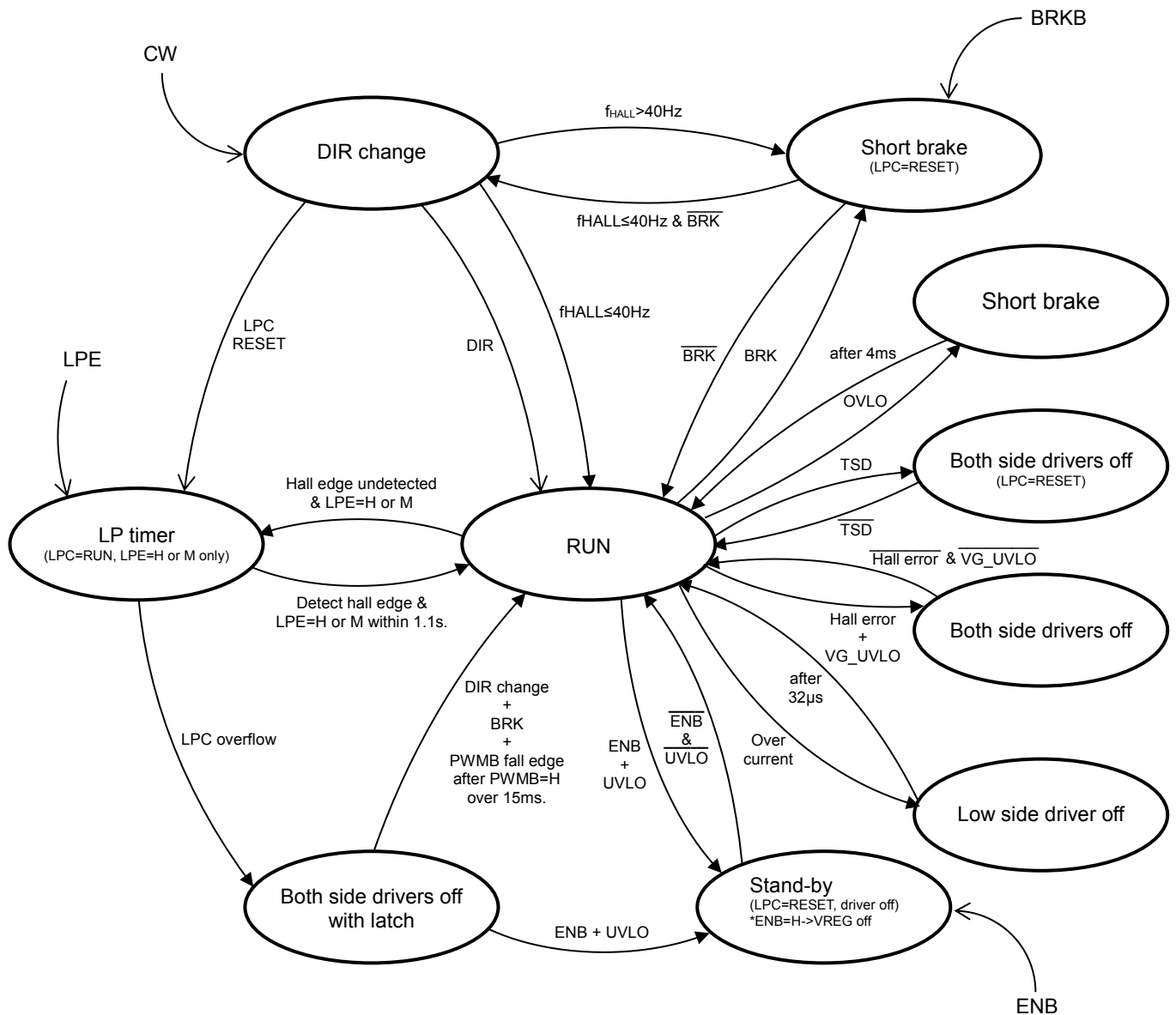


Figure 16. Motor Lock Protection Detect Time vs Temperature

Timing Chart



State Transition Diagram



Legend:

- DIR: motor rotational direction
- LP: motor lock protection
- LPC: internal counter for the motor lock protection (watch-dog timer)
- f_{HALL} : hall signal frequency
- Hall error: HU=HV=HW
- &: logical "AND"
- +: logical "OR"

- State transition
- Command signal

(Note) All values are typical.

I/O Equivalence Circuits

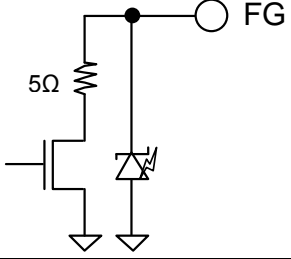
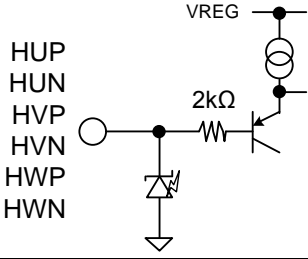
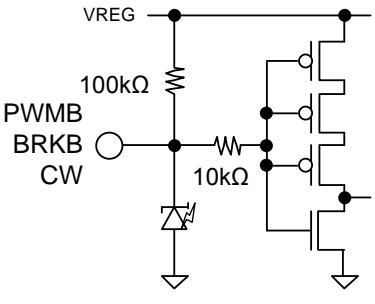
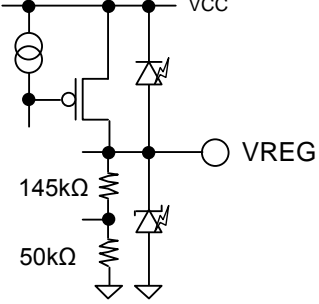
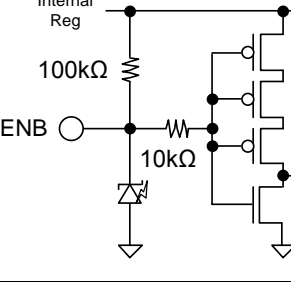
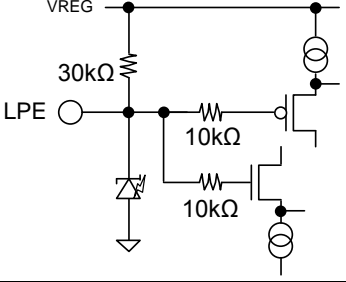
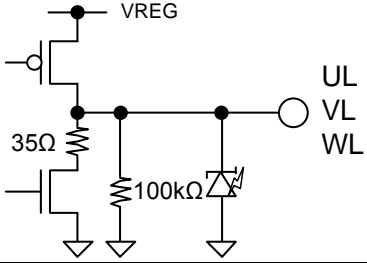
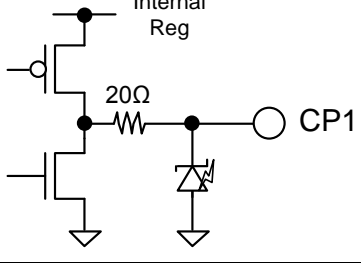
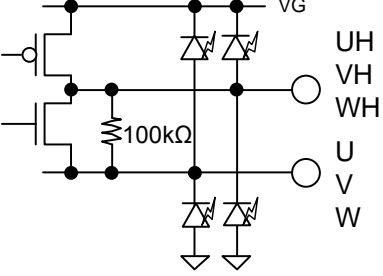
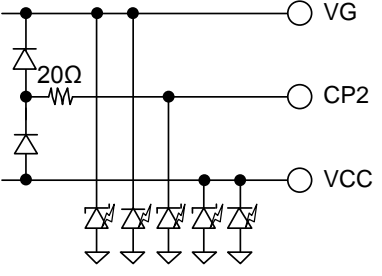
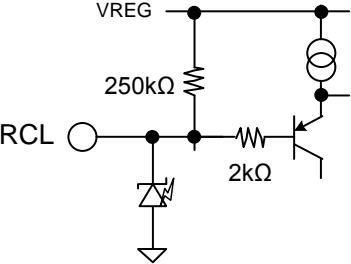
| | | | |
|--|---|--|---|
| <p>FG</p> |  | <p>HUP HUN HVP HVN HWP HWN</p> |  |
| <p>PWMB BRKB CW</p> |  | <p>VREG</p> |  |
| <p>ENB</p> |  | <p>LPE</p> |  |
| <p>UL VL WL</p> |  | <p>CP1</p> |  |
| <p>UH VH WH U V W</p> |  | <p>VG CP2 VCC</p> |  |
| <p>RCL</p> |  | | |

Figure 17. I/O Equivalence Circuits

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, U, V, W and RCL pin may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

9. **Inter-pin Short and Mounting Errors**

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. **Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

- When $GND > Pin\ A$ and $GND > Pin\ B$, the P-N junction operates as a parasitic diode.
- When $GND > Pin\ B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

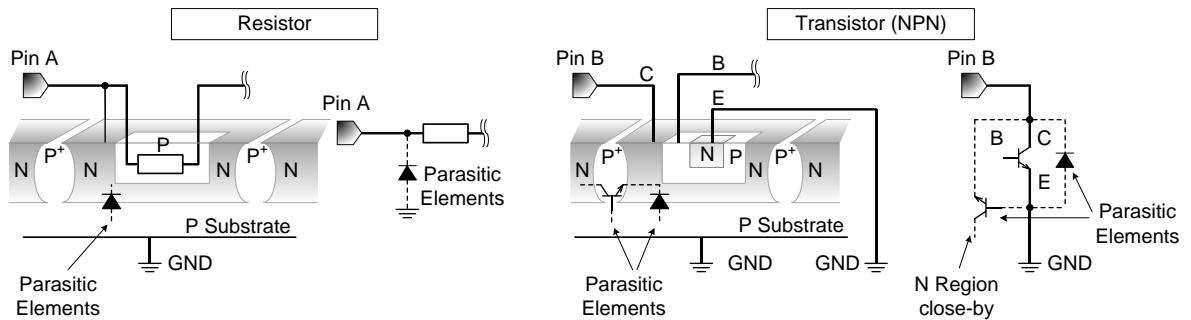


Figure 18. Example of Monolithic IC Structure

12. **Ceramic Capacitor**

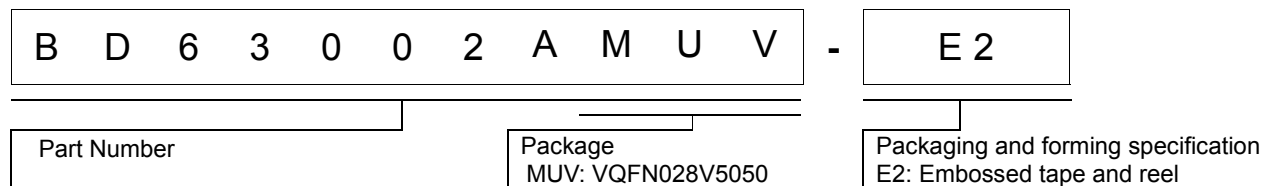
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. **Thermal Shutdown Circuit (TSD)**

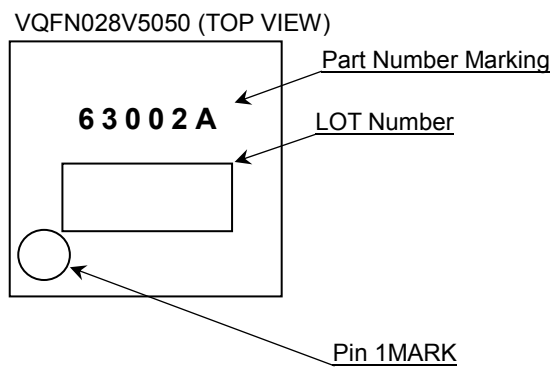
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

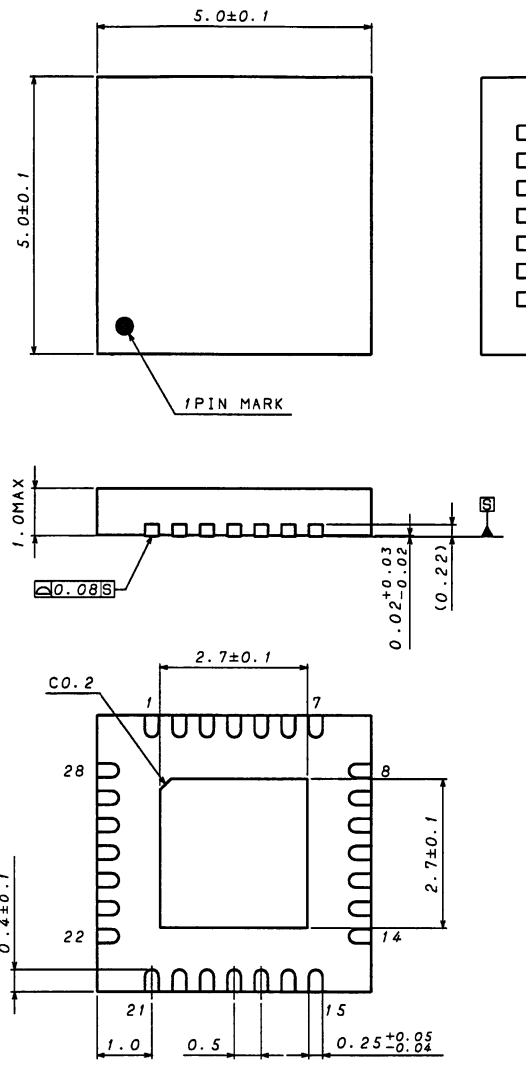


Marking Diagram



Physical Dimension and Packing Information

| | |
|--------------|--------------|
| Package Name | VQFN028V5050 |
|--------------|--------------|

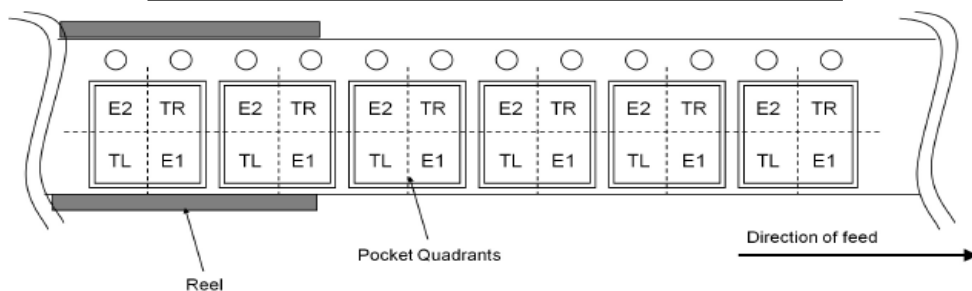


(UNIT: mm)

PKG: VQFN028V5050
Drawing No. EX473-5002-2

<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



Revision History

| Date | Revision | Changes |
|-------------|----------|-------------|
| 11.Jun.2018 | 001 | New Release |

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| CLASS IV | | CLASS III | |

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 - Use of the Products in places subject to dew condensation
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- Confirm that operation temperature is within the specified range described in the product specification.
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[LB11851FA-BH](#) [NCV70627DQ001R2G](#)