

# Three Phase Brushless Motor Driver

## BD63015EFV

### General Description

BD63015EFV is a three phase sinusoidal brushless motor driver. The rating of the power supply is 36V and that of current rating is 1.5A (peak current, 2A). PWM driving signals are generated by the three hall sensors. Input DC voltage signal can control the rotation speed, also, you can control by the power voltage. As the various control circuit and the protection circuit are built-in, this IC can fit the various applications. It can be used for the small diameter motor module because of the small package.

### Features

- Sinusoidal Drive
- Low ON Resistors DMOS Output (Pch / Nch)
- PWM Output
- FG Output (3FG)
- Built-in Current Limit Circuit (CL)
- Built-in Thermal Shut Down Circuit (TSD)
- Built-in Over Current Protection Circuit (OCP)
- Built-in Under Voltage Lock Out Circuit (UVLO)
- Built-in Over Voltage Lock Out Circuit (OVLO)
- Built-in Motor Lock Protection Circuit, Automatic Restart type (MLP)
- Built-in HALL error Protection Circuit (HALLERR)

### Applications

- Various types of Air Conditioning Fan Motor (FAN, Exhaust FAN, Air Cleaner FAN etc.)
- Various types of Cooler Fan Motor

### Typical Application Circuit

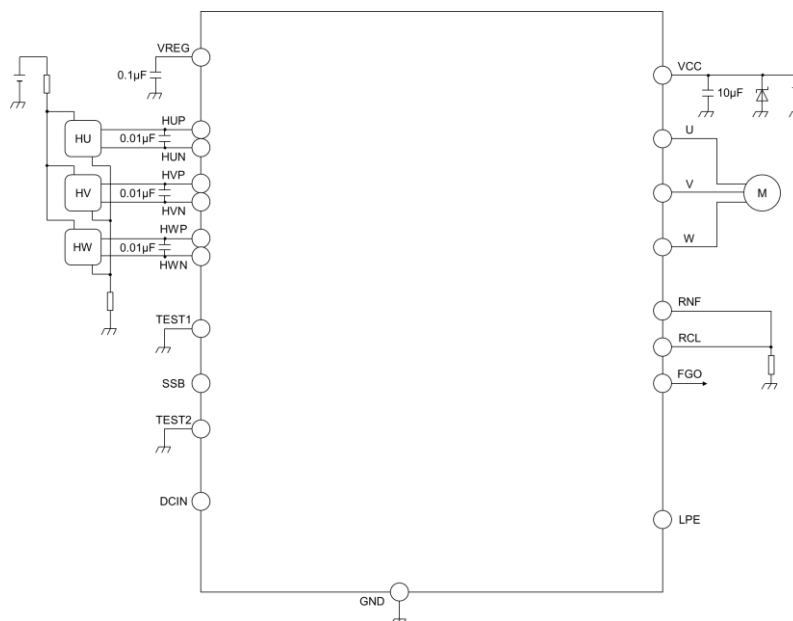


Figure 1. Application Circuit

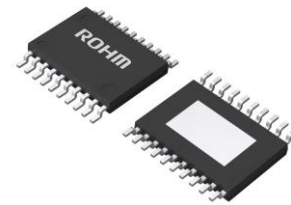
### Key Specifications

- Power Supply Voltage Rating: 36V
  - Output Continuous Current Rating: 1.5A
  - Output Peak Current Rating: 2A (Note 1)
  - Operating Temperature Range: -40°C to +105°C
  - Current Limit Detect Voltage: 0.2V±10%
  - Output ON Resistors (Total): 0.6Ω(Typ)
  - UVLO Voltage: 6V(Typ)
- (Note 1) Pulse width  $t_{ws} \leq 1\text{ms}$ , duty=20% pulse)

### Package

HTSSOP-B20

W(Typ) x D(Typ) x H(Max)  
6.50mm x 6.40mm x 1.00mm



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Pin Configuration

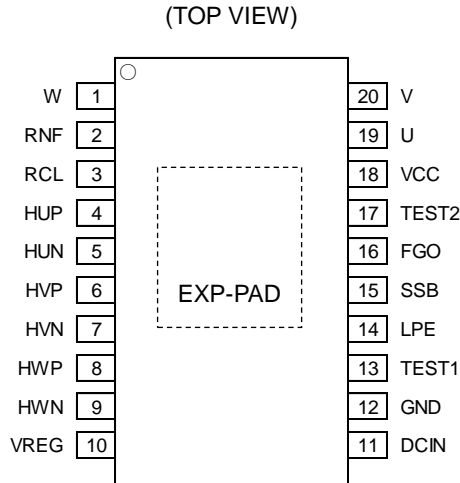


Figure 2. Pin Configuration

Block Diagram

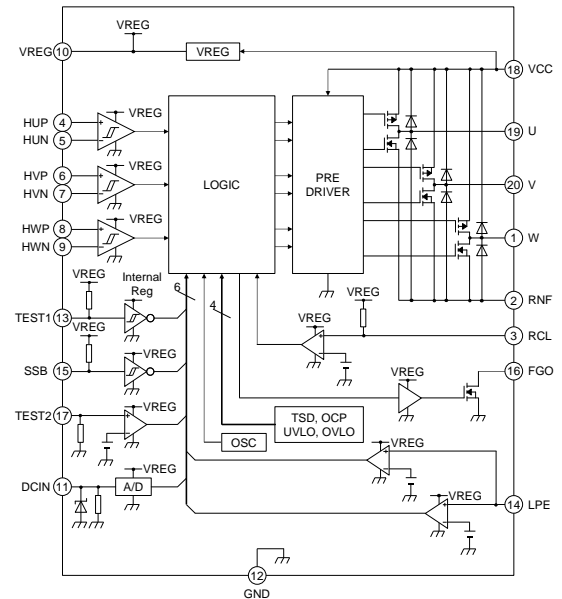


Figure 3. Block Diagram

Pin Description

| Pin No | Pin Name | Function   | Pin No | Pin Name | Function                             |
|--------|----------|--|--------|----------|--------------------------------------|
| 1      | W        | W phase output   | 11     | DCIN     | Controlling rotation speed input     |
| 2      | RNF      | Resistor for detecting output current connecting Input | 12     | GND      | Ground                               |
| 3      | RCL      | Comparator of detecting output current input           | 13     | TEST1    | Test input (for shipment)            |
| 4      | HUP      | U phase hall input +                                   | 14     | LPE      | Motor lock protection setting input  |
| 5      | HUN      | U phase hall input -                                   | 15     | SSB      | Soft start / Soft stop setting input |
| 6      | HVP      | V phase hall input +                                   | 16     | FGO      | FG output (3FG)                      |
| 7      | HVN      | V phase hall input -                                   | 17     | TEST2    | Test input (for shipment)            |
| 8      | HWP      | W phase hall input +                                   | 18     | VCC      | Power supply / Motor power supply    |
| 9      | HWN      | W phase hall input -                                   | 19     | U        | U phase output                       |
| 10     | VREG     | Regulator output                                       | 20     | V        | V phase output                       |
| -      | EXP-PAD  | The EXP-PAD of the center of product connect to GND.   | -      | -        | -                                    |

## Absolute Maximum Ratings (Ta = 25°C)

| Item   | Symbol   | Limit         | Unit    |
|--|--|---------------|---------|
| Power Supply Voltage                             | V <sub>CC</sub>  | -0.3 to +36.0 | V       |
| Control Input Voltage (LPE, SSB)                 | V <sub>LPE</sub> , V <sub>SSB</sub>  | -0.3 to +5.5  | V       |
| Controlling Rotation Speed Input Voltage         | V <sub>DCIN</sub>  | -0.3 to +12.0 | V       |
| Hall Input Voltage                               | V <sub>HUP</sub> , V <sub>HUN</sub> , V <sub>HVP</sub> ,<br>V <sub>HVN</sub> , V <sub>HWP</sub> , V <sub>HWN</sub> | -0.3 to +5.5  | V       |
| TEST1 Input Voltage                              | V <sub>TEST1</sub>   | -0.3 to +5.5  | V       |
| TEST2 Input Voltage                              | V <sub>TEST2</sub>   | -0.3 to +36.0 | V       |
| Driver Output Voltage                            | V <sub>U</sub> , V <sub>V</sub> , V <sub>W</sub> ,   | -0.3 to +36.0 | V       |
| FGO Voltage                                      | V <sub>FGO</sub>   | -0.3 to +7.0  | V       |
| RNF Voltage                                      | V <sub>RNF</sub>   | 0.7           | V       |
| VREG Output Current                              | I <sub>VREG</sub>  | -30           | mA      |
| FGO Output Current                               | I <sub>FGO</sub>   | 5             | mA      |
| Driver Output Current (Continuous)               | I <sub>OUT(DC)</sub>   | 1.5           | A/phase |
| Driver Output Current (Peak) <sup>(Note 1)</sup> | I <sub>OUT(PEAK)</sub>   | 2.0           | A/phase |
| Storage Temperature Range                        | T <sub>stg</sub>   | -55 to +150   | °C      |
| Maximum Junction Temperature                     | T <sub>jmax</sub>  | 150           | °C      |

(Note 1) Pulse width  $t_w \leq 1$ ms, duty=20% pulse

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

## Thermal Resistance (Note 1)

| Parameter  | Symbol        | Thermal Resistance (Typ) |                          | Unit |
|--|---------------|--------------------------|--------------------------|------|
|  |               | 1s <sup>(Note 3)</sup>   | 2s2p <sup>(Note 4)</sup> |      |
| HTSSOP-B20   |               |                          |                          |      |
| Junction to Ambient  | $\theta_{JA}$ | 143.0                    | 26.8                     | °C/W |
| Junction to Top Characterization Parameter <sup>(Note 2)</sup> | $\Psi_{JT}$   | 8                        | 4                        | °C/W |

(Note 1)Based on JESD51-2A(Still-Air)

(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3)Using a PCB board based on JESD51-3.

(Note 4)Using a PCB board based on JESD51-5, 7.

| Layer Number of Measurement Board | Material | Board Size                 |
|-----------------------------------|----------|----------------------------|
| Single                            | FR-4     | 114.3mm x 76.2mm x 1.57mmt |

| Top                   |            |
|-----------------------|------------|
| Copper Pattern        | Thickness  |
| Footprints and Traces | 70 $\mu$ m |

| Layer Number of Measurement Board | Material | Board Size                | Thermal Via <sup>(Note 5)</sup> |               |
|-----------------------------------|----------|---------------------------|---------------------------------|---------------|
|                                   |          |                           | Pitch                           | Diameter      |
| 4 Layers                          | FR-4     | 114.3mm x 76.2mm x 1.6mmt | 1.20mm                          | $\Phi$ 0.30mm |

| Top                   |            | 2 Internal Layers |            | Bottom          |            |
|-----------------------|------------|-------------------|------------|-----------------|------------|
| Copper Pattern        | Thickness  | Copper Pattern    | Thickness  | Copper Pattern  | Thickness  |
| Footprints and Traces | 70 $\mu$ m | 74.2mm x 74.2mm   | 35 $\mu$ m | 74.2mm x 74.2mm | 70 $\mu$ m |

(Note 5) This thermal via connects with the copper pattern of all layers.

## Recommended Operating Conditions

| Item                  | Symbol           | Min | Typ | Max  | Unit |
|-----------------------|------------------|-----|-----|------|------|
| Supply Voltage        | V <sub>CC</sub>  | 8   | 12  | 28   | V    |
| Operating Temperature | T <sub>opr</sub> | -40 | 25  | +105 | °C   |

Description of Blocks

(1) Regulator Output Pin (VREG)

This is the Pin regulated 5V (Typ). Set the capacitors of 0.1μF to 1μF. If using VREG for the bias power supply for HALL elements, don't exceed the ratings of VREG current.

(2) Controlling Rotation Speed Input Pin (DCIN)

Rotation Speed can be controlled by inputting DC signal into DCIN and changing the PWM duty of driver output. If VCC is used for controlling the rotation speed, set DCIN = VREG. When DCIN ≤ 1V (Typ), all of the driver outputs are controlled to "L". DCIN Pin is pulled down to GND by the resistor of 200kΩ ± 60kΩ.

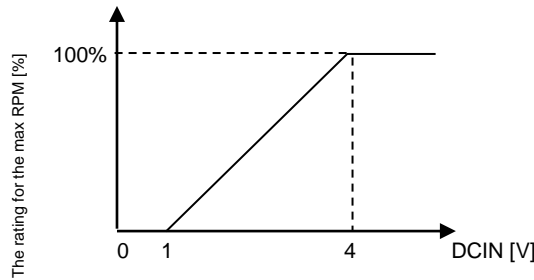


Figure 4. DCIN voltage vs rotation speed

The voltage of DCIN is input into the LOGIC circuit through the A/D inside IC. It sets the duty and makes signals of driver outputs demanding DCIN voltage. A/D samples DCIN voltage repeatedly and updates the set point. The set point is updated when it changes over ±1LSB from the previous point and when the next set point is in ±1LSB of itself three times. (The time is 1ms(Typ)). Only the setting point of initial value is updated by the first sampling. The A/D has 8 bit digital value and the power supply is VREG. 1LSB is about 19.5mV (5V/256,8bit). If VREG fluctuates, the rotation speed fluctuates, too. So stabilize VREG. It is better that DCIN is inputted the voltage divider of VREG.

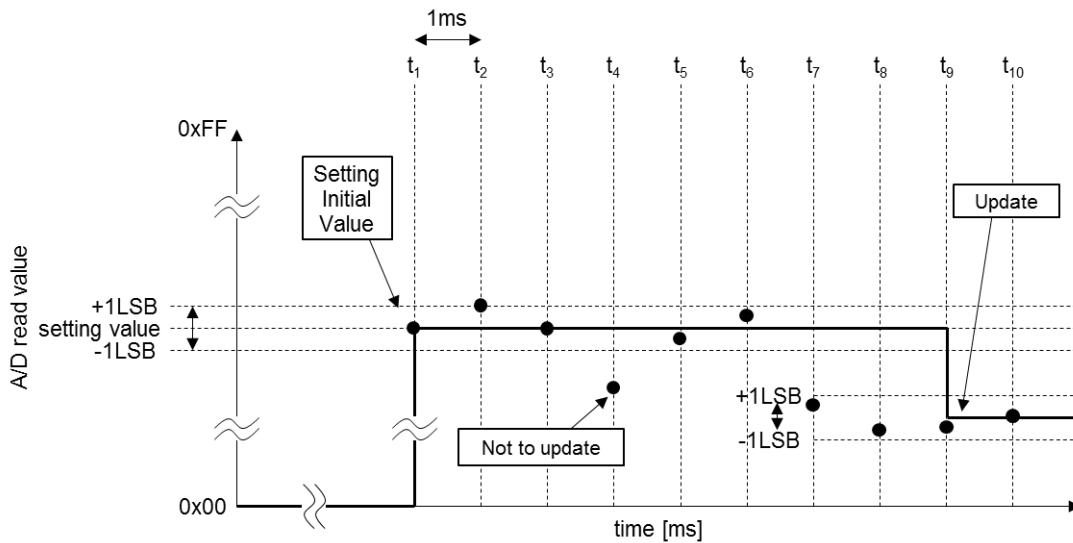


Figure 5. A/D sampling operation

Description of Blocks - continued

(3) Soft Start / Soft Stop Setting Pin (SSB)

The circuit of Soft Start and Soft Stop (SS mode) is built in to save the start/stop current. Soft Start and Soft Stop mode is set by inputting  $V_{SSBL}$  (Note 1). When SSB is  $V_{SSBH}$  (Note 1), only CL circuit save the start and stop current. Don't change SSB pin voltage during operating because of the incorrect operation. SSB pin is pulled up to VREG by the resistors of  $100k\Omega \pm 30k\Omega$ . With regard to the bias current, [see the table of Electrical Characteristics shown P11](#).  
 (Note 1) [See the table of Electrical Characteristics shown P11](#).

Table1. SSB Pin Function

| SSB       | Operation       |
|-----------|-----------------|
| H or OPEN | Disable SS mode |
| L         | Enable SS mode  |

An example of SS mode operation is shown in the following. This operation is enable at starting, stopping, and changing the rotation speed. (The times shown in Figure 6 are typical value)

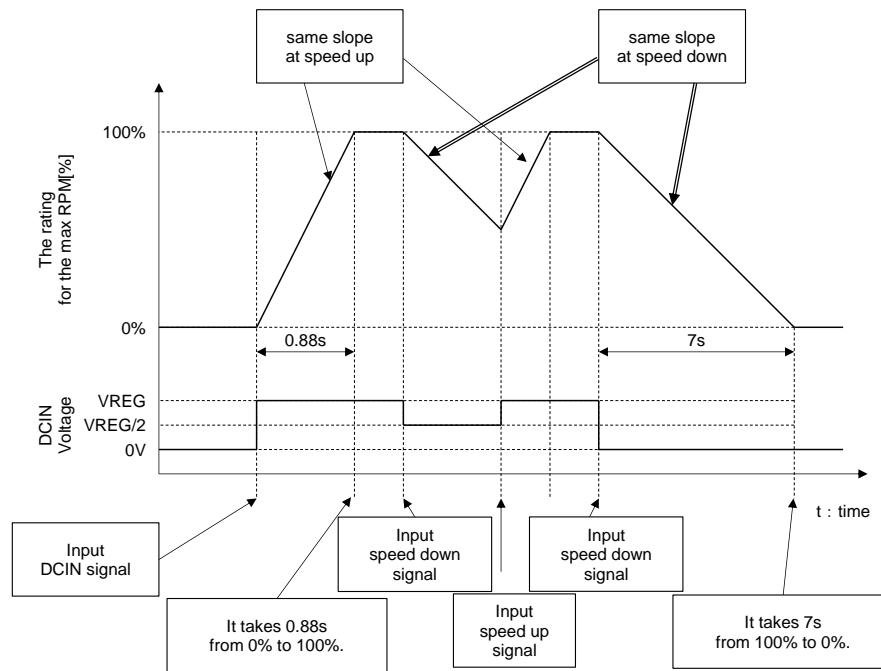


Figure 6. Soft start / Soft stop operation

(4) HALL Input Pin (HALL: HUP, HUN, HVP, HVN, HWP, HWN)

HUP, HUN, HVP, HVN, HWP, HWN is the input pin of HALL comparator in IC. The hysteresis voltage ( $\pm 15mV$ (Typ) (Note 2)) is set in HALL comparator to prevent the incorrect operation by the noise. Set the bias current of HALL elements the minimum input voltage ( $V_{HALLMIN}$ (Note 2)) or more. Also set the ceramic capacitors about 1000pF to 0.01uF between the inputs of HALL comparator. As HALL comparator has the range of In-phase Input Voltage ( $V_{HALLCM}$ (Note 2)), set the bias current of HALL elements in  $V_{HALLCM}$ . All of the driver outputs are Hi-Z by the error detection circuit of HALL inputs signals when all of the outputs of HALL comparator (HU, HV, and HW) are "H" or "L". In addition, if one of the outputs of HALL comparator keeps "H" or "L" on a certain time, all of the driver outputs are Hi-Z for 5s(Typ), "a certain time" shows the period which positive/negative edge of the other outputs are counted 32 times. This circuit is automatic restarted if the HALL signals return to the normal state after 5s and HU, HV and HW are judged correctly. (This detection repeats every 5s.)

Pay attention to the position of HALL elements for fear that the efficiency and the silence characteristic become worse.

(Note 2) [See the table of Electrical Characteristics shown P11](#)

## Description of Blocks - continued

- (5) FG Output Pin (FGO)  
3FG signal which is synthesized from the HALL signals is output from FGO. Set FGO pulled up by the resistors about 10kΩ to 100kΩ because FGO is the pin of open-drain. Pay attention not to exceed the voltage rating and current rating of FGO because of the destruction of IC.
- (6) Power Supply Pin (VCC)  
Make VCC line low impedance (thick and short) because the Motor current flows.  $V_{CC}$  might be changed considerably by MOTOR BEMF and PWM switching, so place the bypass capacitors as near as possible between VCC and GND pin. When the Motor generates large current or big BEMF, add the value of capacitors. Also, set the ceramic capacitors about 0.01μF to 1μF to decrease the impedance of power supply broadband. Pay attention not to exceed the rating for a moment. Also, the device against ESD exists on VCC pin, so if the surge voltage which is the rating or more, this ESD device operates and so IC may destroy. Don't exceed the rating. It is so useful to add the Zener diode whose breakdown voltage is slightly lower than the rating. In addition, if the voltage input in reverse, IC may destroy because of the ESD device between VCC and GND.
- (7) Ground Pin (GND)  
Make GND line as thick and short as possible to decrease the switching noise and stabilize the reference voltage inside IC and set GND the lowest voltage for a moment. Also, design that GND of IC should not have the common impedance.
- (8) Driver Output Pin (U, V, W)  
Pay attention about the following points in using driver output.  
  - Wiring of U, V, and W should be thick and short (low impedance) because the motor current flows.
  - IC might destroy because the diodes against ESD operate when the surge pulse signal or the voltage which is the rating or more input into the pins. Don't exceed the rating.
When the driver outputs change considerably toward positive and negative (for ex. BEMF voltage is so big), IC operates abnormally or destroys. In the above case, add the Schottky diode to the driver output pin.
- (9) Resistor for Detecting Output Current Connecting Input Pin (RNF)  
Insert resistor for detecting current 0.15Ω to 0.7Ω between RNF and GND. Pay attention that the power consumption of resistor for detecting output current (multiply  $I_{OUT}^2$  by R[W]) doesn't exceed the rating of the resistor. Because the Motor current flows, make the low impedance between RNF pin and GND. Also it should not have the common impedance. If RNF voltage exceeds the rating, IC might malfunction or be destroyed, so don't exceed the rating. When RNF pin is shorted to GND, large current flows due to a lack of normal current limit operation. Pay attention that OCP or TSD might operate in that case. Similarly, if RNF Pin is OPEN, output current might not flow, and it causes malfunction.
- (10) Comparator of Detecting Output Current Input Pin (RCL)  
RCL pin (the pin that the input of the current detect comparator) exists independently in order to avoid the deterioration of current detect accuracy by wire impedance inside IC of RNF pin. Therefore, when operating current limit, be sure to connect RNF pin and RCL pin. Moreover, it is possible to reduce the deterioration of current detect accuracy that is caused by the impedance of board pattern between RNF pin and resistor for detecting current, to connect wiring from RCL pin most adjacent to resistor for detecting current. Design the PCB pattern considering wiring that is less influenced by noise. Additionally, when RCL pin is shorted to GND, IC can't operate normally and so the large current might flow. Pay attention that OCP or TSD might operate in that case.
- (11) TEST Pin (TEST1, TEST2)  
TEST pin is for the shipping inspection. Short to GND at normally use.



**Description of Blocks - continued**

## (12) Sequence of control signal

It is recommended to input the signal into LPE after  $V_{CC}$ . If LPE is input before  $V_{CC}$ , IC operates correctly. However in the case of LPE is "H" or "M", pay attention that Motor can't be started if the Motor rotation can't be detected in the setting time. IC has the priority between the control signals and the protection signals. See the following table.

Table2. Priority of control signals

| Priority        | Input / Internal Signals |
|-----------------|--------------------------|
| 1 <sup>st</sup> | UVLO                     |
| 2 <sup>nd</sup> | OCP, TSD                 |
| 3 <sup>rd</sup> | OVLO                     |
| 4 <sup>th</sup> | MLP, HALLERR             |
| 5 <sup>th</sup> | CL                       |

## Protection Circuits

### (1) Current Limit Circuit (CL circuit)

To change from the output current to the voltage by the resistor between RNF and GND and to input that voltage into RCL work as Current Limit (CL circuit). CL has the mask time to avoid the false detection because of the spike noise when the output turns ON. Current limit doesn't work in the mask time that RCL become 0.2V (Typ) or more. In the case of SSB is "H", all of the driver outputs turn "L" and it returns by itself after a certain time (1 $\mu$ s(Typ)). In the case of SSB is "L", the Motor torque is saved, after RCL voltage is 0.2V (Typ) or less, it turns to the normal operation. In both of case the mask time of CL operation is 0.6 $\mu$ s (Typ).

### (2) Thermal Shut Down Circuit (TSD Circuit)

TSD (Thermal Shut Down: TSD) operates when the chip temperature is 175°C (Typ) or more and all of the driver outputs turn to Hi-Z. TSD circuit has the hysteresis (25°C (Typ)) so if the chip temperature is down, it operates normally. The purpose of the TSD circuit is to protect driver IC from thermal breakdown. The temperature is over the rating when TSD operates. Thus, it must have sufficient margin against TSD, and don't use continuously by TSD as a precondition.

### (3) Over Current Protection Circuit (OCP Circuit)

OCP (Over Current Protection: OCP) circuit prevent from the destruction of shorted between the output pins and VCC/GND shorted. The outputs are latched to Hi-Z when the output current exceeds the current rating and reaches the OCP current. OCP can be reset by UVLO. It must have sufficient margin against OCP and pay attention not to use continuously by OCP as a precondition because the output current exceeds the current rating when OCP operates. Also when the outputs shorted to GND or shorted between the outputs, OCP operation might be reset by UVLO operation of VCC or VREG. So consider fully.

### (4) Under Voltage Lock Out Circuit (UVLO Circuit)

UVLO (Under Voltage Lock Out: UVLO) circuit prevent the false operation from under voltage which driver IC can operate. When  $V_{CC}$  declines to  $V_{UVL}$  (6V (Typ)), all of the outputs turn to Hi-Z. UVLO circuit has hysteresis (1V (Typ)), so when  $V_{CC}$  reaches  $V_{UVH}$  (7V (Typ)) or more, it operates normally. Also when VREG is 4V (Typ) or less, UVLO operates.

### (5) Over Voltage Lock Out Circuit (OVLO circuit)

Over voltage lock out circuit (Over Voltage Lock Out: OVLO) is built in for the purpose to save the lifted voltage at the rotation speed down. All of the driver outputs turn "L" if LPE is "H" or "L" and  $V_{CC}$  is  $V_{OVH2}$  (31V (Typ)) or more, if LPE is "M" and  $V_{CC}$  is  $V_{OVH1}$  (16V (Typ)) or more. OVLO circuit has the hysteresis. In the case of  $V_{OVH2}$ , it operates normally  $V_{OVL2}$  (30.5V (Typ)) or less. In the case of  $V_{OVH1}$ , it operates normally  $V_{OVL1}$  (15V (Typ)) or less.

### (6) Motor Lock Protection Circuit (MLP Circuit)

Motor lock protection circuit (Motor Lock Protection: MLP) is built in. Enable/Disable of MLP and OVLO threshold can be set by LPE pin. All of the driver outputs are Hi-Z when the outputs of HALL comparator keep "H" or "L" during 1.1s (Typ) at LPE is "H" or "M". It restarts after 5s (Typ). When LPE is "L", MLP circuit does not work. LPE pin is pulled up by VREG through a resistance of 100k $\Omega$ ±30k $\Omega$ .

Table3. LPE Pin Function

| LPE       | Monitoring Time | OVLO Threshold          |
|-----------|-----------------|-------------------------|
| H or OPEN | 1.1s±30%        | $V_{OVH2}$ , $V_{OVL2}$ |
| M         | 1.1s±30%        | $V_{OVH1}$ , $V_{OVL1}$ |
| L         | Disable         | $V_{OVH2}$ , $V_{OVL2}$ |

Electrical Characteristics (Unless otherwise specified Ta=25°C, V<sub>CC</sub> =12V)

| Item                            | Symbol               | Limit                |      |                       | Unit              | Conditions  |
|---------------------------------|----------------------|----------------------|------|-----------------------|-------------------|---|
|                                 |                      | Min                  | Typ  | Max                   |                   |   |
| <b>[Whole]</b>                  |                      |                      |      |                       |                   |   |
| Circuit Current                 | I <sub>CC</sub>      | -                    | 8    | 16                    | mA                |   |
| VREG Voltage                    | V <sub>REG</sub>     | 4.75                 | 5.0  | 5.25                  | V                 | I <sub>VREG</sub> =-10mA                          |
| <b>[Driver Output]</b>          |                      |                      |      |                       |                   |   |
| Output On Resistance            | R <sub>ON</sub>      | -                    | 0.6  | 1.1                   | Ω                 | I <sub>OUT</sub> =±1.5A<br>(sum of High/Low side) |
| Carrier Frequency               | F <sub>PWM</sub>     | 20                   | 22.7 | 25                    | kHz               |   |
| <b>[HALL Input]</b>             |                      |                      |      |                       |                   |   |
| Input Bias Current              | I <sub>HALL</sub>    | -2.0                 | -0.1 | +2.0                  | μA                | V <sub>HALL</sub> =0V                             |
| Range of In-phase Input Voltage | V <sub>HALLCM</sub>  | 0                    | -    | V <sub>REG</sub> -1.8 | V                 |   |
| Minimum Input Voltage           | V <sub>HALLMIN</sub> | 65                   | -    | -                     | mV <sub>p-p</sub> |   |
| HYS Level +                     | V <sub>HALLHY+</sub> | 3                    | 15   | 30                    | mV                |   |
| HYS Level -                     | V <sub>HALLHY-</sub> | -30                  | -15  | -3                    | mV                |   |
| <b>[Control Input: DCIN]</b>    |                      |                      |      |                       |                   |   |
| Input Bias Current              | I <sub>DCIN</sub>    | 12.5                 | 25   | 40                    | μA                | V <sub>DCIN</sub> =V <sub>REG</sub>               |
| Min Duty Input Voltage          | V <sub>MIN</sub>     | 0.75                 | 1    | 1.25                  | V                 |   |
| Max Duty Input Voltage          | V <sub>MAX</sub>     | 3.75                 | 4    | 4.25                  | V                 |   |
| <b>[Control Input: SSB]</b>     |                      |                      |      |                       |                   |   |
| Input Current                   | I <sub>SSB</sub>     | -80                  | -50  | -30                   | μA                | V <sub>SSB</sub> =0V                              |
| Voltage Input H                 | V <sub>SSBH</sub>    | 2.0                  | -    | V <sub>REG</sub>      | V                 |   |
| Voltage Input L                 | V <sub>SSBL</sub>    | 0                    | -    | 0.8                   | V                 |   |
| <b>[Control Input: LPE]</b>     |                      |                      |      |                       |                   |   |
| Input Current                   | I <sub>LPE</sub>     | -80                  | -50  | -30                   | μA                | V <sub>LPE</sub> =0V                              |
| Input Voltage "H"               | V <sub>LPEH</sub>    | 0.8xV <sub>REG</sub> | -    | V <sub>REG</sub>      | V                 |   |
| Input Voltage "M"               | V <sub>LPEM</sub>    | 0.4xV <sub>REG</sub> | -    | 0.6xV <sub>REG</sub>  | V                 |   |
| Input Voltage "L"               | V <sub>LPEL</sub>    | 0                    | -    | 0.2xV <sub>REG</sub>  | V                 |   |
| <b>[FG Output: FGO]</b>         |                      |                      |      |                       |                   |   |
| Output Voltage L                | V <sub>FGOL</sub>    | 0                    | 0.1  | 0.25                  | V                 | I <sub>FGO</sub> =2mA                             |
| <b>[Current Limit]</b>          |                      |                      |      |                       |                   |   |
| Detect Voltage                  | V <sub>CL</sub>      | 0.18                 | 0.20 | 0.22                  | V                 |   |
| <b>[UVLO]</b>                   |                      |                      |      |                       |                   |   |
| Release Voltage                 | V <sub>UVH</sub>     | 6.3                  | 7.0  | 7.7                   | V                 |   |
| Lock Out Voltage                | V <sub>UVL</sub>     | 5.4                  | 6.0  | 6.6                   | V                 |   |
| <b>[OVLO]</b>                   |                      |                      |      |                       |                   |   |
| Release Voltage1                | V <sub>OVL1</sub>    | 13.5                 | 15.0 | 16.5                  | V                 | LPE="M"   |
| Lockout Voltage1                | V <sub>OVH1</sub>    | 14.5                 | 16.0 | 17.5                  | V                 | LPE="M"   |
| Release Voltage2                | V <sub>OVL2</sub>    | 28.5                 | 30.5 | 33.5                  | V                 | LPE="H" or "L"                                    |
| Lockout Voltage2                | V <sub>OVH2</sub>    | 29.0                 | 31.0 | 34.0                  | V                 | LPE="H" or "L"                                    |

Timing Chart

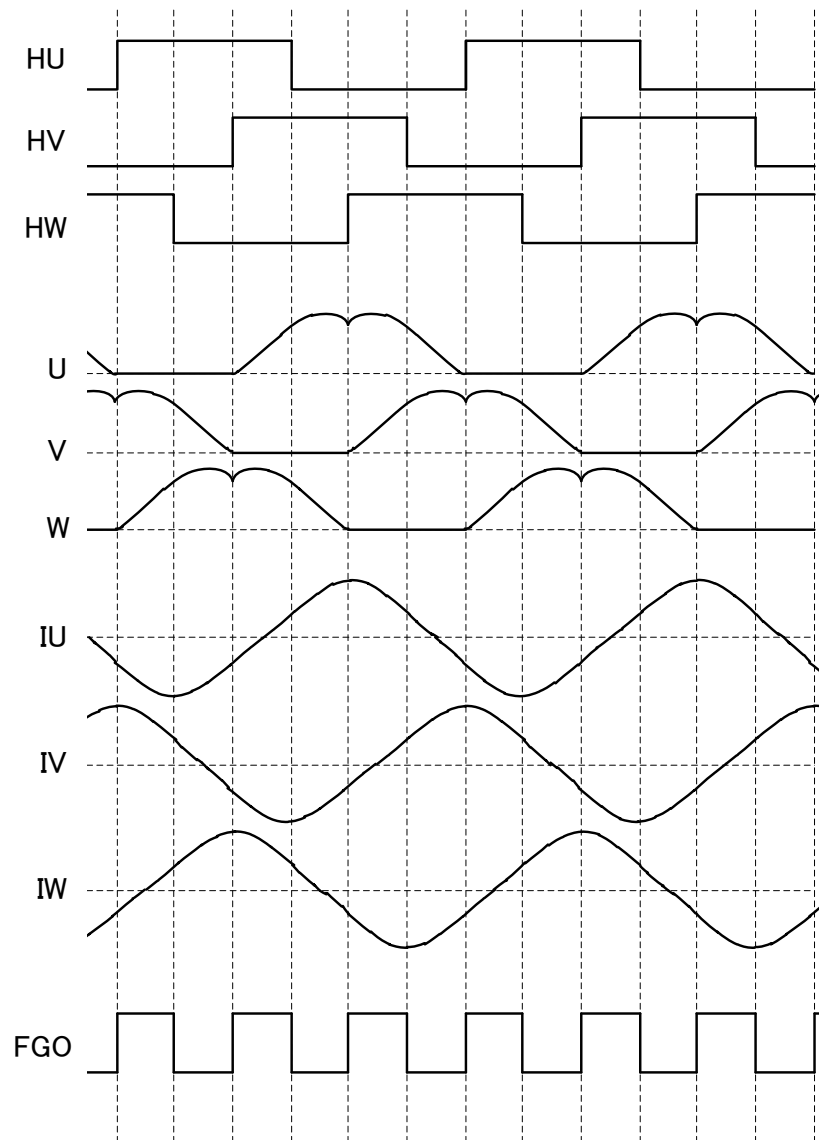


Figure 7. Timing Chart

State Transition Diagram

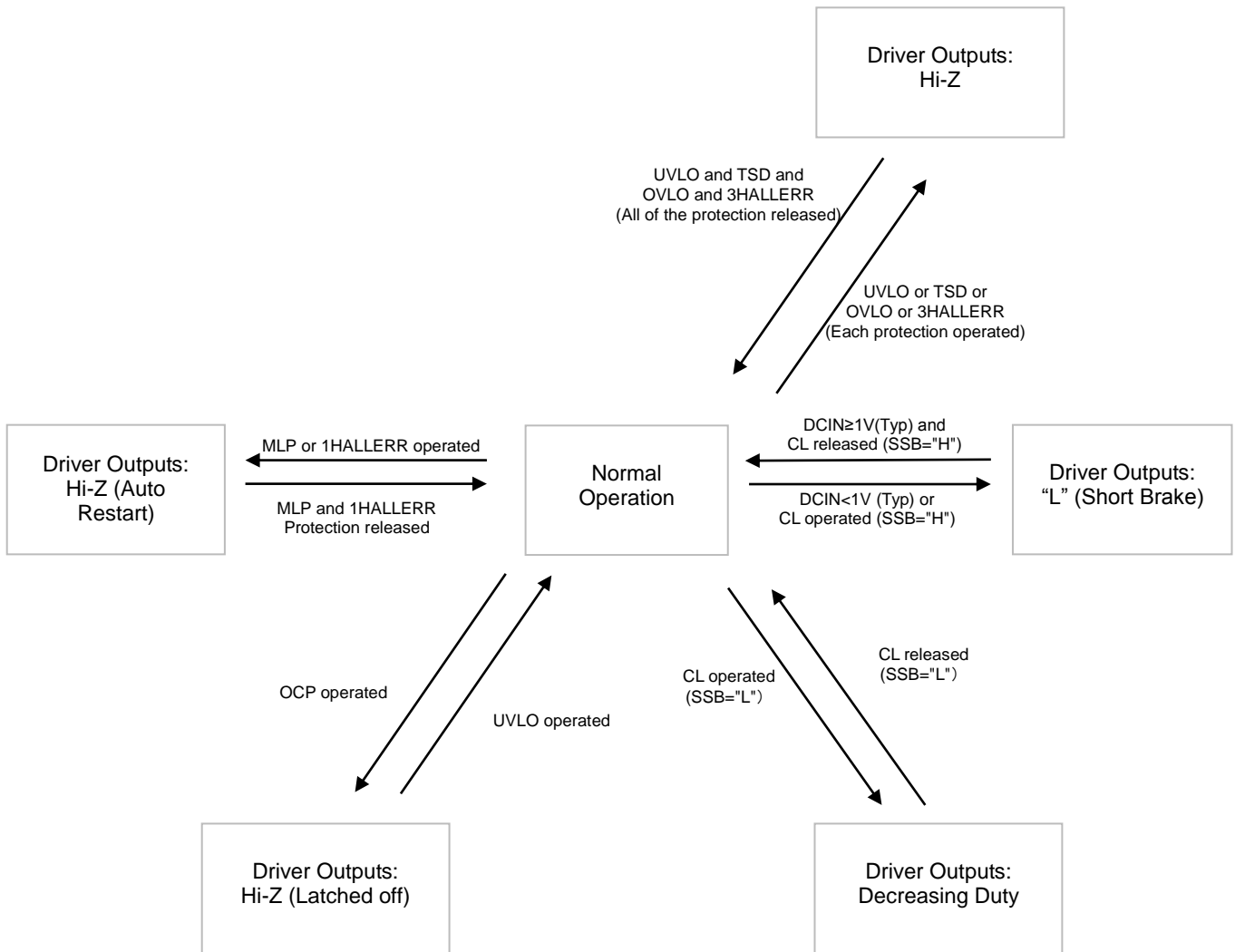


Figure 8. State Transition Diagram

I/O Equivalence circuits

| Pin No                     | Pin Name                               | I/O Equivalence circuit | Pin No   | Pin Name    | I/O Equivalence circuit |
|----------------------------|--|-------------------------|----------|-------------|-------------------------|
| 1<br>19<br>20<br>2         | W<br>U<br>V<br>RNF                     |                         | 3        | RCL         |                         |
| 4<br>5<br>6<br>7<br>8<br>9 | HUP<br>HUN<br>HVP<br>HVN<br>HWP<br>HWN |                         | 10<br>18 | VREG<br>VCC |                         |
| 11                         | DCIN                                   |                         | 13       | TEST1       |                         |
| 14                         | LPE                                    |                         | 15       | SSB         |                         |
| 16                         | FGO                                    |                         | 17       | TEST2       |                         |

(Note 1)The above value of resistor is shown typical.

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## Operational Notes – continued

**10. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

**11. Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

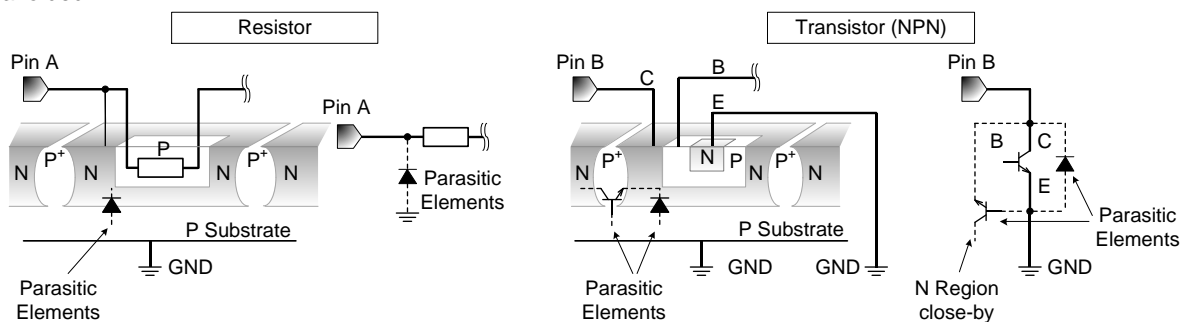


Figure 9. Example of monolithic IC structure

**12. Ceramic Capacitor**

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

**13. Area of Safe Operation (ASO)**

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

**14. Thermal Shutdown Circuit (TSD)**

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF power output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

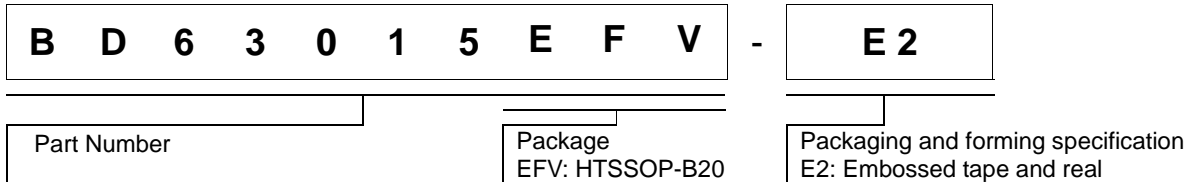
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

**15. Over Current Protection Circuit (OCP)**

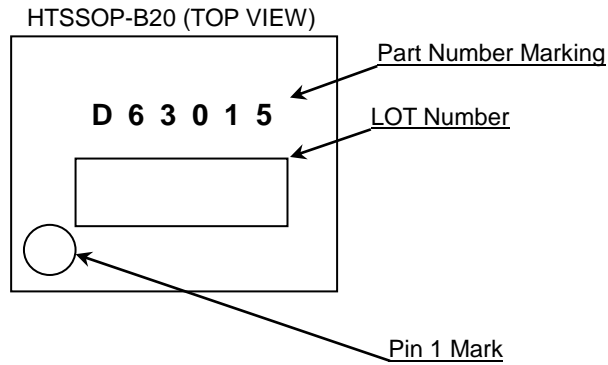
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.



Ordering Information

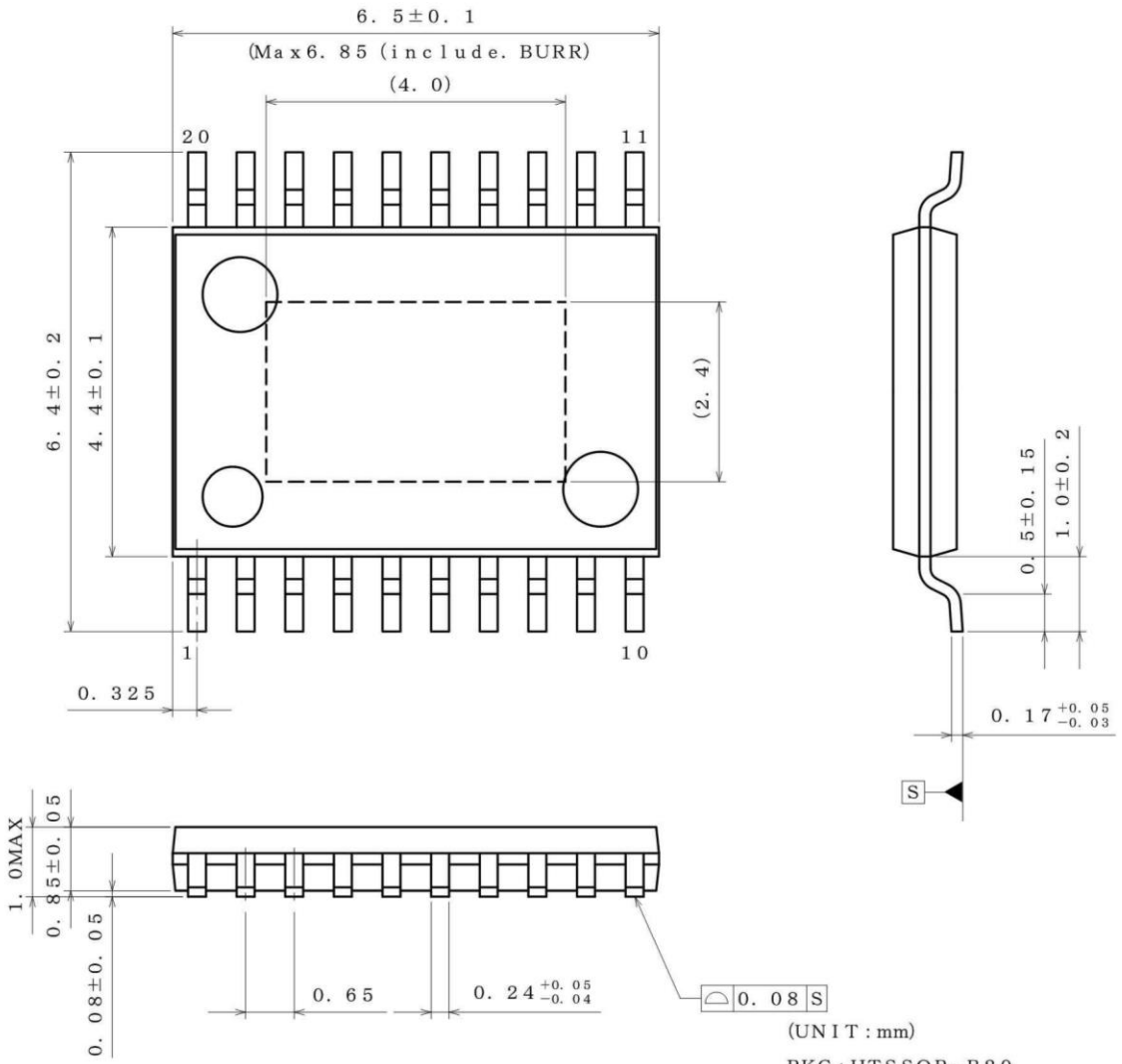


Marking Diagrams



Physical Dimension and Packing Information

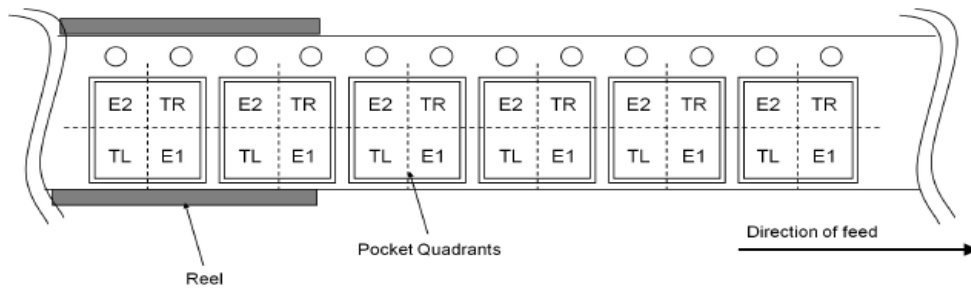
|              |            |
|--------------|------------|
| Package Name | HTSSOP-B20 |
|--------------|------------|



(UNIT : mm)  
 PKG : HTSSOP-B20  
 Drawing No. EX192-5002

<Tape and Reel information>

|                   |   |
|-------------------|---|
| Tape              | Embossed carrier tape (with dry pack)   |
| Quantity          | 2500pcs   |
| Direction of feed | E2<br>(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



## Revision History

| Date        | Rev. | Changes     |
|-------------|------|-------------|
| 13.Feb.2018 | 001  | New Release |

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| JAPAN     | USA       | EU         | CHINA     |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV  |           | CLASS III  |           |

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  - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

### Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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