

H-Bridge Drivers for DC Brush Motors

Single H-Bridge Driver High-Speed Switching Type

BD6376GUL

General Description

The BD6376GUL provides a single H-bridge motor driver which features wide range of motor power supply voltage from 2.0V to 9.0V and low power consumption to switch low ON-Resistance DMOS transistors at high speed. This small surface mounting package is most suitable for mobile system, home appliance and various applications.

Features

- Low ON-Resistance Power DMOS Output
- Charge Pump-Less with PDMOS High-Side Driver
- Under Voltage Locked Out protection & Thermal Shut Down Function

Applications

- Mobile System
- Home Appliance
- Amusement System, etc

Key Specifications

- Power Supply Voltage Range: 2.5V to 3.6V
- Motor Power Supply Voltage Range: 2.0V to 9.0V
- Circuit Current (Open Mode): 360 μ A(Typ)
- Stand-By Current: 1 μ A(Max)
- Control Input Voltage Range: 0V to V_{CC}V
- Logic Input Frequency: 200kHz(Max)
- Minimum Logic Input Pulse Width: 0.5 μ s(Min)
- Turn On Time: 200ns(Typ)
- Turn Off Time: 60ns(Typ)
- H-Bridge Output Current (DC): -1.0A to +1.0A
- Output ON-Resistance (Total): 0.45 Ω (Typ)
- Operating Temperature Range: -30°C to +85°C

Package

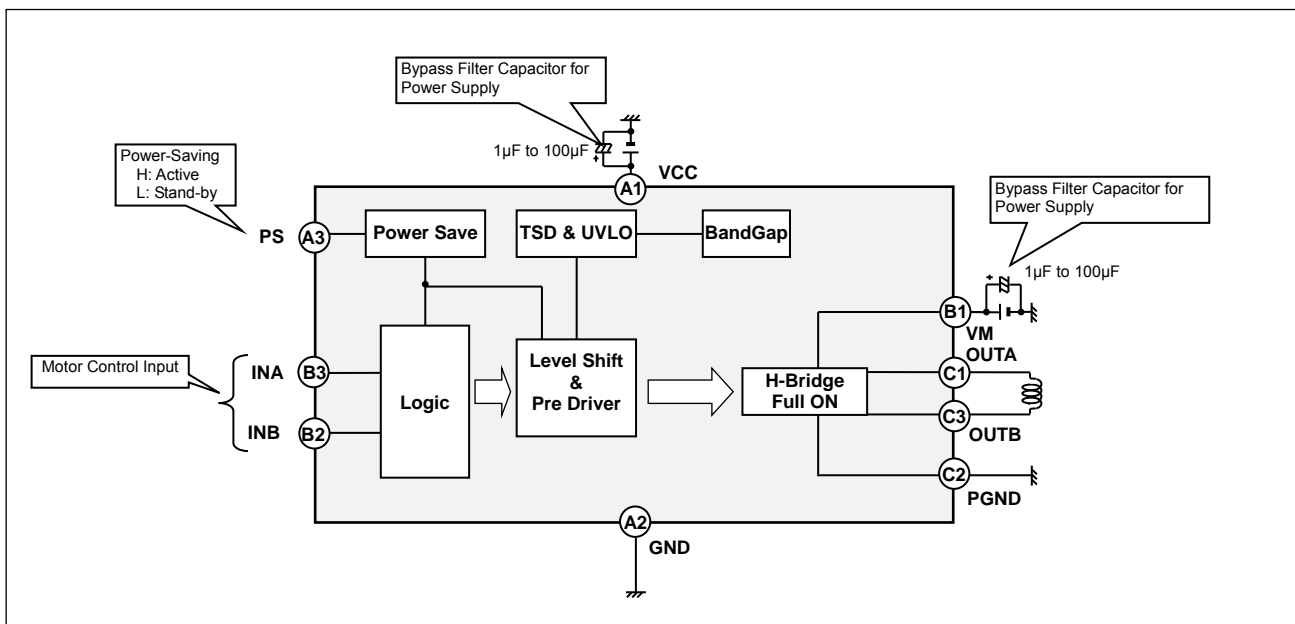
VCSP50L1

W(Typ) x D(Typ) x H(Max)

1.60mm x 1.60mm x 0.55mm



Typical Application Circuit



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

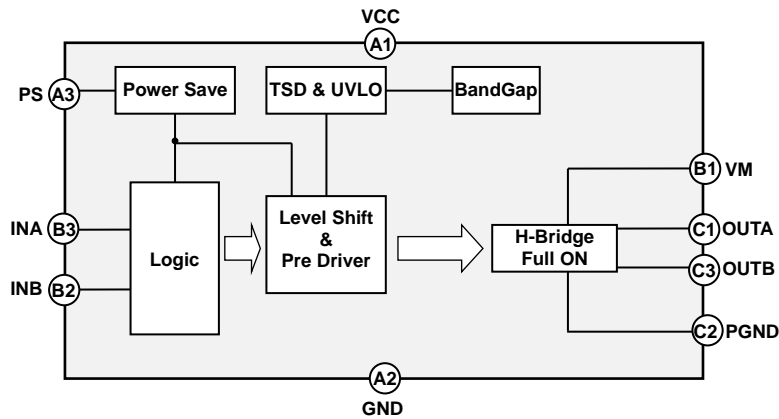
(Top View)

	1	2	3
A	VCC	GND	PS
B	VM	INB	INA
C	OUTA	PGND	OUTB

Pin Description

Pin No.	Pin Name	Function
A1	VCC	Power supply
A2	GND	Ground
A3	PS	Power-saving function
B1	VM	Motor power supply
B2	INB	Control logic input B
B3	INA	Control logic input A
C1	OUTA	H-bridge output A
C2	PGND	Motor ground
C3	OUTB	H-bridge output B

Block Diagram



Description of Blocks

1. Power-Saving Function
A power-saving function is included, which allows the system to save power when not driving the motor. The voltage level on this pin should be set high so as to keep the operation mode. (See the Electrical Characteristics; p.4/14)
2. Motor Control Input: INA and INB Pins
Logic level controls the output logic of H-Bridge.
(See the Electrical Characteristics; p.4/14, and I/O Truth Table; p.7/14)

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V _{CC}	-0.3 to +4.5	V
Motor Power Supply Voltage	V _M	-0.3 to +10.0	V
Control Input Voltage	V _{IN}	-0.3 to +V _{CC} +0.3	V
Power Dissipation	P _d	0.72 (Note 1)	W
H-bridge Output Current (DC)	I _{OUT}	-1.0 to +1.0 (Note 2)	A
Storage Temperature Range	T _{stg}	-55 to +150	°C
Junction Temperature	T _{jmax}	150	°C

(Note 1) Reduced by 5.8mW/°C over 25°C, when mounted on a glass epoxy 8-layers board (50mm x 58mm x 1.75mm).

(Note 2) Must not exceed P_d, A_{SO}, or T_{jmax} of 150°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V _{CC}	2.5	-	3.6	V
Motor Power Supply Voltage	V _M	2.0	-	9.0	V
Control Input Voltage	V _{IN}	0	-	V _{CC}	V
Logic Input Frequency	F _{IN}	0	-	200	kHz
Minimum Logic Input Pulse Width	T _{IN}	0.5	-	-	µs
Operating Temperature Range	T _{opr}	-30	-	+85	°C

Electrical Characteristics (Unless otherwise specified $V_{CC}=3.0V$, $V_M=5.0V$, $T_a=25^{\circ}C$)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
All Circuits						
Stand-by Current	I_{CCST}	-	0	1	μA	$V_{PS}=0V$
Circuit Current 1	I_{CC1}	180	360	550	μA	$V_{PS}=3V$, Open Mode
Circuit Current 2	I_{CC2}	180	375	550	μA	$V_{PS}=3V$, CW & CCW Mode
Circuit Current 3	I_{CC3}	180	375	550	μA	$V_{PS}=3V$, Short Brake Mode
PS Input (PS)						
High-Level Input Voltage	V_{PSH}	2.0	-	V_{CC}	V	
Low-Level Input Voltage	V_{PSL}	0	-	0.7	V	
High-Level Input Current	I_{PSH}	6	15	30	μA	$V_{PS}=3V$
Low-Level Input Current	I_{PSL}	-1	0	+1	μA	$V_{PS}=0V$
Control Input (IN=INA, INB)						
High-Level Input Voltage	V_{INH}	2.0	-	V_{CC}	V	
Low-Level Input Voltage	V_{INL}	0	-	0.7	V	
High-Level Input Current	I_{INH}	6	15	30	μA	$V_{IN}=3V$
Low-Level Input Current	I_{INL}	-1	0	+1	μA	$V_{IN}=0V$
Under Voltage Locked Out (UVLO)						
UVLO Voltage	V_{UVLO}	2.0	-	2.4	V	
Full ON Type H-Bridge Driver						
Output On-Resistance	R_{ON}	-	0.45	0.60	Ω	$I_{OUT}=\pm 500mA$, High & Low-side total
Turn On Time	T_{ON0}	-	200	400	ns	20 Ω Loading
Turn Off Time	T_{OFF0}	-	60	400	ns	20 Ω Loading

Typical Performance Curves (Reference data)

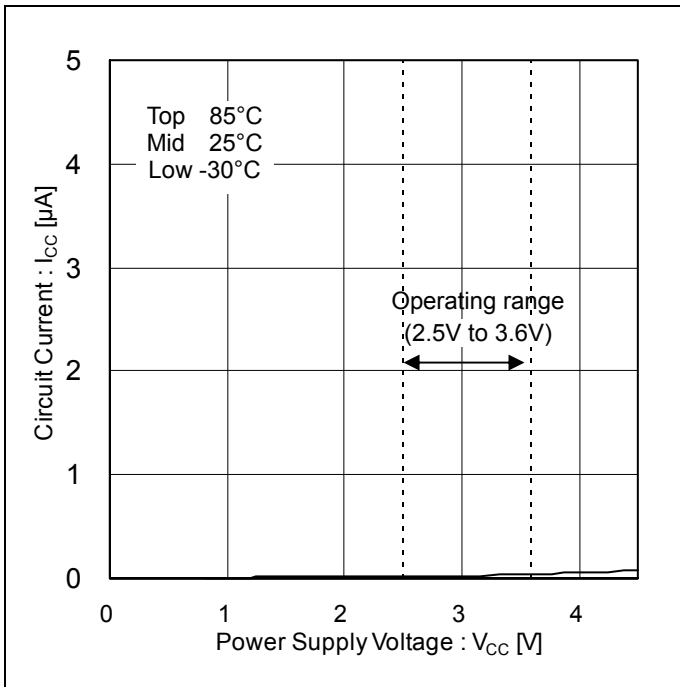


Figure 1.
Circuit Current vs Supply Voltage
(Stand-by Mode)

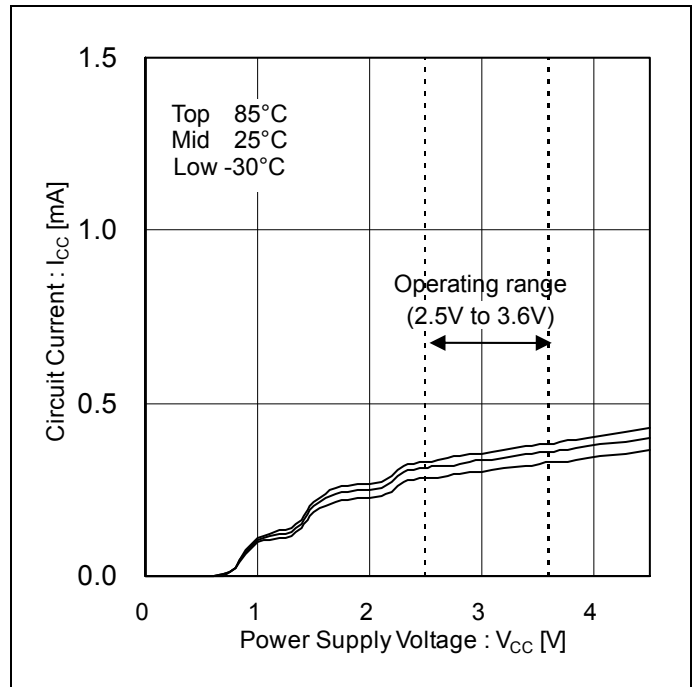


Figure 2.
Circuit Current vs Supply Voltage
(Open Mode)

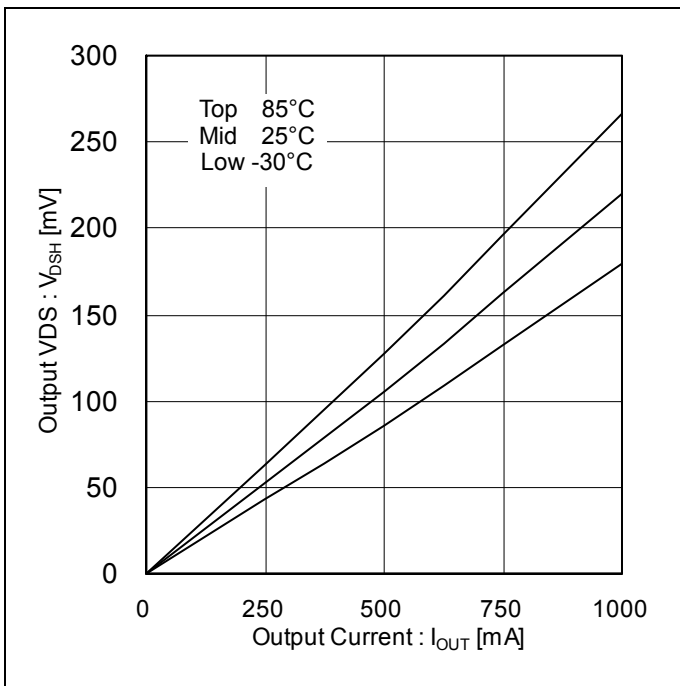


Figure 3.
Output VDS vs Output Current
(Output On-Resistance on high-side, $V_M=5V$, $V_{CC}=3V$)

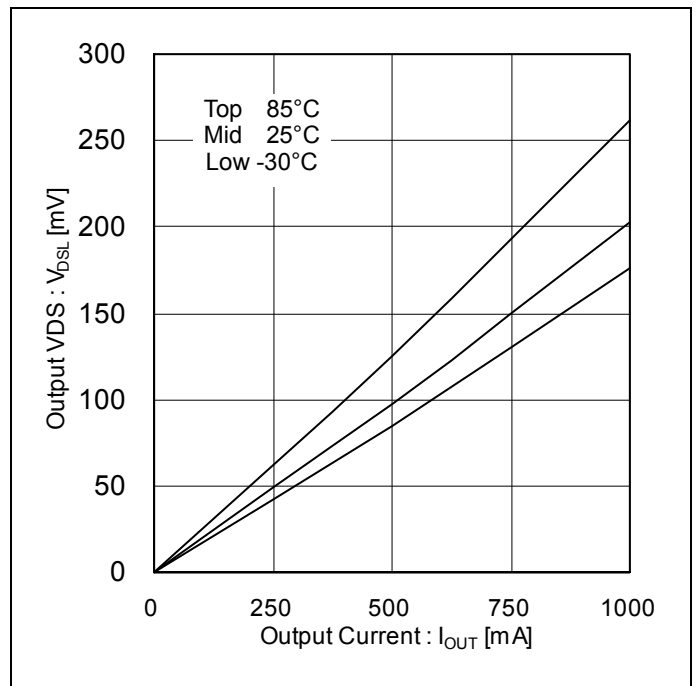


Figure 4.
Output VDS vs Output Current
(Output On-Resistance on low-side, $V_M=5V$, $V_{CC}=3V$)

Typical Performance Curves (Reference Data) - continued

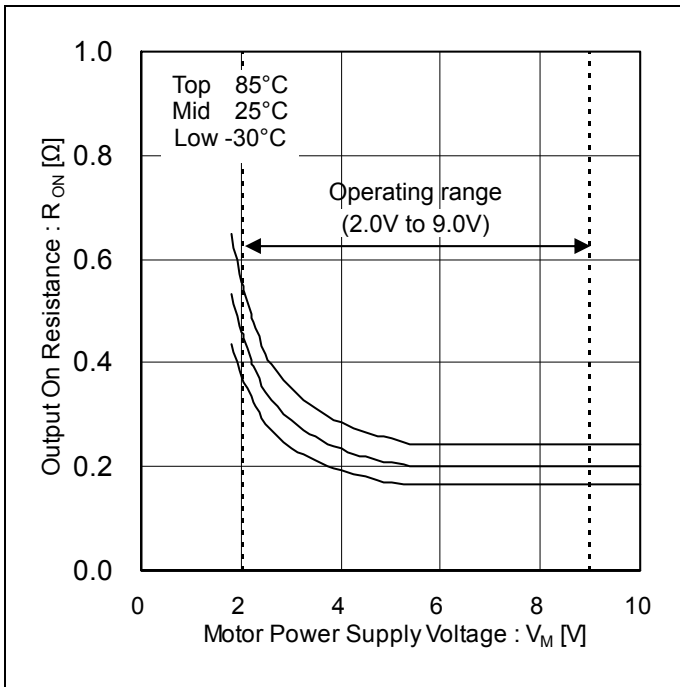


Figure 5.
Output On-Resistance vs Motor Power Supply Voltage
(Output On-Resistance on high-side V_M Dependency, V_{CC}=3V)

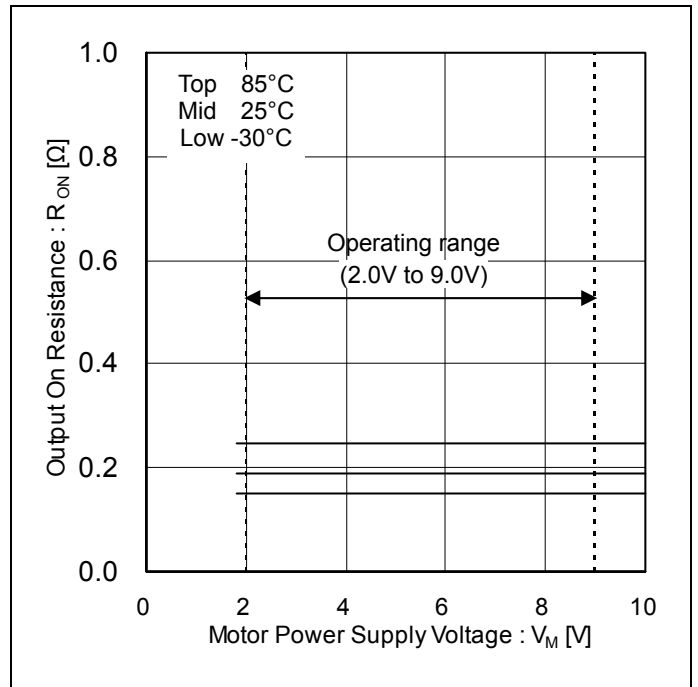


Figure 6.
Output On-Resistance vs Motor Power Supply Voltage
(Output On-Resistance on low-side V_M Dependency, V_{CC}=3V)

Timing Chart

Table 1. I/O Truth Table

Input Mode	INPUT			OUTPUT		
	PS ^(Note 3)	INA	INB	OUTA	OUTB	Output Mode ^(Note 4)
IN/IN	H	L	L	Z	Z	Open
		H	L	H	L	CW
		L	H	L	H	CCW
		H	H	L	L	Short Brake
-	L	X	X	Z	Z	Open

L: Low, H: High, X: Don't care, Z: High-Impedance

(Note 3) PS=High: Operation Mode, PS=Low: Stand-by Mode

(Note 4) CW: Current flows from OUTA to OUTB, CCW: Current flows from OUTB to OUTA

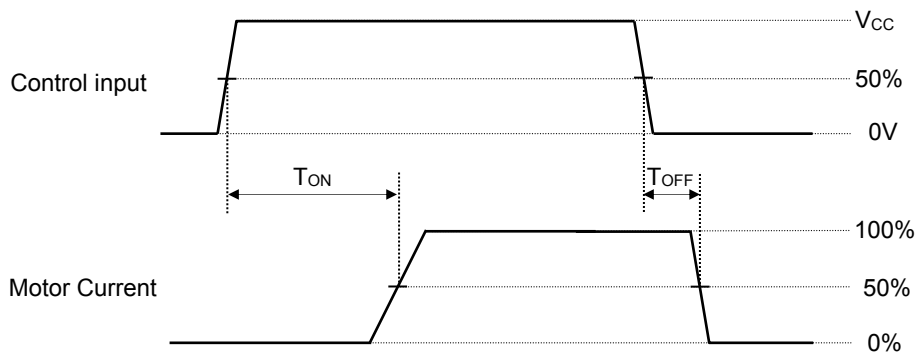
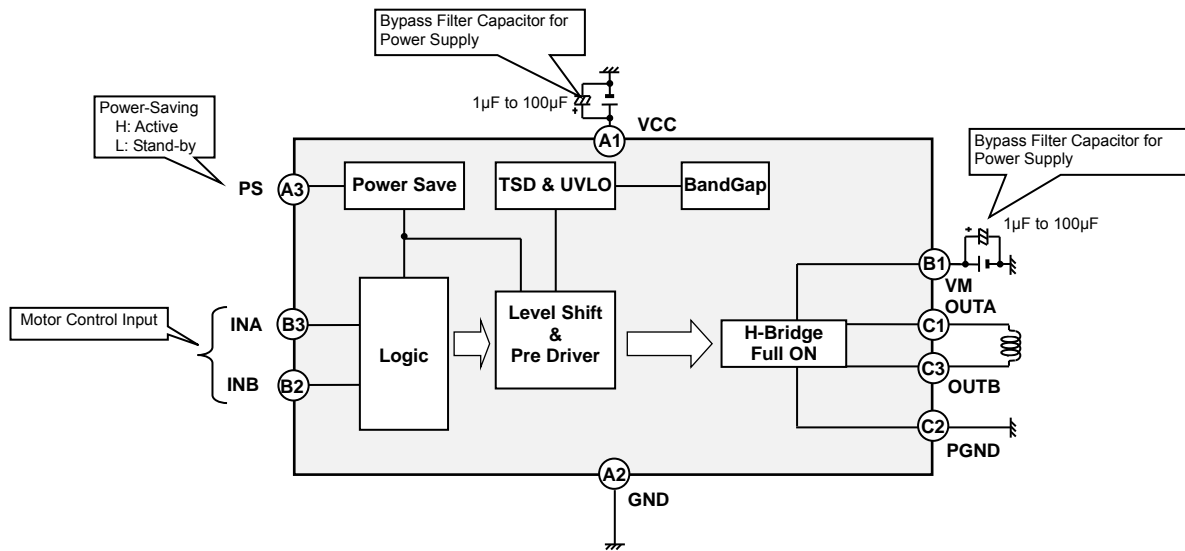


Figure 7.
Input-Output AC Characteristic

Application Example



Selection of Components Externally Connected

When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.

Power Dissipation

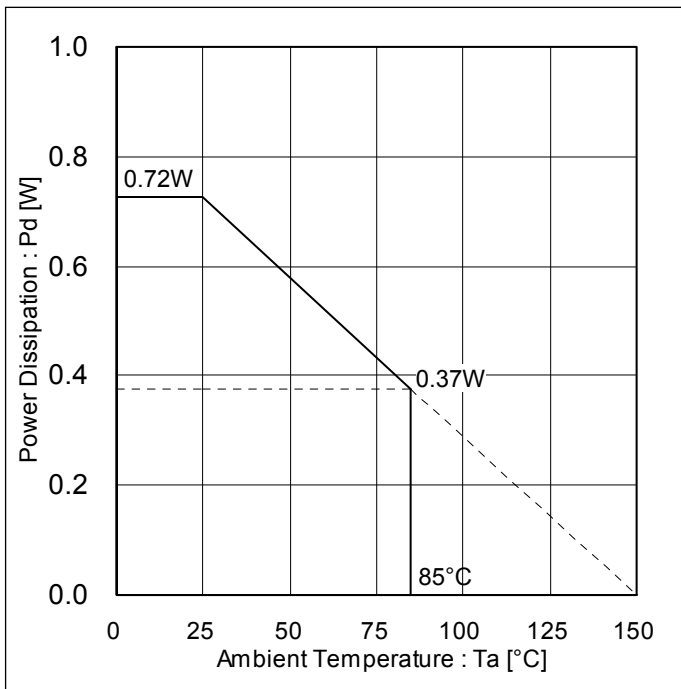
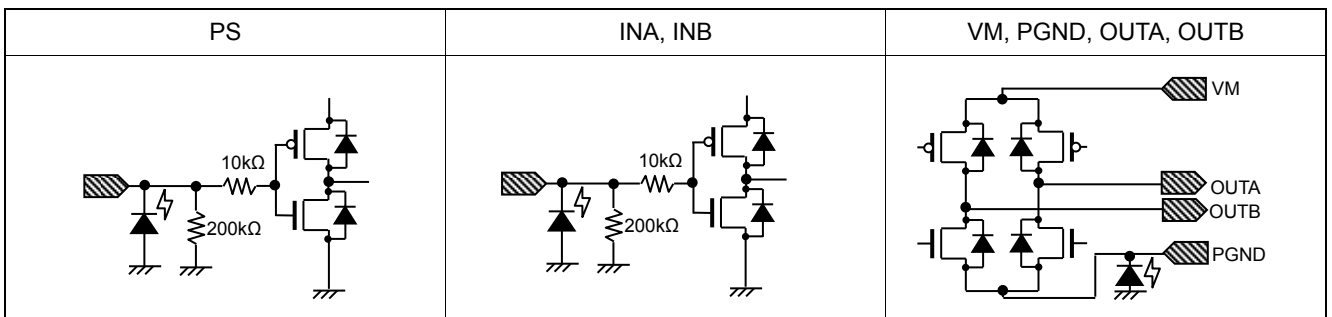


Figure 8.
Power Dissipation vs Ambient Temperature

I/O equivalent circuits



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal(GND) and large-current ground(PGND) traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

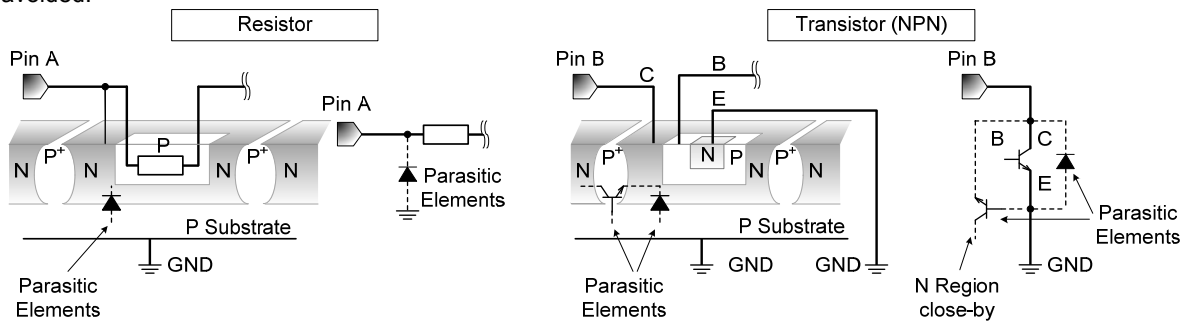


Figure 9.

Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

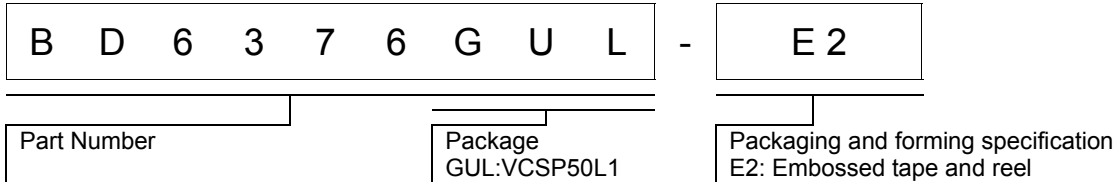
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

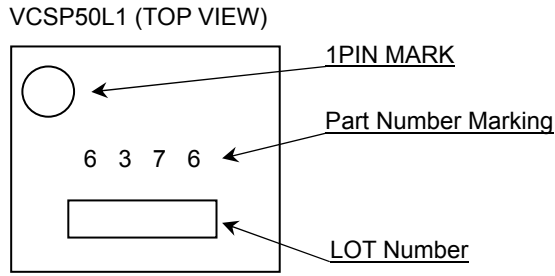
16. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information



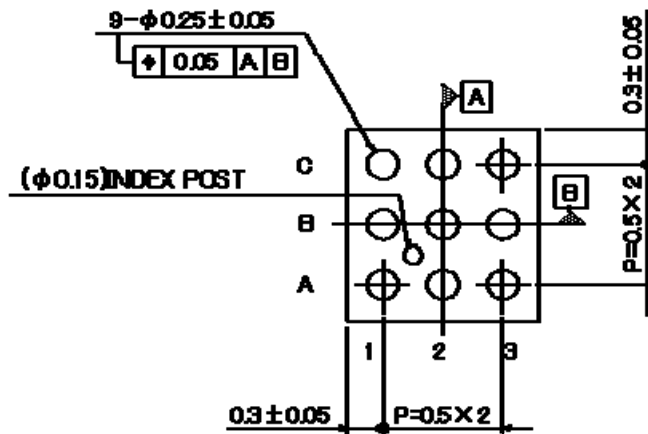
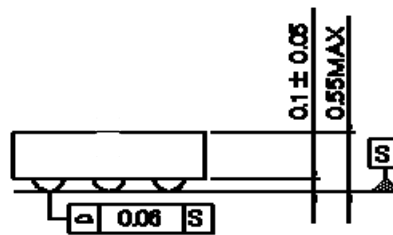
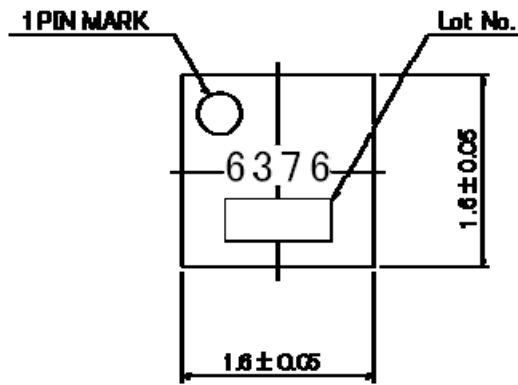
Marking Diagram



Part Number Marking	Package	Orderable Part Number
6376	VCSP50L1	BD6376GUL-E2

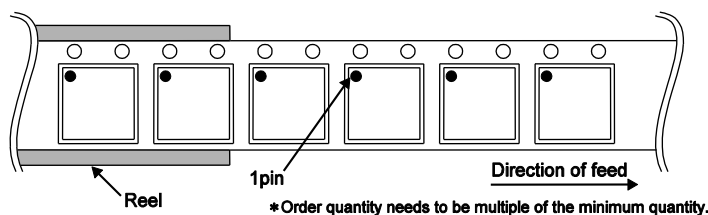
Physical Dimension, Tape and Reel Information

Package Name	VCSP50L1
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<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
03.Aug.2012	001	New release
06.Feb.2014	002	p1 Change [1-2ch] to [1ch]
10.Feb.2016	003	Applied the ROHM Standard Style and improved understandability.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
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- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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[LB1938FAGEVB](#)