Motor Drivers for Printers

System Driver for Ink Jet Printers

BD64550EFV

No.10016EAT03

●Description

This is 1-chip system motor driver integrating 2-channel H-bridge driver, step-down switching regulator with built-in power DMOS, series regulator and reset output.

●Features

1) Low-on resistance output H-bridge driver (2-channel)
2) Constant-current chopping drive H-bridge driver
3) Switching regulator with built-in P-channel power DMOS FET
4) Soft start function: 23.6 ms (Typ.)
5) Reset release timer: 80 ms (Typ.)
6) 16 bit serial interface
7) Logic input interface (serial/parallel changeable)
8) Ultra thin type high heat dissipation HTSSOP-B40 package
9) Overcurrent protection in H-bridge driver block
10) Input voltage low voltage protection in H-bridge driver block
11) Overcurrent protection in switching regulator block
12) Output overvoltage protection in switching regulator block
13) Output low voltage protection in switching regulator block
14) Thermal shutdown

●Applications

Inkjet printer, photo printer, etc.

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
VM applied voltage	V_M	40	V
Logic input voltage	V_L	-0.4 ~ 5.5	V
RIN applied voltage	V_{RIN}	5.5	V
RNF voltage	V_{RNF}	0.5	V
Power dissipation	Pd	1600*	mW
Operating temperature range	T_{OPR}	-25 ~ +85	℃
Storage temperature range	T_{STG}	-55 ~ +150	℃
Junction temperature	T_{jmax}	150	℃
Motor driver output current (peak 500 ns)	I_{omax} (peak)	8.0	A
Motor driver output current (DC)	I_{omax} (DC)	2.5**	A
Switching regulator output current (DC)	I_{omax}	0.5	A
Series regulator output current (DC)	I_{omax}	0.25	A

* Reduced by 12.8 mW/℃ over 25 ℃, when mounted on a glass epoxy board (70 mm x 70 mm x 1.6 mm).
** Must not exceed Pd or ASO.

●Operating Conditions

Parameter	Symbol	Limit	Unit
VM operating power supply voltage range	V_M	7 ~ 36	V
SCLK max. operating frequency	F_{SCLK}	20	MHz
Switching regulator output voltage range	V_{swreg}	3 ~ 5	V

●Electrical Characteristics (Unless otherwise specified, Ta=25℃, V_M=24V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
VM current 1	I_{VM1}	-	-	8	mA	V_M=7V
VM current 2	I_{VM2}	-	-	12	mA	V_M=24V
H-bridge 1						
Output on resistance (source side))	R_{ONH1}	-	0.6	0.78	Ω	I_o=1A
Output on resistance (sinking side)	R_{ONL1}	-	0.4	0.52	Ω	I_o=1A
Output leak current	I_{LEAK1}	0	-	10	μA	V_M=36V
Built-in diode forward direction voltage (source side)	V_{FH1}	0.6	0.9	1.2	V	I_o=1A
Built-in diode forward direction voltage (sinking side)	V_{FL1}	0.6	0.9	1.2	V	I_o=1A
H-bridge 2						
Output on resistance (source side)	R_{ONH2}	-	0.7	0.91	Ω	I_o=1A
Output on resistance (sinking side)	R_{ONL2}	-	0.5	0.65	Ω	I_o=1A
Output leak current	I_{LEAK2}	0	-	10	μA	V_M=36V
Built-in diode forward direction voltage (source side)	V_{FH2}	0.6	0.9	1.2	V	I_o=1A
Built-in diode forward direction voltage (sinking side)	V_{FL2}	0.6	0.9	1.2	V	I_o=1A
Current control						
VREF voltage range	V_{REF}	0.8	-	3.5	V	
VREF pin outflow current	I_{REF}	-	0	1	μA	
RNF pin outflow current	I_{RNF}	5	15	30	μA	
RNFS pin outflow current	I_{RNFS}	-	0	1	μA	
VREF-RNFS offset voltage	V_{OFFSET}	-15	0	15	mV	VREF=2V
Control logic						
High input voltage	V_{INH}	2.0	-	5.5	V	
Low input voltage	V_{INL}	0	-	0.8	V	
Input current	I_{IN}	21	33	45	μA	Input voltage=3.3V
Switching power source						
DSEN threshold voltage	V_{SWBIAS}	0.873	0.9	0.927	V	
Output on resistance	R_{SWON}	-	0.8	1.04	Ω	At I_o=250mA
Leak current	I_{SWLEAK}	0	-	10	μA	V_M=36V
DUTY_MAX value	D_{MAX}	-	92	-	%	
Clock frequency	F_{SW}	130	200	270	kHz	
DSEN pin outflow current	I_{DSEN}	-	0	1	μA	
Series power source						
Output voltage	V_{SOUT}	1.425	1.5	1.575	V	At I_o=70mA
Leak current	I_{SLEAK}	0	-	10	μA	
RESET pin						
Output voltage	V_{RSTL}	0	-	0.2	V	I_{DRAIN}=1mA
Leak current	$I_{RSTLEAK}$	0	-	10	μA	
High VM threshold voltage	V_{MPORH}	6.3	6.5	6.7	V	V_M at power on
Low VM threshold voltage	V_{MPORL}	5.9	6.1	6.3	V	V_M at power off
High motor UVLO voltage	V_{MMTH}	13.5	15	16.5	V	Off motor only
Low motor UVLO voltage	V_{MMTL}	12.5	14	15.5	V	
Reset delay time	T_{POR}	50	80	110	ms	

●Reference Data

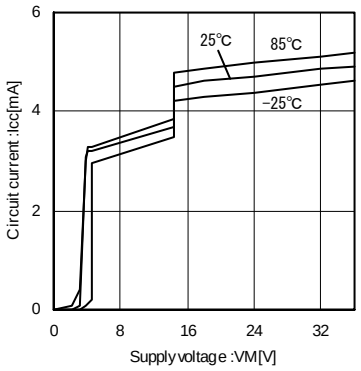


Fig.1 VM Current

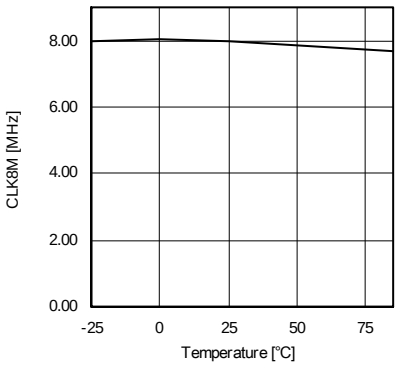


Fig.2 Internal Reference Clock (VM=24V)

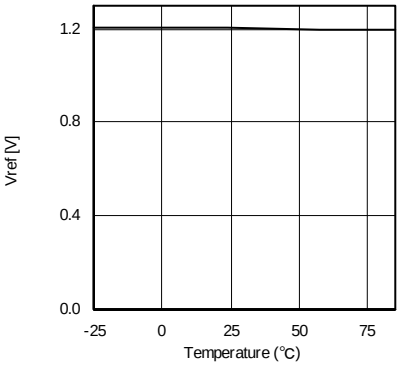


Fig.3 Temperature dependence of Internal Standard Voltage (VM=24V)

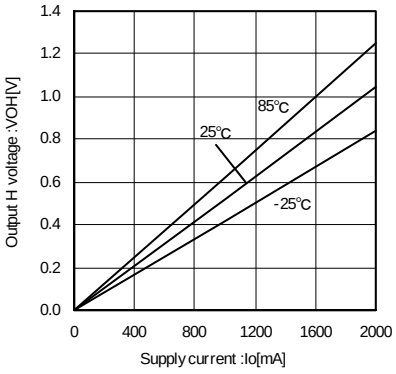


Fig.4 OUT1 High Output Voltage (source side)

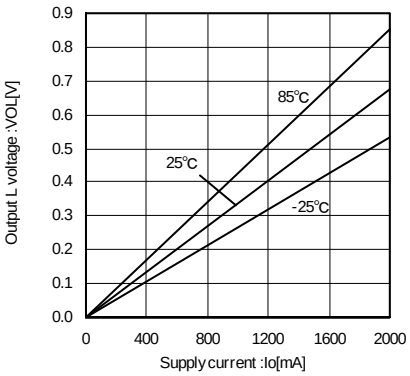


Fig.5 OUT1 Low Output Voltage (sinking side)

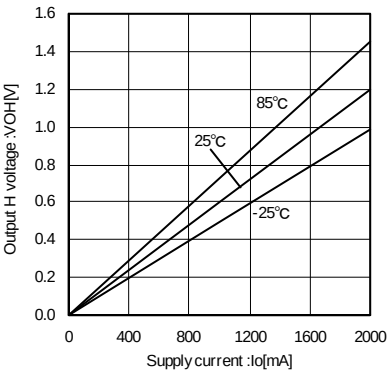


Fig.6 OUT2 High Output Voltage (source side)

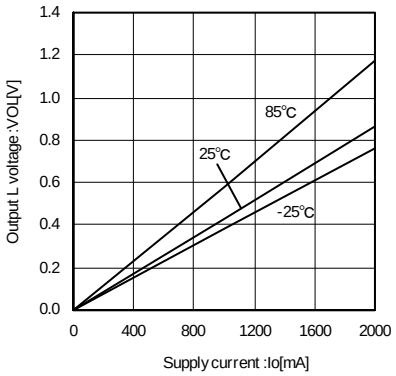


Fig.7 OUT2 Low Output Voltage (sinking side)

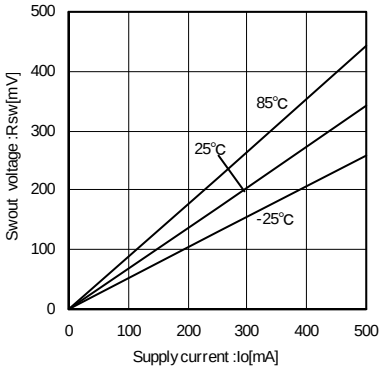


Fig.8 Switching Regulator High Output Voltage

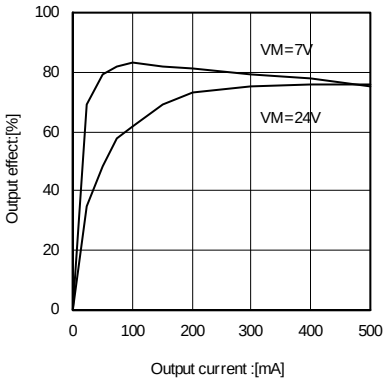


Fig.9 Switching Regulator Efficiency (Ta=25℃)

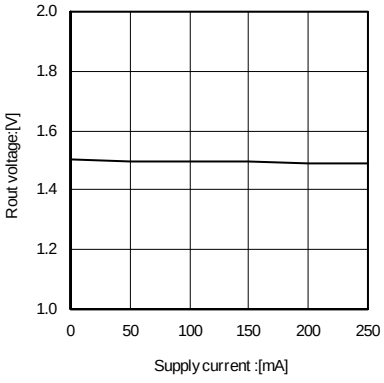


Fig.10 Series Regulator Load Regulation (VM=24V, Ta=25℃)

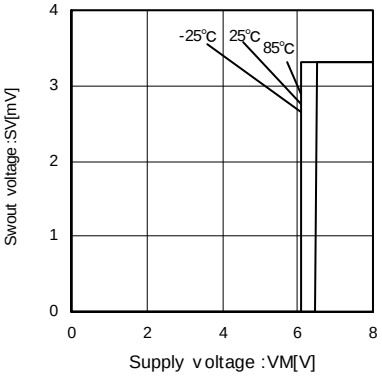


Fig.11 Reset Output (Pull up to switching regulator at 10kΩ)

●Block Diagram, Application Circuit Diagram, and Pin Function

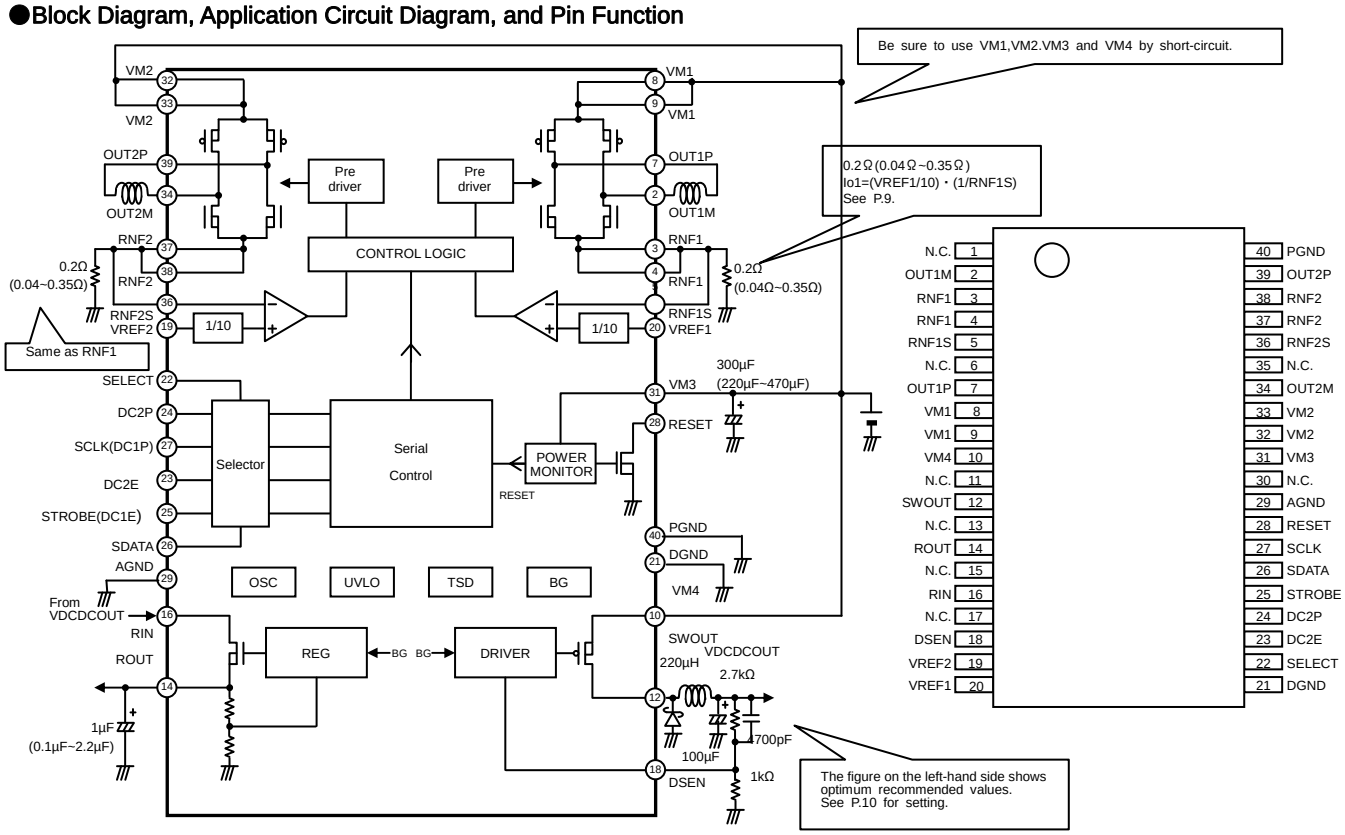


Fig.12 Block Diagram and Application Circuit Diagram

Fig.13 Pin Assignment Diagram

No.	Pin name	Function
1	NC	Non Connection
2	OUT1M	H-bridge output pin 1M
3	RNF1	Output current detection pin 1
4	RNF1	Output current detection pin 1
5	RNF1S	Output current detection input pin
6	NC	Non Connection
7	OUT1P	H-bridge output pin 1P
8	VM1	Motor power supply pin
9	VM1	Motor power supply pin
10	VM4	Switching regulator power supply pin
11	NC	Non Connection
12	SWOUT	Switching regulator output pin
13	NC	Non Connection
14	ROUT	Series regulator output pin
15	NC	Non Connection
16	RIN	Series regulator power supply pin
17	NC	Non Connection
18	DSEN	Switching regulator voltage sense pin
19	VREF2	Reference voltage input pin
20	VREF1	Reference voltage input pin

No.	Pin name	Function
21	DGND	Digital GND
22	SELECT	Input pin select pin
23	DC2E	H-bridge 2 side enable input pin
24	DC2P	H-bridge 2 side phase pin
25	STROBE	Serial port strobe input pin / H-bridge 1 side enable pin
26	SDATA	Serial port data input pin
27	SCLK	Serial port clock input pin / H-bridge 1 side phase input pin
28	RESET	Reset signal output pin
29	AGND	ANALOG GND
30	NC	Non Connection
31	VM3	Power supply pin
32	VM2	Motor power supply pin
33	VM2	Motor power supply pin
34	OUT2M	H-bridge output pin 2M
35	NC	Non Connection
36	RNF2S	Output current detection input pin
37	RNF2	Output current detection pin 2
38	RNF2	Output current detection pin 2
39	OUT2P	H-bridge output pin 2P
40	PGND	POWER GND

* Precaution regarding VM pin
If you use VM1, VM2, VM3 and VM4 not by short-circuit, they may be destroyed. Be sure to use them by short-circuit.
And be sure to set up a bypass capacitor (220μF to 470μF) closer to VM3 pin as much as possible.

●Pin selection function

Either serial control or external PWM control can be selected for motor control type with SELECT pin (pin 22).

SELECT	Output state
L	Serial input mode
H	External PWM control mode

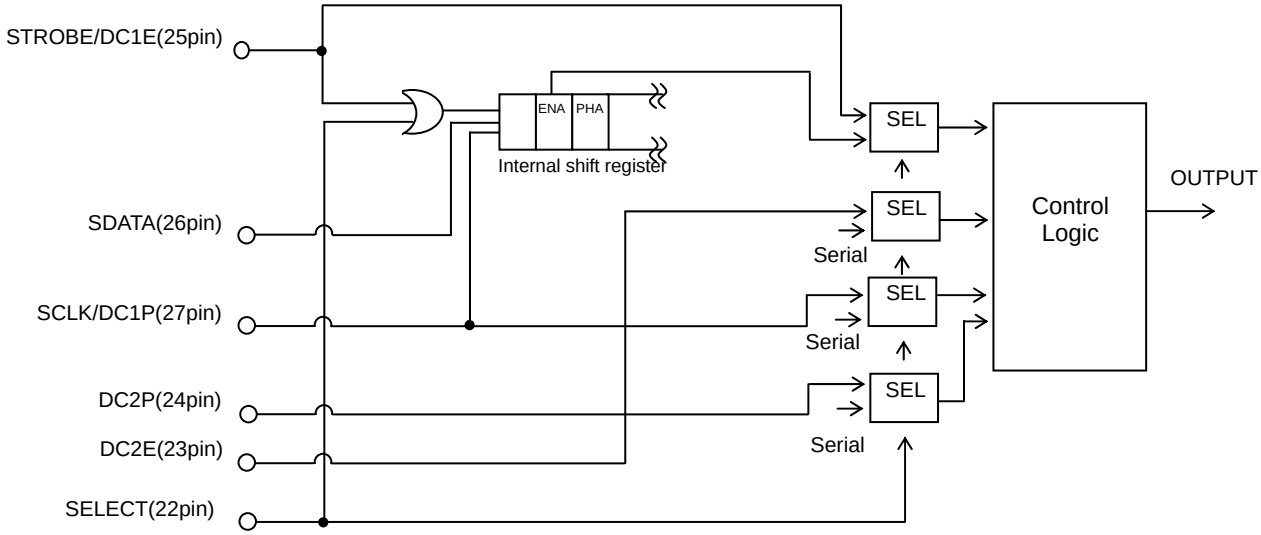


Fig.14 Serial Input Block Diagram

The input/output logic at SELECT = H is as follows.

DC1E/DC2E	Output state
L	Open
H	ACTIVE

DC1P/DC2P	OUTP	OUTM
L	SINK	SOURCE
H	SOURCE	SINK

○Procedure of DC motor drive by external PWM control

1) Serial setting
   Set the serial by SELECT pin = L. (WORD_S and WORD_D setting)
   - WORD_S (see P.7) is a drive parameter for setting OFF_TIME, BLANK TIME etc.
   - WORD_D (see P.7) is for drive setting to set drive mode of each H-bridge.
     When setting WORD_D (see P.7), make sure that ENABLE signal (ENABLE_1、ENABLE_2) of serial bit is L.
     If ENABLE signal is H, the motor may operate.
     Input of DC2P pin can be either H or L.

2) External PWM drive mode switch
   Set external PWM drive mode by SELECT pin = H.
   Switch by DC1E (STROBE)/CD2E pin = L when switching SELECT pin.

3) Drive
   PHASE, ENABLE pin input signal (DC1E/DC1P/DC2E/DC2P) drives in external PWM mode.

●Serial interface

16-bit 3-linear type serial interface (SDATA (pin 26), SCLK (pin 27), STROBE (pin 25)) is provided to set the operation and the value of current limit. Data are sent to the internal shift register by falling edge of SCLK pin in the area L of STROBE pin. Data of shift register are written in an appropriate address of internal memory of 2*15 bits by rising edge of STROBE pin according to address data of D15.The input order of serial data is from D0 to D15.

Address data

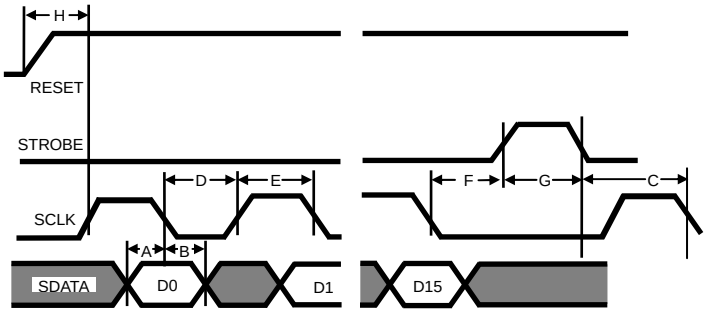
D15	Word select
0	WORD_S
1	WORD_D

Memory data allocation

BIT	WORD_S	Default	WORD_D	Default
D0	Rohm_Reserve[2]	0	Rohm_Reserve[11]	0
D1	Rohm_Reserve[1]	0	Rohm_Reserve[10]	0
D2	Rohm_Reserve[0]	0	Rohm_Reserve[9]	0
D3	OFF TIME_2[2]	0	Rohm_Reserve[8]	0
D4	OFF TIME_2[1]	0	Rohm_Reserve[7]	0
D5	OFF TIME_2[0]	0	Rohm_Reserve[6]	0
D6	BLANK TIME_2[1]	0	Rohm_Reserve[5]	0
D7	BLANK TIME_2[0]	0	Rohm_Reserve[4]	0
D8	OFF TIME_1[2]	0	Rohm_Reserve[3]	0
D9	OFF TIME_1[1]	0	PWM_MODE_2	0
D10	OFF TIME_1[0]	0	S_PHASE_2	0
D11	BLANK TIME_1[1]	0	S_ENABLE_2	0
D12	BLANK TIME_1[0]	0	PWM_MODE_1	0
D13	MASK SELECT	0	S_PHASE_1	0
D14	SWOFF	0	S_ENABLE_1	0

The timing of serial report writing is shown in the right figure.
And the minimum timing of each is as follows:

A：SDATA setup time‥‥‥‥‥‥‥‥‥‥‥‥‥‥‥‥‥‥ 10nsec
B：SDATA hold time‥‥‥‥‥‥‥‥‥‥‥‥‥‥‥‥‥‥‥ 10nsec
C：Setup STROBE to SCLK falling edge‥‥ 50nsec
D：SCLK low pulse width‥‥‥‥‥‥‥‥‥‥‥‥‥‥ 25nsec
E：SCLK High pulse width‥‥‥‥‥‥‥‥‥‥‥‥‥ 25nsec
F：Setup SCLK falling edge to STROBE‥‥ 25nsec
G：STROBE pulse width‥‥‥‥‥‥‥‥‥‥‥‥‥‥‥ 50nsec
H：Setup RESET to SCLK Rising‥‥‥‥‥‥‥‥‥ 50µsec



○RESET signal is an internal RESET signal and generated inside IC at the same timing of external RESET output.
○STROBE, SCLK and SDATA signals are input signals through external ASIC.

Fig.15 Serial Signal Input Timing

●Serial Port Explanation

WORD_S

○SWOFF

Set on/off of switching regulator circuit.

0	Switching regulator on
1	Switching regulator off

○MASK SELECT

Common mask can be provided to 2-phase H-bridge drive noise mask (BLANK time).

0	Independent mask on single-phase/two-phase.
1	Common mask on single-phase/two-phase.

○BLANK TIME

Current-limit comparator monitors RNF pin voltage to set limit to current, but during the period from switching on to BLANK TIME, detection becomes invalid in order to avoid wrong detection caused by spike noise that happens at the time of switching on. See P.8 for details.And during the period from ENABLE signal on to BLANK TIME at switching of PHASE signal, detection becomes invalid as well.

[1]	[0]	BLANK TIME	Unit
0	0	2.0	µs
0	1	3.0	µs
1	0	4.0	µs
1	1	5.0	µs

○OFF TIME

Set current decay time.

[2]	[1]	[0]	OFF TIME	Unit
0	0	0	6	µs
0	0	1	8	µs
0	1	0	10	µs
0	1	1	12	µs
1	0	0	14	µs
1	0	1	16	µs
1	1	0	18	µs
1	1	1	20	µs

WORD_D

○S_ENABLE_1/S_ENABLE_2

Each bridge on/off signal. Output state is as follows.

	Output state
0	Open
1	ACTIVE

○S_PHASE_1/S_PHASE_2

Set the direction of current of each bridge. Output state is as follows.

	P	M
0	SINK	SOURCE
1	SOURCE	SINK

○PWM_MODE_1/PWM_MODE_2

Set current decay mode in bridge1 and 2. (See page 8 for details about each mode.)

0	FAST DECAY
1	SLOW DECAY

(※)Rohm_Reserve

Rohm_Reserve is special mode setting port for inspection at shipment. Especially, if Rohm Reserve [3], [4], [5], [7], [8], [9], [10], [11] is set to H by mistake, malfunction may be caused. Be sure not to set.

●H-bridge Driver Operation

This IC has built-in 2-channel H-bridge driver.
Each can be used for DC motor drive independently.

1. Current setting

Motor output current-limit value can be set according to the equation below.

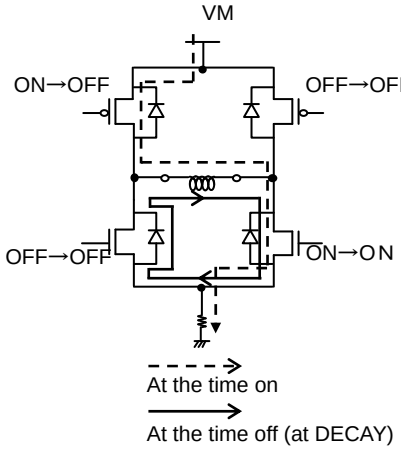
Io=(VREF/10)・(1/RNFS) [A]

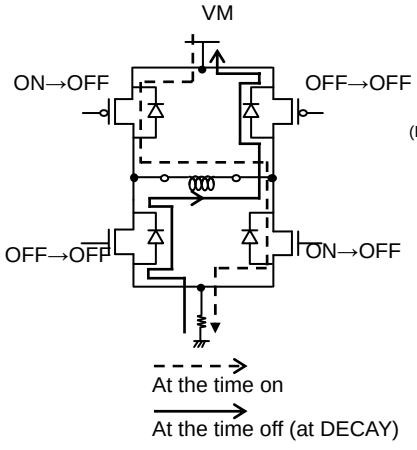
Decide within the range VREF = 0.8V to 3.5V, RNFS = 0.04Ωto 0.35Ω.

2. DECAY mode

Current decay mode can be selected from serial input at the time of motor chopping drive.
Each mode and timing is as follows.

○SLOW DECAY mode ○FAST DECAY Mode ○Timing chart





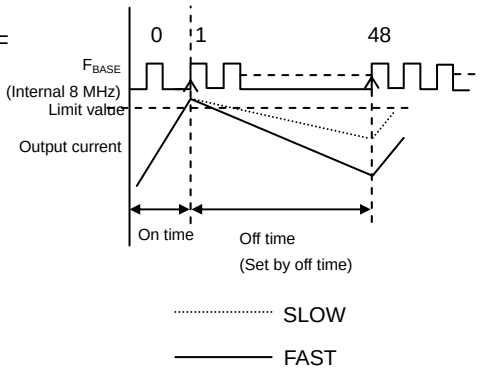


Fig.16 On/Off Timing at SLOW Fig.17 On/Off Timing at FAST Fig.18 DECAY Mode Timing Chart

3. Protection area for output current value wrong detection

In order to avoid wrong detection of current detection comparator by varistor current element in each motor, current detection are masked at the timing as follows.

①PHASE switching time
②ENABLE on time
③When output is on after OFF_TIME is finished at the time of current chopping drive

①PHASE switching time

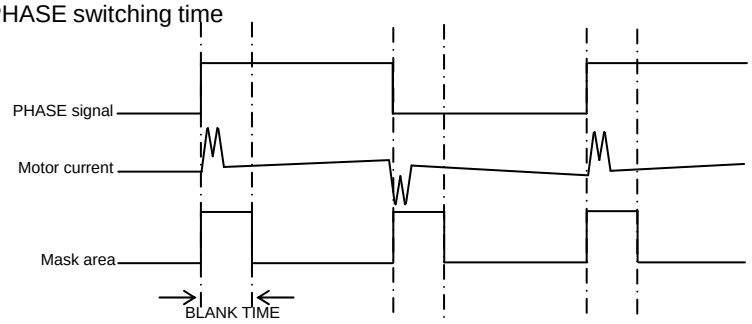
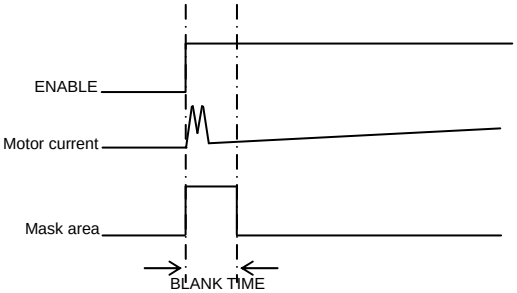


Fig.19 Timing Chart of PHASE Switching Time

②ENABLE on time



③Current chopping driving time

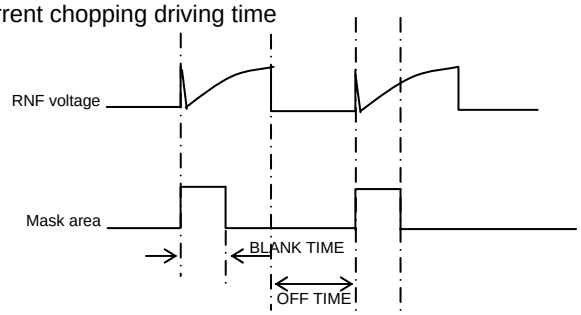


Fig.20 Timing Chart of ENABLE On Timing Fig.21 Timing Chart of Current Chopping Driving Time

●Switching regulator operation

○Basic operation

A switching regulator circuit that repeats on/off being synchronized with internal CLK (200 KHz) is built-in.

The start up output voltage SWOUT (pin 12) becomes up and run step by step with soft start at the VM power-on ($VM \geqq V_{MPORH}$).The output voltage is determined by the equation below with external resistance.

$$VOUTDCDC = VBIAS \cdot \{(R1+R2)/R2\} \quad [V]$$

The setting should be performed so that the switching regulator output voltage (VOUTDCDC) waveform is optimized within the range of VOUTDCDC = 3V to 5V, VBIAS = 0.9V (Typ.), R1 + R2 = 1kΩ to 10kΩ, C1 = 1,000pF to 10,000pF.

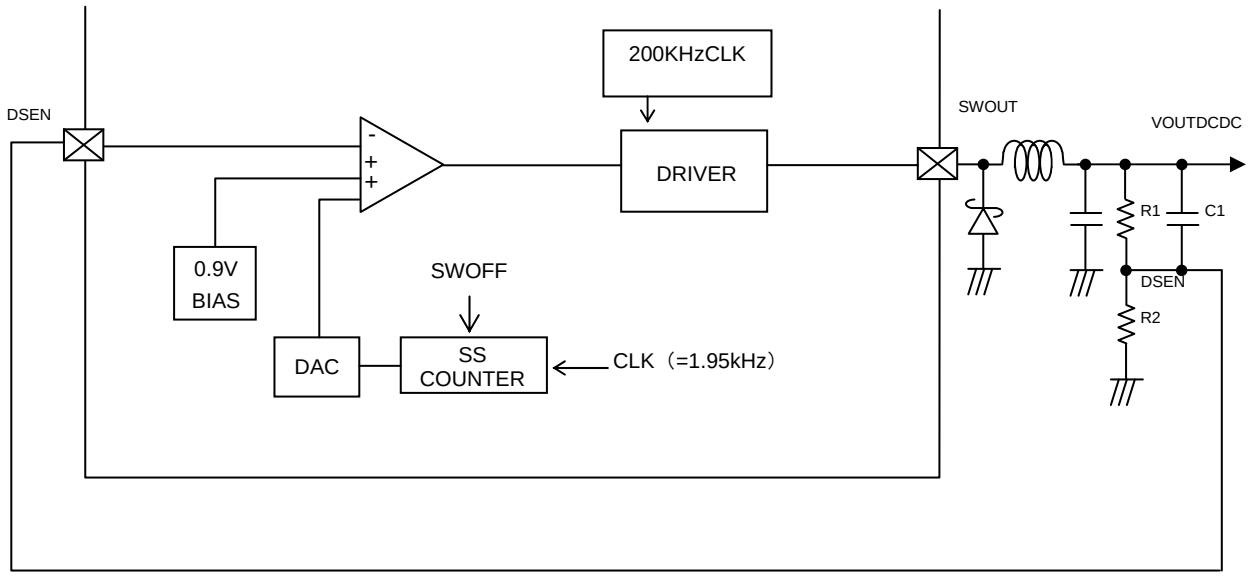


Fig.22 Switching Regulator Block Diagram

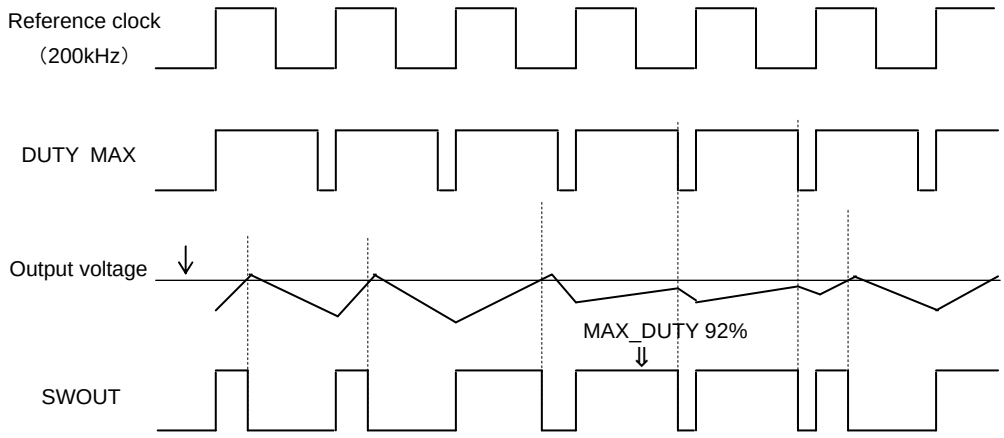


Fig.23 Timing Chart of Switching Regulator Operation

○Soft start

As shown in Fig.24, VOUTDCDC output voltage becomes up and run step by step with soft start at the time of power-on.

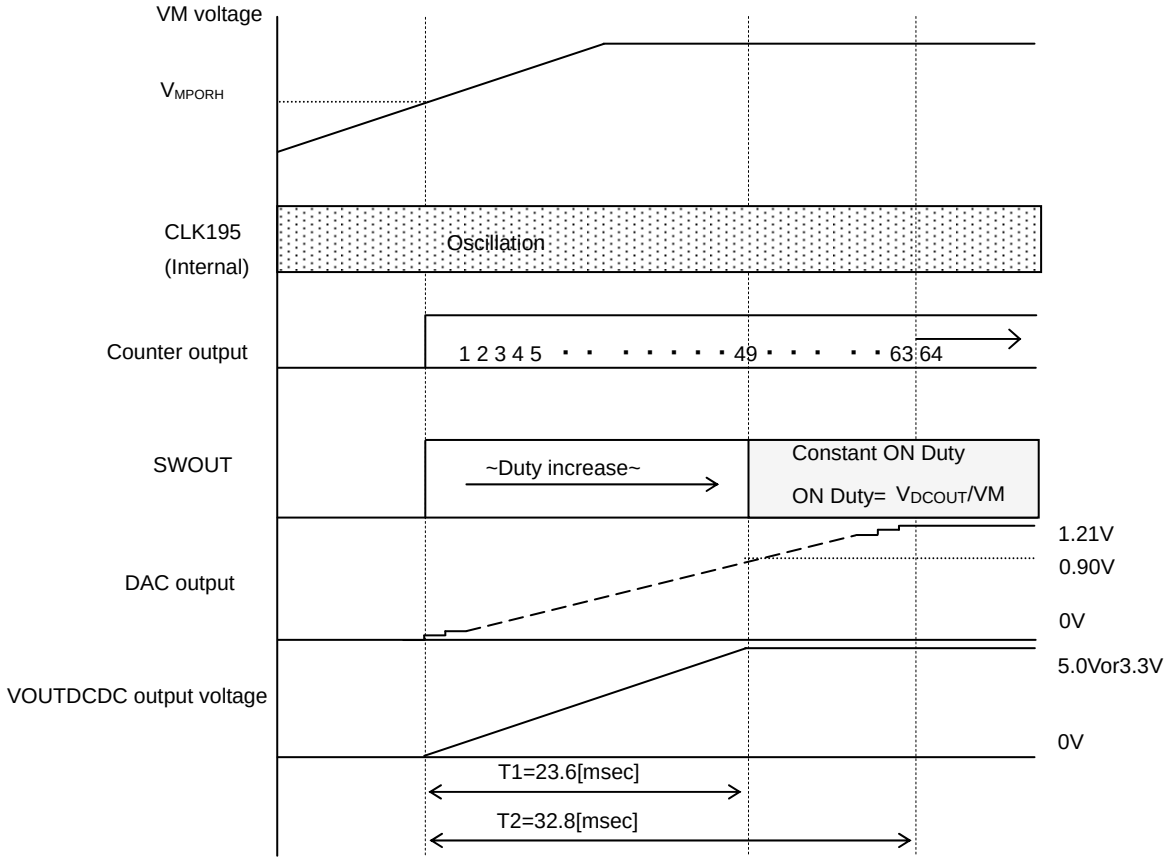


Fig.24 Soft Starting Time Timing Chart

This soft start method is realized by changing comparator positive side voltage that determines output duty of switching regulator to linear using DAC.

Soft start time T1 is constant value regardless of VM voltage.

Soft start time	T1=23.6msec(typ.)
Count finish time	T2=32.8msec(typ.)

○Series regulator operation

Inputting switching regulator output into RIN pin (pin 16) enables to drive series regulator circuit.

At the time of power-on, output voltage start up step by step with soft starting at the same timing as switching regulator circuit.^Soft start time is 23.6ms (Typ.).

Regarding external capacitor of ROUT pin (pin 14), it works normally without setting. But switching noise of switching regulator becomes easy to get in due to dragging on board pattern and the like. Pay attention to switching noise.

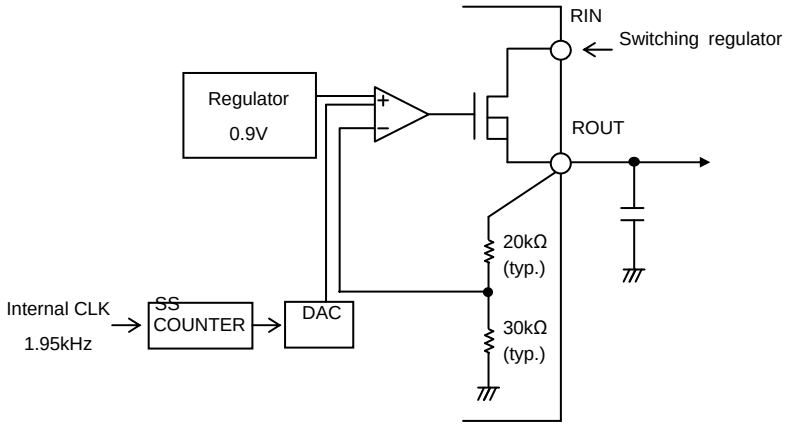


Fig.25 Series Regulator Block Diagram

●Protection function

○Protection circuit function

Overall	Overheating protection
DC motor drive circuit	Overcurrent protection
Switching regulator circuit	Overcurrent protection, output overvoltage protection, output low voltage protection
Series regulator circuit	None

○Operation at protection circuit operation

①Overheating protection・・・All functions are shutout along with junction temperature rise

Thermal shutdown temperature	175℃(typ.)

	Switching regulator	Series regulator	DC motor	RESET	Re-start
At protection operation	OFF	OFF	OFF	L	Again power-on

②Overcurrent protection (Switching regulator)

	Set current	Mask time	State after operation
I_{SWOC}	2.6(A)	0.5μsec(※)	All function shutout

	Switching regulator	Series regulator	DC motor	RESET	Re-start
Operating	OFF	OFF	OFF	L	Again power-on

③Overcurrent protection (DC motor)

	Set current	Mask time	State after operation
I_{DCOC}	3.8(A)	1.5μsec	Shown below

	Switching regulator	Series regulator	DC motor	RESET	Re-start
Operating	ON	ON	OFF	L_PULSE	Serial re-input

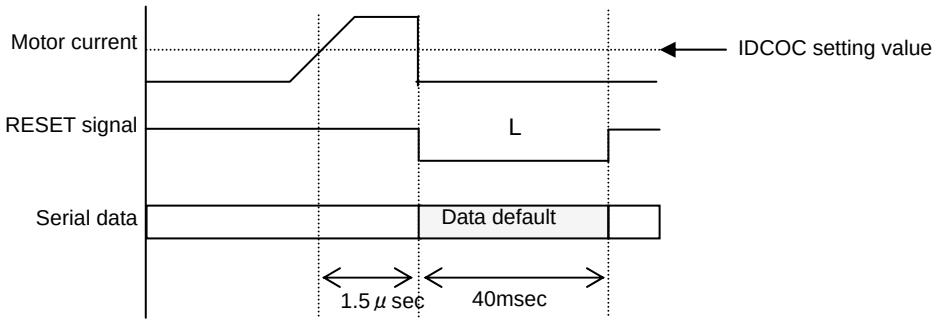


Fig.26 Timing Chart of Motor Overcurrent Protection

(※) If the output pulse of switching regulator is 0.5μs or below, the overcurrent function does not operate even at the time of overcurrent outflow.

④Low voltage protection/overvoltage protection circuit

All functions are shutout on the condition of setting value (+30%, -30%) while DSEN pin voltage (pin 18) of switching regulator circuit is monitored.

	Set voltage	Mask time	State after operation
VSWLV	0.60(V)	10µsec	All function shutout
VSWOH	1.20(V)	10µsec	All function shutout

Note that output overvoltage and output low voltage protection does not work until soft start count finish (32.8 ms, Typ.) at the time of start up of DC/DC power after power-on.

	Switching regulator	Series regulator	DC motor	RESET	Re-start
Operating	OFF	OFF	OFF	L	Again power-on

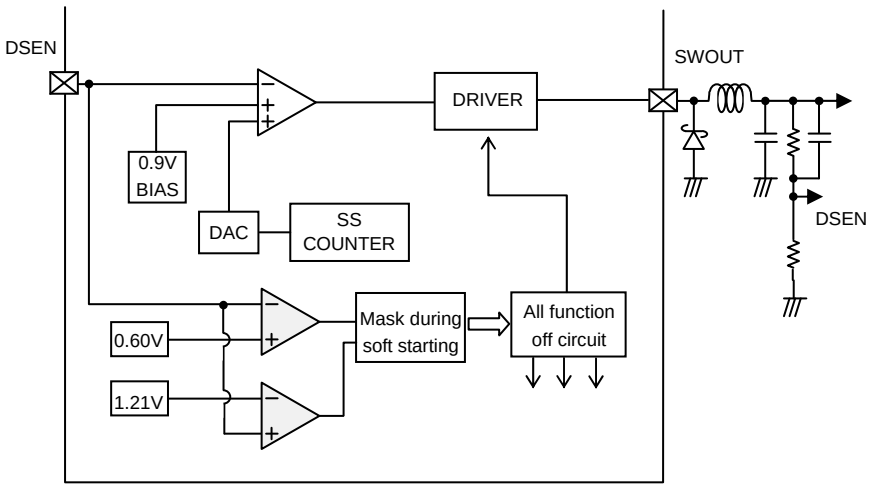


Fig.27 Switching Regulator Block Diagram

○RESET function

Power-on RESET circuit is built-in for VM power source.

H is output at RESET pin through DELAY time of internal counter when power voltage goes up to V_{MPORH} (6.5 V, Typ.) or higher at the time of power-on. In addition, hysteresis is set up at the time of power-down to output L at RESET pin with VMPORL (6.1 V, Typ.) And no response time (2.5µs, Typ.) of voltage detection is set in order to avoid wrong detection by sudden power-off.If protection circuits other than overcurrent protection of motor starts operating, RESET is not released if VM power is not on again.

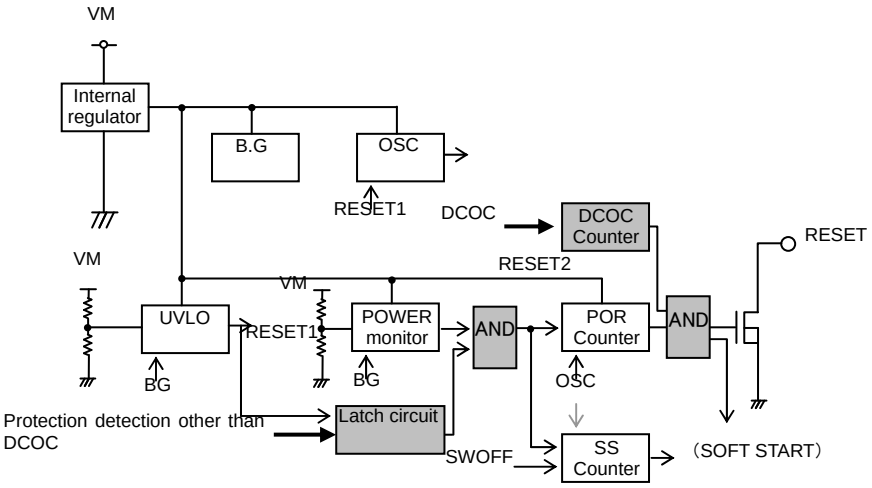
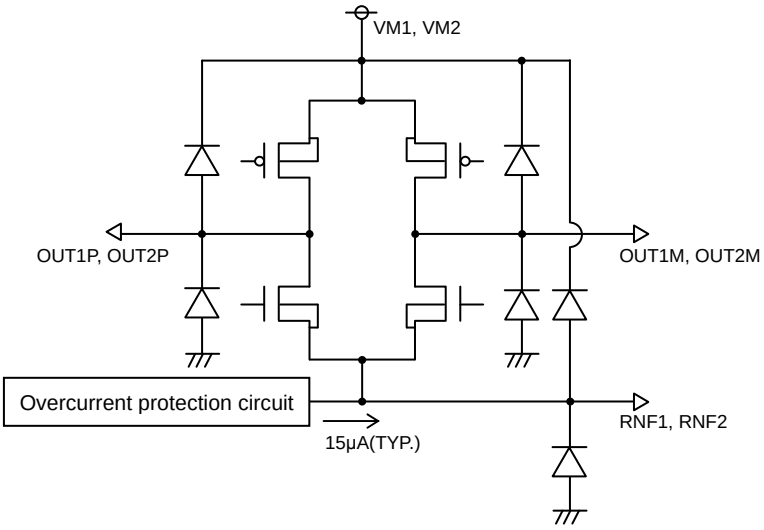


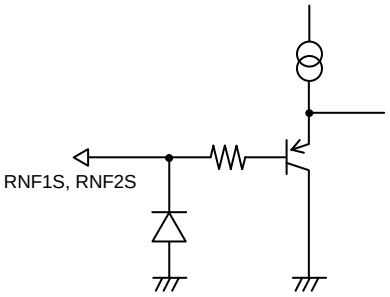
Fig.28 RESET Internal Circuit Block Diagram

●I/O Circuit Diagram

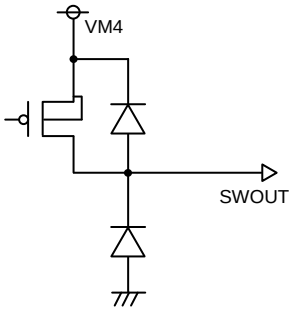
① OUT1P, OUT1M, OUT2P, OUT2M, RNF1 and RNF2



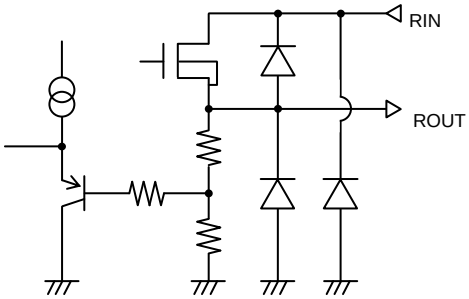
② RNF1S and RNF2S



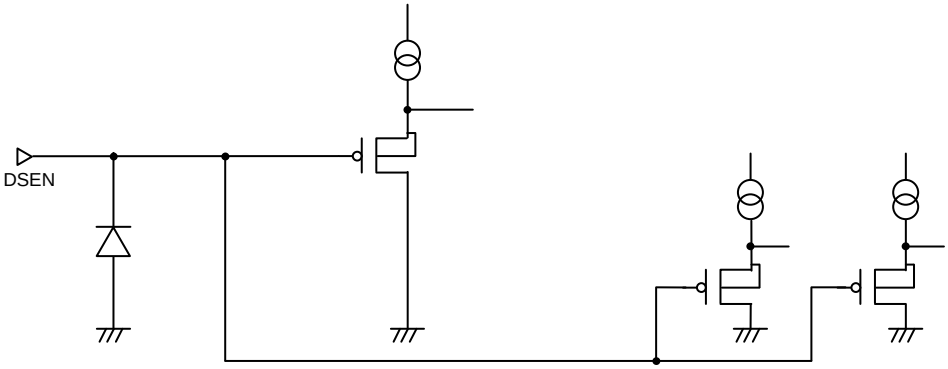
③ SWOUT



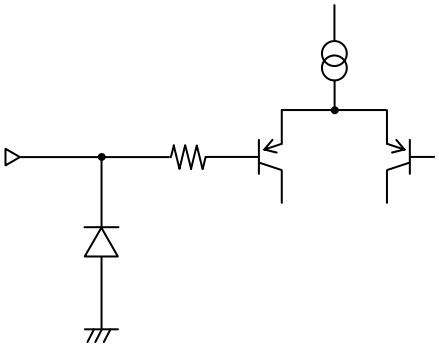
④ RIN and ROUT



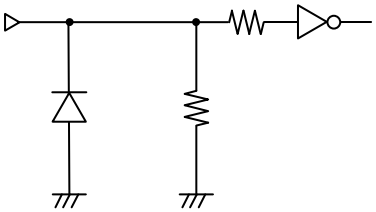
⑤ DSEN



⑥ VREF1 and VREF2



⑦ Logic input



⑧ RESET

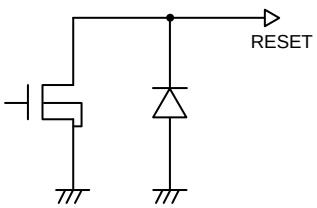


Fig.29 I/O Circuit

●Power Dissipation Reduction

On the backside of HTSSOP-B40 package, metal is filled in. Heat dissipation is possible by letting in a through hole from backside. Power dissipation can be improved by providing heat dissipation pattern of copper foil or the like not only on the board surface but also on the backside. The metal on the backside shorts with the backside of IC tip and the potential is GND. Therefore, avoid shorts with other potential than GND, or malfunction or destruction may happen. It is recommended that backside metal should short with GND by soldering.

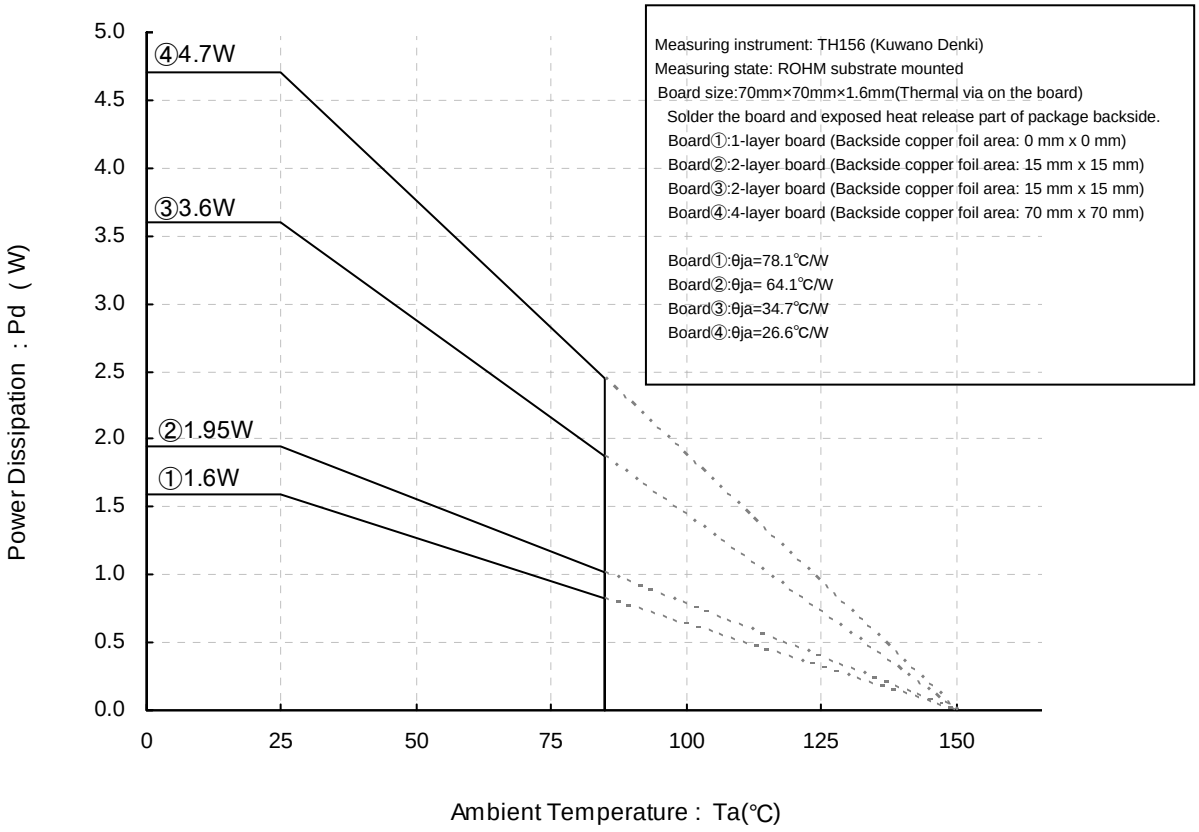


Fig.30 Power Dissipation Reduction

●Notes for Use

1) Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) Connecting the power supply connector backward
   Connecting the power supply connector backwards may result in damage to the IC. Insert external diodes between the power supply and the IC's power supply pins as well as the motor coil to protect against damage from backward connections.

3) Power supply lines
   As return of current regenerated by back EMF of motor happens, take steps such as putting capacitor between power supply and GND as a electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value.
   If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

4) GND potential
   Ensure a minimum GND pin potential in all operating conditions.

5) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. BD64550EFV expose its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency . Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.

6) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

7) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

8) ASO
When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9) Thermal shutdown circuit
The IC has a built-in thermal shutdown circuit (TSD circuit). If the chip temperature becomes Tjmax=150℃, and higher, coil output to the motor and regulator output will be OFF, and reset output will be L. The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect or indemnify peripheral equipment. Do not use the TSD function to protect peripheral equipment.

10) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

11) Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when a resistor and transistor are connected to pins as shown in Fig. 31,

- ○the P/N junction functions as a parasitic diode
  when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
- ○Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins.

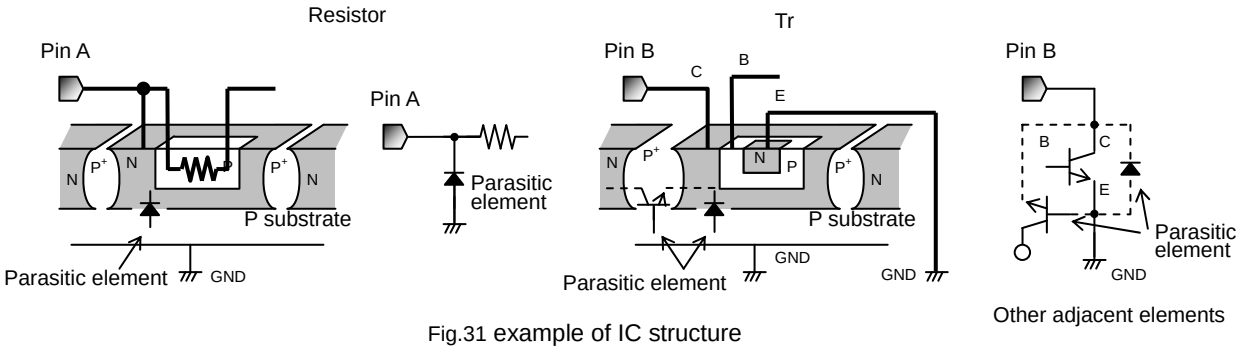


Fig.31 example of IC structure

12) Ground Wiring Pattern
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●Ordering Part Number

B	D	6	4	5	5	0	E	F	V	-	E	2

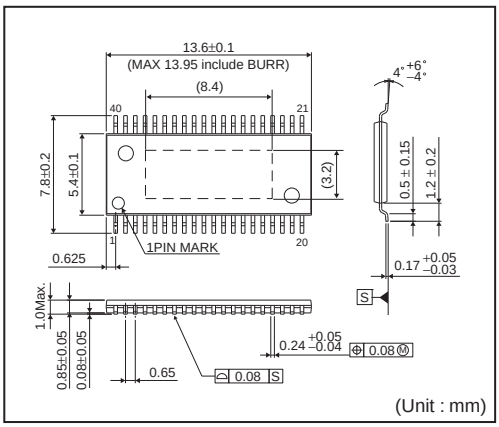
Part No. (BD)

Part No. (64550)

Package
EFV : HTSSOP-B40

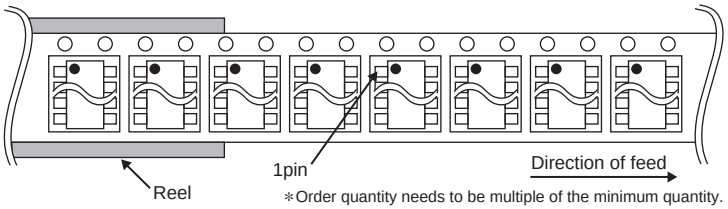
Packaging and forming specification
E2: Embossed tape and reel

HTSSOP-B40



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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