## Load Switch ICs

# 0.5A Current Load Switch ICs <br> for Portable Equipment 

## BD6524HFV

## General Description

BD6524HFV is a high side switch IC using an N -Channel MOSFET and used as a power switch for in memory card slot. This switch has an ON-Resistance of $200 \mathrm{~m} \Omega$ (Typ). Operations using low input voltage ( $\mathrm{V}_{\text {IN }} \geq 3.0 \mathrm{~V}$ ) are possible for various switch applications. The switch turns ON slowly by the built-in charge pump; therefore, it is possible to reduce inrush current during switch ON. There is no parasitic diode between the drain and the source so reverse current flowing at switch OFF is prevented. Furthermore, it has a discharge circuit that releases electric charge from capacitive load at switch OFF. This IC is available in a space-saving HVSOF6 package.

## Features

■ Built in N-MOS Switch with Low ON-Resistance (200m $\Omega$, Typ)
■ Maximum Output Current : 500mA

- Soft Start Function
- Under Voltage Lockout (UVLO) Protection
- Built in Discharge Circuit: Operations at Switch OFF, UVLO
- Reverse Current Flow Blocking at Switch OFF Condition


## Applications

Memory Card Slots for Notebook PC, Digital still Camera, Portable Music Player, Compact Portable Devices such as PDA and so forth.

## Key Specifications

■ Input Voltage Range:
3.0 V to 5.5 V

- ON-Resistance: $\left(\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}\right)$

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\left(\mathrm{V}_{\mathrm{IN}}=3.3 \mathrm{~V}\right)
$$

$200 \mathrm{~m} \Omega$ (Typ)
250m (Typ)

- Continuous Current:
- Standby Current:
$0.1 \mu \mathrm{~A}$ (Typ)
- Operating Temperature Range:
$-25^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$

$$
\begin{array}{llll}
\text { Package } & \text { W(Typ) } & \mathrm{D}(\mathrm{Typ}) & \mathrm{H}(\text { Max })
\end{array}
$$



## Typical Application Circuit



## Block Diagram



## Pin Configuration



Pin Description

| Pin No. | Symbol | Pin Function |
| :---: | :--- | :--- |
| 1 | IN | Switch input pin. <br> When in use, connect each pin outside. |
| 2 | EN | Switch control input pin (hysteresis input) <br> Switch ON at High. |
| 3 | GND | Ground |
| 4 | OUT | Switch output pin <br> When in use, connect each pin outside. |
| 5 |  |  |
| 6 |  |  |

## Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\text {IN }}$ | -0.3 to +6.0 | V |
| Control Input Voltage | $\mathrm{V}_{\mathrm{EN}}$ | -0.3 to $\mathrm{V}_{\text {IN }}+0.3$ | V |
| Switch Output Voltage | $\mathrm{V}_{\text {OUT }}$ | -0.3 to +6.0 | V |
| Storage Temperature | Tstg | $-55^{\text {to }+150}$ | ${ }^{\circ} \mathrm{C}$ |
| Power Dissipation | Pd | $0.85^{(\text {Note } 1)}$ | W |

(Note 1) Mounted on $70 \mathrm{~mm} \times 70 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ glass-epoxy PCB. Derating : $6.8 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $\mathrm{Ta}=25^{\circ} \mathrm{C}$.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Conditions

| Parameter | Symbol | Rating |  |  | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Supply Voltage | $\mathrm{V}_{\mathbb{I N}}$ | 3.0 | - | 5.5 | V |
| Operating Temperature | Topr | -25 | - | +75 | ${ }^{\circ} \mathrm{C}$ |
| Switch Current | IOUT | - | - | 500 | mA |

Electrical Characteristics (Unless otherwise specified, $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathbb{I N}}=5 \mathrm{~V}$ )

| Parameter | Symbol | Limit |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| Operating Current | ID | - | 50 | 75 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {EN }}=5 \mathrm{~V}$, $\mathrm{V}_{\text {OUT }}=$ Open |
| Standby Current | $\mathrm{I}_{\text {StB }}$ | - | 0.1 | 1 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {EN }}=0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=$ Open |
| EN Input Voltage | $\mathrm{V}_{\text {ENH }}$ | - | - | 2.5 | V | High Level Input Voltage |
|  | $\mathrm{V}_{\text {ENL }}$ | 0.7 | - | - | V | Low Level Input Voltage |
| EN Input Leak Current | $I_{\text {EN }}$ | -1 | +0.01 | +1 | $\mu \mathrm{A}$ |  |
| Switch ON-Resistance | Ron | - | 200 | 255 | $\mathrm{m} \Omega$ | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$ |
|  |  | - | 250 | 335 | $\mathrm{m} \Omega$ | $\mathrm{V}_{\text {IN }}=3.3 \mathrm{~V}$ |
| Switch Leak Current | $I_{\text {LEAK }}$ | - | - | 10 | $\mu \mathrm{A}$ | At Switch OFF |
| Switch Rise Time | ton1 | - | 0.4 | 0.8 | ms | $\mathrm{R}_{\mathrm{L}}=10 \Omega$. Refer to the Timing Diagram in Figure 2. |
| Switch Rise Delay Time | ton2 | - | 0.5 | 1.0 | ms | $\mathrm{R}_{\mathrm{L}}=10 \Omega$. Refer to the Timing Diagram in Figure 2. |
| Switch Fall Time | toff1 | - | 1 | 2 | $\mu \mathrm{s}$ | $\mathrm{R}_{\mathrm{L}}=10 \Omega$. Refer to the Timing Diagram in Figure 2. |
| Switch Fall Delay Time | $\mathrm{t}_{\text {OFF2 }}$ | - | 2 | 4 | $\mu \mathrm{s}$ | $\mathrm{R}_{\mathrm{L}}=10 \Omega$. Refer to the Timing Diagram in Figure 2. |
| UVLO Threshold Voltage | Vuvıo | 1.9 | 2.2 | 2.5 | V | $V_{\text {IN }}$ Increasing |
|  |  | 1.8 | 2.1 | 2.4 | V | $\mathrm{V}_{\text {IN }}$ Decreasing |
| Discharge Resistance | $\mathrm{R}_{\text {DISC }}$ | - | 200 | 350 | $\Omega$ | $\mathrm{V}_{\mathrm{EN}}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~mA}$ |
| Discharge Current | I DISC | 0.8 | 1.8 | - | mA | $\mathrm{V}_{\text {EN }}=0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=\mathrm{V}_{\text {OUT }}=1.8 \mathrm{~V}$ |

## Measurement Circuit



Figure 1. Measurement Circuit

Timing Diagram


Figure 2. Timing Diagram

## Typical Performance Curves



Figure 3. Operating Current vs Ambient Temperature


Figure 5. EN Input Voltage vs Ambient Temperature (High Level Input Voltage)


Figure 4. Standby Current vs Ambient Temperature


Figure 6. EN Input Voltage vs Ambient Temperature (Low Level Input Voltage)

## Typical Performance Curves - continued



Figure 7. Switch ON-Resistance vs Ambient Temperature


Figure 9. Switch Rise Delay Time vs Ambient Temperature


Figure 8. Switch Rise Time vs Ambient Temperature


Figure 10. Switch Fall Time vs Ambient Temperature

## Typical Performance Curves - continued



Figure 11. Switch Fall Delay Time vs Ambient Temperature


Figure 13. Discharge Resistance vs Ambient Temperature


Figure 12. UVLO Threshold Voltage vs Ambient Temperature


Figure 14. Operating Current vs Input Voltage


Figure 15. EN Input Voltage vs Input Voltage


Figure 17. Switch Rise Time vs Input Voltage


Figure 16. Switch ON-Resistance vs Input Voltage


Figure 18. Switch Fall Time vs Input Voltage

Typical Performance Curves - continued


Figure 19. Discharge Resistance vs Input Voltage

## Typical Wave Forms



Figure 20. Switch Rise Time


Time ( $200 \mu \mathrm{~s} / \mathrm{div}$ )


Figure 21. Switch Fall Time


Figure 23. Switch Fall Time

## Typical Wave Forms - continued



Figure 24. Inrush Current


Figure 26. UVLO


Figure 25. Inrush Current


Figure 27. UVLO

## Typical Application Circuit



## Functional Description

1. Input / Output

The IN and OUT pins are connected to the drain and the source of the N-MOS switch respectively. The IN pin is also used as power supply input to the internal control circuit.

When EN input is set to High level and the switch is turned ON, the IN and OUT pins are connected by a $200 \mathrm{~m} \Omega$ switch. Under normal conditions, current flows from IN to OUT. If voltage at pin OUT pin is higher than pin IN, current flows from OUT to IN since the switch is bidirectional. There is no parasitic diode between the drain and the source, so it is possible to prevent current from flowing reversely from OUT pin to IN pin when the switch is disabled.
2. Discharge Circuit

When the switch between the IN and the OUT is turned OFF, the $200 \Omega$ (Typ) discharge switch between OUT and GND turns on. By turning on this switch, electric charge at capacitive load is discharged.
3. Under Voltage Lockout (UVLO)

The UVLO circuit monitors the voltage of the IN pin when the EN input is active. UVLO circuit prevents the switch from turning ON until the IN exceeds 2.2 V (Typ). If the IN drops below 2.1 V (Typ) while the switch turns on, then UVLO shuts off the switch.

While the switch between the IN pin and OUT pin is OFF due to UVLO operations, the switch of the discharge circuit turns ON. However, when the voltage of IN declines tremendously, then the OUT pin becomes Hi-Z.


Figure 28. Operation Timing

## Power Dissipation

(HVSOF6 package)

$70 \mathrm{~mm} \times 70 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ Glass Epoxy Board
Figure 29. Power dissipation curve ( $\mathrm{Pd}-\mathrm{Ta}$ Curve)

I/O Equivalence Circuit


## Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.
2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

## 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

## 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

## 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a $70 \mathrm{~mm} \times 70 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.
6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
7. In rush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

## 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

## 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## Operational Notes - continued

## 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.
12. Regarding the Input Pin of the IC

This monolithic IC contains $\mathrm{P}+$ isolation and P substrate layers between adjacent elements in order to keep them isolated. $\mathrm{P}-\mathrm{N}$ junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.


Figure 30. Example of monolithic IC structure

## 13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

## Ordering Information



## Marking Diagram



## Physical Dimension, Tape and Reel Information

| Package Name | HVSOF6 |
| :--- | :--- |



0. $145 \pm 0.05$


## (UN I T : mm)

PKG: HVSOF 6
Drawing No. EX162-5002


## Revision History

| Date | Revision |  |
| :---: | :---: | :--- |
| 11.Mar.2013 | 001 | New Release |
| 21.Aug.2014 | 002 | Applied the ROHM Standard Style and improved understandability. |

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