

# **Motor Drivers for Digital Still Cameras**

# 7-Channel System Lens Driver for Digital Still Cameras

# **BD6889GU**

# **General Description**

The BD6889GU is a motor driver that integrates 6 Full-ON type H-Bridges and 1 Linear Constant-Current type H-Bridge. The device is intended to drive three stepping motor for auto focus system, zoom, and iris, and making it possible to design a sophisticated, high precision lens drive system.

#### **Features**

- Low ON-Resistance Power CMOS Output
- 4 Digital NPN Transistor Circuits for Rectangular Waveform of Photo-Interrupter: Input-Dividing Type with Output Pull-up Resistor
- 4 Digital PNP Transistor Circuits for Rectangular Waveform of Photo-Interrupter: Input-Dividing Type with Output Pull-down Resistor
- Voltage-Regulator Circuit for Photo-Interrupter
- High-Precision (0.9V±2%) Reference Voltage Output
- Phase Compensation Capacitor-Free Design for Linear Constant-Current Drive Block
- High-Precision (±3%) Linear Constant-Current Driver
- Under Voltage Locked Out Protection
   & Thermal Shut Down Circuit

#### **Applications**

- Mobile system
- Home appliance
- Amusement system, etc

# **Key Specifications**

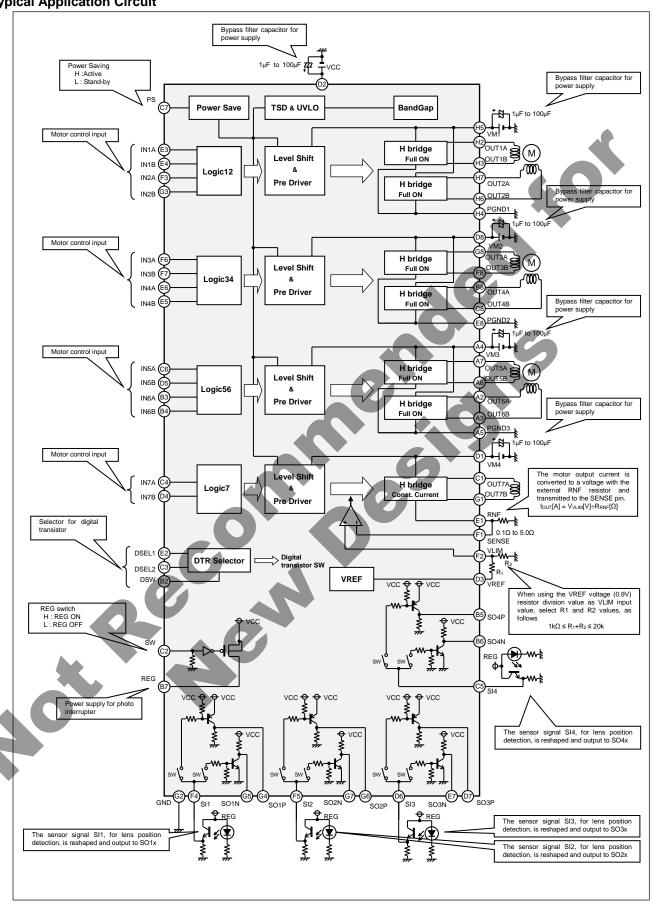
- Power Supply Voltage Range: 2.5V to 5.7V
- Motor Power Supply Voltage Range: 2.5V to 5.7V
- Circuit Current (No Signal): 1.5mA(Typ)
- Stand-By Current: 10µA (Max)
   Control Input Voltage Range: 0V to VccV
- Control Input Voltage Range:
   H-Bridge Output Current:
   -0.5A/ch to +0.5A/ch
- Output ON-Resistance (Channel 1 to 6): 1.3Ω(Typ)
- Output ON-Resistance (Channel 7): 0.9Ω(Typ)
- Operating Temperature Range: -25°C to +85°C

# Package VBGA063T050

**W(Typ)** x **D(Typ)** x **H(Max)** 5.00mm x 5.00mm x 1.20mm



**Typical Application Circuit** 



# **Pin Configurations**

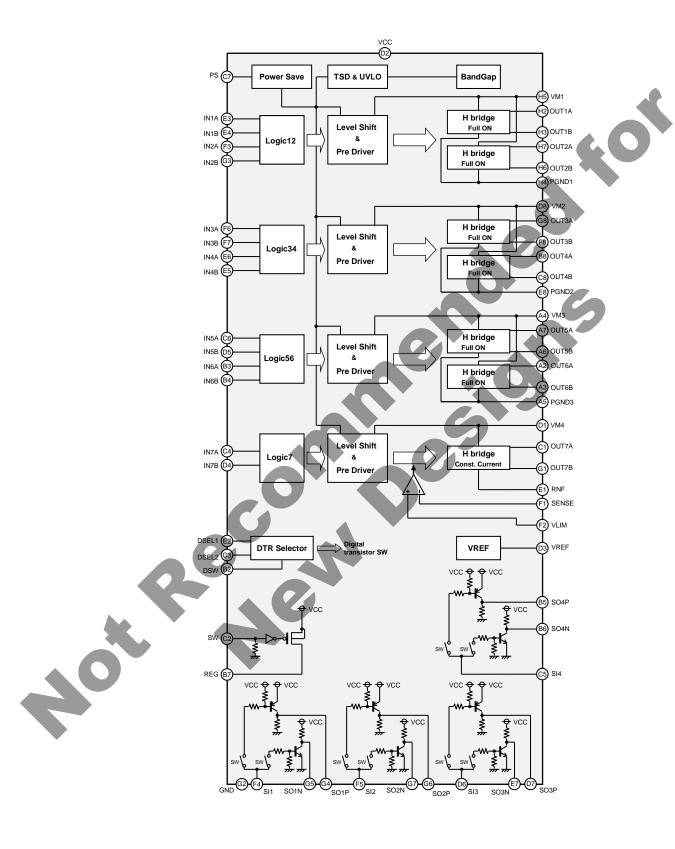
# (TOP VIEW)

	1	2	3	4	5	6	7	8
Α	N.C.	OUT6A	OUT6B	VM3	PGND3	OUT5B	OUT5A	N.C.
В	INDEX POST	DSW	IN6A	IN6B	SO4P	SO4N	REG	OUT4A
С	OUT7A	SW	DSEL2	IN7A	SI4	IN5A	PS	OUT4B
D	VM4	vcc	VREF	IN7B	IN5B	SI3	SO3P	VM2
E	RNF	DSEL1	IN1A	IN1B	IN4B	IN4A	SO3N	PGND2
F	SENSE	VLIM	IN2A	SI1	SI2	IN3A	IN3B	ОИТ3В
G	OUT7B	GND	IN2B	SO1P	SO1N	SO2P	SO2N	OUT3A
н	N.C.	OUT1A	OUT1B	PGND1	VM1	OUT2B	OUT2A	N.C.

# **Pin Descriptions**

Pin No.Pin NameFunctionPin No.Pin No.Pin NameFunctionA1N.CE1RNFCurrent detect resistor of transistor of t	.4 n ch.7
A2 OUT6A H-bridge output 6A E2 DSEL1 Selector for transistor of A3 OUT6B H-bridge output 6B E3 IN1A Control logic input 1A A4 VM3 Motor power supply ch.5, ch.6 E4 IN1B Control logic input 1B A5 PGND3 Motor ground ch.5, ch.6 E5 IN4B Control logic input 4B A6 OUT5B H-bridge output 5B E6 IN4A Control logic input 4A A7 OUT5A H-bridge output 5A E7 SO3N NPN transistor output 3 A8 N.C E8 PGND2 Motor ground ch.3 & ch B1 INDEX POST F1 SENSE Output current detection B2 DSW Enable for transistors	.4 n ch.7
A3 OUT6B H-bridge output 6B E3 IN1A Control logic input 1A  A4 VM3 Motor power supply ch.5, ch.6 E4 IN1B Control logic input 1B  A5 PGND3 Motor ground ch.5, ch.6 E5 IN4B Control logic input 4B  A6 OUT5B H-bridge output 5B E6 IN4A Control logic input 4A  A7 OUT5A H-bridge output 5A E7 SO3N NPN transistor output 3  A8 N.C E8 PGND2 Motor ground ch.3 & ch  B1 INDEX POST F1 SENSE Output current detection  B2 DSW Enable for transistors F2 VLIM Output current setting control input 4A	.4 n ch.7
A4 VM3 Motor power supply ch.5, ch.6 E4 IN1B Control logic input 1B A5 PGND3 Motor ground ch.5, ch.6 E5 IN4B Control logic input 4B A6 OUT5B H-bridge output 5B E6 IN4A Control logic input 4A A7 OUT5A H-bridge output 5A E7 SO3N NPN transistor output 3 A8 N.C E8 PGND2 Motor ground ch.3 & ch B1 INDEX POST F1 SENSE Output current detection B2 DSW Enable for transistors F2 VLIM Output current setting controls.	.4 n ch.7
A5 PGND3 Motor ground ch.5, ch.6 E5 IN4B Control logic input 4B A6 OUT5B H-bridge output 5B E6 IN4A Control logic input 4A A7 OUT5A H-bridge output 5A E7 SO3N NPN transistor output 3 A8 N.C E8 PGND2 Motor ground ch.3 & ch B1 INDEX POST F1 SENSE Output current detection B2 DSW Enable for transistors F2 VLIM Output current setting controls.	.4 n ch.7
A6 OUT5B H-bridge output 5B E6 IN4A Control logic input 4A A7 OUT5A H-bridge output 5A E7 SO3N NPN transistor output 3 A8 N.C E8 PGND2 Motor ground ch.3 & ch B1 INDEX POST F1 SENSE Output current detection B2 DSW Enable for transistors F2 VLIM Output current setting controls.	.4 n ch.7
A7 OUT5A H-bridge output 5A E7 SO3N NPN transistor output 3 A8 N.C E8 PGND2 Motor ground ch.3 & ch B1 INDEX POST F1 SENSE Output current detection B2 DSW Enable for transistors F2 VLIM Output current setting co	.4 n ch.7
A8 N.C E8 PGND2 Motor ground ch.3 & ch B1 INDEX POST F1 SENSE Output current detection B2 DSW Enable for transistors F2 VLIM Output current setting co	.4 n ch.7
B1 INDEX POST F1 SENSE Output current detection B2 DSW Enable for transistors F2 VLIM Output current setting of	ch.7
B2 DSW Enable for transistors F2 VLIM Output current setting of	
	า.7
B3 IN6A Control logic input 6A F3 IN2A Control logic input 2A	
Bo INDA Control logic input of 10	
B4 IN6B Control logic input 6B F4 SI1 Digital transistor input 1	
B5 SO4P PNP transistor output 4 F5 SI2 Digital transistor input 2	
B6 SQ4N NPN transistor output 4 F6 IN3A Control logic input 3A	
B7 REG Regulator output for PI F7 IN3B Control logic input 3B	
B8 OUT4A H-bridge output 4A F8 OUT3B H-bridge output 3B	
C1 OUT7A H-bridge output 7A G1 OUT7B H-bridge output 7B	
C2 SW Regulator input G2 GND Device ground	
C3 DSEL2 Selector for transistor output 2 G3 IN2B Control logic input 2B	
C4 IN7A Control logic input 7A G4 SO1P PNP transistor output 1	
C5 SI4 Digital transistor input 4 G5 SO1N NPN transistor output 1	
C6 IN5A Control logic input 5A G6 SO2P PNP transistor output 2	
C7 PS Power-saving G7 SO2N NPN transistor output 2	
C8 OUT4B H-bridge output 4B G8 OUT3A H-bridge output 3A	
D1 VM4 Motor power supply ch.7 H1 N.C	
D2 VCC Power supply H2 OUT1A H-bridge output 1A	
D3 VREF Reference voltage output H3 OUT1B H-bridge output 1B	
D4 IN7B Control logic input 7B H4 PGND1 Motor ground ch.1, ch.2	
D5 IN5B Control logic input 5B H5 VM1 Motor power supply ch.	1, ch.2
D6 SI3 Digital transistor input 3 H6 OUT2B H-bridge output 2B	
D7 SO3P PNP transistor output 3 H7 OUT2A H-bridge output 2A	
D8 VM2 Motor power supply ch.3, ch.4 H8 N.C	

# **Block Diagram**



#### **Description of Blocks**

#### 1. Power-Saving Function

A power-saving function is included, which allows the system to save power when not driving the motor. The voltage level on this pin should be set high so as to keep the operation mode. (See the Electrical Characteristics; P.7/17)

#### 2. Motor Control Input (IN1A to IN7B)

Logic level controls the output logic of H-Bridge. The logic of Full-ON H-Bridges corresponds to IN/IN mode, and the logic of Constant-Current H-bridge EN/IN mode.

(See the Electrical Characteristics; P.7/17, and I/O Truth Table; P.9/17)

#### H-Bridge

Each H-bridge can be controlled independently. It is therefore possible to drive the H-bridges simultaneously, as long as the package thermal tolerances are not exceeded. Because the respective output transistors consist of power CMOS which consumes a motor power supply V<sub>M</sub>, the ON-Resistance value of high and low-side total is dependent on V<sub>M</sub> voltage. Further, the whole application must be designed so that the maximum current of each channel may be 500mA or below. (See the Recommended Operating Conditions; p.6/17)

#### 4. Linear Constant-Current H-bridge (Channel 7)

(a) Reference Voltage Output (with a tolerance of  $\pm 2\%$ )

The VREF pin can output 0.9V based on the internal reference voltage. The output current of the Constant-Current Drive block can be controlled by connecting external resistor to the VREF pin and setting the voltage which is divided by the resistor to the output current setting pin (VLIM pin). It is recommended to place the external  $1k\Omega$  or above resistor in consideration of the load current capacity of the VREF pin, and to place the  $20k\Omega$  or below resistor in order to minimize the fluctuation caused by the base current of the internal transistor.

#### (b) Output Current Detection and Current Settings

A low-value  $(0.1\Omega \text{ to } 5.0\Omega)$  resistor can be placed between the RNF pin and ground to detect the motor winding current. When making the RNF and SENSE pins short-circuit, the internal circuits can output the accurate constant current by comparing the VLIM voltage with detecting voltage. To make more accurate motor winding current, trim the external RNF resistor, and supply VLIM pin with another precise external voltage. In case of this condition, VREF pin should be kept open.

Output Current  $I_{OUT}[A] = VLIM[V] / RNF[\Omega]$ 

The motor winding current will be  $400\text{mA}\pm3\%$ , if 0.2V is set to the VLIM pin and a  $0.5\Omega$  external resistor is connected to the RNF pin. If the VLIM pin is shorted to the VCC pin (or the same voltage as the V<sub>CC</sub> is set) and the SENSE and RNF pins are shorted to the ground, this channel can drive as a Full-ON type H-bridge like other channels.

# 5. Digital Transistor for Rectangular Waveform

The internal 4 NPN and 4 PNP digital transistors can be used to make photo-interrupter waveform rectangular. To detect lens position, the sensed signal is reshaped by internal circuitry and then may be output to the MCU etc. The device includes pull-up resistors for each NPN output pin (SO1N to SO4N) and pull-down resistors for each PNP output pin (SO1P to SO4P). If not supplying an external voltage to input pins (SI1 to SI4), the NPN output pins will output Vcc voltage and the PNP output pins ground. DSW, DSEL1 and DSEL2 pins can control the switching of NPN and PNP transistors. (See I/O Truth Table; P.9/17)

#### 6. Voltage-Regulator for Photo-Interrupter

The device includes voltage-regulator circuits for photo-interrupter. Set high logic on SW pin to enable output of the internal regulator, and set low to disable. It also includes a pull-down resistor so that regulator output (REG pin) may be off even if SW pin is opened.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	Vcc	-0.5 to +7.0	V
Motor Power Supply Voltage	V <sub>M</sub>	-0.5 to +7.0	V
Control Input Voltage	Vin	-0.5 to +Vcc+0.5	V
Power Dissipation	Pd	0.98 (Note 1)	W
H-bridge Output Current	l <sub>оит</sub>	-0.8 to +0.8 <sup>(Note 2)</sup>	A/ch
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	150	°C

(Note 1) Reduced by 7.84mW/°C over 25°C, when mounted on a glass epoxy board (70mm x 70mm x 1.6mm)

(Note 1) Reduced by 7.54fffv7 Gover 25 G, Ministrict and 3.1 s glass spin, 1211 (Note 2) Must not exceed Pd, ASO, or Tjmax of 150°C **Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Recommended Operating Conditions** 

Johnnended Operating Conditions					
Parameter	Symbol	Min	Тур	Max	Unit
Power Supply Voltage	Vcc	2.5		5.7	V
Motor Power Supply Voltage	V <sub>M</sub>	2.5		5.7	٧
Control Input Voltage	V <sub>IN</sub>	0	-	Vcc	V
H-bridge Output Current <sup>(Note 3)</sup>	Іоит	-0.5	-	+0.5	A/ch
Operating Temperature Range	Topr	-25	-	+85	°C

Electrical Characteristics (Unless otherwise specified V<sub>CC</sub>=3.0V, V<sub>M</sub>=5.0V, Ta=25°C)

Parameter	Symbol	Min	Тур	Max	Unit	Conditions
All Circuits		1				
Stand-by Current	Іссят	-	0	10	μA	V <sub>PS</sub> =0V
Circuit Current	Icc	-	1.5	3.0	mA	V <sub>PS</sub> =3V, with no signal
Control Input (IN=PS, IN1A to	N7B, SW	, DSW, DSI	EL1, DSEL	2)		
High Level Input Voltage	VINH	2.0	-	Vcc	V	
Low Level Input Voltage	VINL	0	-	0.7	V	
High Level Input Current	linh	15	30	60	μA	V <sub>IN</sub> =3V
Low Level Input Current	I <sub>INL</sub>	-1	0	-	μA	V <sub>IN</sub> =0V
Pull-down Resistor	Rın	50	100	200	kΩ	
Under Voltage Locked Out (l	JVLO)					
UVLO Voltage	Vuvlo	1.6		2.4	V	
Full-ON Drive Block (Channe	el 1 to Chan	nel 6)				
Output ON-Resistance	Ron	-	1.3	1.6	Ω	louτ=±400mA, High & Low-side total
Pulse Input Response	t₽	100	ı	ı	ns	With an input pulse 200ns
Linear Constant-Current Driv	e Block (Ch	nannel 7)				
Output ON-Resistance	Ron	-	0.9	1.1	Ω	Iouт=±400mA, High & Low-side tota
VREF Output Voltage	V <sub>REF</sub>	0.88	0.90	0.92	V	louт=0 to 1mA
Output Limit Current 1	I <sub>OL1</sub>	388	400	412	mA	10 $\Omega$ load, R <sub>RNF</sub> =0.5 $\Omega$ , V <sub>VLIM</sub> =0.20V
Output Limit Current 2	I <sub>OL2</sub>	285	300	315	mA	10Ω load, $R_{RNF}$ =0.5Ω, $V_{VLIM}$ =0.15 $V$
Output Limit Current 3	I <sub>OL3</sub>	190	200	210	mA	10Ω load, $R_{RNF}$ =0.5Ω, $V_{VLIM}$ =0.10 $V$
Digital NPN Transistor Block	for Rectang	gular Wavef	orm of Pho	to-Interrup	oter	
Input Current	I <sub>SIH</sub>	-		0.1	mA	V <sub>SIx</sub> =3V
Low Level Output Voltage	Vsol	-	0.1	0.25	V	V <sub>SIx</sub> =3V, I <sub>SO</sub> =0.5mA
Input Dividing Resistor	Rsin	70	100	130	kΩ	
Output Pull-up Resistor	Rson	23	33	43	kΩ	
Input Dividing Resistors Comparison	·	0.8	1.0	1.2	-	Comparison of dividing resistors between SIx and GND (Note 4)
Digital PNP Transistor Block	for Rectang	I .	orm of Pho	to-Interrup	ter	
Input Current	IsiL	-0.1	-	-	mA	V <sub>SIx</sub> =0V
High Level Output Voltage	Vsон	Vcc-0.25	Vcc-0.1	-	V	V <sub>SIx</sub> =0V, I <sub>SO</sub> =-0.5mA
Input Dividing Resistor	RSIP	70	100	130	kΩ	
Output Pull-down Resistor	R <sub>SOL</sub>	23	33	43	kΩ	
Input Dividing Resistors Comparison		0.8	1.0	1.2	-	Comparison of dividing resistors between SIx and VCC (Note 4)
Voltage-regulator for Photo-I		<b>P</b>			T	
High Level Output Voltage	VREGH	V <sub>CC</sub> -0.25	V <sub>CC</sub> -0.2	-	V	I <sub>REG</sub> =100mA
Output ON-Resistance	Ronreg	-	2	2.5	Ω	I <sub>REG</sub> =100mA
Output Leak Current	I <sub>LPI</sub>	-	0	1	μA	SW=VCC

(Note 4) Not guaranteed by testing

# **Typical Performance Curves**

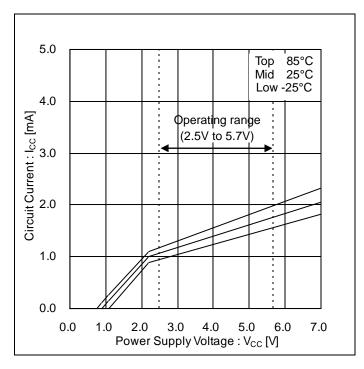


Figure 1.
Circuit Current vs Power Supply Voltage

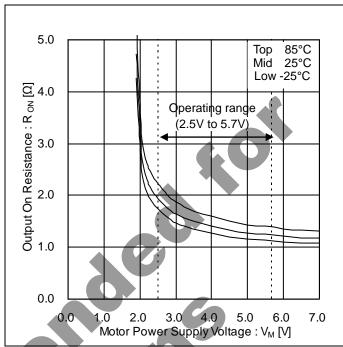


Figure 2.
Output ON-Resistance vs Motor Power Supply Voltage
(Channel 1 to Channel 6, Vcc=3V)

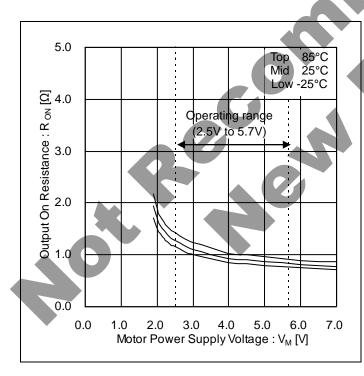


Figure 3. Output ON-Resistance vs Motor Power Supply Voltage (Channel 7,  $V_{CC}$ =3V)

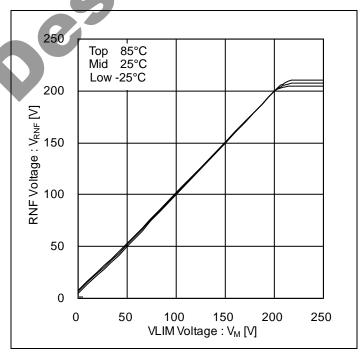


Figure 4. RNF Voltage vs VLIM Voltage (Output Limit Voltage, R<sub>RNF</sub>=0.5Ω)

# **Timing chart**

Table 1. I/O Truth Table (Channel 1 to Channel 6)

Innut Mada	INF	PUT	OUTPUT				
Input Mode	INxA	INxB	OUTxA	OUTxB	Output Mode <sup>(Note 5)</sup>		
	L	L	Z	Z	Open		
INI/INI	Н	L	Н	L	CW		
IN/IN	L	Н	L	Н	CCW		
	Н	Н	L	L	Short Brake		

L: Low, H: High, X: Don't care, Z: Hi impedance

(Note 5) CW: Current flows from OUTxA to OUTxB, CCW: Current flows from OUTxB to OUTxA (x=1 to 6)

Table 2. I/O Truth Table (Channel 7)

Input Mada	INF	TU	OUTPUT				
Input Mode	IN7A	IN7B	OUT7A	OUT7B	Output Mode <sup>(Note 6)</sup>		
	L	X	Z	Z	Open		
EN/IN	Н	L	Н	4	CW		
	Н	Н	L	Н	CCW		

L: Low, H: High, X: Don't care, Z: Hi impedance

(Note 6) CW: Current flows from OUT7A to OUT7B, CCW: Current flows from OUT7B to OUT7A

Table 3. Digital Transistor I/O Truth Table

Table of Digital Translator if C Train Table											
		INPUT			OUTPUT						
	DSW	DSEL1	DSEL2	PNP1	NPN1	PNP2	NPN2	PNP3	NPN3	PNP4	NPN4
	L	Х	Х	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
	Н	L	L	OFF	ON	OFF	ON	OFF	ON	OFF	ON
LOGIC	Н	L	Н	OFF	ON	OFF	ON	ON	OFF	ON	OFF
	Н	Н	L	ON	OFF	ON	OFF	OFF	ON	OFF	ON
	Н	Н	Н	ON	OFF	ON	OFF	ON	OFF	ON	OFF

L: Low, H: High, X: Don't care, OFF: GND (PNP), VCC (NPN)

PNPx can output to SOxP pins, NPNx can output to SOxN pins (x=1 to 4)



# Timing chart - continued

Table 4. I/O Truth Table (In the case of 2phases driving the Stepping Motor by channel 1 and channel 2)

	INP	PUT		OUTPUT				
IN1A	IN1B	IN2A	IN2B	OUT1A	OUT1B	OUT2A	OUT2B	Output Mode (Note 7)
L	L	L	L	Z	Z	Z	Z	Open
Н	L	Н	L	Н	L	Н	L	1. CW / CW
L	Н	Н	L	L	Н	Н	L	3. CCW / CW
L	Н	L	Η	L	Н	L	Н	5. CCW / CCW
Н	L	L	Η	Н	L	L	Н	7. CW / CCW

L: Low, H: High, X: Don't care, Z: Hi impedance

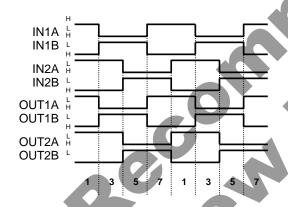
(Note 7) CW: Current flows from OUTxA to OUTxB, CCW: Current flows from OUTxB to OUTxA (x=1, 2)

Table 5. I/O Truth Table (In the case of 1-2 phases driving the Stepping Motor by channel 1 and channel 2)

	INP	TUT		OUTPUT					
IN1A	IN1B	IN2A	IN2B	OUT1A	OUT1B	OUT2A	OUT2B	出力モード <sup>(Note 8)</sup>	
L	L	L	L	Z	Z	Z	Z	Open / Open	
Н	L	Н	L	Н	L	Н		1. CW / CW	
L	L	Н	L	Z	Z	H	L	2. Open / CW	
L	Н	Н	L	L	Н	Н		3. CCW / CW	
L	Н	L	L	L	Н	Z	Z	4. CCW / Open	
L	Н	L	Н	L	Н		Н	5. CCW / CCW	
L	L	L	Н	Z	Z	\	Н	6. Open / CCW	
Н	L	L	Н	Н	L	L	H	7. CW / CCW	
Н	L	L	L	Н	L 🗸	Z	Z	8. CW / Open	

L: Low, H: High, X: Don't care, Z: Hi impedance

(Note 8) CW: Current flows from OUTxA to OUTxB, CCW: Current flows from OUTxB to OUTxA (x=1, 2)



IN1A HIN1B LIN2A HIN1B LIN2B H

Figure 5.
2 Phases Timing Sequence with IN/IN Input

Figure 6.
1-2 Phases Timing Sequence with IN/IN Input

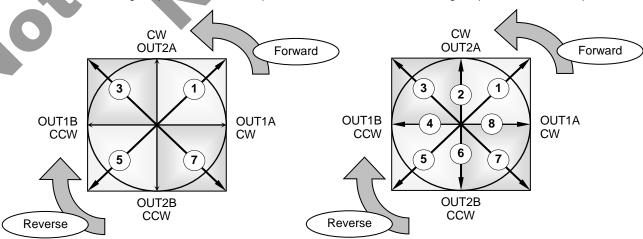
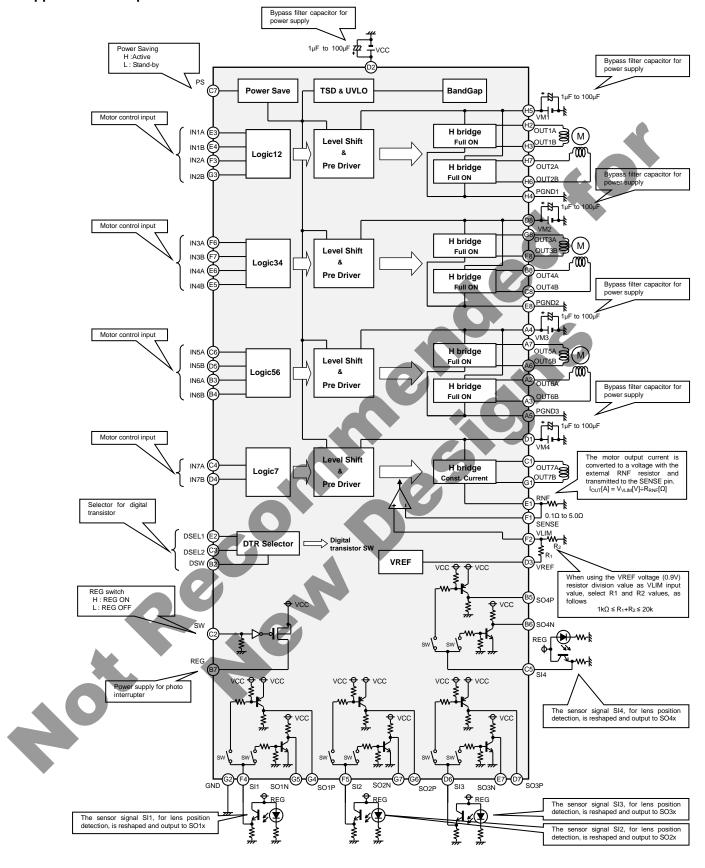


Figure 7.
Torque Vector of 2 Phases Mode

Figure 8.
Torque Vector of 1-2 Phases Mode

#### **Application Example**



# **Selection of Components Externally Connected**

When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.

#### **Power Dissipation**

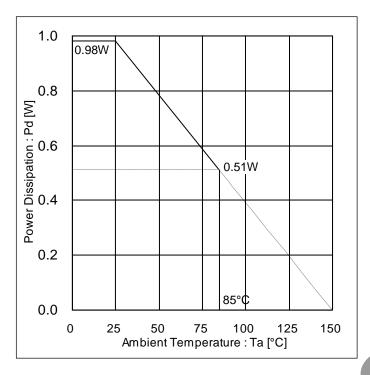
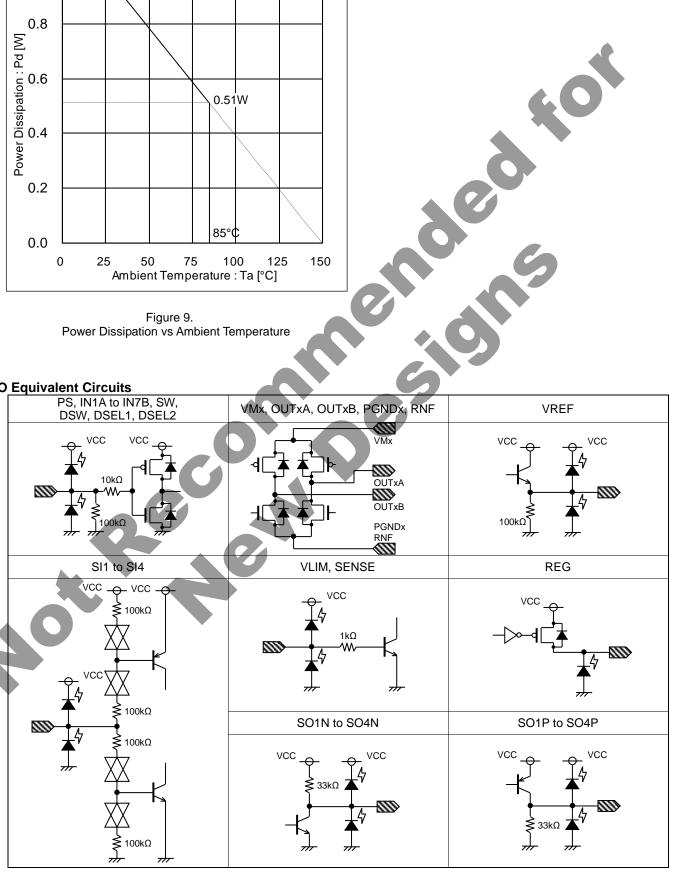


Figure 9. Power Dissipation vs Ambient Temperature

I/O Equivalent Circuits



#### **Operational Notes**

#### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

#### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

#### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

#### 4. Ground Wiring Pattern

When using both small-signal(GND) and large-current ground(PGND) traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

#### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

#### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

#### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

# 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

#### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

# 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

# 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

#### **Operational Notes - continued**

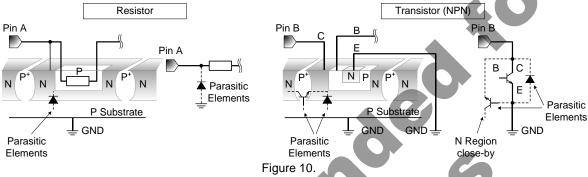
#### 12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

#### 13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

#### 14. Area of Safe Operation (ASO)

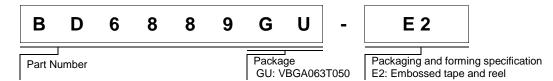
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

# 15. Thermal Shutdown Circuit(TSD)

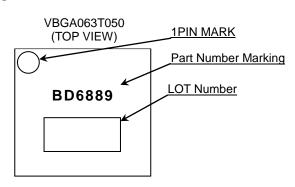
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

# **Ordering Information**



# **Marking Diagram**



gram					
VBGA063T050 (TOP VIEW)	1PIN MARK				60.
	Part Number M	arking			
BD6889	LOT Number			0	
			9		
Part Number Marking	Package	Orderable Part	Number		
BD6889	VBGA063T050	BD6889GU-E2			

**Physical Dimension Tape and Reel Information** Package Name VBGA063T050 5.  $0\pm0.1$ 1PIN MARK 0.08S  $0.75\pm0.1$  $63-\phi0.3\pm0.05$ ⊕ 0. 05M SAB 0000000 0000000 00000000 00000000 00000000 00000000 0 0000000 000000 (UNIT; mm) PKG: VBGA063T050 Drawing No. EX832-5001 <Tape and Reel information> Embossed carrier tape (with dry pack) Tape 2500pcs Quantity **E2** Direction The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand of feed Direction of feed \*Order quantity needs to be multiple of the minimum quantity.

# **Revision History**

Date	Revision	Changes
09.Dec.2015	001	New Release



# **Notice**

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSIII	CLASSIIb	CLASSII
CLASSIV		CLASSⅢ	

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  - [h] Use of the Products in places subject to dew condensation
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- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
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For details, please refer to ROHM Mounting specification

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