

PWM Control Type DC/DC Converter IC for AC/DC Driver

BD7673AG

●General Description

BD7673AG is a PWM controller typed DC/DC converter for AC/DC that provides an optimum system for all products that requires an electrical outlet. This product supports both isolated and non-isolated devices. IC enables simple design of low-power converters. With switching MOSFET and current detection resistor as external devices, it enables more freedom in design. Since the peak current control is utilized, peak current is controlled in each cycle, application excels wide bandwidth and transient response.

BD7673AG includes various protective functions such as soft start function, burst function, per-cycle over current limiter, VCC overvoltage protection and overload protection.

An external latch pin (COMP pin) is provided, so that latch stopping (OFF) can be set by external signals. This function is available as overheating protection and over output voltage protection.

The PWM switching frequency is fixed at 65 kHz.

A frequency hopping function is included which contributes to low EMI.

●Features

- PWM frequency of 65kHz
- PWM current mode method
- Low circuit current when UVLO is ON (12μA at VCC=12V)
- Low circuit current in no load (Burst operation when load is light)
- Built-in SW frequency hopping function
- 250nsec leading-edge blanking
- VCC UVLO / OVP
- Per-cycle over current protection circuit
- Soft start
- Output overload protection (latch protection)
- External latch function for COMP pin (Over heating protection function)

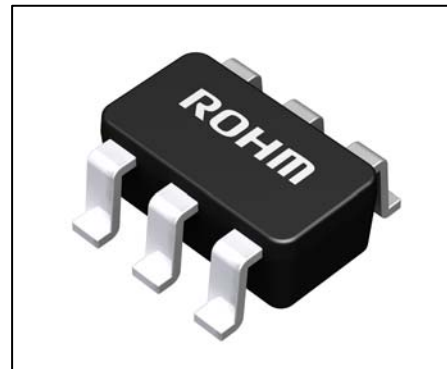
●Key Specifications

- Power Supply Voltage range: 8.5V to 25.0V
- Operating Current: Normal: 0.60mA (Typ)
Burst: 0.40mA (Typ)
- Oscillation Frequency: 65kHz (Typ)
- Operating Temperature range: -40°C to +85°C

●Package

SSOP6

W(Typ) x D (Typ) x H (Max)
2.90mm x 2.80mm x 1.25mm



●Applications

AC adapters and household appliances (vacuum cleaners, humidifiers, air cleaners, air conditioners, refrigerators, IH cooking heaters, rice cookers, etc.)

●Typical Application Circuit

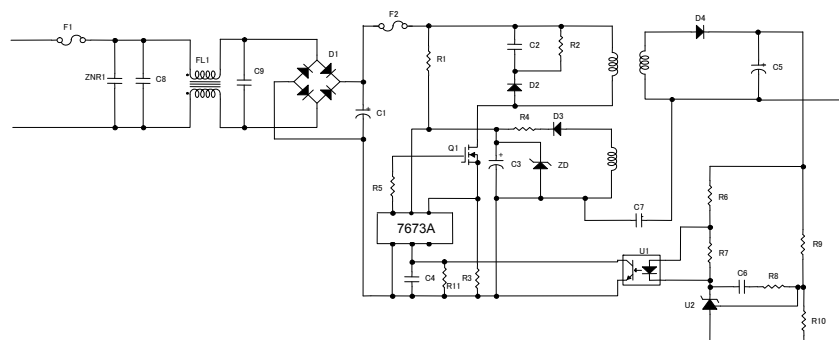


Figure 1, Application Diagram (12 V 1A Isolated Type)

●Pin Configuration (SSOP6)

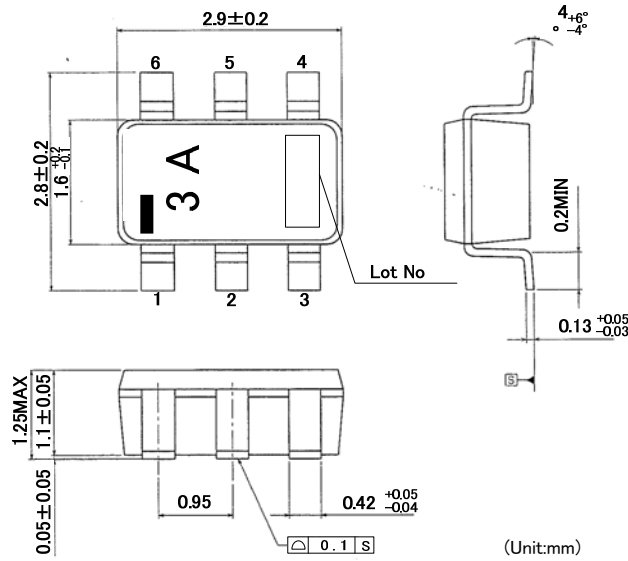


Figure 2, External Dimensions of SSOP6 Package

●Pin Description

Table 1 I/O PIN Functions

NO.	Pin Name	I/O	Function	ESD protection system	
				VCC	GND
1	GND	I/O	GND pin	○	-
2	FB	I	Feedback signal input pin	○	○
3	COMP	I	Comparator input pin	○	○
4	CS	I	Primary current sensor pin	○	○
5	VCC	I	Power supply input pin	-	○
6	OUT	O	External MOS drive pin	○	○

●I/O Equivalent Circuit

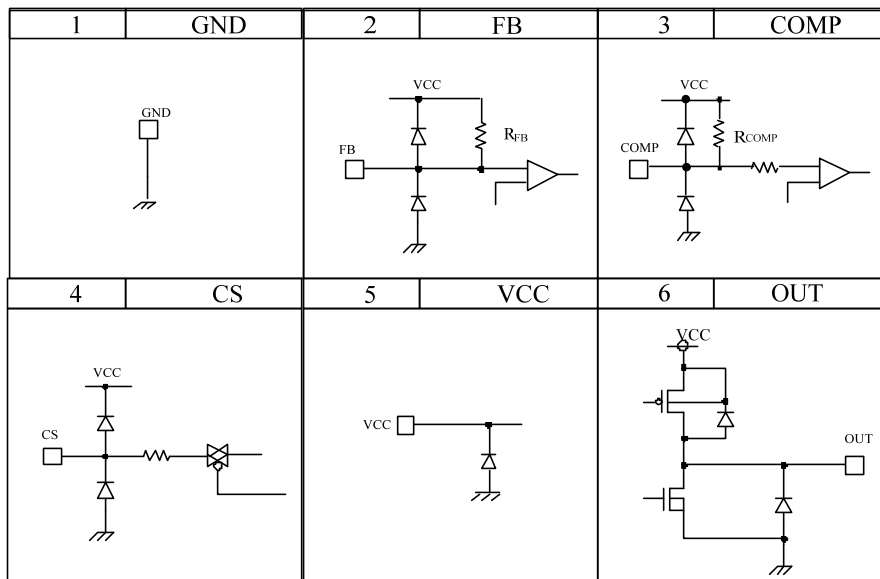


Figure 3, I/O Equivalent Circuit

●Description of Each Block

(1) Start Sequences (Soft Start Operation, Light Load Operation, and Latch Protection for Overload)

Start sequences are shown in Figure 5. This is also shown the operation of latch protection for overload. See the sections below for detailed descriptions

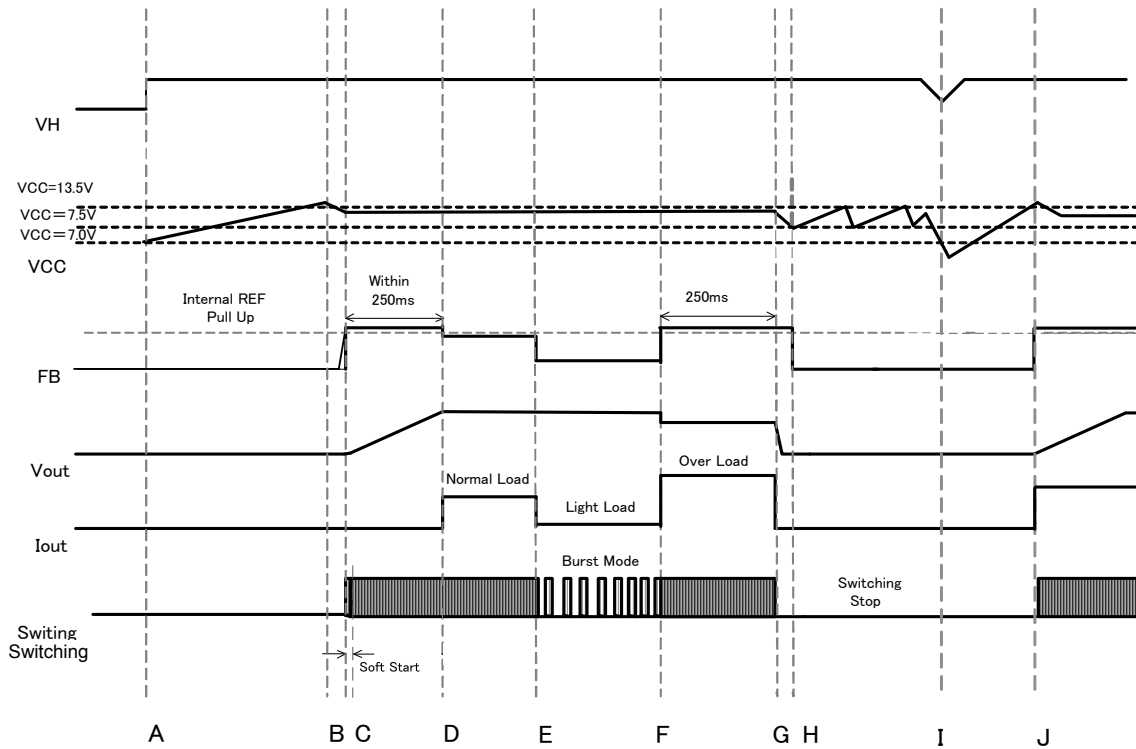


Figure 5, Start Sequence Timing Chart

- A: Input voltage V_H is applied
- B: V_{CC} pin voltage rises by being supplied from V_H line through start resistor “ R_{start} ” and the IC starts operating when $V_{CC} > V_{UVLO1}$ (13.5V Typ). Switching operation starts when other protection functions are judged as normal. From startup to be stable output voltage, application should be set to stabilize output voltage during $V_{CC} > V_{UVLO2}$ (7.5V Typ) because the V_{CC} pin consumption current causes the V_{CC} voltage drop.
- C: Operated soft start function, maximum duty is restricted to 15% during a 1ms period to prevent any excessive rise in voltage or current. From 1ms to 8ms, maximum duty is restricted to 25%. Maximum duty is restricted to 75% after 8ms.
- D: V_{OUT} voltage rises when the switching operation starts. Once the output voltage starts, it is set to the rated voltage level within the T_{FOLP} period (250ms Typ). The output voltage is regulated within T_{FOLP} (=250ms Typ) from starting.
- E: During Light Load, when FB pin voltage $< V_{BST}$ (=0.3V Typ), Burst method is operated to keep power consumption down.
- F: Over Load condition occurs when FB pin voltage $> V_{FOLP1A}$ (=2.8V Typ).
- G: When FB pin voltage is at V_{FOLP1A} (= 2.8V Typ) for more than T_{FOLP} (250ms Typ), the overload protection function is triggered and switching is stopped by LATCH operation. The IC’s internal 250ms timer is reset during the T_{FOLP} period (250ms Typ) if $FB < V_{FOLP1B}$ even once.
- H: V_{CC} voltage is changed from V_{UVLO1} (13.5V Typ) to V_{UVLO2} (7.5V Typ) because of switching stop by latch protection. In case of high V_H voltage if V_{CC} voltage is not changed to less than V_{LATCH} (7.0V Typ), IC is not released from latch protection.
- I: If the condition which V_H voltage is lower continues, V_{CC} voltage is also lower. When V_{CC} voltage is lower than V_{LATCH} (7.0V Typ), the IC is released from latch protection.
- J: Same as B

In Figure 4, start resistor R_{start} is needed to start the application.

When the start resistor R_{start} value is reduced, standby power is increased and the startup time is shortened. Conversely, when the start resistor R_{start} value is increased, standby power is reduced and the startup time is increased. Standby current is less than 20uA at V_{CC} UVLO is disable, and it can calculate V_{CC} UVLO voltage from $V_{UVLO1}=14.5V$ (Max).

ex) Starting resistor R_{start} setting method;

$$R_{start} = (V_{Hmin} - V_{UVLO1} (\text{Max})) / I_{OFF} (\text{Max})$$

In the case of $V_{ac}=100V$ (-20% of a margin), R_{start} requirement can be found by the following formulas:

$$V_{Hmin} = 100 \times \sqrt{2} \times 0.8 = 113V$$

Because of $V_{UVLO1} (\text{Max}) = 14.5V$, $R_{start} \leq (113V - 14.5V) / 20\mu A = 4.925M\Omega$

Start-up time can be found by the following formulas:

$$T_{start} = -R_{start} \times C_{VCC} \times \ln(1 - V_{UVLO1}/V_{Hmin})$$

ex) $R_{start}=3.0M\Omega$

$$R_{start} \text{ resistor loss in this case is : } P_d (R_{start}) = (V_H - V_{CC})^2 / R_{start} = (141V - 14.5V)^2 / 3.0M = 5.33mW.$$

(2) VCC Pin Protection

BD7673AG includes UVLO (Under Voltage Locked Out) and OVP (Over Voltage Protection) functions to monitor VCC pin voltage (see Figure 6 for OVP latch operation).

The UVLO function prevents damage to MOSFET by stopping switching operations by latch protection when the VCC pin voltage drops to $V_{CC} < V_{UVLO2}$ (= 7.5V Typ).

The VCC OVP function prevents damage to MOSFET by stopping switching operations when the VCC pin voltage exceeds V_{OVP1} (= 27.5V Typ).

The latch release condition is when $V_{CC} < V_{LATCH}$ ($V_{UVLO2} - 0.5V$, Typ = 7.0V). A latch blanking time is used for protecting mal-function. This time is 100us.

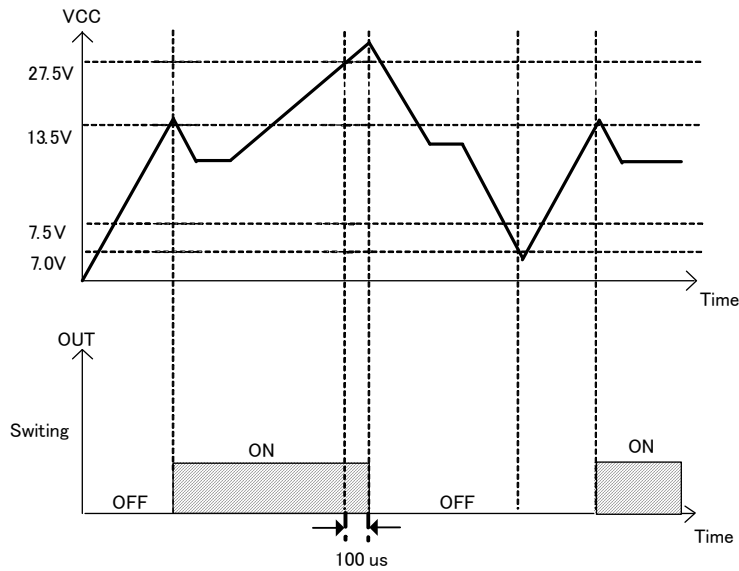


Figure 6, VCC UVLO/OVP Operation (Latch)

(3) DCDC Driver (PWM Comparator, Frequency Hopping, Slope Compensation, OSC, Burst)

BD7673AG uses current mode PWM control. In the internal generator, the average switching frequency is 65 kHz. Furthermore, switching frequency hopping function is built-in while the switching frequency fluctuation is shown as in Figure 7. Fluctuation cycle is 125Hz (=8ms).



Figure 7, Frequency Hopping Function

The max-duty cycle is fix to 75% (Typ) at OUT pin and minimum pulse width is fix at 500ns (Typ). When the duty cycle exceeds 50% at Current Mode control, the sub-harmonic oscillation occurs. To prevent it, IC is built-in slope compensation function.

BD7673AG has burst mode function to attain less power consumption when load is light. This function monitors FB pin voltage and detects light load when FB voltage < V_{BST} (=0.3V Typ).

The secondary output voltage, the FB voltage and the DCDC function are shown in Figure 8.

FB pin is pulled up by R_{FB} (=20k Ω Typ). At light load, when the secondary output voltage rises, the FB pin voltage will drop and when this goes below V_{BST} (=0.3V Typ) burst function will follow to reduce the power consumption.

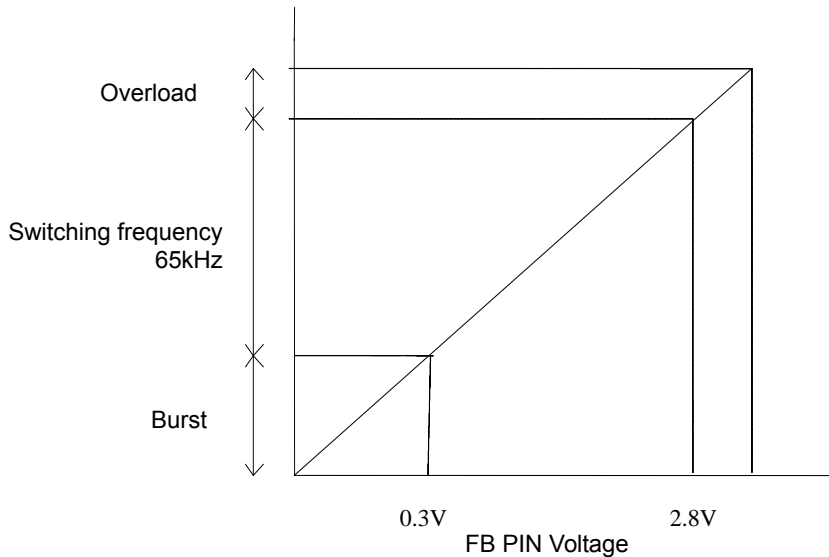


Figure 8, Switching Operation Status Changes by FB Pin Voltage

(4) Over Current Limiter and Leading Edge Blanking Period

BD7673AG has over current limiter for each switching cycle.

When the CS pin voltage exceeds the V_{CS} voltage ($=0.5V$ Typ), switching is turned OFF.

In addition, when the driver MOSFET is turned ON, surge current occurs at each capacitor component and drive current. Therefore, when the CS pin voltage rises temporarily, the detection errors may occur in the over current limiter circuit. To prevent detection errors, the OUT pin is switched from low to high and the CS signal is blanked for 250nsec by the LEB (Leading Edge Blanking) function. This blanking function enables a reduction of CS pin noise filtering in response to noise that occurs when the OUT pin is switched from low to high.

(5) Output Overload Protection Function (FB OLP Comparator)

Overload Protection Function monitors the load status of secondary output through FB pin and stops the switching of OUT pin during excessive load. In over load condition, there is no current in photo-coupler because output voltage decreases (drops) while FB pin voltage rises.

When FB pin voltage exceeds V_{FOLP1A} ($=2.8V$ Typ) at T_{FOLP} ($=250ms$ Typ) interval continuously, a load is excessive and OUT pin is fixed to L. The timer of overload protection is reset when FB pin drops further than V_{FOLP1B} ($=2.6V$ Typ) within T_{FOLP} ($=250ms$ Typ) after exceeding V_{FOLP1A} ($=2.8V$ Typ). Switching functions within this T_{FOLP} ($=250ms$ Typ).

FB voltage, which is pulled up in resistance to IC internal voltage operates from V_{FOLP1A} ($=2.8V$ Typ) or more at start-up. For this matter, set the start-up time of the secondary output voltage such that the FB voltage is always V_{FOLP1B} ($=2.6V$ Typ) or less within T_{FOLP} ($=250ms$ Typ) at start-up.

Excessive load is detected and latch stops when T_{FOLP} ($=250ms$ Typ) passes. Release of latch plugs/unplugs the power supply and is cancelled when $V_{CC} < V_{LATCH}$ ($=7.0V$ Typ).

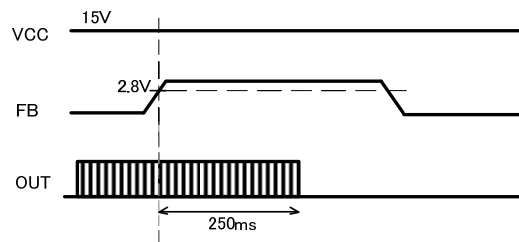


Figure 9, Overload Protection Latch

(6) COMP Pin External Latch Function

IC is latched when the COMP pin voltage goes below V_{COMP} (0.5V Typ). A latch timer for T_{LATCH} (100us Typ) added to prevent operation errors caused by noise. The COMP pin is pulled up by R_{COMP} (25.9kΩ Typ), and when R_T (3.7kΩ Typ) is pulled down at the COMP pin, latch protection is operated. Some application examples are shown in Figure 10, Figure 11, and Figure 12.

Overheating Protection by NTC Thermistor

A thermistor is attached to the COMP pin so that latching can be stopped when overheating occurs. In the case of this application, it should be designed so that the thermistor resistance becomes R_T (3.70kΩ Typ) when overheating is detected.

(Figure 10 and Figure 11 are application circuit examples in which latch operation occurs when $T_a = 110^{\circ}C$)

The variation in R_T (=3.70kΩ Typ) shown in an electrical property includes only IC. Please add the variation of external thermistor resistance to it and design.

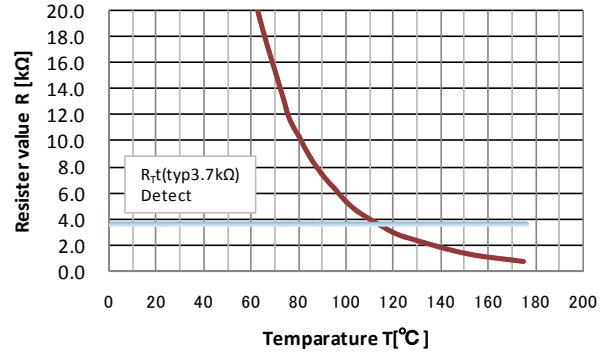
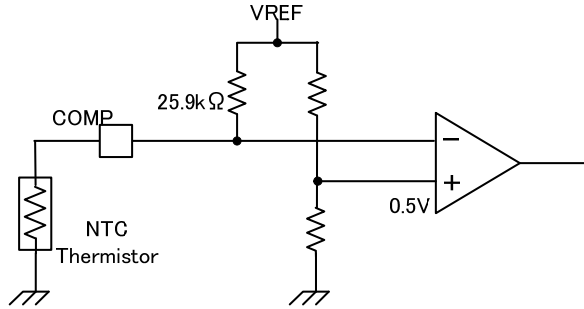


Figure 10, COMP Pin Overheating Protection Application

Figure 11, Temperature-Thermistor Resistance Value

Secondary Output Voltage Overvoltage Protection

A photo-coupler is attached to the COMP pin to perform detection of secondary output overvoltage.

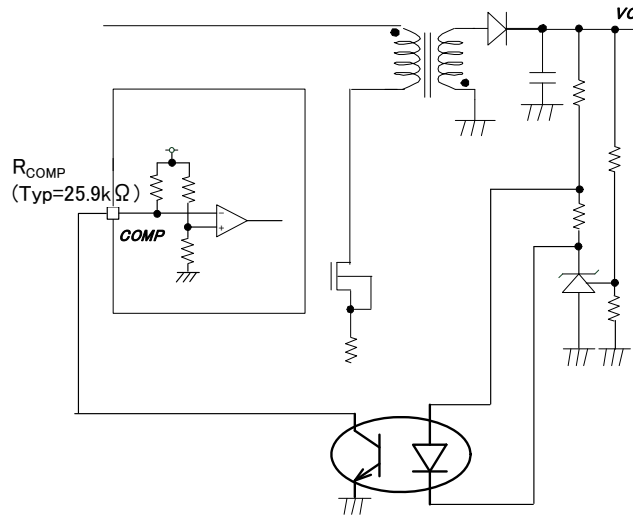


Figure 12. Output Overvoltage Protection Application

● Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	Vmax1	30	V	VCC, OUT
Maximum Applied Voltage 2	Vmax2	6.5	V	CS, FB, COMP
OUT pin output Peak Current	I _{OUT}	±1.0	A	
Allowable Dissipation	Pd	674.9 (Note1)	mW	When implemented
Operating Temperature Range	Topr	-40 to +85	°C	
Storage Temperature Range	Tstr	-55 to +150	°C	

(Note1): Derate by 5.399 mW/°C when operating above Ta=25°C (when mounted on 70 mm × 70 mm, 1.6 mm thick, glass epoxy on single-layer substrate).

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

● Recommended Operating Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Conditions
Power Supply Voltage Range	VCC	8.5 to 26.0	V	VCC pin voltage

● Electrical Characteristics (Unless otherwise noted, Ta = 25°C, VCC=12V)

Parameter	Symbol	Specifications			Unit	Conditions
		MIN	TYP	MAX		
[Circuit Current]						
Circuit Current (OFF)	I _{OFF}	-	12	20	μA	VCC = 12V (UVLO = Detection)
Circuit Current (ON) 1	I _{ON1}	-	600	1000	μA	FB = 2.0V COMP: 100kΩ (during pulse operation)
Circuit Current (ON) 2	I _{ON2}	-	400	650	μA	FB = 0.0V COMP: 100kΩ (during pulse operation when OFF)
[VCC Pin Protection Function]						
VCC UVLO Voltage 1	V _{UVLO1}	12.50	13.50	14.50	V	VCC rise
VCC UVLO Voltage 2	V _{UVLO2}	6.50	7.50	8.50	V	VCC drop
VCC UVLO Hysteresis	V _{UVLO3}	-	6.00	-	V	V _{UVLO3} = V _{UVLO1} - V _{UVLO2}
VCC OVP Voltage 1	V _{OVP1}	25.0	27.5	30.0	V	VCC rise

●Electrical Characteristics of control block (Unless otherwise noted, Ta = 25°C, VCC=12V)

Parameter	Symbol	Specifications			Unit	Conditions
		MIN	TYP	MAX		
[PWM Type DCDC Driver Block]						
Oscillation Frequency	F _{SW1}	60	65	70	KHz	FB=2.0V average frequency
Frequency Hopping Width 1	F _{DEL1}	-	4.0	-	KHz	FB=2.0V
Hopping Fluctuation Frequency	F _{CH}	93	125	157	Hz	
Minimum Pulse Width	T _{min}	-	500	-	ns	
Soft Start Time 1	T _{SS1}	0.75	1.00	1.25	ms	
Soft Start Time 2	T _{SS2}	6.00	8.00	10.00	ms	
Maximum Duty 1	D _{max}	68.0	75.0	82.0	%	During normal operation
Maximum Duty 2	D _{SS1}	5.0	15.0	25.0	%	During soft start 0[ms] to T _{SS1} [ms]
Maximum Duty 3	D _{SS2}	15.0	25.0	35.0	%	During soft start T _{SS1} [ms] to T _{SS2} [ms]
FB pin Pull-up Resistance	R _{FB}	15	20	25	kΩ	
∠FB / ∠CS Gain	Gain	-	5	-	V/V	
FB Burst Voltage	V _{BST}	0.20	0.30	0.40	V	During FB drop
FB OLP Voltage 1a	V _{FOLP1A}	2.5	2.8	3.1	V	When overload is detected (FB rise)
FB OLP Voltage 1b	V _{FOLP1B}	-	$V_{FOLP1A} - 0.2$	-	V	When overload is detected (FB drop)
FB OLP Timer	T _{FOLP}	187	250	312	ms	
Latch Release Voltage (VCC pin voltage)	V _{LATCH}	-	$V_{UVLO2} - 0.5$	-	V	Latch release voltage VCCUVLO2-0.5 [V]
Latch Mask Time	T _{LATCH}	50	100	200	us	VCCOVP, COMP Mask time
[Overcurrent Detection Block]						
Overcurrent Detection Voltage	V _{CS}	0.475	0.500	0.525	V	
Leading Edge Blanking Time	T _{LEB}	-	250	-	ns	
[Output Driver Block]						
OUT pin Pch MOS Ron	R _{POUT}	10	25	39	Ω	
OUT pin Nch MOS Ron	R _{NOUT}	3	7	12	Ω	
[External Latch Comparator Block]						
COMP pin Latch Detection Voltage	V _{COMP}	-	0.5	-	V	
COMP pin Pull-up Resistance	R _{COMP}	-	25.9	-	kΩ	
Thermistor Resistance Detection Value	R _T	3.30	3.70	4.10	kΩ	Thermistor connected to COMP pin

● Typical Performance Curves

(This is not a guarantee since this is the reference data. Figure 37 shows the measurement circuit diagram.)

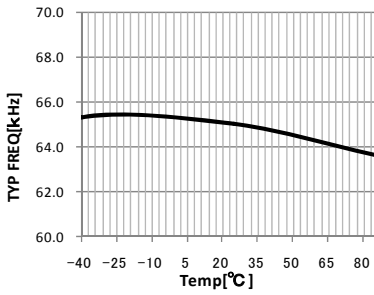


Figure 13, Typ Frequency Fsw1

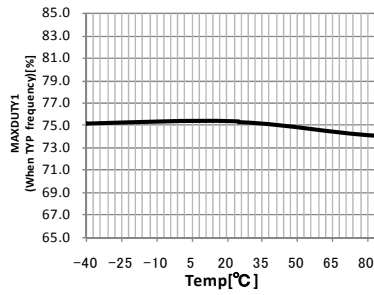


Figure 14, MAXDUTY1 (With Typ frequency)

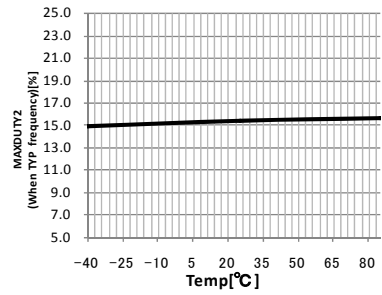


Figure 15, MAXDUTY2 (With Typ frequency)

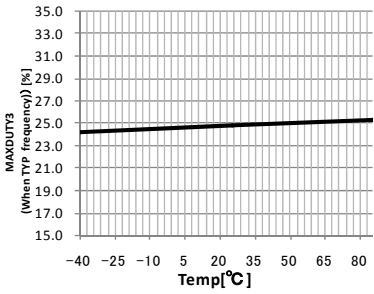


Figure 16, MAXDUTY3 (With Typ frequency)

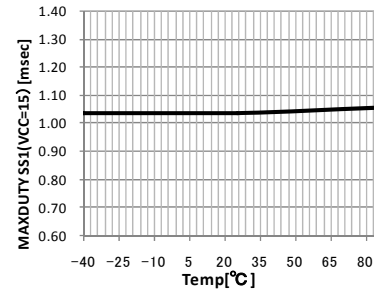


Figure 17, MAXDUTY SS1 (VCC=15)

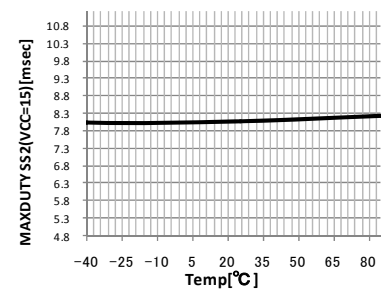


Figure 18, MAXDUTY SS2 (VCC=15)

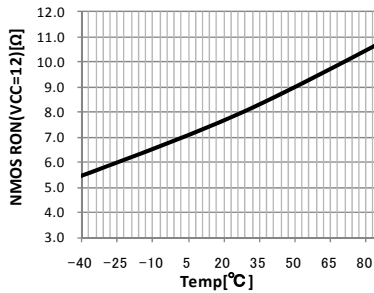


Figure 19, NMOS RON (VCC=12)

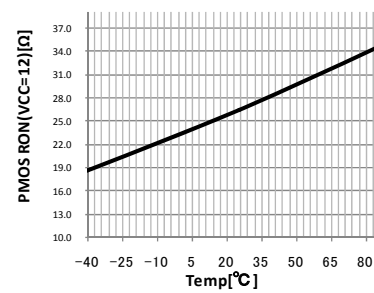


Figure 20, PMOS RON (VCC=12)

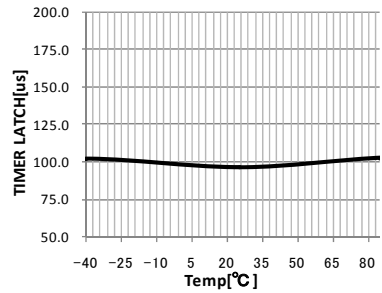


Figure 21, Timer Latch

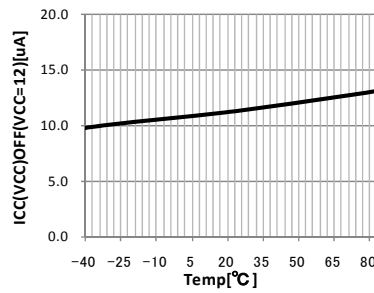


Figure 22, ICC (VCC) OFF (VCC=12)

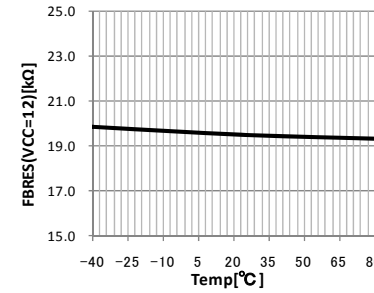


Figure 23, FBRES (VCC=12)

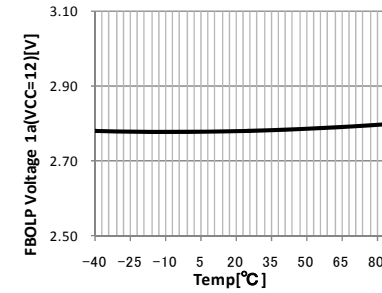


Figure 24, FBOLP Voltage 1a (VCC=12)

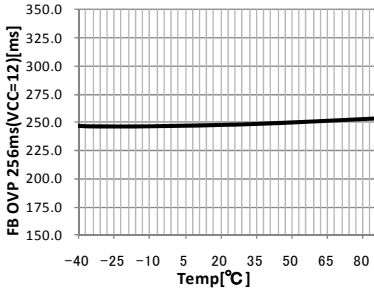


Figure 25, FB OVP 256ms(VCC=12)

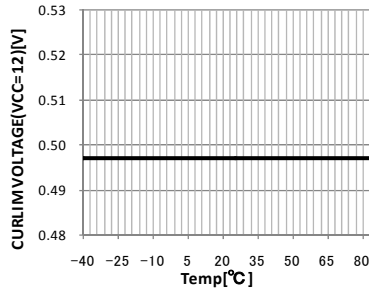


Figure 26, CURLIM Voltage (VCC=12)

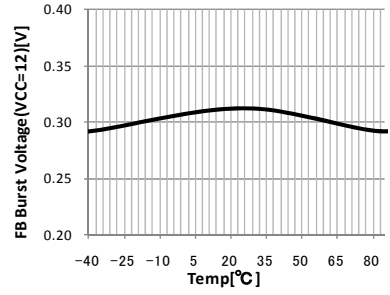


Figure 27, FB Burst Voltage (VCC=12)

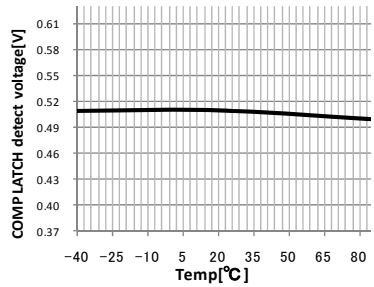


Figure 28, COMP Latch Detect Voltage

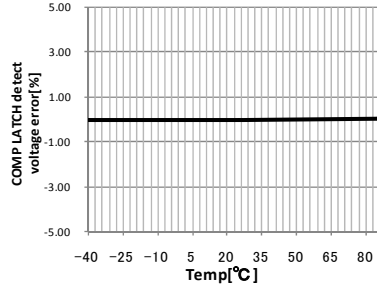


Figure 29, COMP Latch Detect Voltage Error

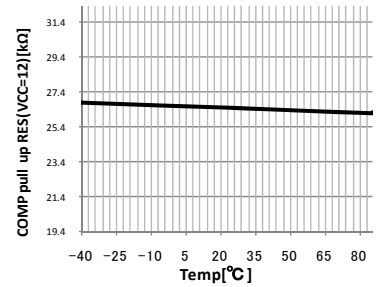


Figure 30, COMP Pull-up RES (VCC=12)

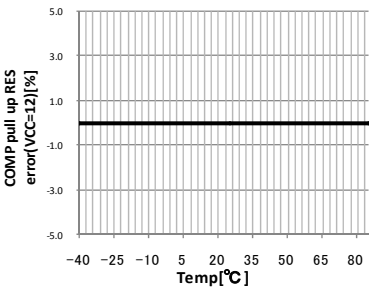


Figure 31, COMP Pull-up RES Error (VCC=12)

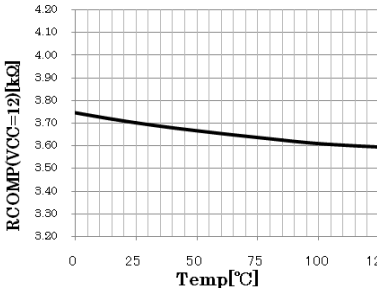


Figure 32, RCOMP (VCC=12)

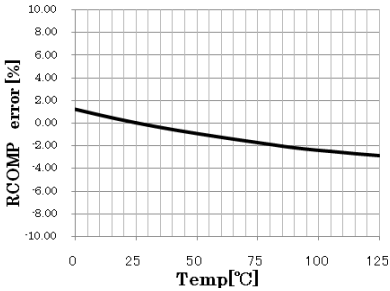


Figure 33, RCOMP Error

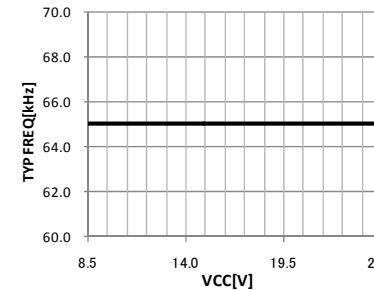


Figure 34, Typ Frequency Fsw1 (temp=25°C)

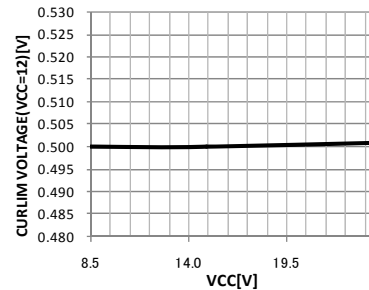


Figure 35, CURLIM Voltage (temp=25°C)

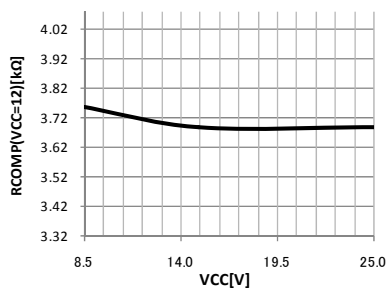


Figure 36, RCOMP (temp=25°C)

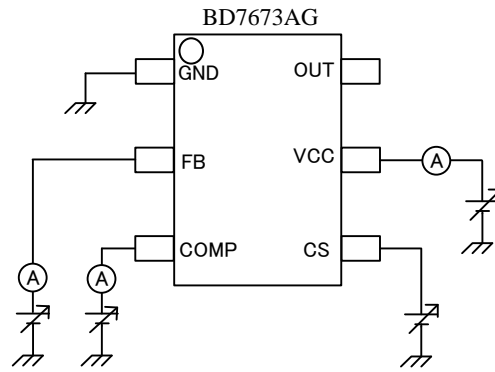


Figure 37, Measurement Circuit Diagram

●Power Dissipation

The thermal design should set the operation for the following conditions.
 (Since the temperature shown below is the guaranteed temperature, be sure to take margin into account.)

1. The ambient temperature T_a must be 85°C or less.
2. The IC's loss must be within the allowable dissipation P_d .

The thermal reduction characteristics are as follows.
 (PCB : $70\text{mm}\times 70\text{mm}\times 1.6\text{mm}$ mounted on glass epoxy single-layer substrate)

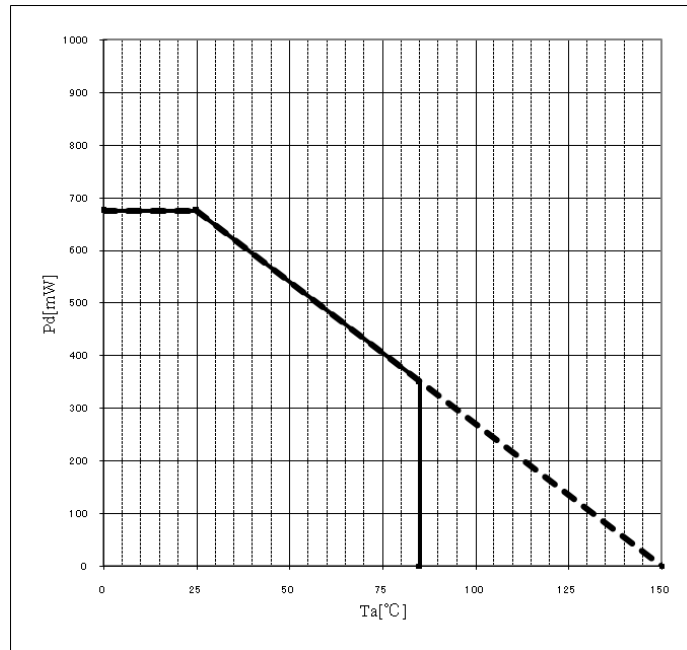


Figure 38, SSOP6 Thermal Reduction Characteristics

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to GND at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. GND Voltage

Ensure that no pins are at a voltage below that of the GND pin at any time, even during transient condition.

4. GND Wiring Pattern

When using both small-signal and large-current GND traces, the two GND traces should be routed separately but connected to a single GND at the reference point of the application board to avoid fluctuations in the small-signal GND caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The GND lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, GND the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to GND, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or GND line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

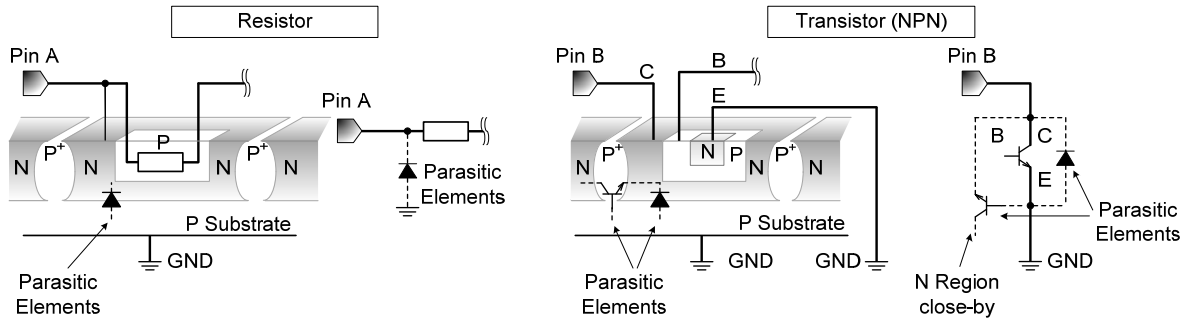


Figure xx. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

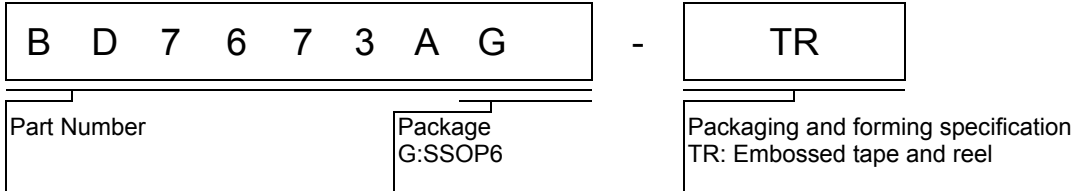
Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

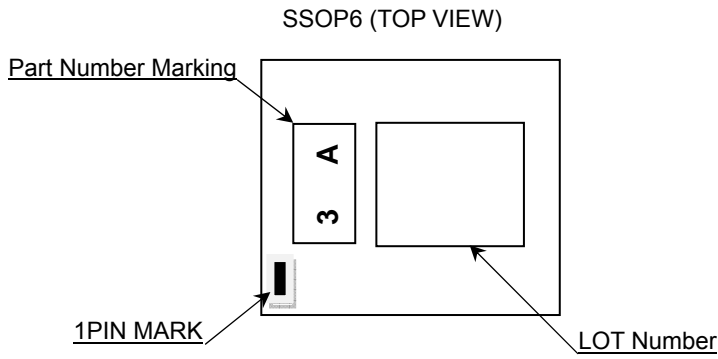
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

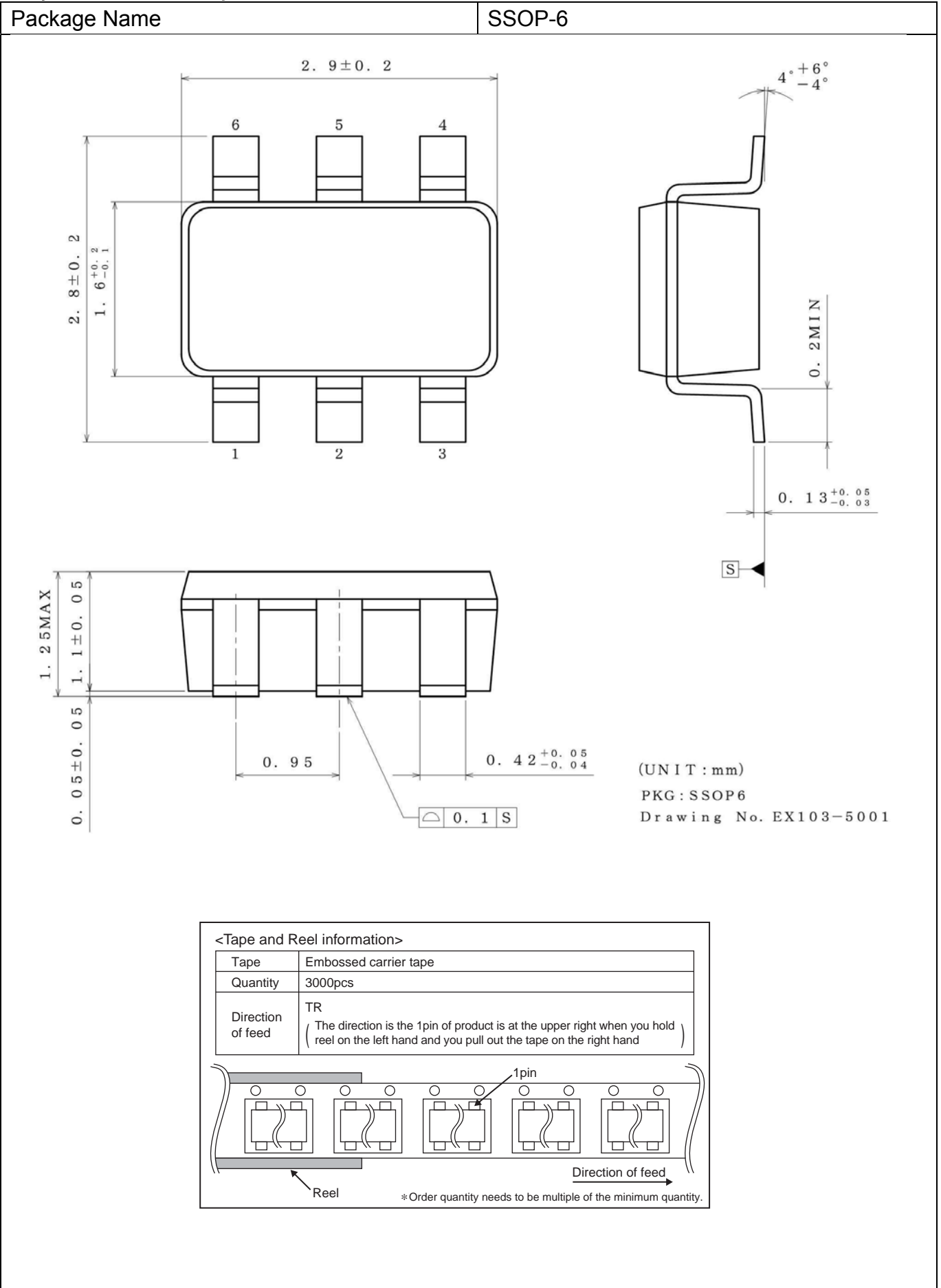
●Ordering Information



●Marking Diagram



●Physical Dimension, Tape and Reel Information



●Revision History

Date	Revision	Changes
28.May.2013	001	New preparation
16.Jul.2015	002	P1 Modify Figure 1 P4 Modify Figure 5 P8 Modify written error P9 Modify written error P10 Modify t written error P 13 Modify circuit Figure36 P13 Modify circuit Figure37 P16 Move Physical dimension page
22.Mar.2017	003	P6 Modify written error P7 Modify written error P8 Modify written error P9 explanation of package power

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- Confirm that operation temperature is within the specified range described in the product specification.
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