

# **System Motor Driver IC**

# for Half Height Drive(3 sensors)

BD7998EFS, BD7956FS/96EFV

# Description

BD7998EFS, BD7956FS/96EFV are ICs developed for spindle motor, actuator coil, stepping motor and loading motor drive of the desktop PC/DVD recorder. BD7998EFS is composed of 6ch, while BD7956FS/96EFV is composed of 7ch, with a built-in channel for the tilt motor drive.

The spindle and sepping use MOS FET to reduce power consumption and the actuator, tilt and loading driver use linear BTL drive system to redduce noise.

# Features

1) The spindle motor driver achieves low noise by ROHM's own energizing method. (BD7956FS/96EFV)

- 2) PWM control method of the low heat type is adopted in the stepping motor driver.
- 3) The actuator, tilt, loading driver achieve low noise by using linear BTL drive system.
- 4) ON/OFF of loading and other channels, brake mode of spindle driver and standby mode are selectable by the two control terminals.
- 5) Built-in thermal-shut down circuit.
- 6) Built-in triangular wave generator.
- 7) Improved heat radiation efficiency utilizing HTSSOP package (BD7998EFS,BD7996EFV).

# Applications

Optical disk equipments, such as desktop PC / DVD recorder

# Absolute maximum ratings

			-
Parameter	Symbol	Limits	Unit
POWER MOS power supply voltage	SPVM1,2,SLRNF1,2	15 #1	v
Preblock/BTL power block power supply voltage	Vcc(SPVM_S)=SLVDD,AVM	15	v
PWM control block power supply voltage	DVcc	7	v
Power dissipation	Pd	2.0#2 2.6#3	w
Operating temperature range	Topr	-35 ~ 85	°C
Storage temperature	Tstg	-55 ~ 150	°C

#1 POWER MOS output terminals is contained

#2 PCB (70mm × 70mm × 1.6mm glass epoxy) mounting Reduce by 16 mW/°C over 25°C (BD7998EFS, BD7996EFV) #3 PCB (70mm × 70mm × 1.6mm glass epoxy) mounting

Reduce by 20.8 mW/°C over 25°C. (BD7956FS)

# Recommended operating conditions

# (Set the power supply voltage taking allowable dissipation into considering)

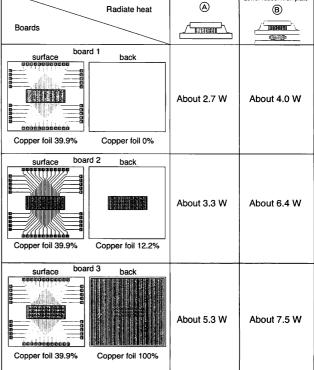
Parameter	Symbol	Min.	Тур.	Max.	Unit
POWER MOS Power supply voltage 1	SPVM1,2	-	(SPVM_S)	-	v
POWER MOS Power supply voltage 2	SLRNF1,2	-	SLVDD **	-	v
Preblock Power supply voltage	SLVDD=VCC(SPVM_S)	AVM	12	14	v
Power block Power supply voltage	AVM	4.3	5.0	VCC (SPVM_S)	v
PWM control block Power supply voltage	DVcc	4.3	5.0	6.0	v
Spindle output current	losp	-	1.2	2.5#5	A
SL/FO/TR/LO output current	loo	-	0.5	0.8	Α

#4 Set SPVM1, 2 and SLRNF1, 2 by the same voltage Vcc (SPVM\_S), SLV DD. Vcc (SPVM\_S) and SLVob are short-circuited. Please use accordint to potential.

#5 The current is guaranteed 3.0A in case of the current is tuned on/off in a duty-raio of less than 1/10 with a maximum on-time of 5msec.

board 3 surface back About 5.3 W About 7.5 W Copper foil 39.9% Copper foil 100% Glass epoxy board 70mm × 70mm × 1.6mm, under solder 4mm × 4mm,

upper rudder 18mm×10mm×1mm, Iron plate 190mm×150mm×0.5mm The thermal design should allow enough margin for actual power dissipation and must not exceed junction temperature of 150°C.



Under solder

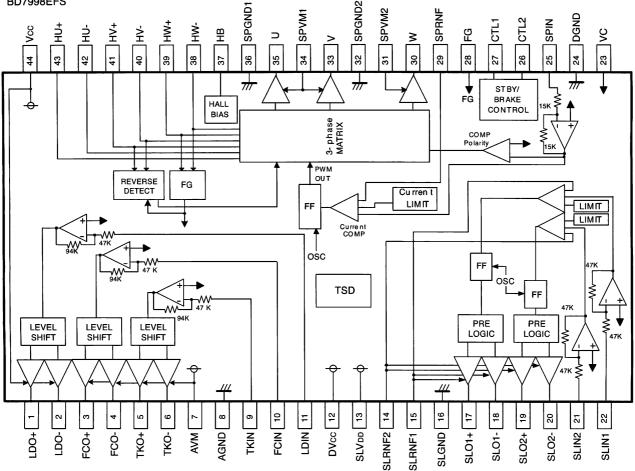
Lower rubber+iron plate

G1/DMM282

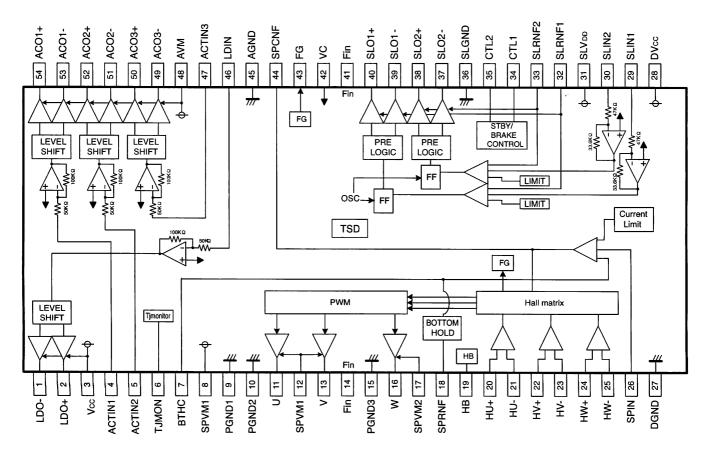


Block diagram





BD7956FS



# • Pin description

# BD7998EFS

BD1888	EFO				
No.	Symbol	Description	No.	Symbol	Description
1	LDO+	Loading driver positive output	44	Vcc	BTL pre and Loading power supply
2	LDO-	Loading driver negative output	43	HU+	Hall amp. U positive input
3	FCO+	Focus driver positive output	42	HU–	Hall amp. U negative input
4	FCO-	Focus driver negative output	41	HV+	Hall amp. V positive input
5	TKO+	Tracking driver positive output	40	HV-	Hall amp. V negative input
6	ТКО-	Tracking driver negative output	39	HW+	Hall amp. W positive input
7	AVM	Actuator driver block power supply	38	HW-	Hall amp. W negative input
8	AGND	Ground	37	НВ	Hall bias
9	TKIN	Tracking driver input	36	SPGND1	Spindle driver power ground 1
10	FCIN	Focus driver input	35	U	Spindle driver output U
11	LDIN	Loading driver input	34	SPVM1	Spindle driver power supply 1
12	DVcc	PWM block control power supply	33	V	Spindle driver output V
13	SLVDD	Sled driver PowerMOS pre-supply	32	SPGND2	Spindle driver power ground 2
14	SLRNF2	Sled driver 2 current sense	31	SPVM2	Spindle driver power supply 2
15	SLRNF1	Sled driver 1 current sense	30	W	Spindle driver output W
16	SLGND	Sled driver power ground	29	SPRNF	Spindle driver current sense
17	SLO1+	Sled driver 1 positive output	28	FG	Frequency generator output
18	SLO1-	Sled driver 1 negative output	27	CTL1	Driver logic control input 1
19	SLO2+	Sled driver 2 positive output	26	CTL2	Driver logic control input 2
20	SLO2-	Sled driver 2 negative output	25	SPIN	Spindle driver input
21	SLIN2	Sled driver 2 input	24	DGND	PWM block pre-ground
22	SLIN1	Sled driver 1 input	23	VC	Reference voltage input

· Positive/negative of the output terminals are determined in reference to those of the input terminals.

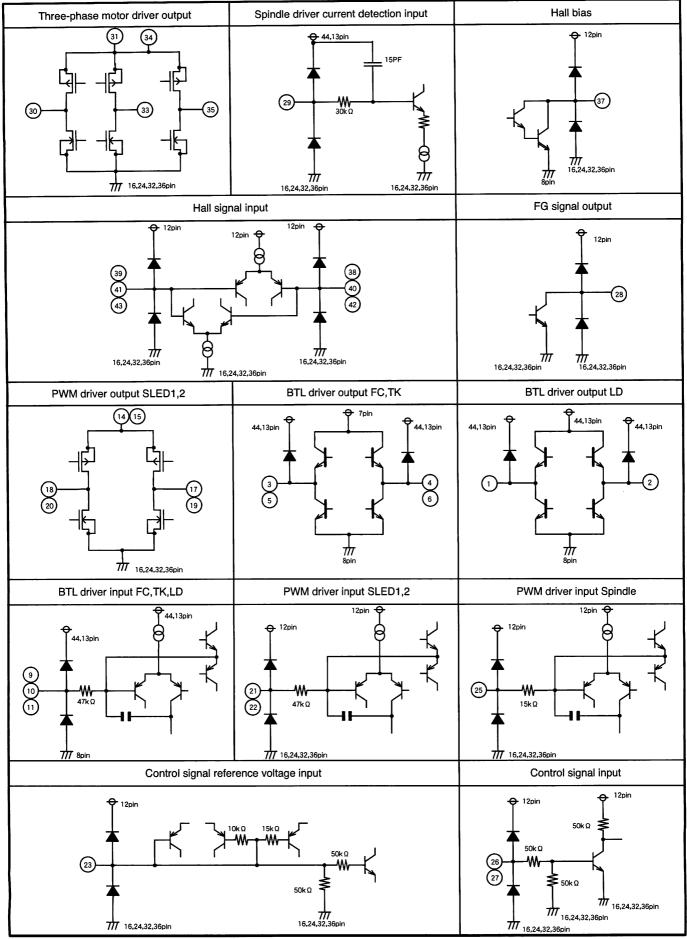
# BD7956FS

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No.	Symbol	Description	No.	Symbol	Description
1	LDO-	Loading driver negative output	54	ACO1+	Actuator driver 1 positive output
2	LDO+	Loading driver positive output	53	ACO1-	Actuator driver 1 negative output
3	Vcc	BTL pre and Loading power supply	52	ACO2+	Actuator driver 2 positive output
4	ACTIN1	Actuator driver 1 input	51	ACO2-	Actuator driver 2 negative output
5	ACTIN2	Actuator driver 2 input	50	ACO3+	Actuator driver 3 positive output
6	TJMON	Monitor of chip temperature	49	ACO3-	Actuator driver 3 negative output
7	BTHC	Capacitor connection terminal for spindle current bottom holding	48	AVM	Actuator driver block power supply
8	SPVM_S	Spindle driver sense power supply	47	ACTIN3	Actuator driver 3 input
9	PGND1	Spindle driver power ground 1	46	LDIN	Loading driver input
10	PGND2	Spindle driver power ground 2	45	AGND	BTL driver block power ground
11	U	Spindle driver output U	44	SPCNF	Spindle driver feedback filter
12	SPVM1	Spindle driver power supply 1	43	FG	Frequency generator output
13	V	Spindle driver output V	42	VC	Reference voltage input
14	Fin	Fin	41	Fin	Fin
15	PGND3	Spindle driver power ground 3	40	SLO1+	Sled driver 1 positive output
16	W	Spindle driver output W	39	SLO1-	Sled driver 1 negative output
17	SPVM2	Spindle driver power supply 2	38	SLO2+	Sled driver 2 positive output
18	SPRNF	Spindle driver current sense	37	SLO2-	Sled driver 2 negative output
19	НВ	Hall bias	36	SLGND	Sled driver power ground
20	HU+	Hall amp. U positive input	35	CTL2	Driver logic control 2 input
21	HU	Hall amp. U negative input	34	CTL1	Driver logic control 1 input
22	HV+	Hall amp. V positive input	33	SLRNF2	Sled driver 2 current sense
23	HV–	Hall amp. V negative input	32	SLRNF1	Sled driver 1 current sense
24	HW+	Hall amp. W positive input	31	SLVDD	Sled driver power MOS pre-supply
25	HW–	Hall amp. W negative input	30	SLIN2	Sled driver 2 input
26	SPIN	Spindle driver input	29	SLIN1	Sled driver 1 input
27	DGND	PWM block pre-ground	28	DVcc	PWM block control power supply

Positive/negative of the output terminals are determined in reference to those of the input terminals.

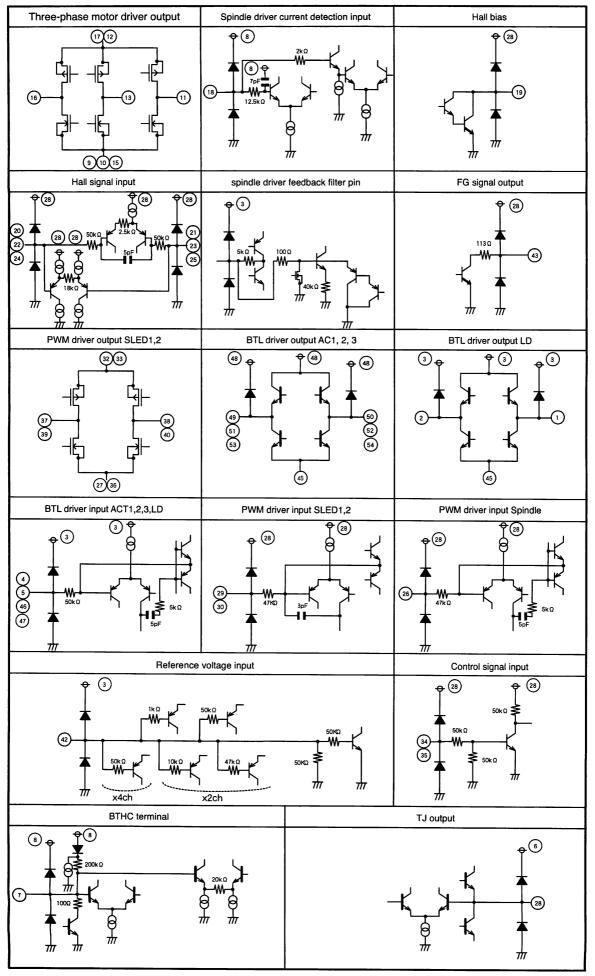
• Equivalent-circuit diagram of the terminals

# BD7998EFS



• Equivalent-circuit diagram of the terminals

BD7956FS



# • Electrical characteristics

# BD7998EFS

# (Unless otherwise noted Ta=25°C, VCC=SLVDD=12V, AVM=DVCC=5V, VC=1.65V, SPRNF=0.33Q, SLRNF=0.5Q, RL=8Q, RLSP=2Q)

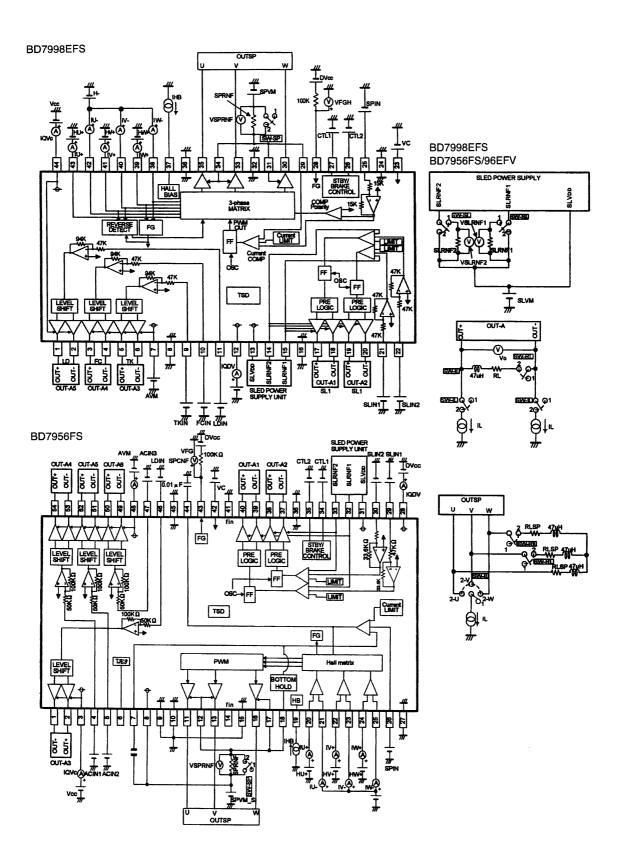
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Circuit current						•
Quiescent current 1	IQ1	-	12	20	mA	Vcc(Loading OFF mode)
Quiescent current 2	IQ2	-	7	12	mA	Vcc(Loading ON mode)
Quiescent current 3	IQ3	-	2.2	4.4	mA	DVcc
Standby-on current 1	IST1	-	0.18	0.4	mA	Vcc
Standby-on current 2	IST2	-	0.18	0.4	mA	DVcc
Sled driver block						
Input dead zone	VDZSL	15	40	65	mV	
(one side) Input output gain	gmSL	0.8	1.0	1.2	A/V (V/V)	SLRNF=0.5Ω
Output ON resistor	RONUSL	(0.4)	(0.5)	(0.6)	(v/v) Ω	IL=500mA
(upper) Output ON resistor	RONLSL	_	0.85	1.5	Ω	IL=-500mA
(lower) Output limit current	ILIMSL	0.96	1.10	1.24	A	SLRNF=0.5Ω
PWM frequency	fosc	(0.48)	(0.55)	(0.62)	(V) kHz	02.1111 -0.011
	· · · ·		100	_	KI 12	
Spindle driver block <	VHB	0.7	1.15	1.6	v	IHB=10mA
Hall bias voltage		0.7	1.15	1.0	v	
Spindle driver block <	r		<u> </u>	-		1
Input bias current	IHIB	-	1	5	A	
Minimum input level	VHIM	50	-	-	mVpp	
Common mode input Range	VHICM	1	-	4	V	
Spindle driver block <	Torque control >	T	r			
Input dead zone (one side)	VDZSP	20	50 3.0	90 3.6	mV A/V	
Input output gain	gmSP	(0.8)	(1.0)	(1.2)	(V/V)	SPRNF=0.33Ω
Output ON resistor (upper)	RONUSP	-	0.6	1.0	Ω	IL=500mA
Output ON resistor (lower)	RONLSP	-	0.3	0.7	Ω	IL=-500mA
Output limit current	ILIMSP	1.30 (0.43)	1.51 (0.5)	1.73 (0.57)	(V)	SPRNF=0.33Ω
PWM frequency	fosc	-	100	-	kHz	
Spindle driver block $<$	FG output >			_		
High voltage	VFGH	-	4.9	-	v	
Low voltage	VFGL	-	0.1	-	V	
Actuator driver block						
Output offset voltage	VOFFT	ñ50	0	50	mV	T
Output saturation voltage 'H'	VOHFT	-	0.4	0.75	v	IL=500mA
Output saturation voltage 'L'	VOLFT	-	0.55	1.0	v	IL=-500mA
Voltage gain	GVFT	16.0	17.5	19.0	dB	
Loading driver block	1	1	1	<u> </u>		_!
Output offset voltage	VOFLD	-50	0	50	mV	1
Output saturation voltage 'H'	VOHLD	- 1	1.9	2.5	v	IL=500mA
Output saturation voltage 'L'	VOLLD	- 1	0.55	1.0	v	IL=-500mA
Voltage gain	GVLD	16.0	17.5	19.0	dB	
CTL1,CTL2	I	1		1		I
Input high voltage	VIH	2.0		-	v	
Input low voltage	VIL			0.5	v	
Others	1 VIL			0.5		
	14410	0.4	0.7	10		1
VC drop-muting	VMVC	0.4	0.7	1.0	V	+
Vcc drop-muting	VMVcc of designed to b	3.4	3.8	4.2	V	

# BD7956/96EFV

(Unless otherwise noted Ta=25°C, SPVM\_S=SLVpo=Vcc=12V, DVcc=AVM=5V, VC=1.65V, SPRNF=0.22Ω, SLRNF=0.5Ω, RL=8Ω, RLSP=2Ω)

Unless otherwise noted 1a=25	10, 3PVM_3=3LVD0=	VCC=12V, DVCC	ZAVMESV, VC	=1.00V, 3PHN		INF=0.082, RL=082, RLOF=232)
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Circuit current			_			
Quiescent current 1	IQ1	-	12	20	mA	Vcc(Loading OFF mode)
Quiescent current 2	IQ2	-	5	9	mA	Vcc(Loading ON mode)
Quiescent current 3	IQ3	-	4	8.5	mA	DVcc
Stundby-on current 1	IST1	-	-	0.4	mA	Vcc
Stundby-on current 2	IST2	-	-	0.1	mA	DVcc
Sled driver block						
Input dead zone	VDZSL	5	30	55	mV	
(one side) Input output gain	gmSL	1.0 (0.50)	1.3 (0.65)	1.6 (0.8)	A/V (V/V)	SLRNF=0.5Ω
Output ON resistor	RONUSL	(0.50)	1.8	2.3	(4/4)	IL=500mA
(upper) Output ON resistor	RONLSL	_	0.8	1.4		IL=-500mA
(lower)	ILIMSL	0.84	1.0	1.16	A	SLRNF=0.5Ω
Output limit current		(0.42)	(0.50)	(0.58)	()	3LNNF=0.322
PWM frequency	fosc	_	100	-	kHz	
Spindle driver block <						1
Hall bias voltage	VHB	0.7	1.15	1.6	V	IHB=10mA
Spindle driver block <	Hall amplifier >	·				· · · · · · · · · · · · · · · · · · ·
Input bias current	IHIB	-	1	5	A	
Minimum input level	VHIM	50	-	-	mVpp	
Common mode input Range	VHICM	1	-	4	v	
Spindle driver block <	Torque control >	•				
Input dead zone (one side)	VDZSP	0	10	40	mV	
Input output gain	gmSP	1.24 (0.274)	1.54 (0.340)	1.84 (0.405)		SPRNF=0.22Ω
Output ON resistor	RONUSP	-	0.6	1.0	Ω	IL=500mA
(upper) Output ON resistor (lower)	RONLSP	-	0.2	0.4	Ω	IL=-500mA
Output limit current	ILIMSP	1.2 (0.264)	1.5 (0.33)	1.8 (0.396)	A (V)	SPRNF=0.22Ω
PWM frequency	fosc	(0.204)	100	-	kHz	
Spindle driver block <	FG output >	1		1		.i
High voltage	VFGH	_	4.9	-	v	1
Low voltage	VFGL	-	0.1	_	v	
Actuator driver blog			0.1			
Output offset voltage	VOFFT	ñ50	0	50	mV	T
Output onset voltage		1150			V	U. 500 A
voltage 'H' Output saturation	VOHFT		0.45	0.8		IL=500mA
voltage 'L'	VOLFT	-	0.45	0.8	V	IL=-500mA
Voltage gain	GVFT	16	17.5	19	dB	
Loading driver block	<b></b>					
Output offset voltage	VOFLD	-50	0	50	mV	
Output saturation Voltage 'H'	VOHLD	-	1.1	1.4	v	IL=500mA
Output saturation Voltage 'L'	VOLLD	-	0.45	0.8	v	IL=-500mA
Voltage gain	GVLD	16	17.5	19	dB	
CTL1,CTL2	-	-				
Input high voltage	VIH	2.0	-	DVcc	v	
Input low voltage	VIL	GND	-	0.5	v	
Others		1	I		L	- <del>1</del>
VC drop-muting	VMVC	0.4	0.7	1.0	v	
Vcc drop-muting	VMVcc	3.4	3.8	4.2	v	
* This product is no				1	, v	

\* This product is not designed to be radiation-resistant.



# Functional description

1) Driver control terminal 1and 2

All drivers and spindle-drive braking modes can be switched on/off by inputting combinations of H-level signal (higher than 2V) and L-level signal (lower than 0.5V) to these terminals.

CTL1	CTL2	Spindle	Sled	Focus	Tracking	Loading	]
L	L	×	×	×	×	×	1
Н	L	×	×	×	×	0	2
_	Н	0	0	0	0	×	] 0

..ON X...OFF

CTL1	CTL2	SPIN > VC	SPIN < VC	
L	Н	Forward-rotation mode	Reverse-rotation braking mode	3
н	Н	Forward-rotation mode	Short-circuit braking mode	4

① Standby mode

The IC is brought into standby mode, and its power dissipation can be limited.

2 Drivers muting

2) Input/output timing chart

All output channels, except the loading, are muted and their outputs are turned off.

③ Reverse-rotation braking mode(spindle)

A reverse-rotation torque is applied when SPIN < VC.

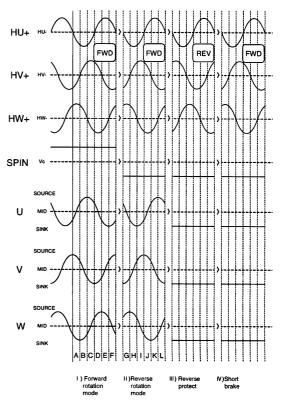
Reverse-rotation is detected with SPIN input and Hall input. If the spindle detects reverse rotation when SPIN < VC, all the outputs are shorted out to GND.

(4) Short-circuit braking mode(spindle)

All the spindle driver outputs are shorted out to GND when SPIN < VC.

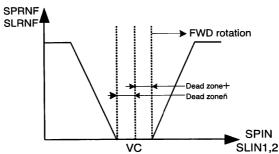
BD7998EFS HU+ FWD w RE HV+ HW+ SPIN SOURC U SIN SOURCE v SINK SOURCE w H⊦Z SIN II)Reverse rotation mode III) Reverse protect rotation V)Short brake





#### 3) Torque command / output current detection terminals

The relation between the torque command input and the output current detection terminals input is expressed in the figure below:



The input-output gain(gm) and the output-limit current(ILIM) depend on the resistance of RNF (output current detection resistor). Refer to the formula in the table on the following page.

The gain to drive the spindle or the sled motor can be decreased by connecting a resister in series, to each input terminal.

#### 4) PWM oscillation frequency

The PWM oscillation for driving the spindle and sled is free running. The oscillating frequency is 100kHz(typ.)

- 5) Muting functions
- 5-1) VC-drop muting

When the voltage at VC terminal drops to a value lower than 0.7V(Typ.), the outputs of all the channels are turned off. Set theVC terminal voltage higher than 1.0V

5-2) Vcc-drop muting

When the voltages at DVcc terminal and Vcc terminal drop to lower than 3.8V(Typ.), the outputs of all the channels are turned off.

6) Thermal-shut down

A themal-shutdown circuit (over-temperature protection circuit) is built in to prevent the IC from thermal breakdown. Use the IC according to the themal loss allowed in the package. In case the IC is left running over the allowable loss, the junction temperature rises, and the thermal-shutdown circuit works at a junction temperature of 175°C(Typ.) (All other chanel outputs are turned off). When the junction temperature drops to 150°C(Typ.) the IC resumes operation.

## External parts description

1) Filtering capacitor (BD7956FS / 96EFV)

It is recommended to connect 0.01F filtering capacitor to SPCNF terminals. This capacitor filters PWM output carrier frequency. Dispersion of the cut off frequency due to circuit board wiring layout is taken into consideration. If it is difficult to filter at the recommended value due to circuit board wiring led round, the capacity can be increased. In this case, note that the output transmission delay time may be longer.

2) Bypass capacitor

Please connect a bypass capacitor(0.1F) across the supply voltage lines close to the IC pins.

# Cautions on use

1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) Reverse polarity connection of the power supply

Connecting the of power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3) Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, note that capacitance characteristic values are reduced at low temperatures.

4) GND voltage

Ground-GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals should be lower than the GND potential voltage including an electric transients.

5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuitís power lines.

## 7) Operation in a strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

- ASO (Area of Safety Operation)
   Do not exceed the maximum ASO and the absolute maximum ratings of the output driver.
- 9) TSD (Thermal Shut-Down)

The TSD is activated when the junction temperature (Tj) reaches 175C (with +/-25C hysteresis), and the output terminal is switched to Hi-z. The TSD circuit aims to intercept IC from high temperature. The guarantee and protection of IC are not purpose. Therefore, please do not use this IC after TSD circuit operates, nor use it for assumption that operates the TSD circuit.

- 10) Capacitor between the output and GND If a large capacitor is connected between the output and GND, this IC might be destroyed when Vcc becomes 0V or GND, because, the electric charge accumulated in the capacitor flows to the output. Please set said capacitor to smaller than 0.1F.
- 11) The capacitor between SPRNF-GND

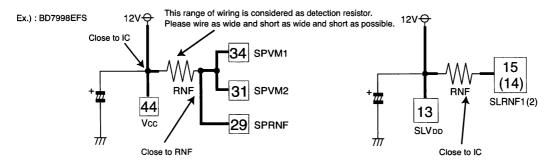
The capacitor between SPRNF-GND absorbs change of steep voltage and current on account of PWM drive, and suppresses disorder of Vcc voltage. However if a capacitor becomes far from IC, the effect will fall under the influence of wiring impedance etc. Please arrange the capacitor between SPRNF-GND near the IC.

12) Current detection reference voltage

The detection of current in the spindle and sled involves the detection of voltage between the detection resistances, but as the reference voltage of internal circuit, the voltage applied to Vcc (BD7998EFS), SPVM\_S (BD7956FS/96EFV) is used by the spindle and that applied to SLVDD by the sled. For this reason, be sure to apply Vcc (BD7998EFS), SPVM\_S (BD7956FS/96EFV) to the spindle and SLVDD to the sled according to the corresponding power supply voltages to prevent voltage differences.

13) Wiring for SPRNF and SLRNF

Considering the wiring resistance, connect each detecting resistor as close as possible to the current detection terminals for the spindle drive SPRNF and the sled motor drive SLRNF 1 and 2 of the IC.

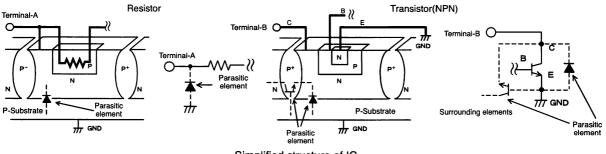


14) Earth wiring pattern

Use separate ground lines for control signals and high current power driver outputs. Because these high current outputs that flows to the wire impedance changes the GND voltage for control signal. Therefore, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above- mentioned.

15) Noise due to reverse polarity voltage

This IC is a monolithic IC, and has P<sup>+</sup> isolation and P substrate for the element separation. Therefore, a parasitic PN junction is firmed in this P-layer and N-layer of each element. For instance, the resistor or the transistor is connected to the terminal as shown in the figure below. When the GND voltage potential is greater than the voltage potential at Terminals A or B, the PN junction operates as a parasitic diode. In addition, the parasitic NPN transistor is formed in said parasitic diode and the N layer of surrounding elements close to said parasitic diode. These parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than GND(P substrate). Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed. Moreover, please impress each input terminal lower than the power-supply voltage or equal to the specified range in the guaranteed voltage when the power-supply voltage is impressing.



Simplified structure of IC

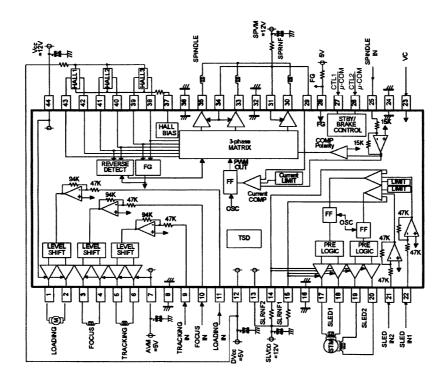
16) Inspection by the set circuit boad

The stress might hang to IC by connecting the capacitor to the terminal with low impedance. Then, Please discharge electricity in each and all process. Moreover, in the inspection process, please turn off the power before mounting the IC, and turn on after mounting the IC. In addition, please take into consideration the countermeasures for electrostatic damage, such as giving the earth in assembly process, transpotation or preservation.

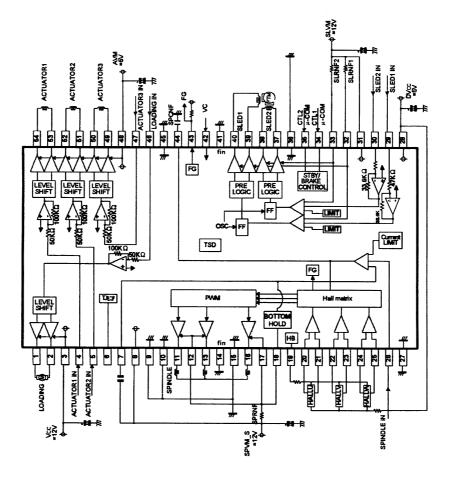
17) Fin (BD7956FS)

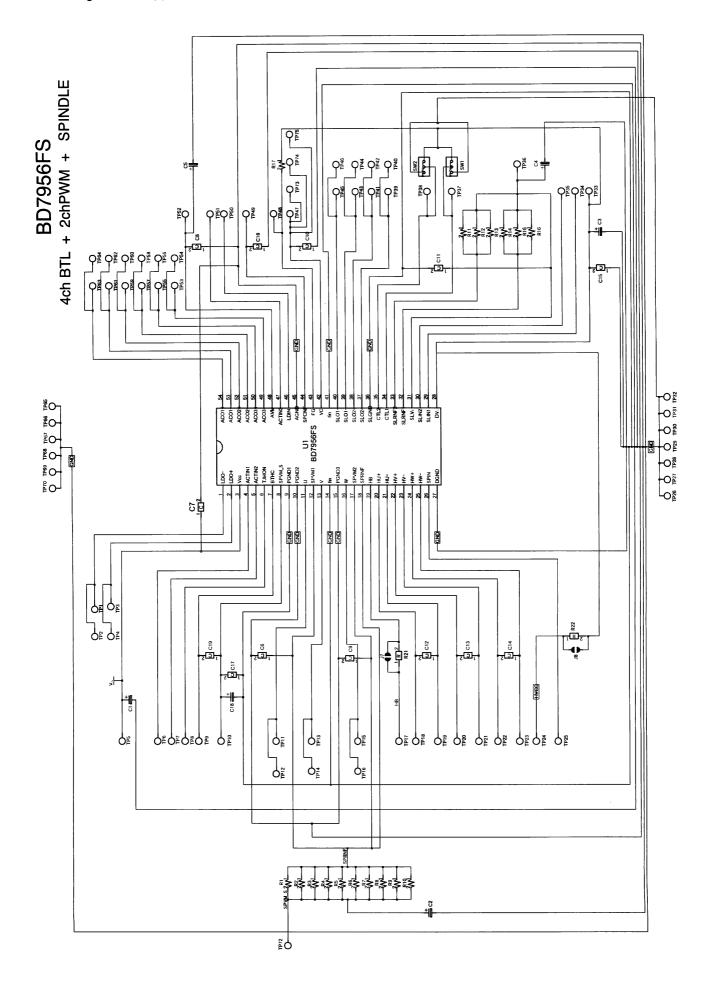
Heat dissipation fins (14,41pin) are attached to the GND on the inside of the package. Make sure to the external GND.

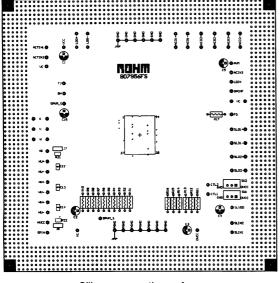
BD7998EFS



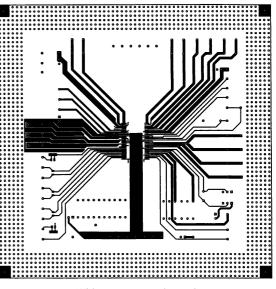
BD7956FS



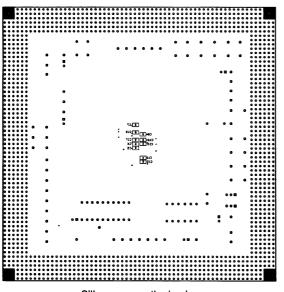




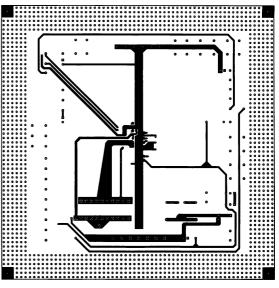
Silk screen on the surface



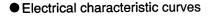
Wiring pattern on the surface

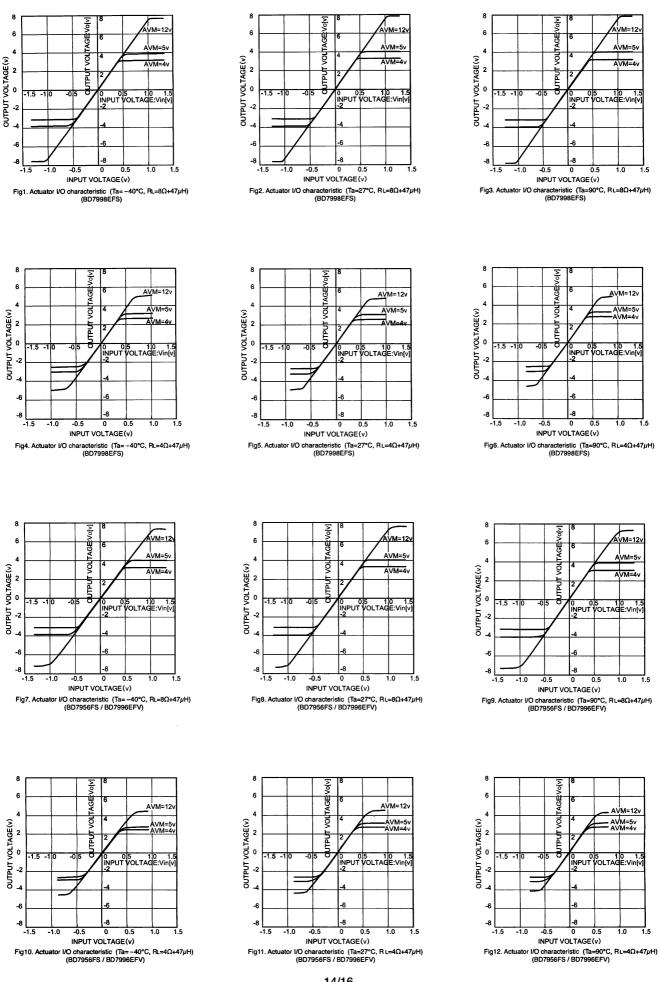


Silk screen on the back



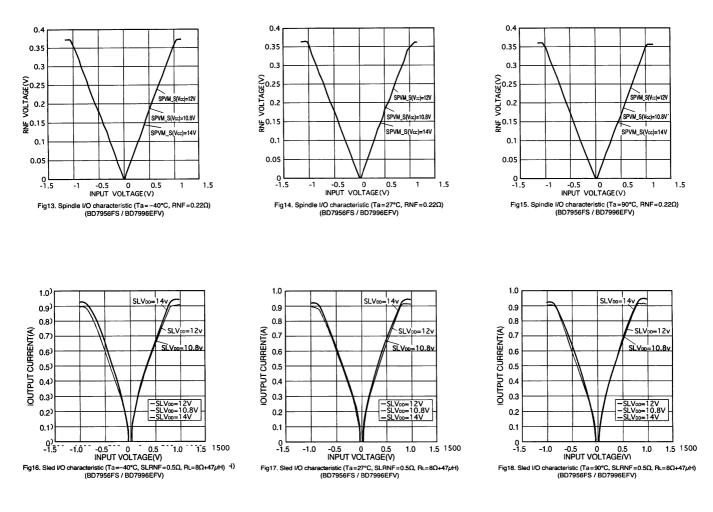
Wiring pattern on the back



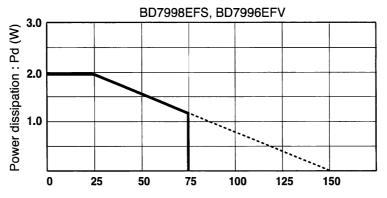


14/16

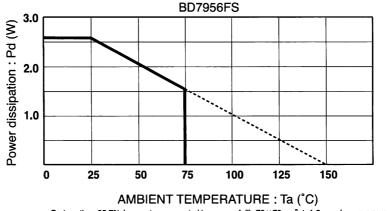
Electrical characteristic curves



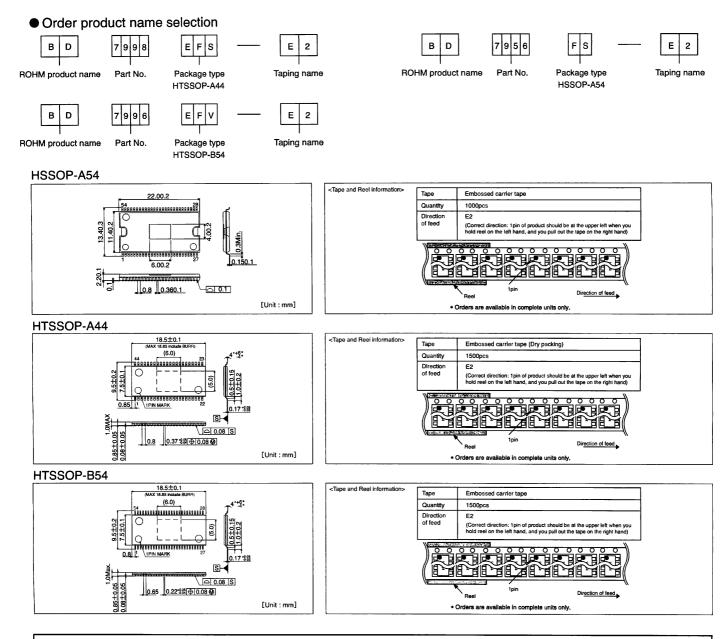
Power dissipation







 On less than 25.7% (percentage occupied by copper foil), 70 × 70mm<sup>2</sup>; t=1.6mm glass epoxy mounting. The maximum value improves with the substrate pattern and the heat radiation method.



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