

For Automotive 700 mA Adjustable Output LDO Regulators

BD800M7WFP2-C

General Description

The BD800M7WFP2-C is a linear regulator designed as a low current consumption product for power supplies in various automotive applications.

This product is designed for up to 45 V as an absolute maximum voltage and to operate until 700 mA for the output current with low current consumption 17 μ A (Typ). This can regulate the output with a very high accuracy^(Note 1), $\pm 2.5\%$. The output voltage can be adjusted between 1.2 V and 16 V by an external resistive divider connected to the adjustment pin. This regulator is therefore an ideal for any applications requiring a direct connection to the battery and a low current consumption.

A logical "HIGH" at the EN pin turns on the device, and in the other side, the device is controlled to disable by a logical "LOW" input to the EN pin.

The device features the integrated Over Current Protection to protect the device from a damage caused by a short-circuiting or an overload. This product also integrates Thermal Shutdown Protection to avoid the damage by overheating.

Furthermore, low ESR ceramic capacitors are sufficiently applicable for the phase compensation.

(Note 1) The tolerance of feedback resistor is not included.

Key Specifications

- Wide Temperature Range (Tj): -40 °C to +150 °C
- Wide Operating Input Range: 3 V to 42 V
- Low Current Consumption: 17 μ A(Typ)
- Output Current Capability: 700 mA
- High Output Voltage Accuracy: $\pm 2.5\%$
- Output Voltage: 1.2 V to 16 V

Package

TO263-5

W(Typ) x D(Typ) x H(Max)

10.16 mm x 15.10 mm x 4.70 mm



Features

- AEC-Q100 Qualified^(Note 2)
- Output Shutdown Function (EN Function)
- Over Current Protection (OCP)
- Thermal Shutdown Protection (TSD)

(Note 2) Grade 1

Applications

- Power Train
- Body
- Audio System
- Navigation System

Typical Application Circuit

- Components Externally Connected

Capacitor: $0.1 \mu\text{F} \leq C_{IN} \text{ (Min)}, 1.47 \mu\text{F} \leq C_{OUT} \text{ (Min)}$ ^(Note 3)

Resistor: $5 \text{ k}\Omega \leq R_1 \leq 200 \text{ k}\Omega$ ^{(Note 4) (Note 5)}

$V_{ADJ} \text{ (Typ): } 0.65 \text{ V}$

$$R_2 = R_1 \left(\frac{V_{OUT}}{V_{ADJ}} - 1 \right)$$

(Note 3) Electrolytic, tantalum and ceramic capacitors can be used.

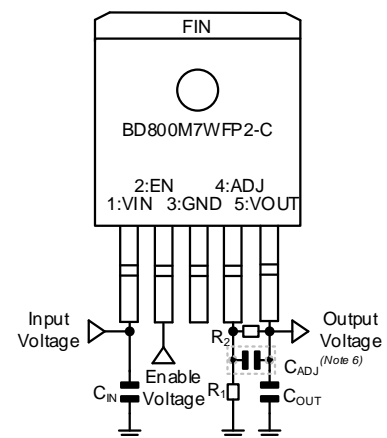
(Note 4) The tolerance of feedback resistor is not included in the accuracy of output voltage.

(Note 5) The value of a feedback resistor R_1 must be within this range.

R_2 value is defined by following the formula using the limitation of R_1 .

(Note 6) If it needs better transient characteristic, insert a capacitor between

the VOUT and ADJ pins. Refer to [Typical Application and Layout Example](#) for the details such as equations.

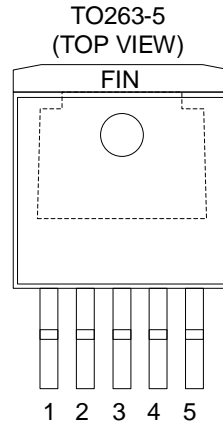


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Pin Configurations

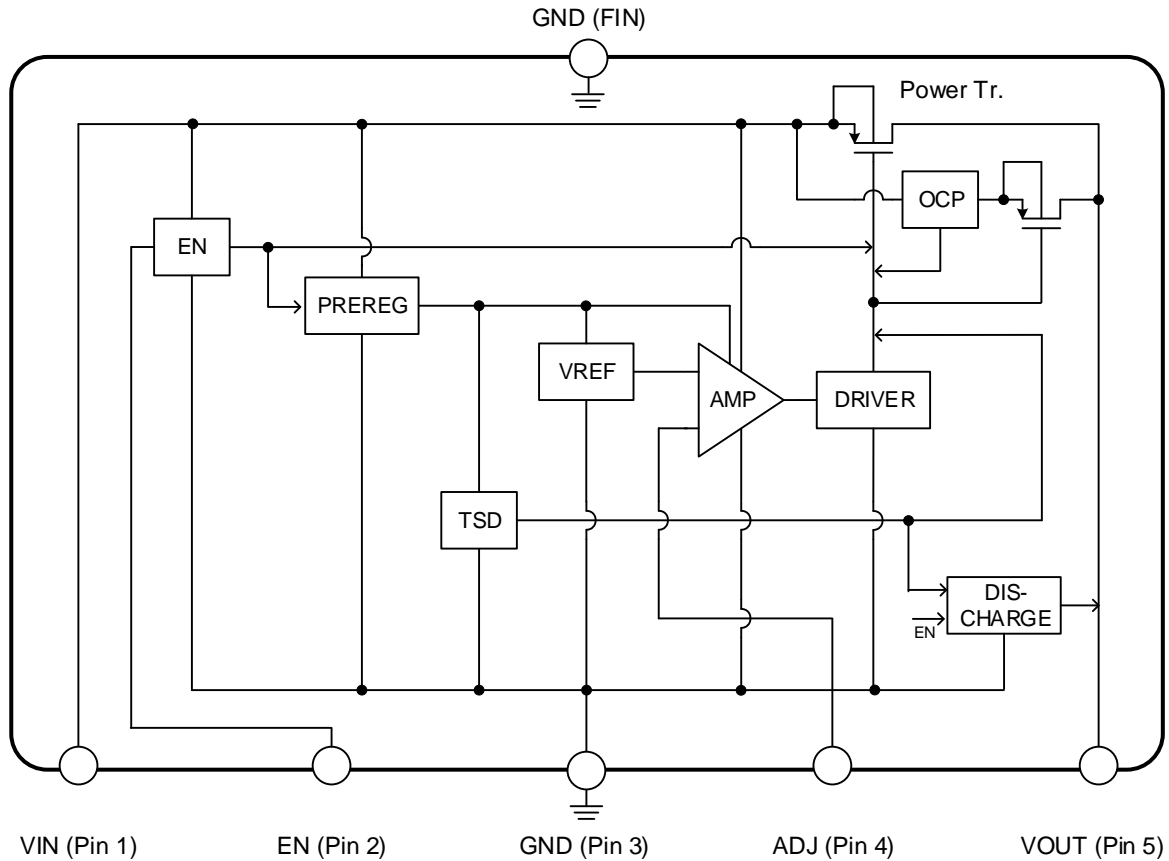


Pin Descriptions

Pin No.	Pin Name	Function	Descriptions
1	VIN	Input Supply Voltage Pin	It is necessary to use a capacitor with a capacitance of 0.1 μF (Min) or higher between the VIN pin and GND. The detail of a selection is described in Selection of External Components . If the inductance of power supply line is high, please adjust input capacitor value.
2	EN	Control Output ON/OFF Pin	A logical "HIGH" ($V_{\text{EN}} \geq 2.0 \text{ V}$) at the EN pin enables the device and "LOW" ($V_{\text{EN}} \leq 0.8 \text{ V}$) at the EN pin disables the device.
3	GND	Ground Pin	Ground.
4	ADJ	Adjustment Pin For Output Voltage	Connect an external resistor to adjust output voltage.
5	VOUT	Output Voltage Pin	Connect an external resistor to adjust output voltage. It is necessary to use a capacitor with a capacitance of 1.47 μF (Min) or higher between the VOUT pin and GND. The detail of a selection is described in Selection of External Components
FIN	GND	Ground Pin	Ground. This pin should be connected to Analog ground / Power ground or Heat Sink.

Block Diagram

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Description of Blocks

Block Name	Function	Description of Blocks
EN	Control Output Voltage ON/OFF	A logical "HIGH" ($V_{EN} \geq 2.0\text{ V}$) at the EN pin enables the device and "LOW" ($V_{EN} \leq 0.8\text{ V}$) at the EN pin disables the device.
PREREG	Internal Power Supply	Power supply for internal circuit.
TSD	Thermal Shutdown Protection	In case maximum power dissipation is exceeded or the ambient temperature is higher than the Maximum Junction Temperature, overheating causes the chip temperature (T_j) to rise. The TSD protection circuit detects this and forces the output to turn off in order to protect the device from overheating. When the junction temperature decreases to low, the output turns on automatically. (Typ:175 °C)
VREF	Reference Voltage	Generate the reference voltage.
AMP	Error Amplifier	The error amplifier amplifies the difference between the feedback voltage of the output voltage and the reference voltage.
DRIVER	Output MOSFET Driver	Drive the output MOSFET (Power Tr.)
OCP	Over Current Protection	If the output current increases higher than the maximum output current, it is limited by Over Current Protection in order to protect the device from a damage caused by an over current. While this block is operating, the output voltage may decrease because the output current is limited. If an abnormal state is removed and the output current value returns to normal, the output voltage also returns to normal state.(Typ:1400 mA)
DISCHARGE	Output Discharge Function	Output pin is discharged when EN = Low input or TSD detected.(Typ:4 kΩ)

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage ^(Note 1)	V _{IN}	-0.3 to +45	V
EN Pin Voltage ^(Note 2)	V _{EN}	-0.3 to +45	V
Output Pin Voltage	V _{OUT}	-0.3 to +20 (≤ V _{IN} + 0.3)	V
ADJ Pin Voltage	V _{ADJ}	-0.3 to +7	V
Junction Temperature Range	T _j	-40 to +150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Maximum Junction Temperature	T _{jmax}	150	°C
ESD Withstand Voltage (HBM) ^(Note 3)	V _{ESD_HBM}	±2000	V
ESD Withstand Voltage (CDM) ^(Note 4)	V _{ESD_CDM}	±750	V

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance and power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) Do not exceed T_{jmax}.

(Note 2) The start-up orders of power supply (V_{IN}) and the V_{EN} do not influence if the voltage is within the operation power supply voltage range.

(Note 3) ESD susceptibility Human Body Model "HBM"; base on ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).

(Note 4) ESD susceptibility Charged Device Model "CDM"; base on JEDEC JESD22-C101.

Thermal Resistance ^(Note 5)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 7)	2s2p ^(Note 8)	
TO263-5				
Junction to Ambient	θ _{JA}	80.2	21.8	°C/W
Junction to Top Characterization Parameter ^(Note 6)	Ψ _{JT}	10	2	°C/W

(Note 5) Based on JESD51-2A(Still-Air). Using BD800M7WFP2-C Chip.

(Note 6) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 7) Using a PCB board based on JESD51-3.

(Note 8) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 9)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 9) This thermal via connects with the copper pattern of all layers.

Operating Conditions(-40°C ≤ Tj ≤ +150°C)

Parameter	Symbol	Min	Max	Unit
Input Voltage ^(Note 1)	V _{IN}	V _{OUT(Max)} + ΔVd(Max)	42	V
Start-Up Voltage ^(Note 2)	V _{IN Start-Up}	3	-	V
Output Voltage	V _{OUT}	1.2	16	V
Feedback Resistor ADJ vs GND ^(Note 3)	R ₁	5	200	kΩ
Output Control Voltage	V _{EN}	0	42	V
Output Current	I _{OUT}	0	700	mA
Input Capacitor ^(Note 4)	C _{IN}	0.1	-	μF
Output Capacitor ^(Note 5)	C _{OUT}	1.47	1000	μF
Output Capacitor Equivalent Series Resistance	ESR(C _{OUT})	-	5	Ω
VOUT-ADJ Capacitor	C _{ADJ}	-	1000	pF
Operating Temperature	T _a	-40	+125	°C

(Note 1) Minimum Input Voltage must be 3.3 V or more.

Please consider that the output voltage would be dropped (Dropout voltage ΔVd) by the output current.

(Note 2) If V_{OUT} setting is 3 V or less, V_{OUT} (Min) = 90 % × V_{OUT} (Typ) when V_{IN} = 3 V, I_{OUT} = 0 mA.

(Note 3) If it needs better transient characteristic, insert a capacitor between the VOUT and ADJ pins. Refer to [Typical Application and Layout Example](#) for the details such as equations.

(Note 4) If the inductance of power supply line is high, please adjust input capacitor value.

(Note 5) Set the value of the capacitor so that it does not fall below the minimum value. Take into consideration the temperature characteristics and DC device characteristics.

Electrical Characteristics

LDO Function (V_{OUT} setting = 5 V, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$)Unless otherwise specified, $T_j = -40\text{ }^\circ\text{C}$ to $+150\text{ }^\circ\text{C}$, $V_{IN} = 13.5\text{ V}$, $V_{EN} = 5\text{ V}$, $I_{OUT} = 0\text{ mA}$ Typical values are defined at $T_j = 25\text{ }^\circ\text{C}$, $V_{IN} = 13.5\text{ V}$

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Shutdown Current	I_{SHUT}	-	1	5	μA	$V_{EN} = 0\text{ V}$ $T_j \leq 125\text{ }^\circ\text{C}$
Current Consumption ^(Note 1)	I_{CC}	-	17	34	μA	$I_{OUT} \leq 700\text{ mA}$ $T_j \leq 25\text{ }^\circ\text{C}$
		-	17	43	μA	$I_{OUT} \leq 700\text{ mA}$ $T_j \leq 85\text{ }^\circ\text{C}$
		-	17	46	μA	$I_{OUT} \leq 700\text{ mA}$ $T_j \leq 105\text{ }^\circ\text{C}$
		-	17	49	μA	$I_{OUT} \leq 700\text{ mA}$ $T_j \leq 125\text{ }^\circ\text{C}$
		-	17	53	μA	$I_{OUT} \leq 700\text{ mA}$ $T_j \leq 150\text{ }^\circ\text{C}$
Reference Voltage	V_{ADJ}	0.633	0.650	0.667	V	$6\text{ V} \leq V_{IN} \leq 42\text{ V}$ $0.5\text{ mA} \leq I_{OUT} \leq 400\text{ mA}$
Dropout Voltage	ΔV_d	-	0.6	1.2	V	$V_{IN} = V_{OUT} \times 0.95$ $I_{OUT} = 700\text{ mA}$
Ripple Rejection	R.R.	60	70	-	dB	$f = 120\text{ Hz}$, $e_{in} = 1\text{ V}_{rms}$ $I_{OUT} = 100\text{ mA}$
Line Regulation	Reg.I	-	0.02	0.4	$\% \times V_{OUT}$	$6\text{ V} \leq V_{IN} \leq 28\text{ V}$ $T_j \leq 125\text{ }^\circ\text{C}$
		-	0.02	0.6	$\% \times V_{OUT}$	$6\text{ V} \leq V_{IN} \leq 28\text{ V}$ $T_j \leq 150\text{ }^\circ\text{C}$
Load Regulation	Reg.L	-	0.02	0.4	$\% \times V_{OUT}$	$0.5\text{ mA} \leq I_{OUT} \leq 400\text{ mA}$ $T_j \leq 125\text{ }^\circ\text{C}$
		-	0.02	0.6	$\% \times V_{OUT}$	$0.5\text{ mA} \leq I_{OUT} \leq 400\text{ mA}$ $T_j \leq 150\text{ }^\circ\text{C}$
Overload Current Protection	$I_{OUT(OC)}$	750	1400	-	mA	$6\text{ V} \leq V_{IN} \leq 42\text{ V}$ $V_{OUT} = 90\% \times V_{OUT(Typ)}$
Thermal Shutdown Temperature	$T_{j(TSD)}$	151	175	-	$^\circ\text{C}$	-

(Note 1) It does not contain the current of R_1 and R_2 .

Enable Function

Unless otherwise specified, $T_j = -40\text{ }^\circ\text{C}$ to $+150\text{ }^\circ\text{C}$, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $V_{EN} = 5\text{ V}$ Typical values are defined at $T_j = 25\text{ }^\circ\text{C}$, $V_{IN} = 13.5\text{ V}$

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Enable Mode Voltage	V_{ENH}	2.0	-	42.0	V	-
Disable Mode Voltage	V_{ENL}	0	-	0.8	V	-
Enable Bias Current	I_{EN}	-	4	8	μA	-

Typical Performance Curves

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V, $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$

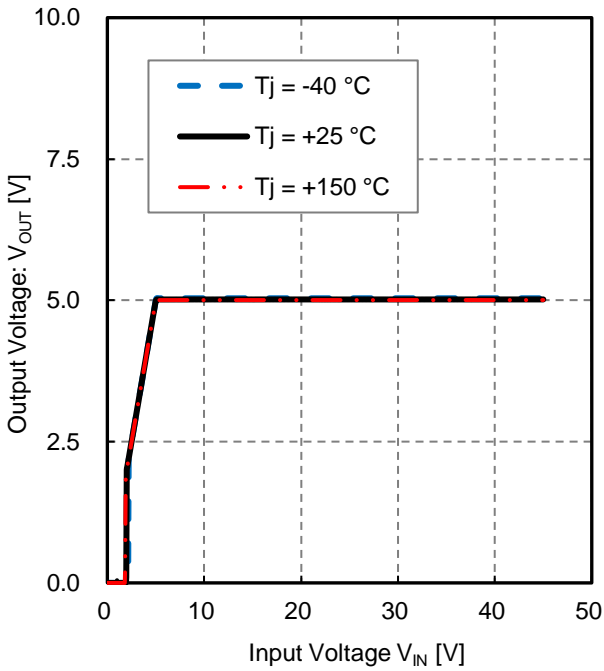


Figure 1.
Output Voltage vs Input Voltage

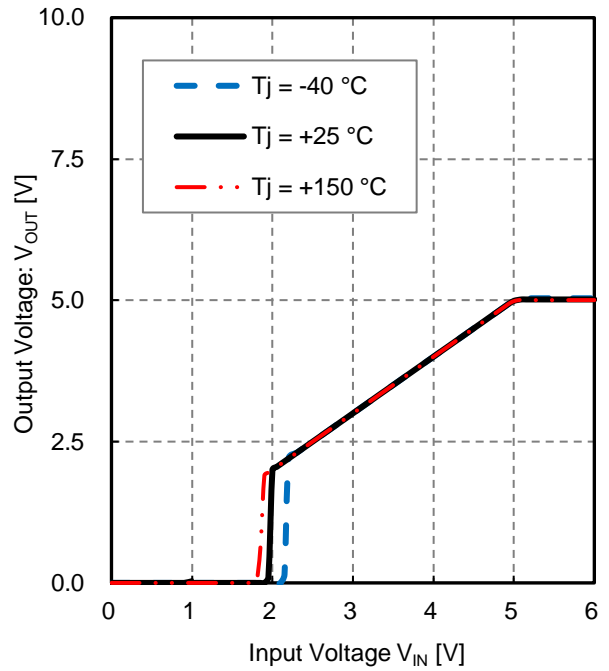


Figure 2.
Output Voltage vs Input Voltage - Enlarged view

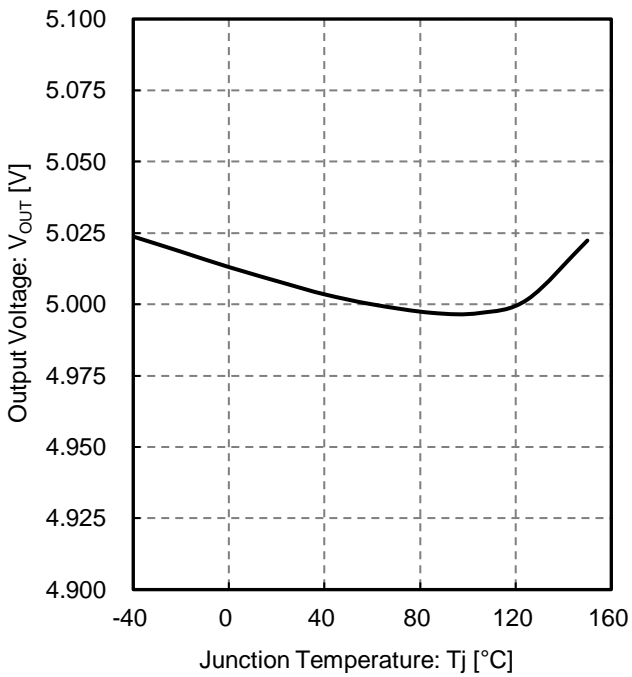


Figure 3.
Output Voltage vs Junction Temperature
($I_{OUT} = 0.5\text{ mA}$)

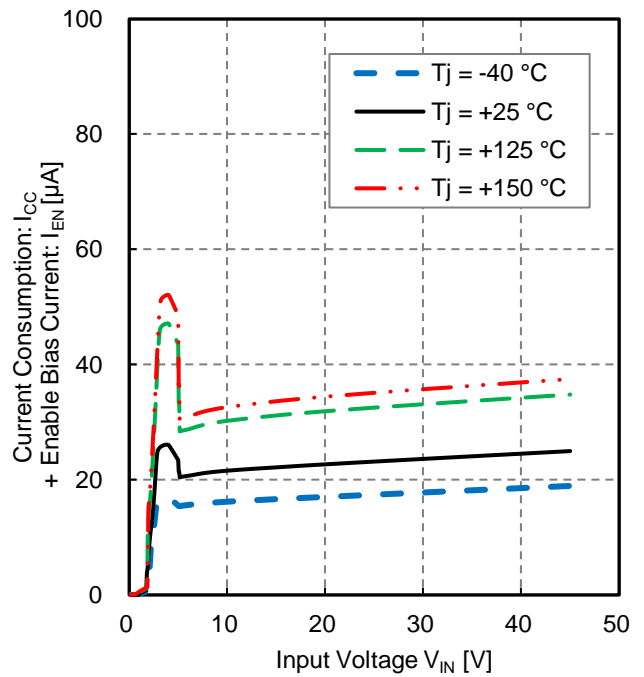


Figure 4.
Current Consumption + Enable Bias Current
vs Input Voltage

Typical Performance Curves - continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V , $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$

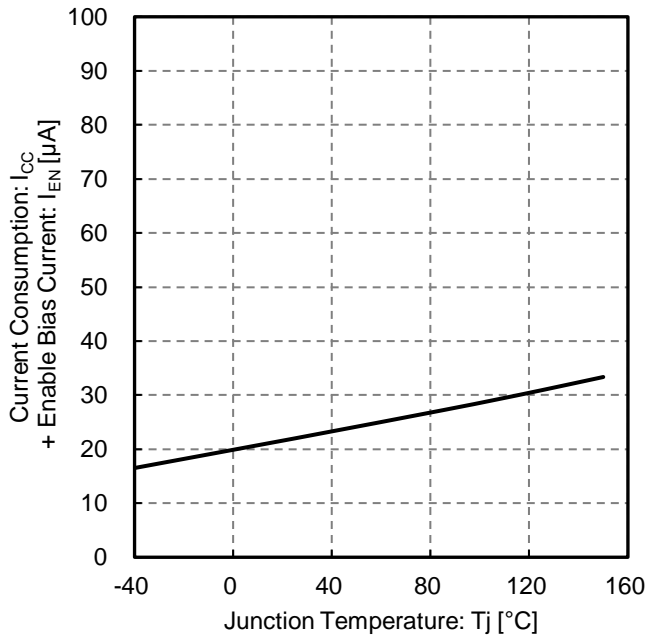


Figure 5.
Current Consumption + Enable Bias Current vs Junction Temperature

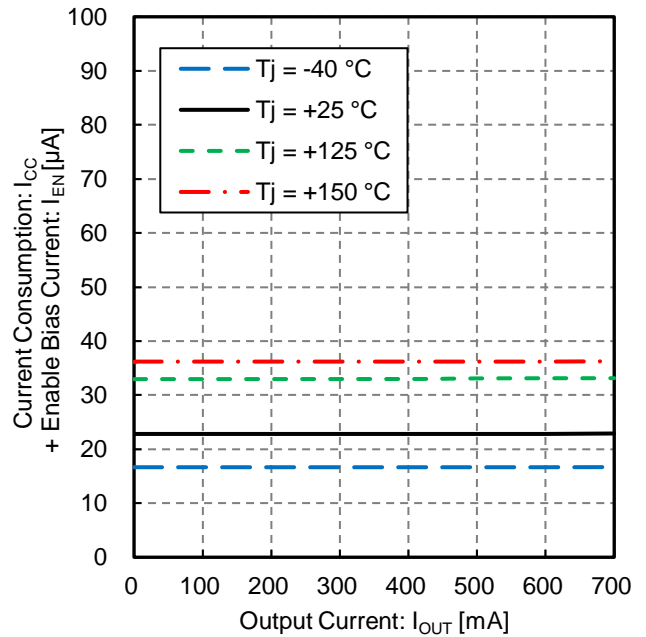


Figure 6.
Current Consumption + Enable Bias Current vs Output Current

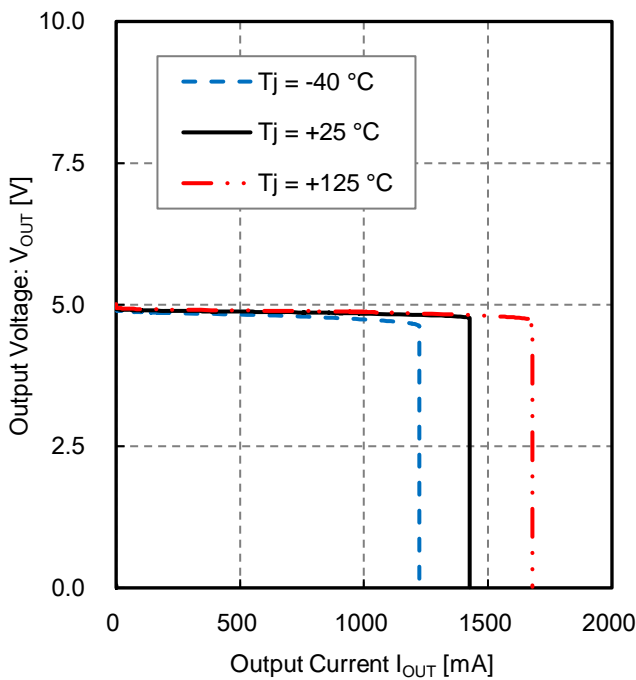


Figure 7.
Output Voltage vs Output Current (Over Current Protection)

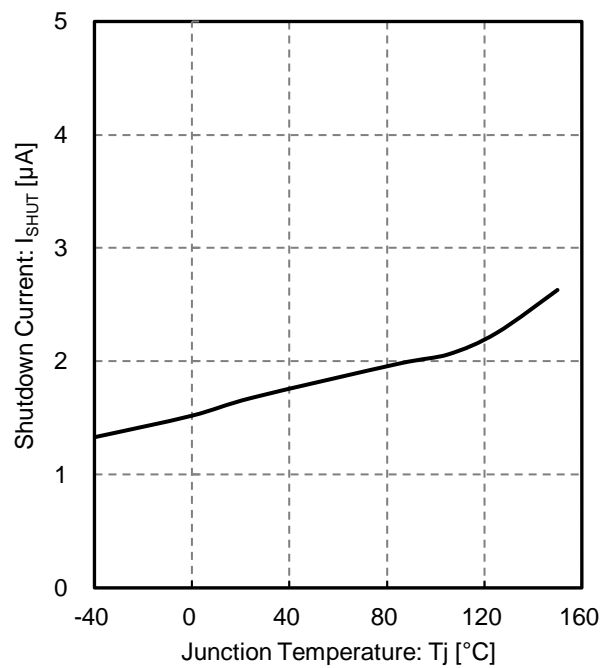


Figure 8.
Shutdown Current vs Junction Temperature ($V_{EN} = 0\text{ V}$)

Typical Performance Curves - continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V , $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$

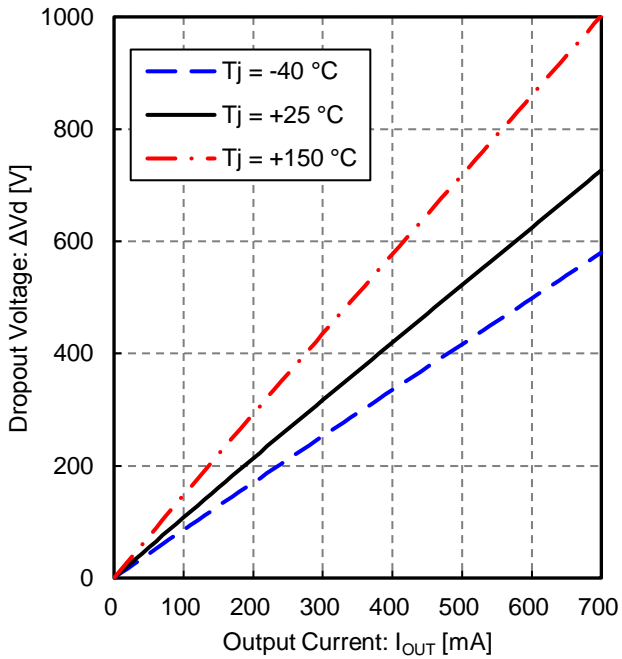


Figure 9.
Dropout Voltage vs Output Current
($V_{IN} = 4.75\text{ V}$)

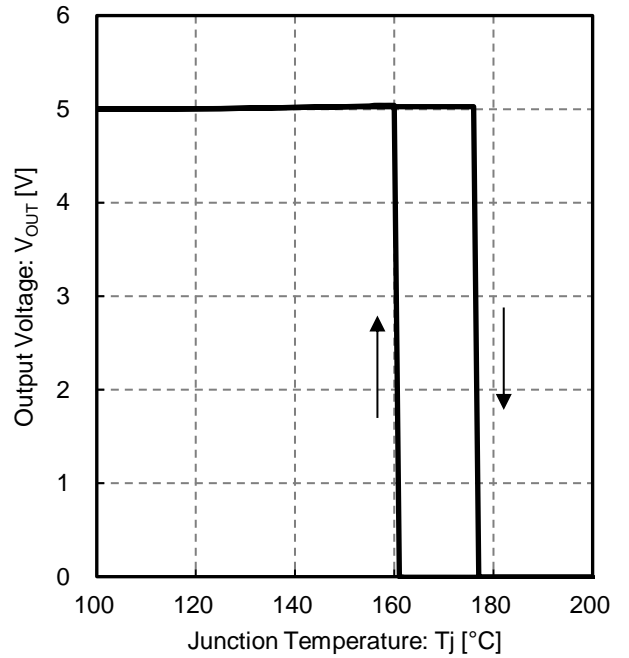


Figure 10.
Output Voltage vs Junction Temperature
(Thermal Shutdown Protection)

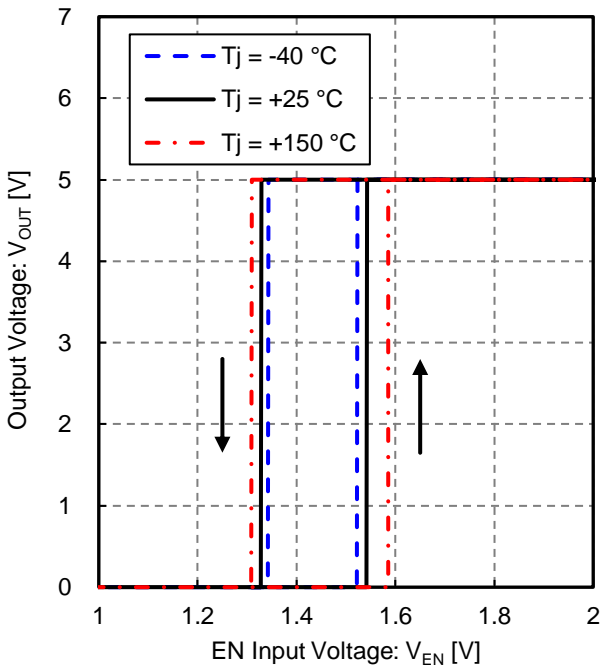


Figure 11.
Output Voltage vs EN Input Voltage

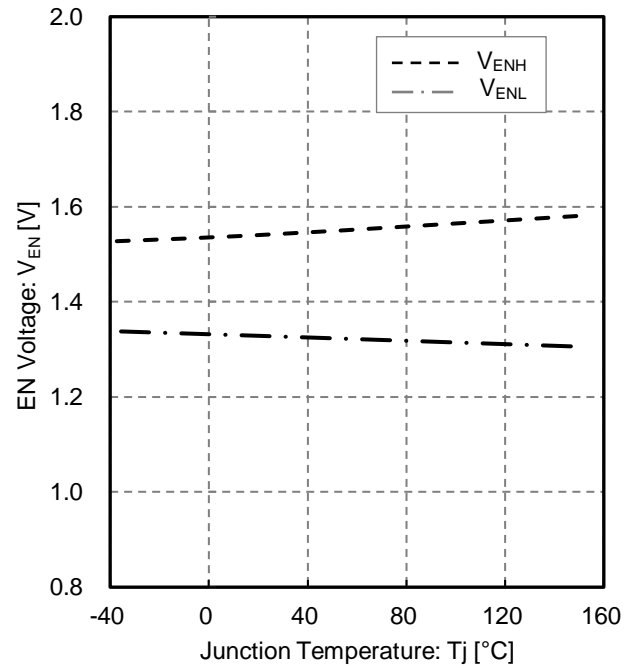


Figure 12.
EN Input Voltage vs Junction Temperature

Typical Performance Curves - continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V, $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$

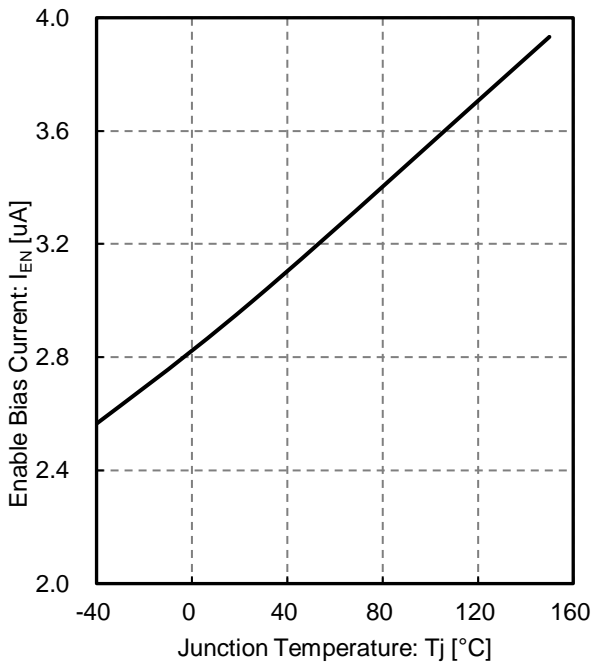


Figure 13.
Enable Bias Current vs Junction Temperature

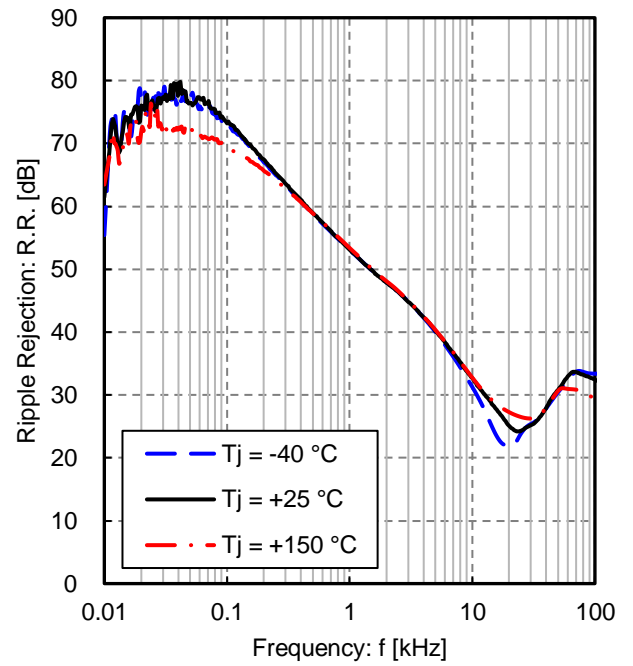


Figure 14.
Ripple Rejection
($e_{in} = 1\text{ V}_{rms}$, $I_{OUT} = 100\text{ mA}$)

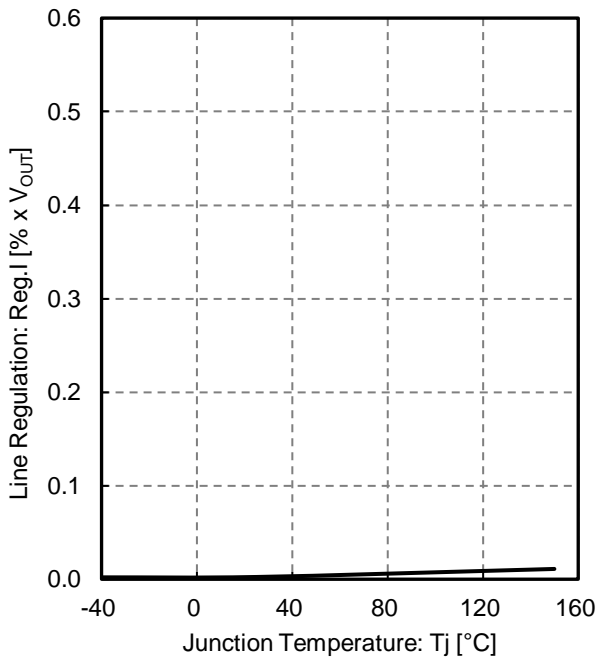


Figure 15.
Line Regulation
($V_{IN} = 6\text{ V} \rightarrow 28\text{ V}$)

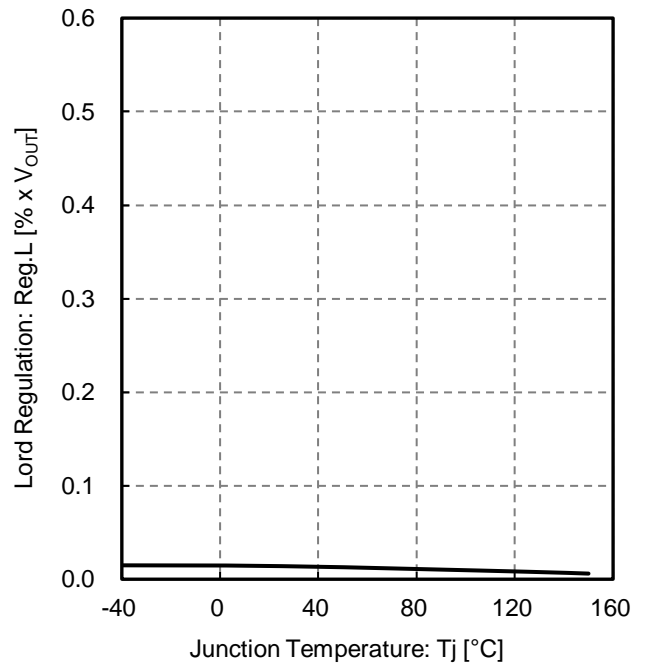


Figure 16.
Load Regulation
($I_{OUT} = 0.5\text{ mA} \rightarrow 400\text{ mA}$)

Typical Performance Curves - continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V, $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$, $T_j = +25\text{ }^\circ\text{C}$

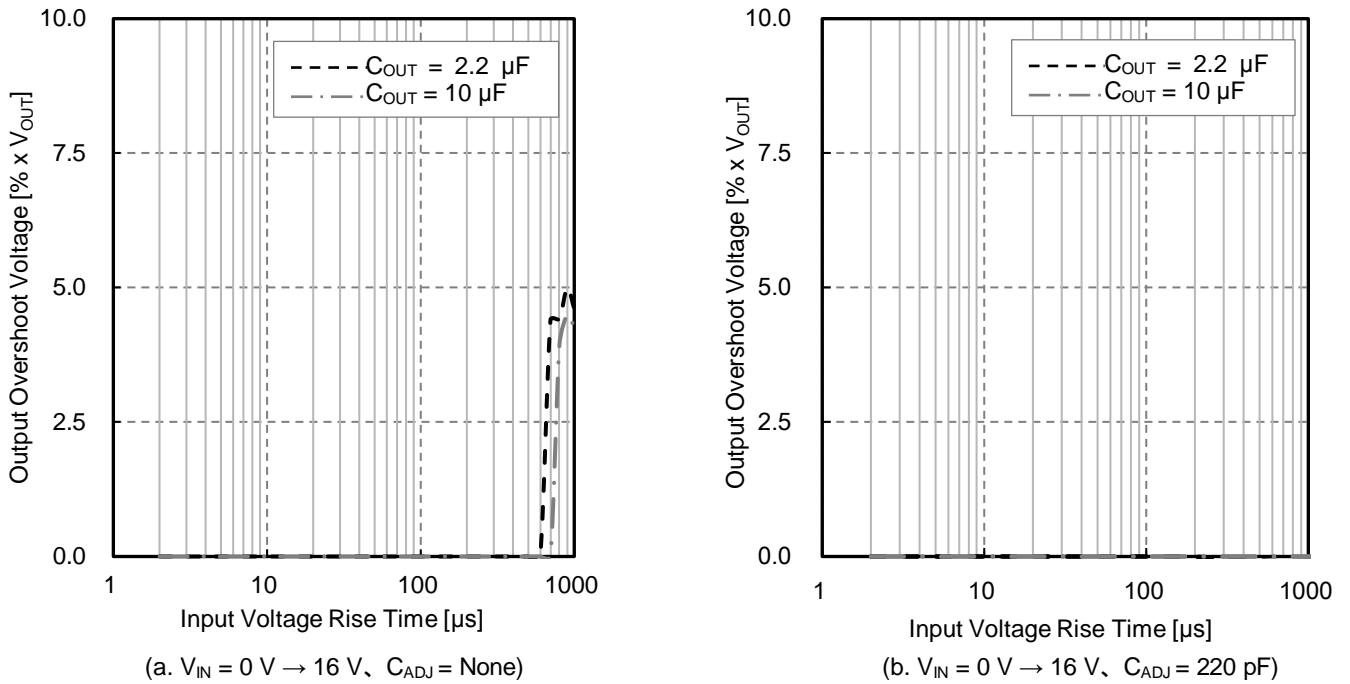


Figure 17. Line Transient Response ($V_{IN} = 0\text{ V} \rightarrow 16\text{ V}$)

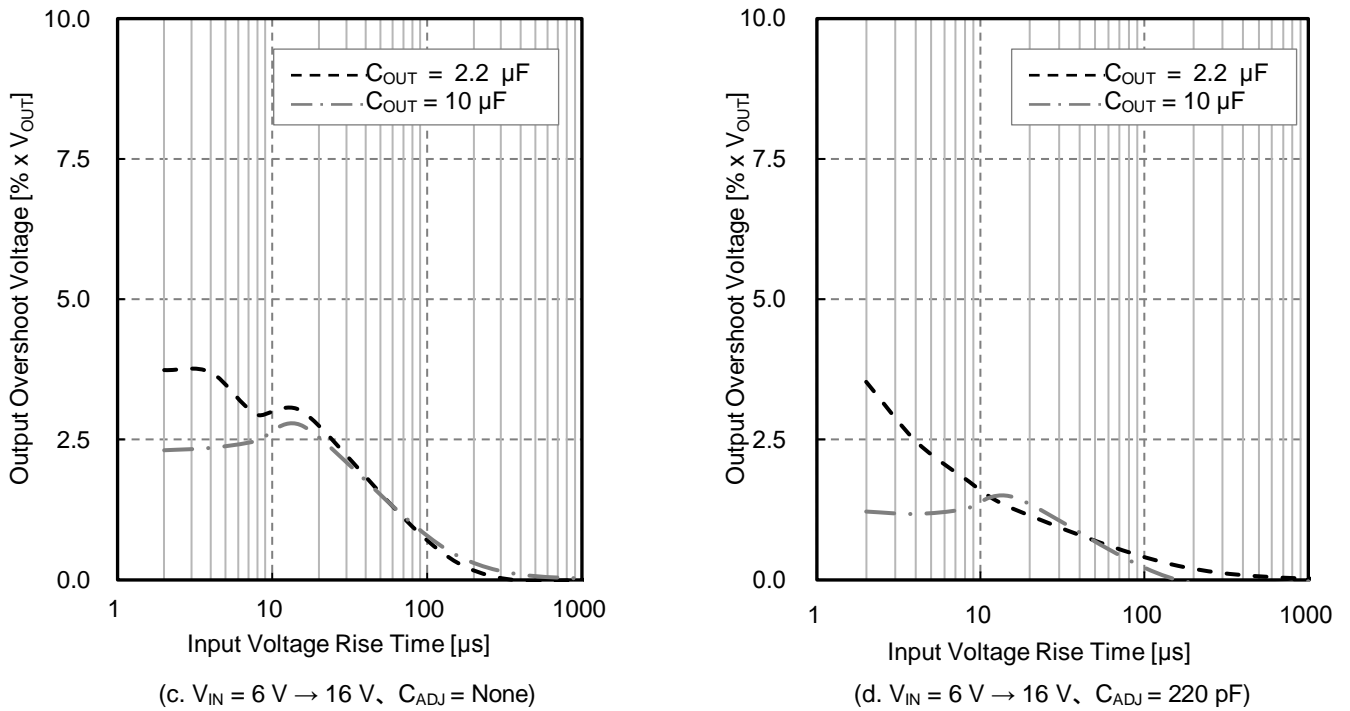
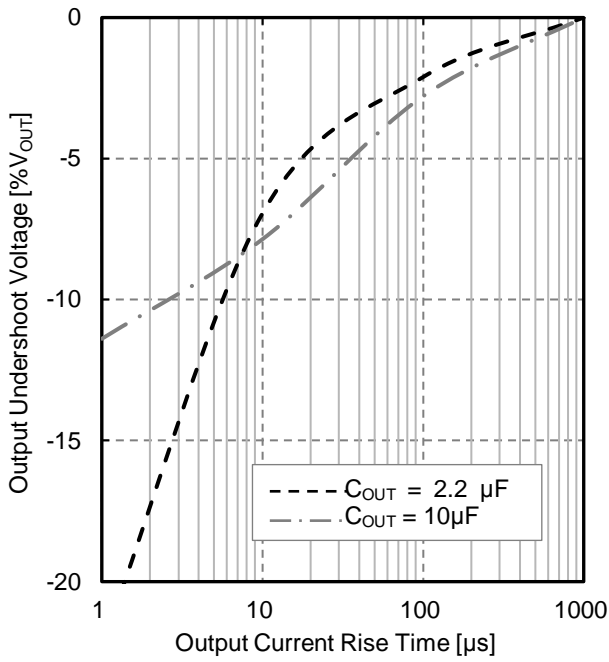


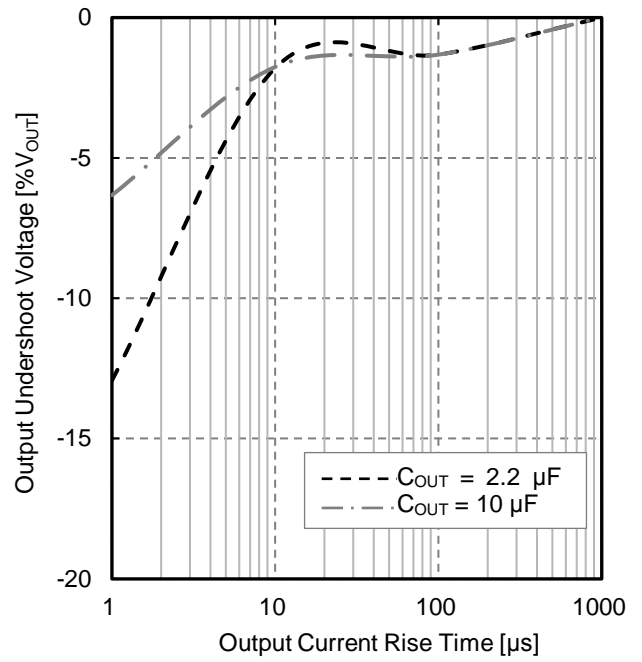
Figure 18. Line Transient Response ($V_{IN} = 6\text{ V} \rightarrow 16\text{ V}$)

Typical Performance Curves - continued

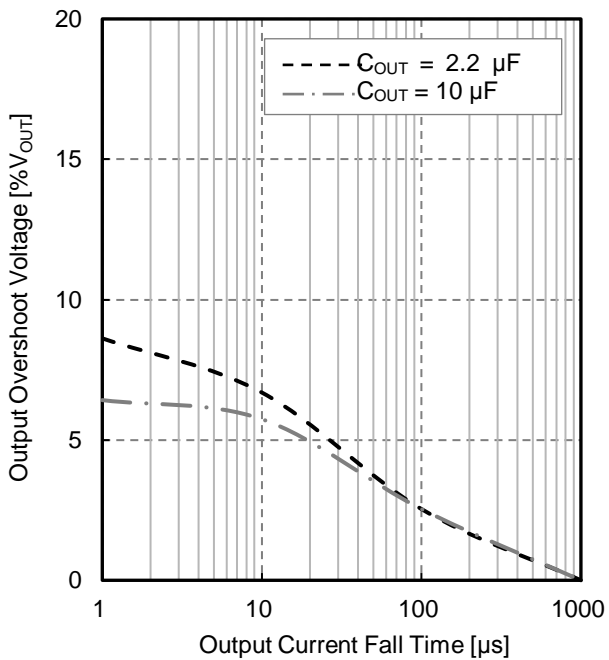
Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V, $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$ $T_j = +25\text{ }^\circ\text{C}$



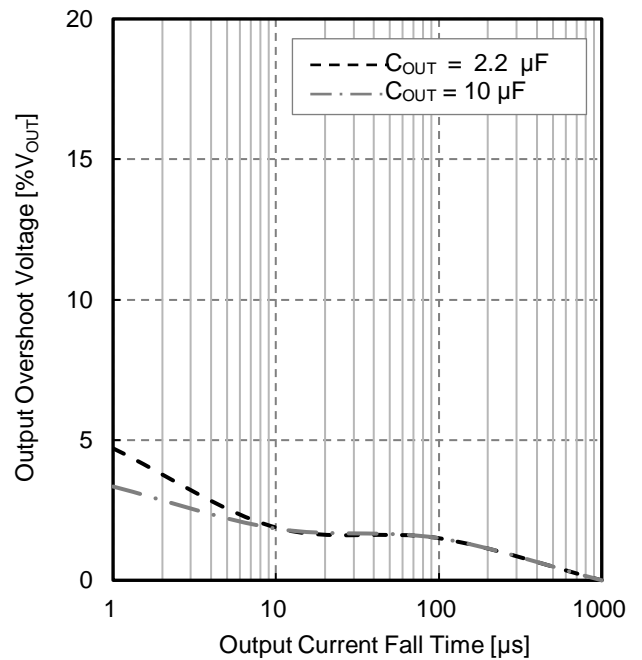
(a. $I_{OUT} = 1\text{ mA} \rightarrow 700\text{ mA}$, $C_{ADJ} = \text{None}$)



(b. $I_{OUT} = 1\text{ mA} \rightarrow 700\text{ mA}$, $C_{ADJ} = 220\text{ pF}$)



(c. $I_{OUT} = 700\text{ mA} \rightarrow 1\text{ mA}$, $C_{ADJ} = \text{None}$)

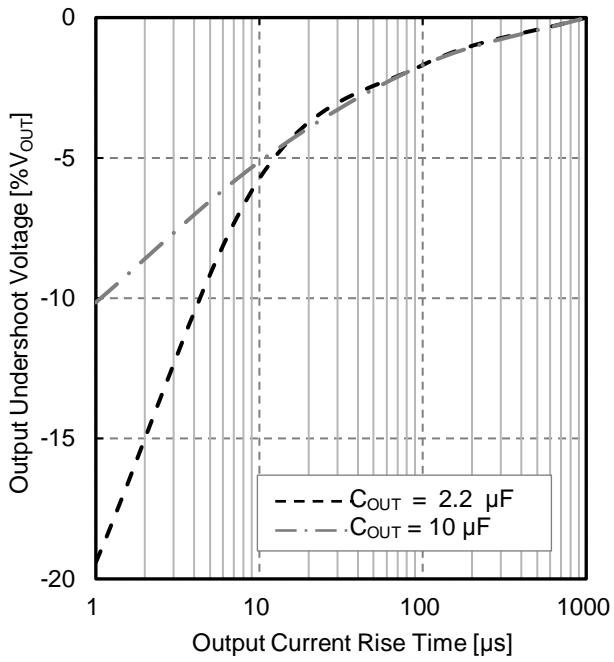


(d. $I_{OUT} = 700\text{ mA} \rightarrow 1\text{ mA}$, $C_{ADJ} = 220\text{ pF}$)

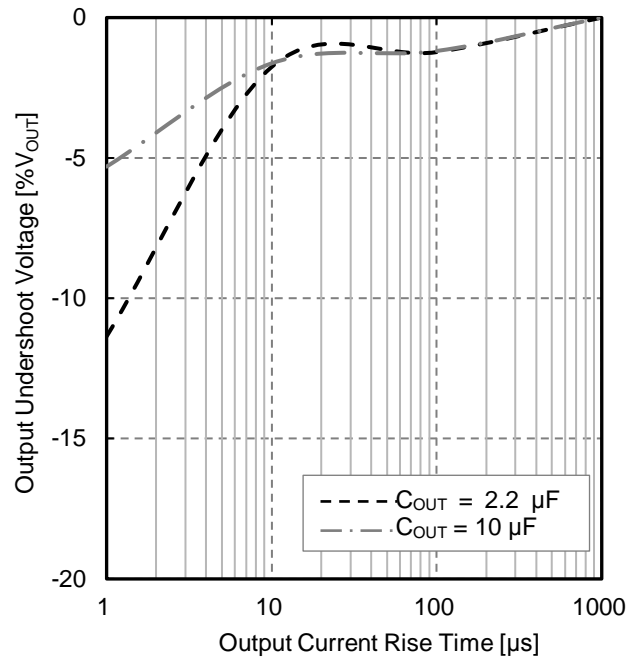
Figure 19. Load Transient Response
($I_{OUT} = 1\text{ mA} \leftrightarrow 700\text{ mA}$)

Typical Performance Curves - continued

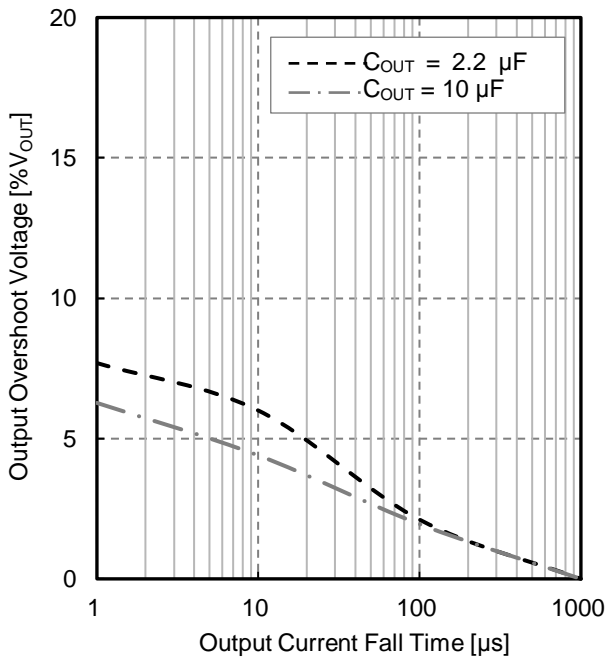
Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V , $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$ $T_j = +25\text{ }^\circ\text{C}$



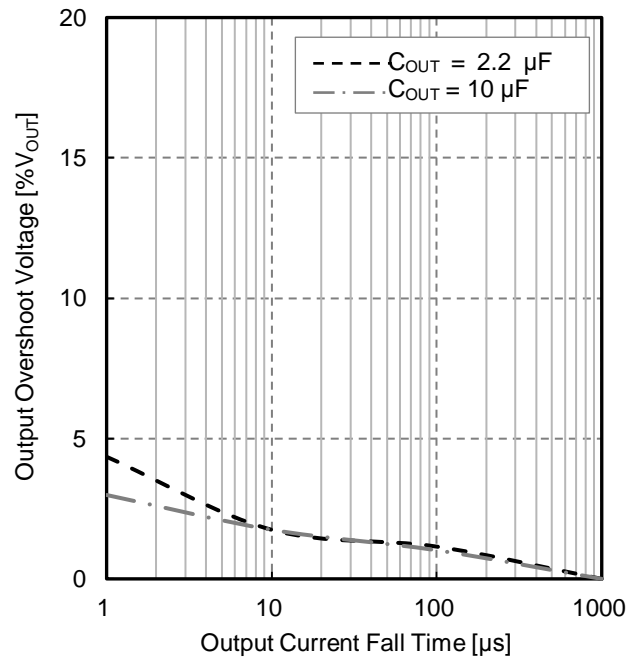
(e. $I_{OUT} = 10\text{ mA} \rightarrow 700\text{ mA}$, $C_{ADJ} = \text{None}$)



(f. $I_{OUT} = 10\text{ mA} \rightarrow 700\text{ mA}$, $C_{ADJ} = 220\text{ pF}$)



(g. $I_{OUT} = 700\text{ mA} \rightarrow 10\text{ mA}$, $C_{ADJ} = \text{None}$)

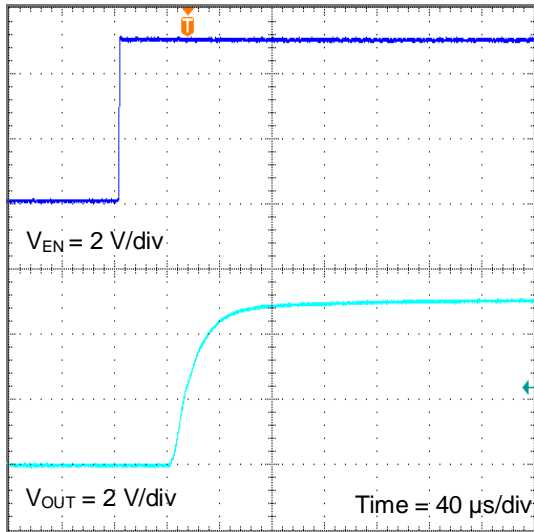


(h. $I_{OUT} = 700\text{ mA} \rightarrow 10\text{ mA}$, $C_{ADJ} = 220\text{ pF}$)

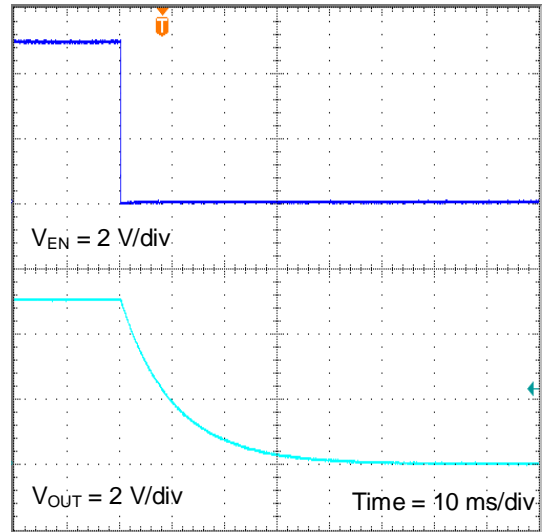
Figure 20. Load Transient Response ($I_{OUT} = 10\text{ mA} \leftrightarrow 700\text{ mA}$)

Typical Performance Curves - continued

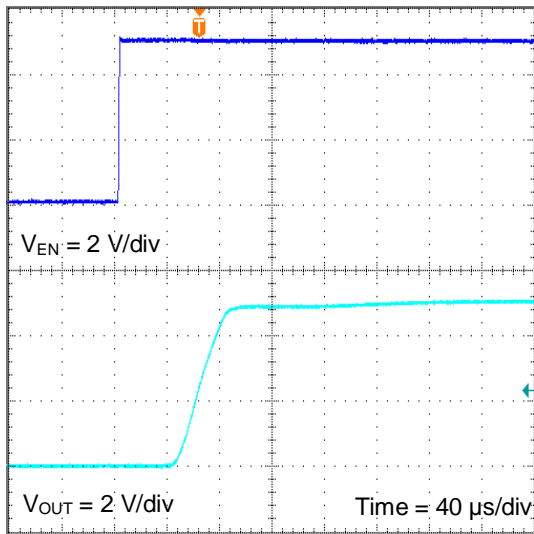
Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V, $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$, $I_{OUT} = 0\text{ mA}$, $T_J = +25\text{ }^\circ\text{C}$



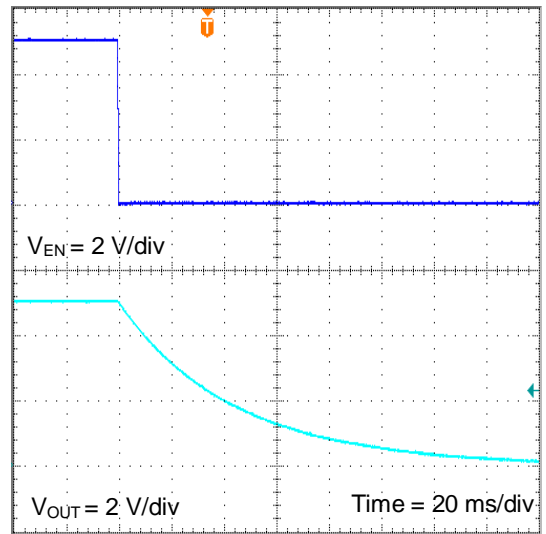
(a. $V_{EN} = 0\text{ V} \rightarrow 5\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$)



(b. $V_{EN} = 5\text{ V} \rightarrow 0\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$)



(c. $V_{EN} = 0\text{ V} \rightarrow 5\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$)

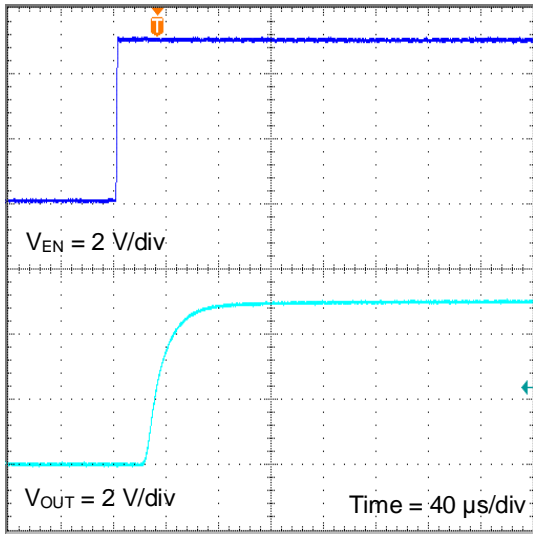


(d. $V_{EN} = 5\text{ V} \rightarrow 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$)

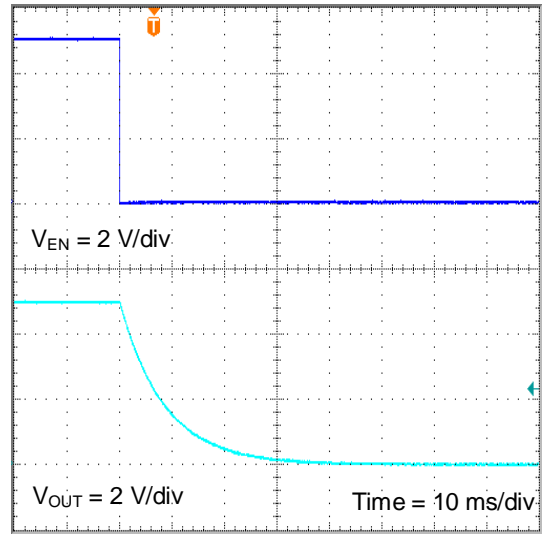
Figure 21. EN ON/OFF Sequence
($V_{EN} = 0\text{ V} \leftrightarrow 5\text{ V}$, $T_J = +25\text{ }^\circ\text{C}$)

Typical Performance Curves - continued

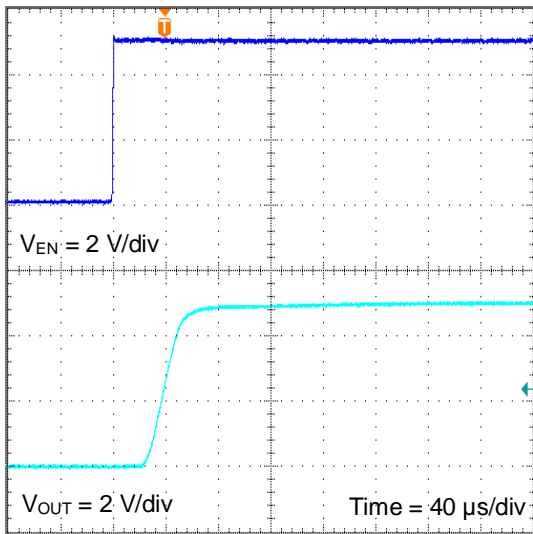
Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V, $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$, $I_{OUT} = 0\text{ mA}$, $T_J = +150\text{ }^\circ\text{C}$



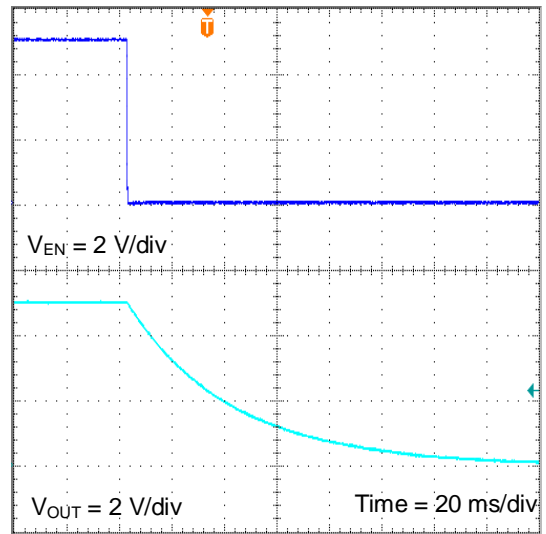
(e. $V_{EN} = 0\text{ V} \rightarrow 5\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$)



(f. $V_{EN} = 5\text{ V} \rightarrow 0\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$)



(g. $V_{EN} = 0\text{ V} \rightarrow 5\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$)

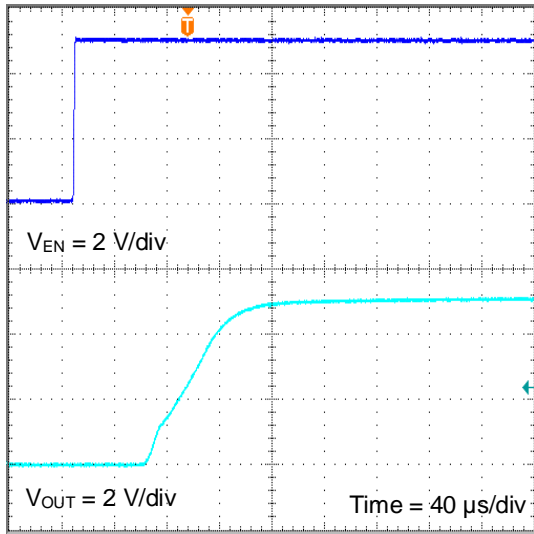


(h. $V_{EN} = 5\text{ V} \rightarrow 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$)

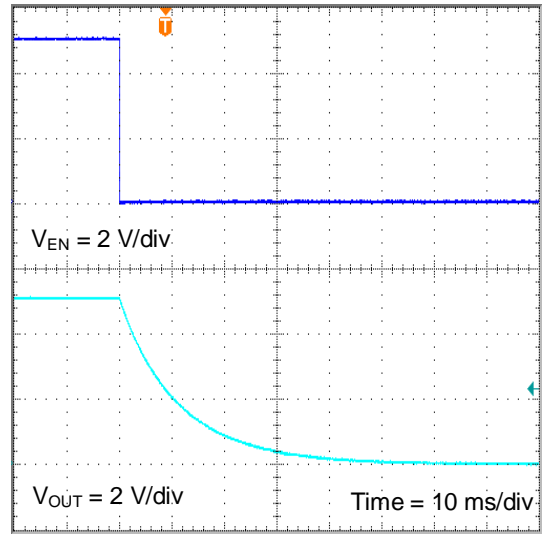
Figure 22. EN ON/OFF Sequence
($V_{EN} = 0\text{ V} \leftrightarrow 5\text{ V}$, $T_J = +150\text{ }^\circ\text{C}$)

Typical Performance Curves - continued

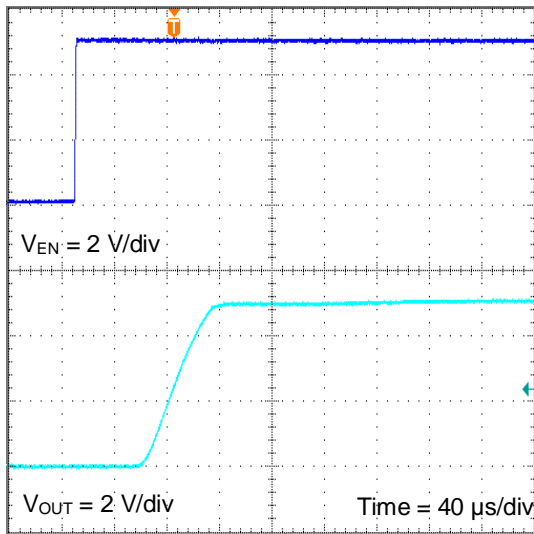
Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V, $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$, $I_{OUT} = 0\text{ mA}$, $T_J = -40\text{ }^\circ\text{C}$



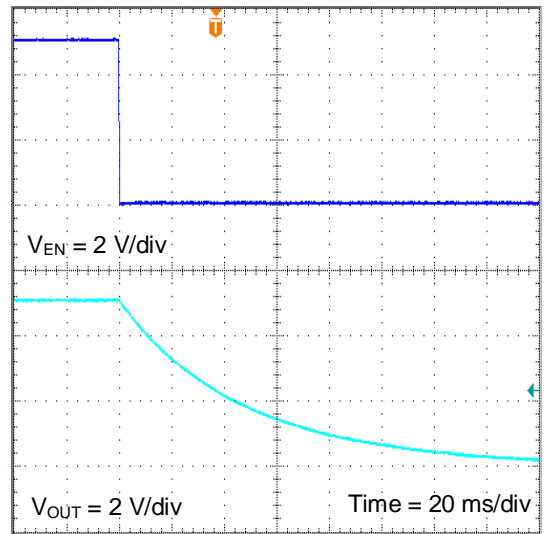
(i. $V_{EN} = 0\text{ V} \rightarrow 5\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$)



(j. $V_{EN} = 5\text{ V} \rightarrow 0\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$)



(k. $V_{EN} = 0\text{ V} \rightarrow 5\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$)



(l. $V_{EN} = 5\text{ V} \rightarrow 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$)

Figure 23. EN ON/OFF Sequence
($V_{EN} = 0\text{ V} \leftrightarrow 5\text{ V}$, $T_J = -40\text{ }^\circ\text{C}$)

Typical Performance Curves - continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V, $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$, $I_{OUT} = 0\text{ mA}$, $T_j = +25\text{ }^\circ\text{C}$

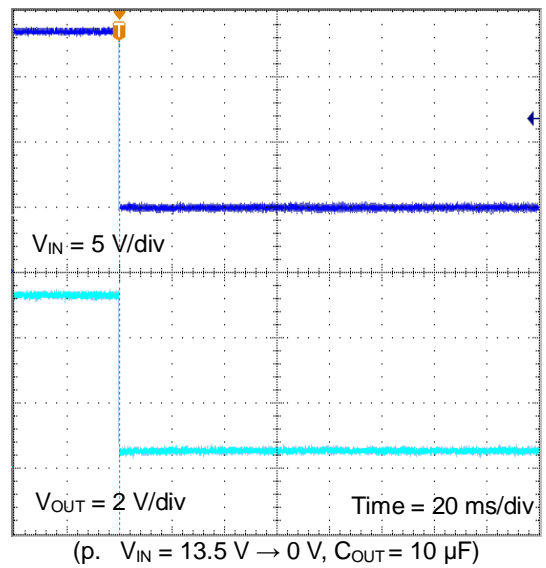
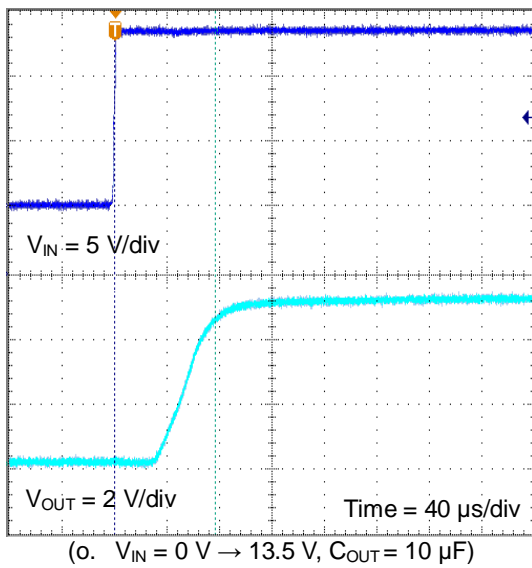
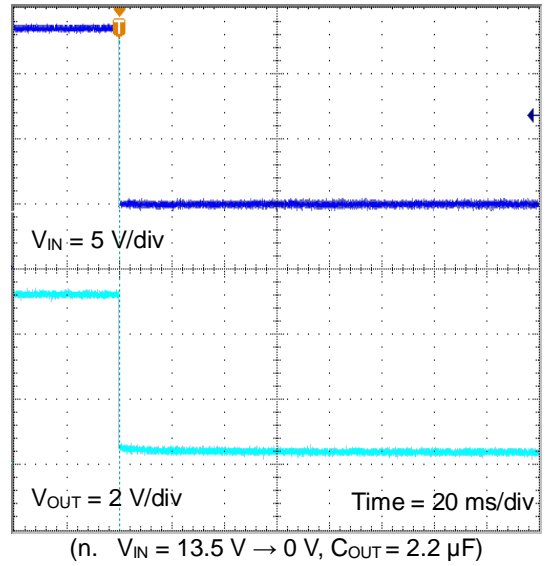
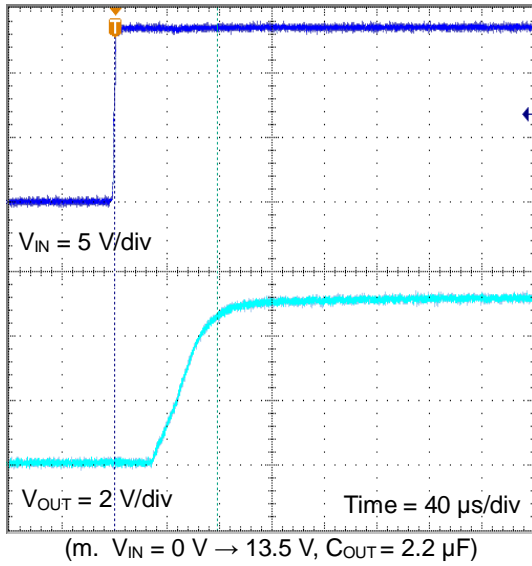


Figure 24. V_{IN} ON/OFF Sequence
 $(V_{IN} = 0\text{ V} \leftrightarrow 13.5\text{ V}, T_j = +25\text{ }^\circ\text{C})$

Typical Performance Curves - continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V, $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$, $I_{OUT} = 0\text{ mA}$, $T_J = +150\text{ }^\circ\text{C}$

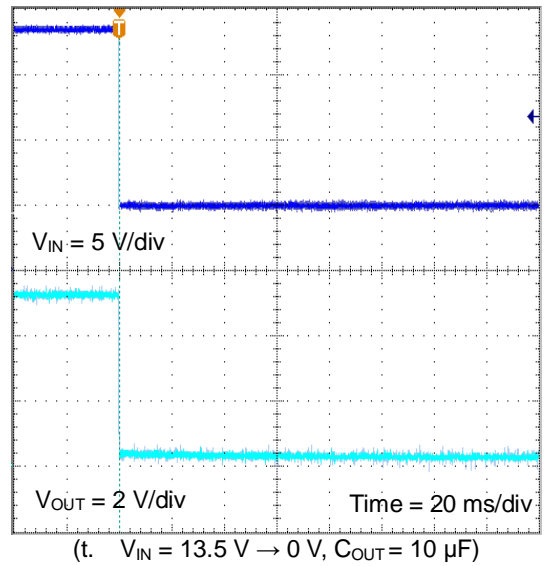
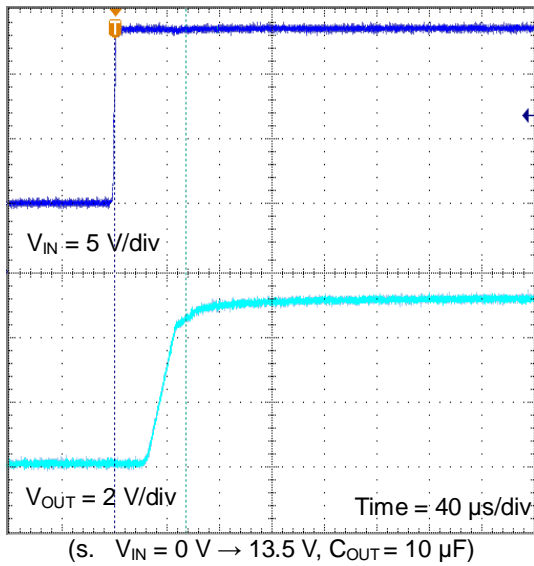
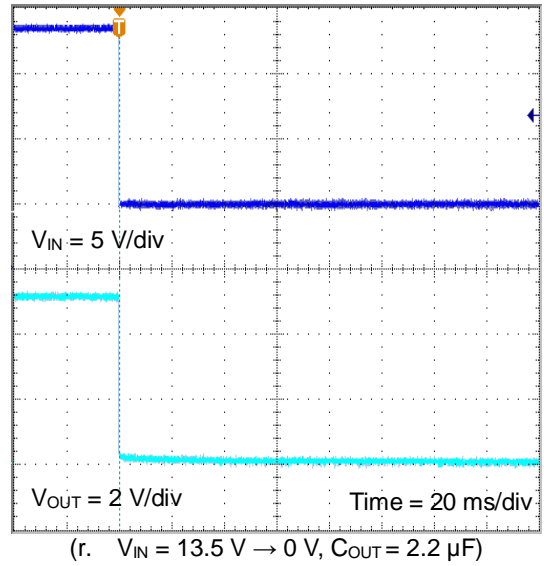
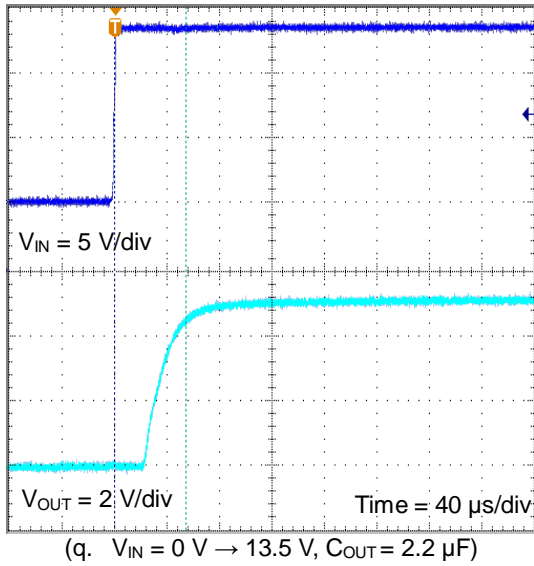


Figure 25. V_{IN} ON/OFF Sequence
($V_{IN} = 0\text{ V} \leftrightarrow 13.5\text{ V}$, $T_J = +150\text{ }^\circ\text{C}$)

Typical Performance Curves - continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, V_{OUT} setting = 5 V, $V_{EN} = 5\text{ V}$, $R_1 = 120\text{ k}\Omega$, $R_2 = 803\text{ k}\Omega$, $I_{OUT} = 0\text{ mA}$, $T_j = -40\text{ }^\circ\text{C}$

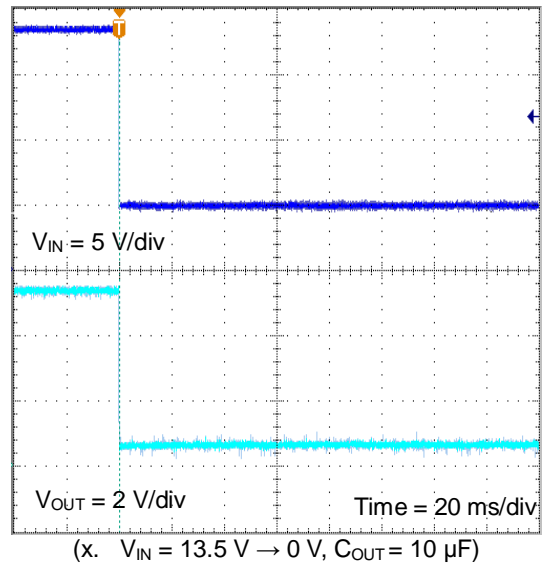
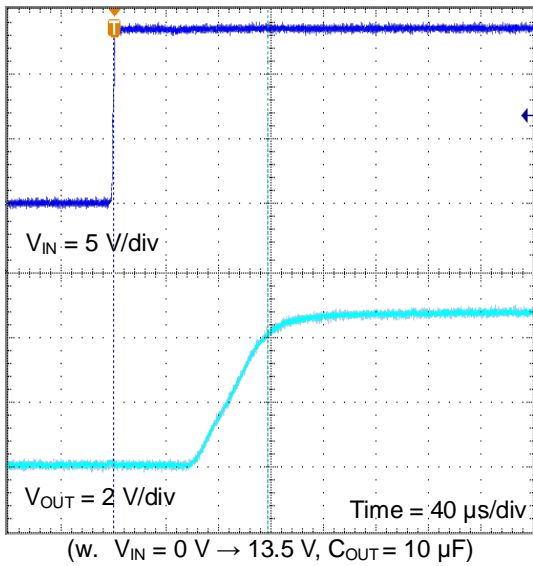
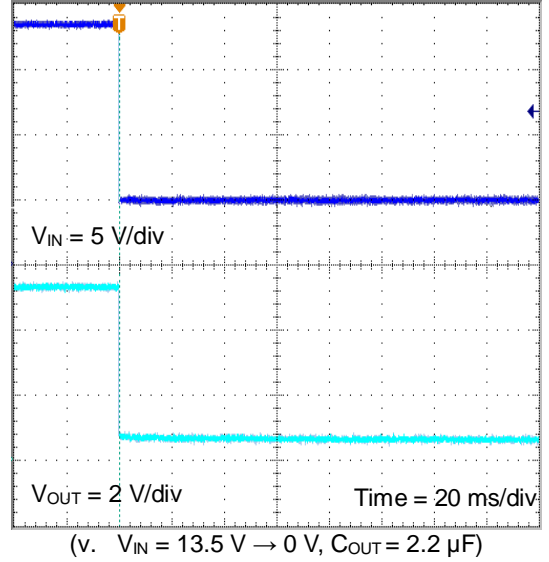
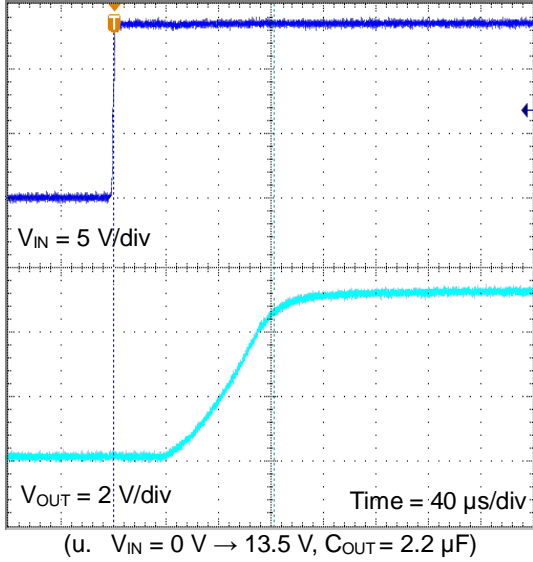
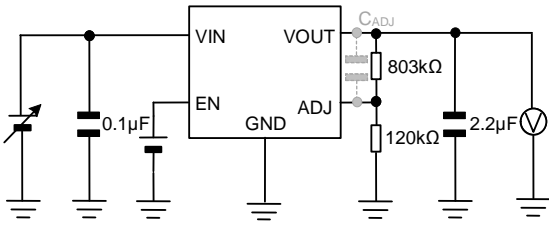
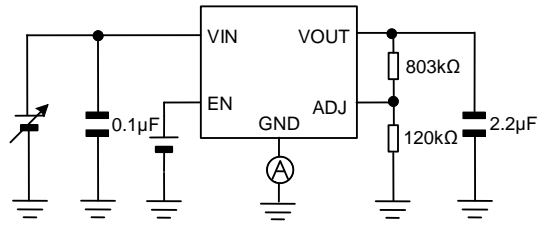


Figure 26. V_{IN} ON/OFF Sequence
 ($V_{IN} = 0\text{ V} \leftrightarrow 13.5\text{ V}$, $T_j = -40\text{ }^\circ\text{C}$)

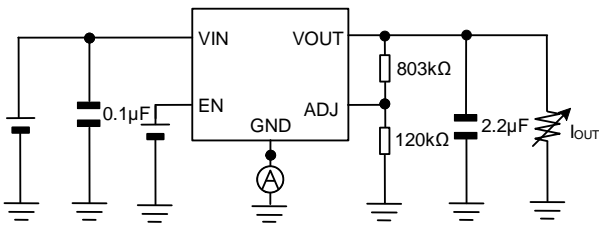
Measurement Circuit for Typical Performance Curves



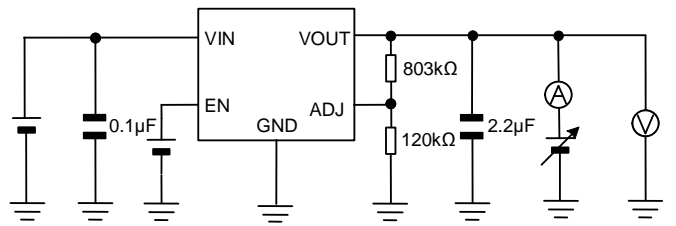
Measurement Setup for Figure 1, 2, 3, 10, 15, 17, 18



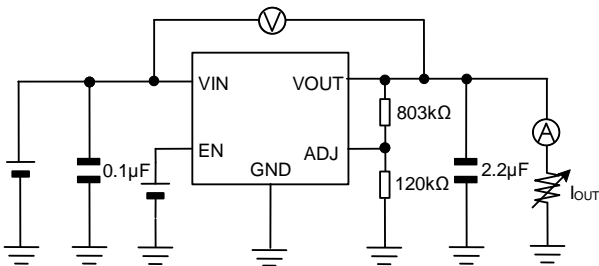
Measurement Setup for Figure 4, 5, 8, 24, 25, 26



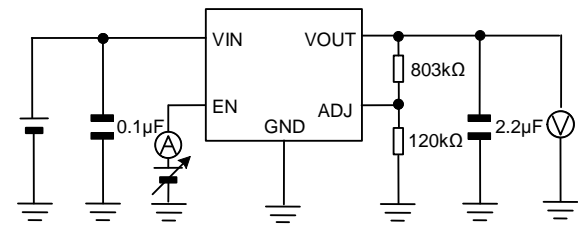
Measurement Setup for Figure 6



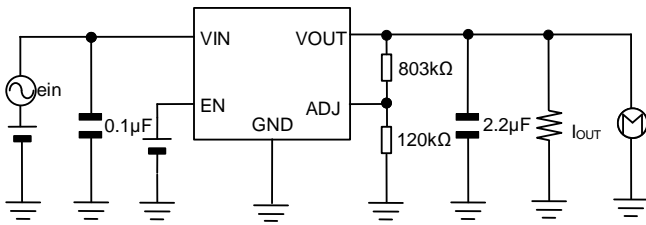
Measurement Setup for Figure 7



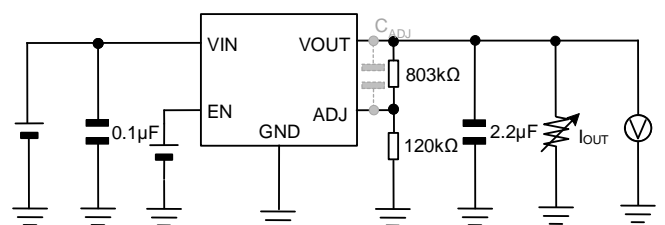
Measurement Setup for Figure 9



Measurement Setup for Figure 11, 12, 13, 21, 22, 23



Measurement Setup for Figure 14



Measurement Setup for Figure 16, 19, 20

Application and Implementation

Notice: The following information is given as a reference or hint for the application and the implementation. Therefore, it does not guarantee its operation on the specific function, accuracy or external components in the application. In the application, it shall be designed with sufficient margin by enough understanding about characteristics of the external components, e.g. capacitor, and also by appropriate verification in the actual operating conditions.

Selection of External Components

Input Pin Capacitor

If the battery is placed far from the regulator or the impedance of the input-side is high, higher capacitance is required for the input capacitor in order to prevent the voltage-drop at the input line. The input capacitor and its capacitance should be selected depending on the line impedance which is between the input pin and the smoothing filter circuit of the power supply. At this time, the capacitance value setting is different each application. Generally, the capacitor with capacitance value of 0.1 μF (Min) with good high frequency characteristic is recommended for this regulator.

Moreover, when inserting filter as ISO7637 countermeasure, insertion of ceramic capacitor from 10 nF to 470 nF (for pulses 2a) and ceramic capacitor from 100 nF to 470 nF (for pulses 3a/b) between input pin and GND pin are effective.

In addition, the consideration should be taken as the output pin capacitor, to prevent an influence to the regulator's characteristic from the deviation or the variation of the external capacitor's characteristic. All output capacitors mentioned above are recommended to have a good DC bias characteristic and a temperature characteristic (approximately $\pm 15\%$, e.g. X7R, X8R) with being satisfied high absolute maximum voltage rating based on EIA standard. These capacitors should be placed close to the input pin and mounted on the same board side of the regulator not to be influenced by implement impedance.

Output Pin Capacitor

The output capacitor is mandatory for the regulator in order to realize stable operation. The output capacitor with capacitance value $\geq 1.47 \mu\text{F}$ (Min) and ESR up to 5 Ω (Max) must be required between the output pin and the GND pin. A proper selection of appropriate both the capacitance value and ESR for the output capacitor can improve the transient behavior of the regulator and can also keep the stability with better regulation loop. The correlation of the output capacitance value and ESR is shown in the graph on the next page as the output capacitor's capacitance value and the stability region for ESR. As described in this graph, this regulator is designed to be stable with ceramic capacitors as of MLCC, with the capacitance value from 1.47 μF to 1000 μF and with ESR value within almost 0 Ω to 5 Ω . The frequency range of ESR can be generally considered as within about 10 kHz to 100 kHz.

Note that the provided the stable area of the capacitance value and ESR in the graph is obtained under a specific set of conditions which is based on the measurement result in single IC on our board with a resistive load. In the actual environment, the stability is affected by wire impedance on the board, input power supply impedance and also loads impedance. Therefore, please note that a careful evaluation of the actual application, the actual usage environment and the actual conditions should be done to confirm the actual stability of the system.

Generally, in the transient event which is caused by the input voltage fluctuation or the load fluctuation beyond the gain bandwidth of the regulation loop, the transient response ability of the regulator depends on the capacitance value of the output capacitor. Basically the capacitance value of $\geq 1.47 \mu\text{F}$ (Min) for the output capacitor is recommended as shown in the table on [Output Capacitance C_{OUT}, ESR Available Area](#). Using bigger capacitance value can be expected to improve better the transient response ability in a high frequency. Various types of capacitors can be used for the output capacitor with high capacity which includes electrolytic capacitor, electro-conductive polymer capacitor and tantalum capacitor. Noted that, depending on the type of capacitors, its characteristics such as ESR ($\leq 5 \Omega$) absolute value range, a temperature dependency of capacitance value and increased ESR at cold temperature needs to be taken into consideration.

In addition, the same consideration should be taken as the input pin capacitor, to prevent an influence to the regulator's characteristic from the deviation or the variation of the external capacitor's characteristic. All output capacitors mentioned above are recommended to have a good DC bias characteristic and a temperature characteristic (approximately $\pm 15\%$, e.g. X7R, X8R) with being satisfied high absolute maximum voltage rating based on EIA standard. These capacitors should be placed close to the output pin and mounted on the same board side of the regulator not to be influenced by implement impedance.

Application and Implementation - continued

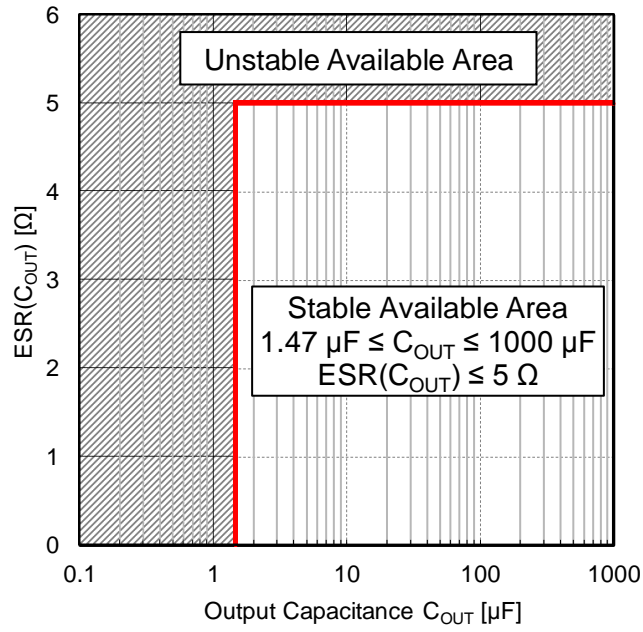


Figure 27. Output Capacitance C_{OUT}, ESR Stable Available Area
 (-40 °C ≤ T_j ≤ +150 °C, 6 V ≤ V_{IN} ≤ 42 V, V_{EN} = 5 V, I_{OUT} = 0 mA to 700 mA)

Application and Implementation – continued

Typical Application and Layout Example

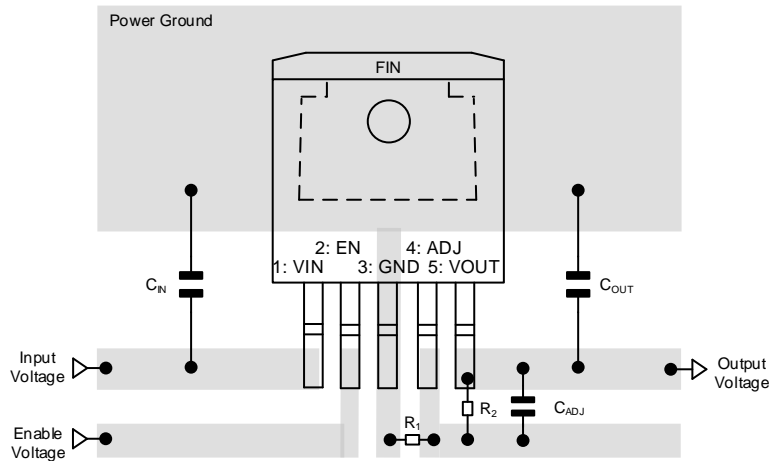


Figure 28. Typical Application and Layout Example

Parameter	Symbol	Reference Value for Application
Output Current Range	I_{OUT}	$I_{OUT} \leq 700 \text{ mA}$
Output Voltage Range	V_{OUT}	1.2 V to 16 V
Feedback Resistor between the ADJ and GND pins	R_1	120 k Ω
Feedback Resistor between the ADJ and VOUT pins	R_2	Calc. (a) $R_2 = R_1 \times (V_{OUT} / V_{ADJ} - 1) = 803 \text{ k}\Omega$ 5 V setting
ADJ Capacitor <i>(Note 1)</i>	C_{ADJ}	Calc. (b) $C_{ADJ} = 1 / (2\pi \times R_2 \times f_{ZERO}) = 220 \text{ pF}$
Output Capacitor	C_{OUT}	4.7 μF
Input Voltage <i>(Note 2)</i>	V_{IN}	13.5 V
Input Capacitor <i>(Note 3)</i>	C_{IN}	0.1 μF
Enable Mode Voltage	V_{ENH}	2 V to V_{IN}
Disable Mode Voltage	V_{ENL}	0 V to 0.8 V

(Note 1) For example, the C_{ADJ} 's value is defined at 220 pF based on the calculation (b) of the above table, if it is required to improve frequency characteristics of regulator at around $f_{ZERO} \cong 1 \text{ kHz}$ with the component of $R_2 \cong 820 \text{ k}\Omega$.

(Note 2) Minimum input voltage must be 3.3 V or more. For the output voltage, please consider the voltage dropping (the minimum dropout voltage) according to the output current.

(Note 3) If the inductance of power supply line is high, please adjust input capacitor value.

Application and Implementation - continued

Surge Voltage Protection for Linear Regulators

The following shows some helpful tips to protect ICs from possible inputting surge voltage which exceeds absolute maximum ratings.

Positive Surge to the Input

If there is any potential risk that positive surges higher than absolute maximum ratings, it is applied to the input, a Zener Diode should be inserted between the VIN pin and the GND to protect the device as shown in Figure 29.

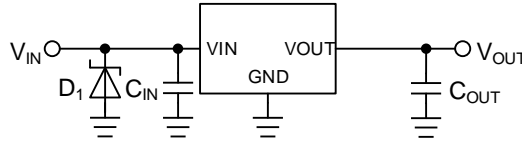


Figure 29. Surges Higher than absolute maximum ratings is Applied to the Input

Negative Surge to the Input

If there is any potential risk that negative surges below the absolute maximum ratings, (e.g.) -0.3 V, is applied to the input, a Schottky Diode should be inserted between the VIN and the GND to protect the device as shown in Figure 30.

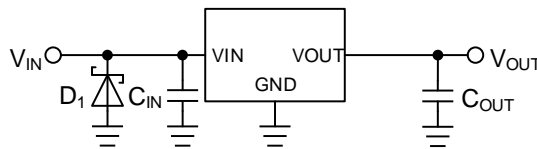


Figure 30. Surges Lower than -0.3 V is Applied to the Input

Reverse Voltage Protection for Linear Regulators

A linear regulator which is one of the integrated circuit (IC) operates normally in the condition that the input voltage is higher than the output voltage. However, it is possible to happen the abnormal situation in specific conditions which is the output voltage becomes higher than the input voltage. A reverse polarity connection between the input and the output might be occurred or a certain inductor component can also cause a polarity reverse conditions. If the countermeasure is not implemented, it may cause damage to the IC. The following shows some helpful tips to protect ICs from the reverse voltage occasion.

Protection against Reverse Input/Output Voltage

In the case that MOSFET is used for the pass transistor, a parasitic body diode between the drain-source generally exists. If the output voltage becomes higher than the input voltage and if its voltage difference exceeds V_F of the body diode, a reverse current flows from the output to the input through the body diode as shown in Figure 31. The current flows in the parasitic body diode is not limited in the protection circuit because it is the parasitic element, therefore too much reverse current may cause damage to degrade or destroy the semiconductor elements of the regulator.

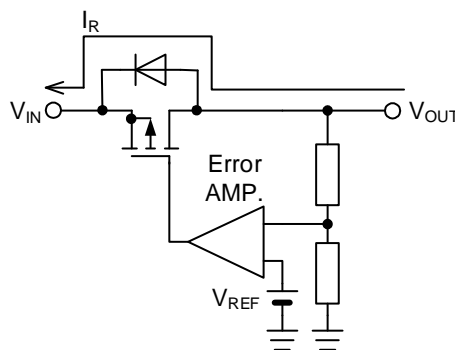


Figure 31. Reverse Current Path in a MOS Linear Regulator

Protection against Reverse Input/Output Voltage – continued

An effective solution for this problem is to implement an external bypass diode in order to prevent the reverse current flow inside the IC as shown in Figure 32. Note that the bypass diode must be turned on prior to the internal body diode of the IC. This external bypass diode should be chosen as being lower forward voltage V_F than the internal body diode. It should be selected a diode which has a rated reverse voltage greater than the IC's input maximum voltage and also which has a rated forward current greater than the anticipated reverse current in the actual application.

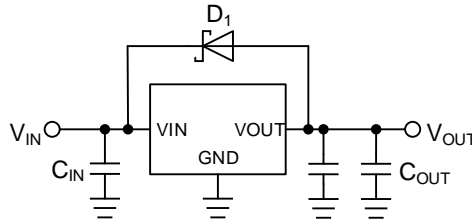


Figure 32. Bypass Diode for Reverse Current Diversion

A Schottky barrier diode which has a characteristic of low forward voltage (V_F) can meet to the requirement for the external diode to protect the IC from the reverse current. However, it also has a characteristic that the leakage (I_R) caused by the reverse voltage is bigger than other diodes. Therefore, it should be taken into the consideration to choose it because if I_R is large, it may cause increase of the current consumption, or raise of the output voltage in the light-load current condition. I_R characteristic of Schottky diode has positive temperature characteristic, which the details shall be checked with the datasheet of the products, and the careful confirmation of behavior in the actual application is mandatory.

Even in the condition when the input/output voltage is inverted, if the VIN pin is open as shown in Figure 33, or if the VIN pin becomes high-impedance condition as designed in the system, it cannot damage or degrade the parasitic element. It's because a reverse current via the pass transistor becomes extremely low. In this case, therefore, the protection external diode is not necessary.

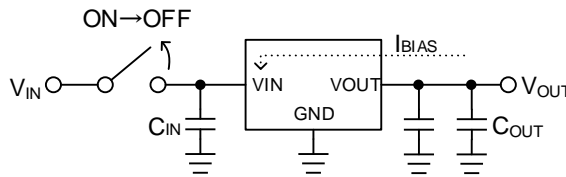


Figure 33. Open VIN

Protection against Input Reverse Voltage

When the input of the IC is connected to the power supply, accidentally if plus and minus are routed in reverse, or if there is a possibility that the input may become lower than the GND pin, it may cause to destroy the IC because a large current passes via the internal electrostatic breakdown prevention diode between the input pin and the GND pin inside the IC as shown in Figure 34.

The simplest solution to avoid this problem is to connect a Schottky barrier diode or a rectifier diode in series to the power supply line as shown in Figure 35. However, it increases a power loss calculated as $V_F \times I_{CC}$, and it also causes the voltage drop by a forward voltage V_F at the supply voltage while normal operation. Generally, since the Schottky barrier diode has lower V_F , so it contributes to rather smaller power loss than rectifier diodes. If IC has load currents, the required input current to the IC is also bigger. In this case, this external diode generates heat more, therefore select a diode with enough margin in power dissipation. On the other hand, a reverse current passes this diode in the reverse connection condition, however, it is negligible because its small amount.

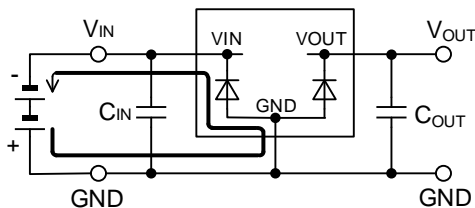


Figure 34. Current Path in Reverse Input Connection

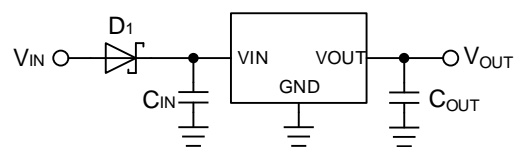


Figure 35. Protection against Reverse Polarity 1

Protection against Input Reverse Voltage - continued

Figure 36 shows a circuit in which a P-channel MOSFET is connected in series to the power. The body diode (parasitic element) is located in the drain-source junction area of the MOSFET. The drop voltage in a forward connection is calculated from the on state resistance of the MOSFET and the output current I_O . It is smaller than the drop voltage by the diode as shown in Figure 35 and results in less of a power loss. No current flows in a reverse connection where the MOSFET remains off in Figure 36.

If the gate-source voltage exceeds maximum rating of MOSFET gate-source junction with derating curve in consideration, reduce the gate-source junction voltage by connecting resistor voltage divider as shown in Figure 37.

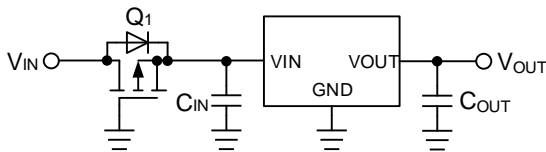


Figure 36. Protection against Reverse Polarity 2

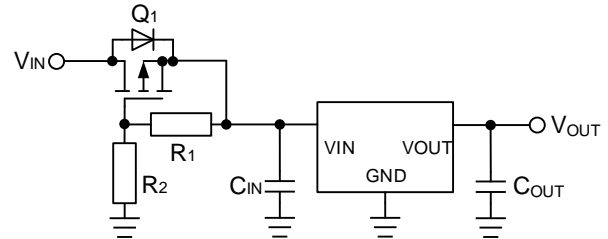


Figure 37. Protection against Reverse Polarity 3

Protection against Reverse Output Voltage when Output Connect to an Inductor

If the output load is inductive, electrical energy accumulated in the inductive load is released to the ground at the moment that the output voltage is turned off. IC integrates ESD protection diodes between the IC output and ground pins. A large current may flow in such condition finally resulting on destruction of the IC. To prevent this situation, connect a Schottky barrier diode in parallel to the integrated diodes as shown in Figure 38.

Further, if a long wire is in use for the connection between the output pin of the IC and the load, confirm that the negative voltage is not generated at the VOUT pin when the output voltage is turned off by observation of the waveform on an oscilloscope, since it is possible that the load becomes inductive. An additional diode is required for a motor load that is affected by its counter electromotive force, as it produces an electrical current in a similar way.

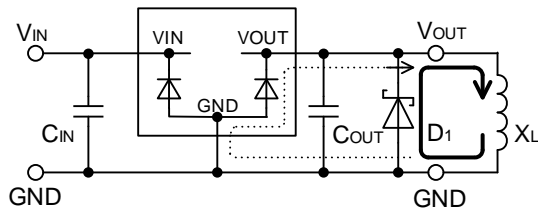


Figure 38. Current Path in Inductive Load (Output: Off)

Power Dissipation

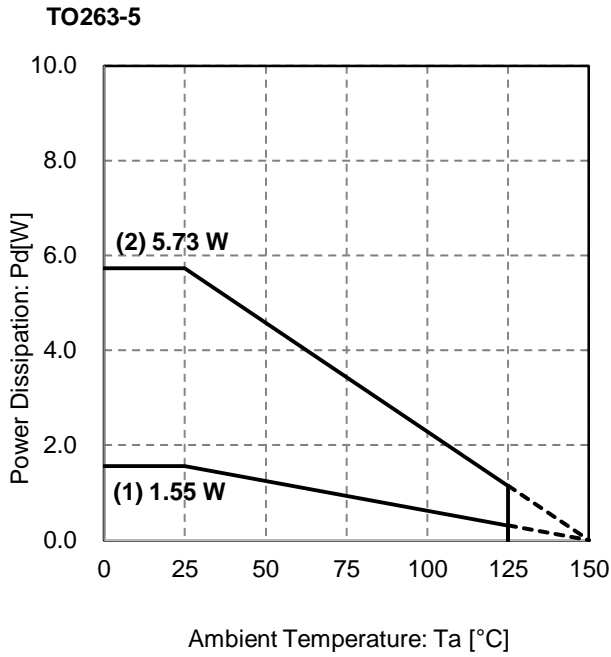


Figure 39. Power Dissipation Graph

(1) : 1-layer PCB
 (Copper foil area on the reverse side of PCB: 0 mm × 0 mm)
 Board material: FR-4
 Board size: 114.3 mm × 76.2 mm × 1.57 mm
 Top copper foil: Footprint and Trace, 70 μm copper.

(2) : 4-layer PCB
 (Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm)
 Board material: FR-4
 Board size: 114.3 mm × 76.2 mm × 1.6 mm
 Top copper foil: Footprint and Traces, 70 μm copper.
 2 inner layers copper foil area of PCB:
 74.2 mm × 74.2 mm, 35 μm copper.
 Bottom copper foil area of PCB:
 74.2 mm × 74.2 mm, 70 μm copper.

Condition (1) : $\theta_{JA} = 80.2 \text{ }^\circ\text{C/W}$, $\Psi_{JT} \text{ (top center)} = 10 \text{ }^\circ\text{C/W}$
 Condition (2) : $\theta_{JA} = 21.8 \text{ }^\circ\text{C/W}$, $\Psi_{JT} \text{ (top center)} = 2 \text{ }^\circ\text{C/W}$

Thermal Design

This product exposes a frame on the back side of the package for thermal efficiency improvement. The power consumption of the IC is decided by the dropout voltage condition, the load current and the current consumption. Refer to power dissipation curves illustrated in Figure 39 when using the IC in an environment of $T_a \geq 25^\circ\text{C}$. Even if the ambient temperature T_a is at 25°C , chip junction temperature (T_j) can be very high depending on the input voltage and the load current. Consider the design to be $T_j \leq T_{j\max} = 150^\circ\text{C}$ in whole operating temperature range.

Should by any condition the maximum junction temperature $T_{j\max} = 150^\circ\text{C}$ rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Therefore, need to be careful because it might be different from the actual use condition. Verify the application and allow sufficient margins in the thermal design by the following method to calculate the junction temperature T_j . T_j can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature T_j with ambient temperature T_a .

$$T_j = T_a + P_C \times \theta_{JA} \text{ [}^\circ\text{C]}]$$

Where:

- T_j is the Junction Temperature
- T_a is the Ambient Temperature
- P_C is the Power Consumption
- θ_{JA} is the Thermal Resistance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature T_j with top center of case's (mold) temperature T_T .

$$T_j = T_T + P_C \times \Psi_{JT} \text{ [}^\circ\text{C]}]$$

Where:

- T_j is the Junction Temperature
- T_T is the Top Center of Case's (mold) Temperature
- P_C is the Power consumption
- Ψ_{JT} is the Thermal Resistance (Junction to Top Center of Case)

3. The following method is used to calculate the power consumption P_C (W).

$$P_C = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC} \text{ [W]}$$

Where:

- P_C is the Power Consumption
- V_{IN} is the Input Voltage
- V_{OUT} is the Output Voltage
- I_{OUT} is the Load Current
- I_{CC} is the Current Consumption

Calculation Example

If $V_{IN} = 13.5\text{ V}$, $V_{OUT} = 5.0\text{ V}$, $I_{OUT} = 200\text{ mA}$, $I_{CC} = 17\text{ }\mu\text{A}$, the power consumption P_C can be calculated as follows:

$$\begin{aligned} P_C &= (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC} \\ &= (13.5\text{ V} - 5.0\text{ V}) \times 200\text{ mA} + 13.5\text{ V} \times 17\text{ }\mu\text{A} \\ &= 1.7\text{ W} \end{aligned}$$

At the maximum ambient temperature $T_{\max} = 85^\circ\text{C}$,
the thermal impedance (Junction to Ambient) $\theta_{JA} = 21.8^\circ\text{C/W}$ (4-layer PCB)

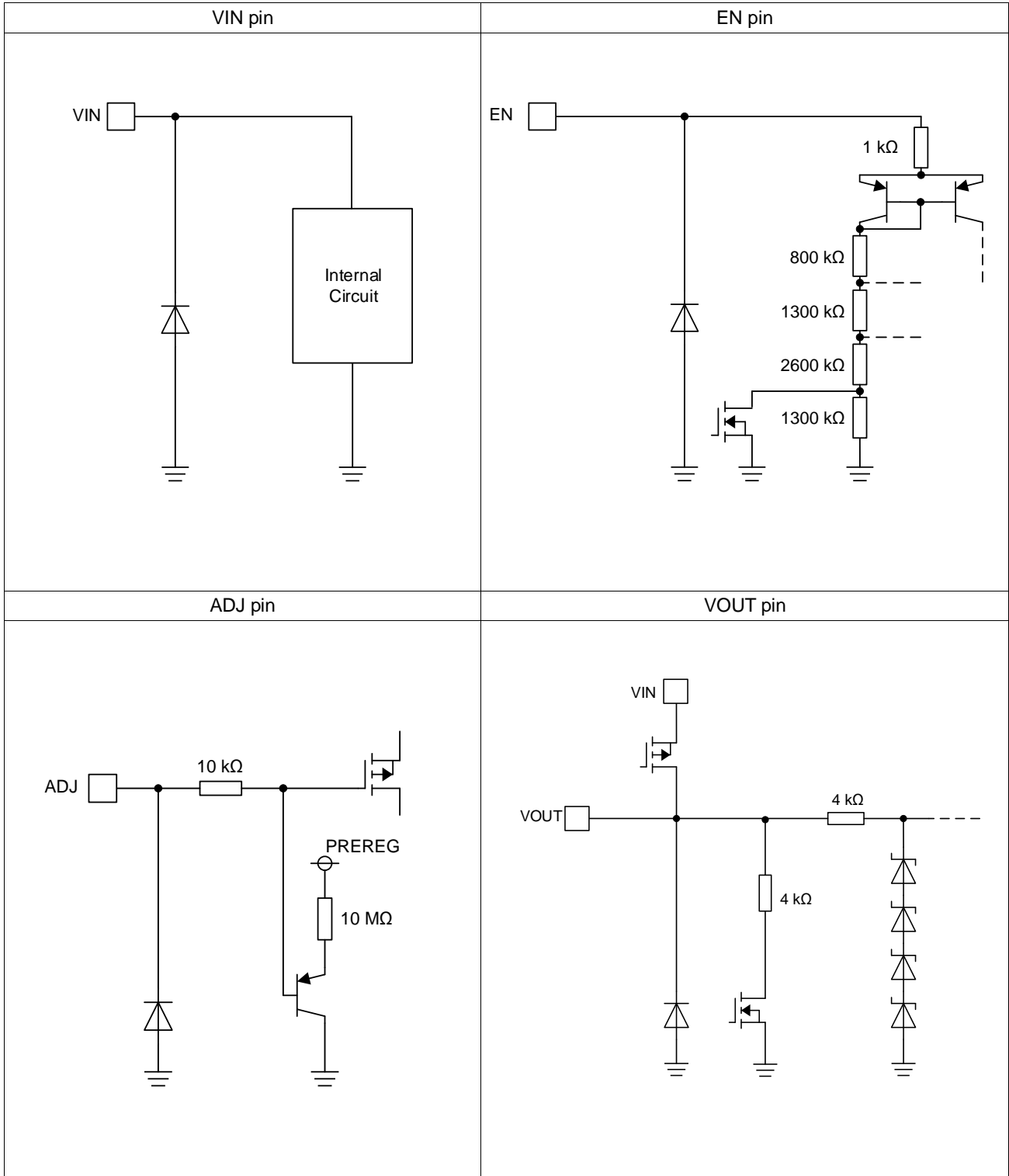
$$\begin{aligned} T_j &= T_{\max} + P_C \times \theta_{JA} \\ &= 85^\circ\text{C} + 1.7\text{ W} \times 21.8^\circ\text{C/W} \\ &= 122.1^\circ\text{C} \end{aligned}$$

When operating the IC, the top center of case's (mold) temperature $T_T = 100^\circ\text{C}$, $\Psi_{JT} = 10^\circ\text{C/W}$ (1-layer PCB)

$$\begin{aligned} T_j &= T_T + P_C \times \Psi_{JT} \\ &= 100^\circ\text{C} + 1.7\text{ W} \times 10^\circ\text{C/W} \\ &= 117.0^\circ\text{C} \end{aligned}$$

If it is difficult to ensure the margin by the calculations above, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad for optimum thermal performance.

I/O Equivalence Circuits *(Note 1)*



(Note 1) Resistance value is Typical.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Thermal Consideration

The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. The amount of heat generation depends on the voltage difference between the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating. If Junction temperature is over Tjmax (=150 °C), IC characteristics may be worse due to rising chip temperature. Heat resistance in specification is measurement under PCB condition and environment recommended in JEDEC. Ensure that heat resistance in specification is different from actual environment.

8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

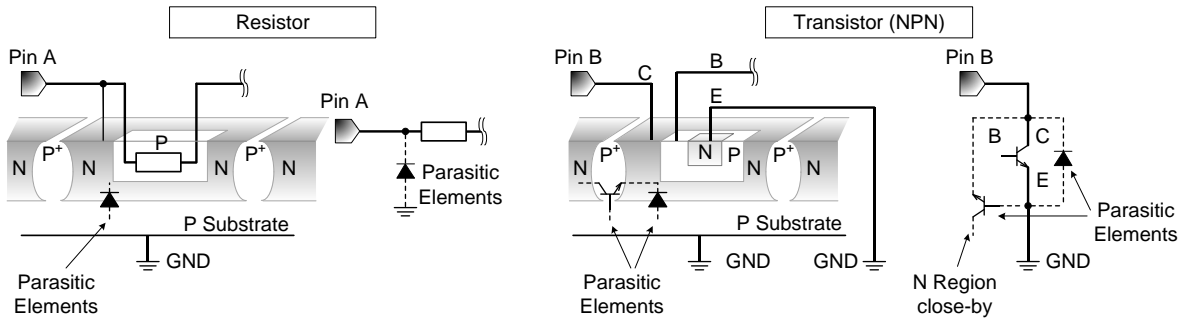
Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

- When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
- When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Shutdown Protection Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

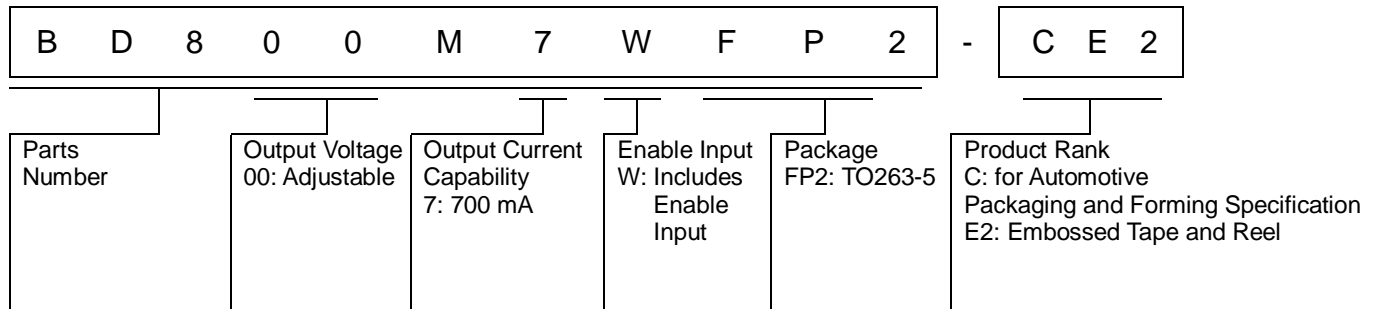
14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

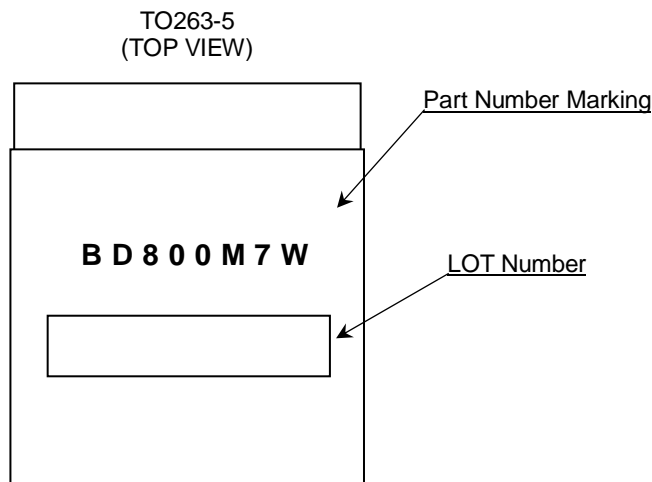
15. Enable Pin

The EN Pin is for controlling ON/OFF the output voltage. Do not make voltage level of chip enable keep floating level, or between V_{ENH} and V_{ENL} . Otherwise, the output voltage would be unstable or indefinite.

Ordering Information

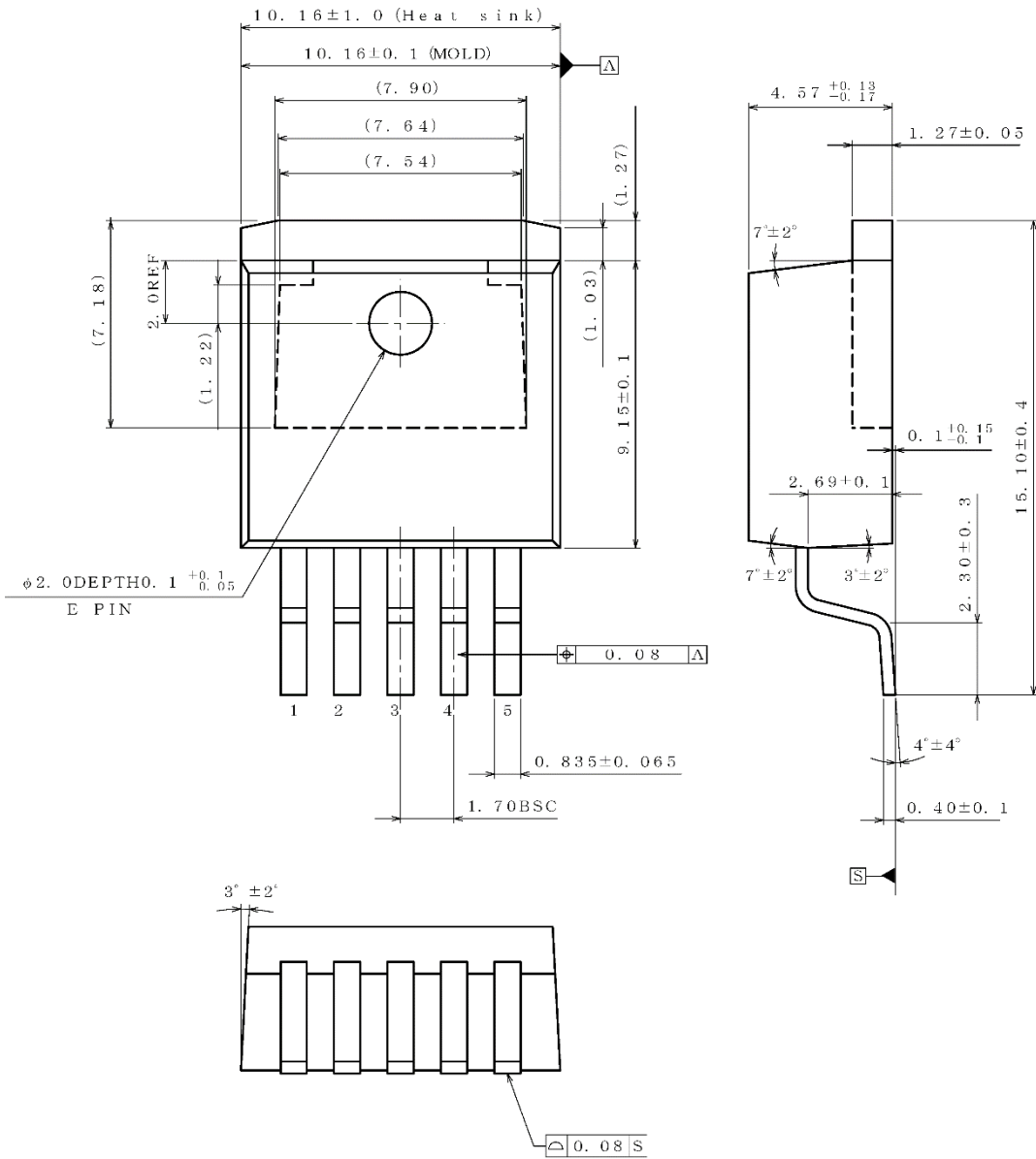


Marking Diagram



Physical Dimension and Packing Information

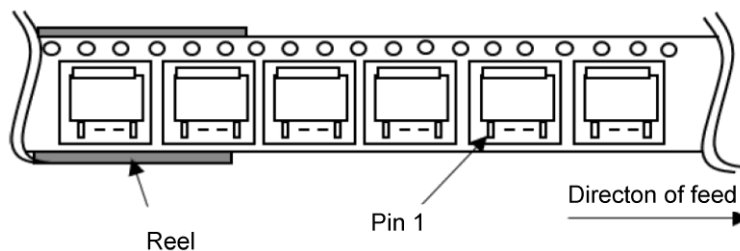
Package Name	TO263-5
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(UNIT : mm)
 PKG : TO263-5
 Drawing No. EX573-5002

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
09.Jul.2019	001	New Release

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[TCR3DG12,LF](#) [MIC5514-3.3YMT-T5](#) [MIC5512-1.2YMT-T5](#) [MIC5317-2.8YM5-T5](#) [SCD7912BTG](#) [NCP154MX180270TAG](#) [SCD33269T-](#)
[5.0G](#) [NCV8170BMX330TCG](#) [NCV8170AMX120TCG](#) [NCP706ABMX300TAG](#) [NCP153MX330180TCG](#) [NCP114BMX075TCG](#)
[MC33269T-3.5G](#) [CAT6243-ADJCMT5T](#) [TCR3DG33,LF](#) [AP2127N-1.0TRG1](#) [TCR4DG35,LF](#) [LT1117CST-3.3](#) [LT1117CST-5](#)
[TAR5S15U\(TE85L,F\)](#) [TAR5S18U\(TE85L,F\)](#) [TCR3UG19A,LF](#) [TCR4DG105,LF](#) [NCV8170AMX360TCG](#)