Datasheet

Power Supply IC Series for TFT-LCD Panels

Gamma voltage generated IC with built-in DAC

BD81026MUV

General Description

The feature of gamma voltage generated IC BD81026MUV provides a single-chip solution with a high-precision 10-bit DAC setting controlled by I^2C serial communications interface and a buffer amp (12ch).

Features

- Built in 10bit DAC (12ch)
- Built in DAC Output Buffer Amplifier (12ch)
- Double Register Switch Synchronously Function (BKSEL)
- DAC Output Latch Function (LD)
- I^2C Interface (SDA, SCL)
  STANDARD-MODE, FAST-MODE changeable
- Thermal Shut-Down Circuit
- Under Voltage Lock-Out Function
- Power ON Reset Circuit
- Input Tolerant (SDA, SCL, BKSEL, LD)

Applications

It may be used with TFT-LCD panels, such as big screen and high resolution LCD televisions.

Key Specifications

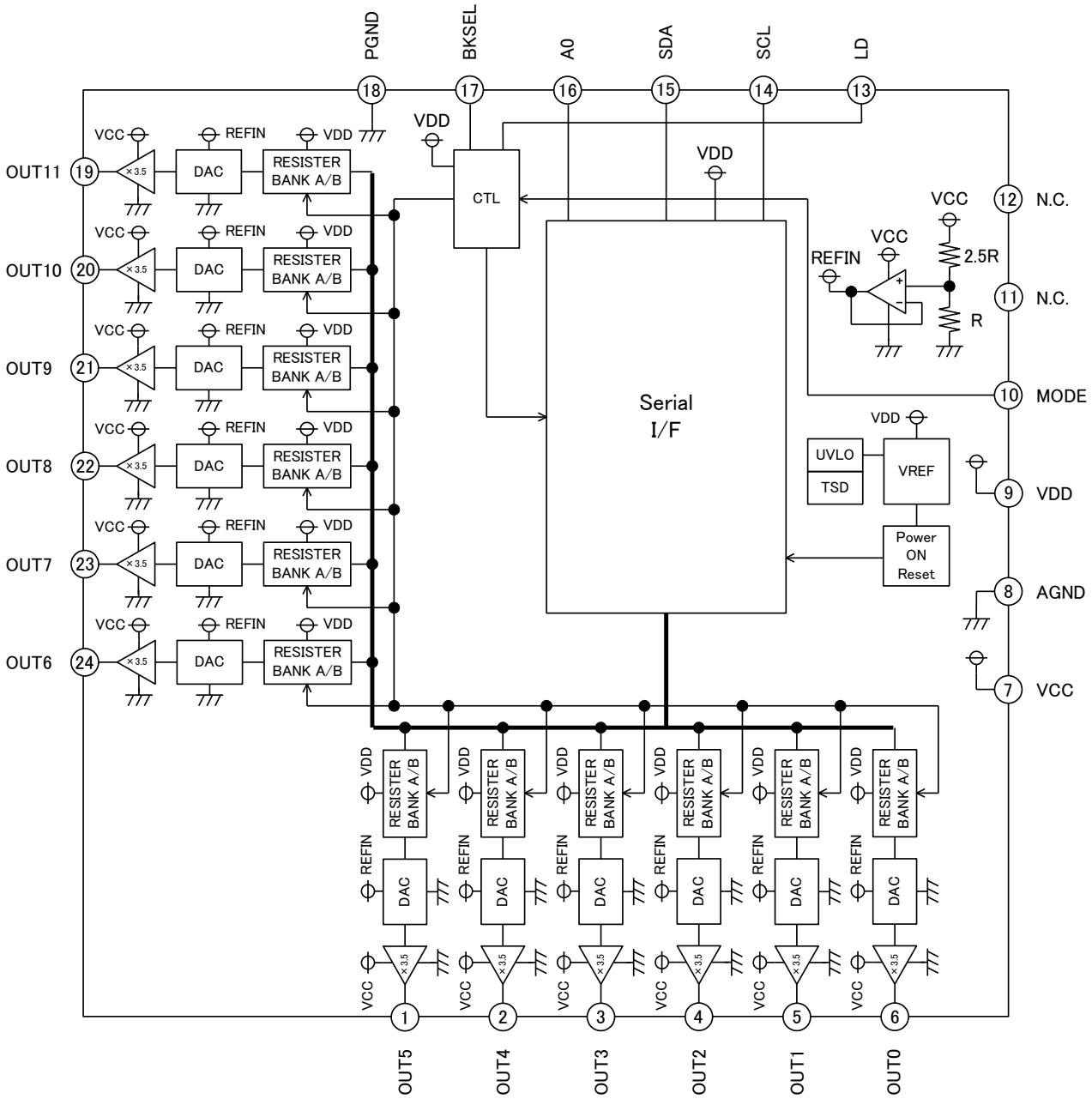
- Power Supply Voltage Range(VDD): 2.1V to 3.6V
- Power Supply Voltage Range(VCC): 8.0V to 18.0V
- Operating Temperature Range: -25°C to +85°C

Package

W(Typ) x D(Typ) x H(Max)

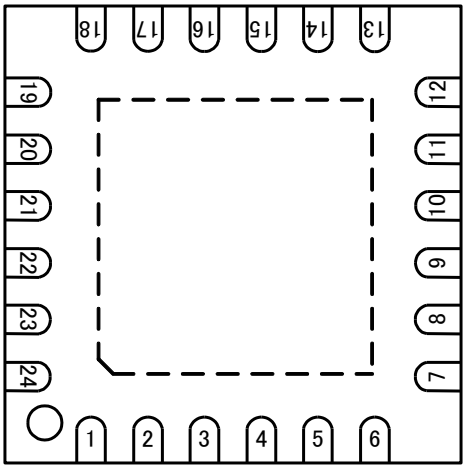
VQFN024V4040
4.00mm x 4.00mm x 1.00mm

Block Diagram



Pin Configuration

TOP VIEW



Pin Description

PIN No.	Pin name	Function	PIN No.	Pin name	Function
1	OUT5	Gamma output pin 5	13	LD	Latch pin (Note 1)
2	OUT4	Gamma output pin 4	14	SCL	Serial clock input pin
3	OUT3	Gamma output pin 3	15	SDA	Serial data input pin
4	OUT2	Gamma output pin 2	16	A0	Device address switching pin
5	OUT1	Gamma output pin 1	17	BKSEL	BANK select pin (Note 2) L : BANK A select H : BANK B select
6	OUT0	Gamma output pin 0	18	PGND	DAC output buffer amplifier GND input
7	VCC	Buffer amplifier power supply input for DAC output	19	OUT11	Gamma output pin 11
8	AGND	Logic, Analog GND input	20	OUT10	Gamma output pin 10
9	VDD	Logic, Analog power supply input	21	OUT9	Gamma output pin 9
10	MODE	BKSEL/LD mode switching pin L : BKSEL writing mode select H : LD writing mode select	22	OUT8	Gamma output pin 8
11	N.C.	-	23	OUT7	Gamma output pin 7
12	N.C.	-	24	OUT6	Gamma output pin 6

(Note 1) When Data writing function by LD pin control is not used, please connect LD pin to GND.
(Note 2) When Data writing function by BKSEL pin control is not used, please connect BKSEL pin to GND.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage 1	V_{DD}	4.5	V
Power Supply Voltage 2	V_{CC}	19.0	V
Functional Pin Voltage	V_{BKSEL}, V_{A0}, V_{LD} V_{MODE}	4.5	V
2 Lines Serial Pin Voltage	V_{SDA}, V_{SCL}	4.5	V
Junction Temperature	Tjmax	150	°C
Power Dissipation	Pd	3.56 (Note 1)	W
Operating Temperature Range	Topr	-25 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) To use the IC at temperatures over Ta=25°C, derate power rating by 28.5mW/°C.
When mounted on a four-layer glass epoxy board measuring 74.2mm x 74.2mm x 1.6mm (All layer with copper foil: 5505mm^2).

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-25°C to +85°C)

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage 1	V_{DD}	2.1	3.6	V
Power Supply Voltage 2	V_{CC}	8.0	18.0	V
Function Pin Voltage	V_{BKSEL}, V_{A0}, V_{LD} V_{MODE}	-0.1	+3.6	V
2 Lines Serial Pin Voltage	V_{SDA}, V_{SCL}	-0.1	+3.6	V
2 Lines Serial Frequency	f_{CLK}	-	400	kHz

Electrical Characteristics (Unless otherwise specified, Ta=25°C, V_{DD}=3.3V, V_{CC}=12.6V)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
【 Gamma Amplifier 】						
Sink Current Capability Nch Side (AMP0)	IooA	-	-	-10	mA	During REG0=3AFh (11.6V) setting, V_{OUT0}=12.6V input
Sink Current Capability Nch Side (AMP1 to AMP5, AMP7 to AMP10)	IooB	-	-	-30	mA	During REG1 to REG5, REG7 to REG10=1E8h (6.0V) setting, V_{OUT1} to V_{OUT5}, V_{OUT7} to V_{OUT10}=7V
Sink Current Capability Nch Side (AMP6)	IooC	-	-	-60	mA	During REG6=1E8h (6.0V) setting, V_{OUT6}=7V
Sink Current Capability Nch Side (AMP11)	IooD		-	-60	mA	During REG11=051h (1.0V) setting, V_{OUT11}=2V input
Source Current Capability Pch Side (AMP0)	IoiA	60	-	-	mA	During REG0=3AFh (11.6V) setting, V_{OUT0}=10.6V input
Source Current Capability Pch Side (AMP1 to AMP5, AMP7 to AMP10)	IoiB	30	-	-	mA	During REG1 to REG5, REG7 to REG10=1E8h (6.0V) setting, V_{OUT1} to V_{OUT5}, V_{OUT7} to V_{OUT10}=5V
Source Current Capability Pch Side (AMP6)	IoiC	60	-	-	mA	During REG6=1E8h (6.0V) setting, V_{OUT6}=5V
Source Current Capability Pch Side (AMP11)	IoiD	10	-	-	mA	During REG11=051h (1.0V) setting, V_{OUT11}=0V input
Load Stability (OUT0)	⊿VO-A	-	10	70	mV	During REG0=1E8h (6.0V) setting, Io=0mA to -30mA
Load Stability (OUT1 to OUT5, OUT7 to OUT10)	⊿VO-B	-	10	70	mV	During REG1 to REG5, REG7 to REG10=1E8h (6.0V) setting, I_O=-15mA to +15mA
Load Stability (OUT6)	⊿VO-C	-	10	70	mV	During REG6=1E8h (6.0V) setting, I_O=-15mA to +15mA
Load Stability (OUT11)	⊿VO-D	-	10	70	mV	During REG11=1E8h (6.0V) setting, I_O=0mA to +30mA
MAX Output Voltage (OUT0)	VOH-A	V_{CC}-0.2	V_{CC}-0.1	-	V	I_O=-30mA
MAX Output Voltage (OUT1 to OUT5, OUT7 to OUT10)	VOH-B	V_{CC}-1.0	V_{CC}-0.6	-	V	I_O=-15mA
MAX Output Voltage (OUT6)	VOH-C	V_{CC}-1.0	V_{CC}-0.6	-	V	I_O=-15mA
MAX Output Voltage (OUT11)	VOH-D	V_{CC}-1.2	V_{CC}-0.75	-	V	I_O=-15mA
MIN Output Voltage (OUT0)	VOL-A	-	0.75	1.20	V	I_O=+15mA
MIN Output Voltage (OUT1 to OUT5, OUT7 to OUT10)	VOL-B	-	0.6	1.0	V	I_O=+15mA
MIN Output Voltage (OUT6)	VOL-C	-	0.6	1.0	V	I_O=+15mA
MIN Output Voltage (OUT11)	VOL-D	-	0.1	0.2	V	I_O=+30mA
Slew Rate (AMP0)	SR-A	1	4	-	V/µsec	OUT0=No load
Slew Rate (AMP1 to AMP5, AMP7 to AMP10)	SR-B	1	4	-	V/µsec	OUT1 to OUT5,OUT7 to OUT10=No load
Slew Rate (AMP6)	SR-C	1	4	-	V/µsec	OUT6=No load
Slew Rate (AMP11)	SR-D	1	4	-	V/µsec	OUT11=No load

Electrical Characteristics – Continued (Unless otherwise specified, Ta=25°C, V_{DD}=3.3V, V_{CC}=12.6V)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
【 10 Bit DAC 】						
Resolution	RES	-	10	-	Bit	
Integral Non-Linearity Error (INL)	LE	-2	-	+2	LSB	005h to 3FAh is the allowable margin of error against the ideal linear.
Differential Non-Linearity Error (DNL)	DLE	-2	-	+2	LSB	005h to 3FAh is the allowable margin of error against the ideal increase of 1LSB.
Output Voltage Precision	V_O	5.945	6.005	6.065	V	During REG0 to REG11=1E8h (6.0V) setting
Output Voltage Thermal Characteristics	V_T	-50	-	+50	mV	During REG0 to REG11=1E8h (6.0V) setting, Ta=-25°C to +85°C
【 Control Signal 1 (BKSEL, A0, LD, MODE) 】						
Threshold Voltage 1	V_{th1A}	0.8	-	1.7	V	V_{DD}=3.3V
Threshold Voltage 2	V_{th1B}	0.6	-	1.7	V	V_{DD}=2.5V
Pull-down Resistor	R_{ctl}	21	30	39	kΩ	
【 Control Signal 2 (SDA, SCL) 】						
Threshold Voltage 1	V_{th2A}	0.8	-	1.7	V	V_{DD}=3.3V
Threshold Voltage 2	V_{th2B}	0.6	-	1.7	V	V_{DD}=2.5V
Minimum Output Voltage	V_{OCL}	-	-	0.4	V	I_{SDA}=3mA
【 Whole Device 】						
VDD Power ON Reset Start-up Voltage	V_{det1}	1.75	1.9	2.05	V	VDD Rising voltage
VDD Under Voltage Lock-Out Voltage	V_{DDUV}	1.55	1.7	1.85	V	VDD Falling voltage
VDD Under Voltage Lock-Out Hysteresis Voltage	V_{DDHY}	-	200	-	mV	
VCC Under Voltage Lock-Out Release Voltage	V_{det2}	3.2	3.4	3.6	V	VCC Rising voltage
VCC Under Voltage Lock-Out Voltage	V_{CCUV}	2.8	3.0	3.2	V	VCC Falling voltage
VCC Under Voltage Lock-Out Hysteresis Voltage	V_{CCHY}	-	400	-	mV	
BKSEL Switching Time (Note 1)	t_{BKSEL}	-	0.3	1.0	µsec	
LD Switching Time (Note 2)	t_{LD}	-	0.3	1.0	µsec	
VDD Circuit Current	I_{CCL}	0.16	0.25	0.34	mA	Output No-load , DAC initial value setting
VCC Circuit Current	I_{CCH}	2	4	6	mA	Output No-load , DAC initial value setting

(Note 1) BKSEL switching time timing is shown below.

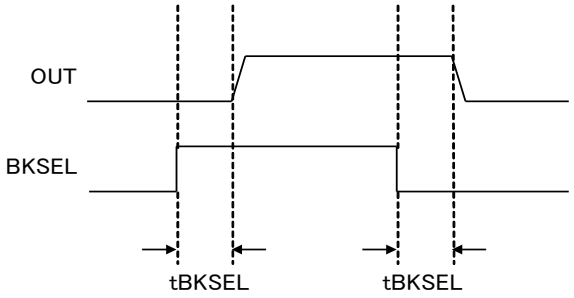


Figure 1. BKSEL Switching time timing

(Note 2) LD switching time timing is shown below.

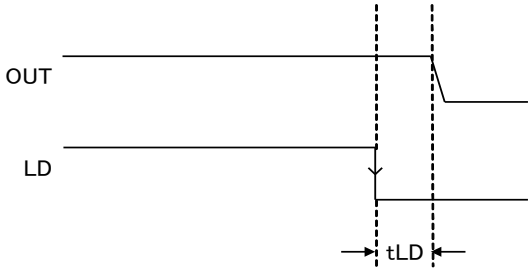


Figure 2. LD Switching time timing

Operation of each block

(1) 10 Bit DAC block

■Serial data control block

The serial interface uses a 2-line serial data format (SCL, SDA).

The serial data control block consists of a register that stores data from the SDA and SCL pins, and a DAC circuit that receives the output from this register and provides adjusted voltages to other IC blocks.

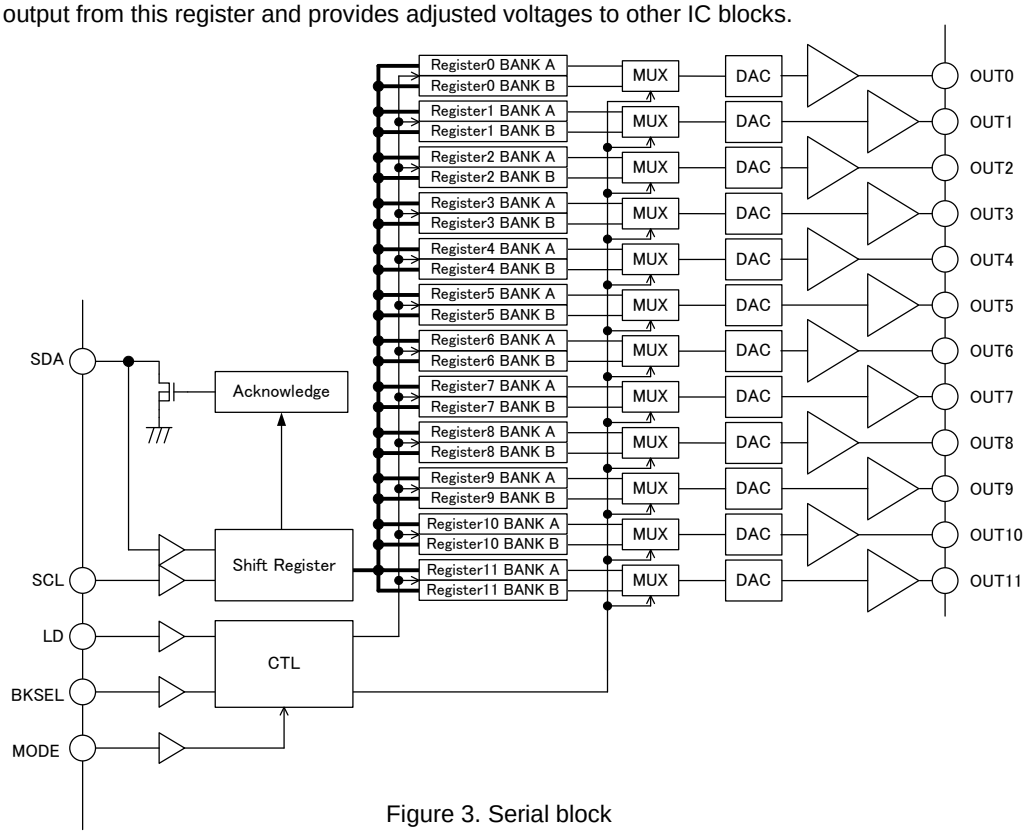


Figure 3. Serial block

・Register (Ch0 to Ch11)

A serial signal (consisting of 10-bit gamma correction voltage values) input using the serial interface or I^2C bus interface is held for each register address.

Data is initialized by the reset signal generated during a power-on reset.

Register is selectable by BKSEL pin. (For detail, refer to P.9.)

Also, it is selectable that either revises the DAC output setting voltage by LD pin to the data, read to register.

(For detail, refer to P.10.)

・Data writing mode selector

Switching MODE pin High/Low enables changing data switching mode.

During MODE=Low, a data is rewrote by Double Register switching function of BKSEL control.

During MODE=High, a data is rewrote by DAC output latch function of LD control.

MODE pin is pulled down inside so that at open state, it is Low.

If it is set to High, connect to VDD.

・DAC

The DAC LOGIC converts the 10-bit digital signal read to the register to a voltage.

・AMP (Ch0 to Ch11)

The Amp amplifies the voltage output from the DAC LOGIC.

While Under Voltage Lock-Out (UVLO) circuit or Thermal Shut Down (TSD) circuit is operating, output goes into Hi-z.

In case connecting high capacity capacitor with low ESR, damping is needed with a resistor to keep phase margin.

■Output Voltage setting mode

Writes to a register address specified by I²C BUS.

Mode for writing from I²C BUS to register are (i)Single mode and (ii)Multi mode.

On single mode, write data to one designated register.

On multi mode, multi data write can be performed continuously from a start address register specified with the second byte of data.

Single mode or multi mode can be configured by having or not having “stop bit”.

(i) Single mode timing chart

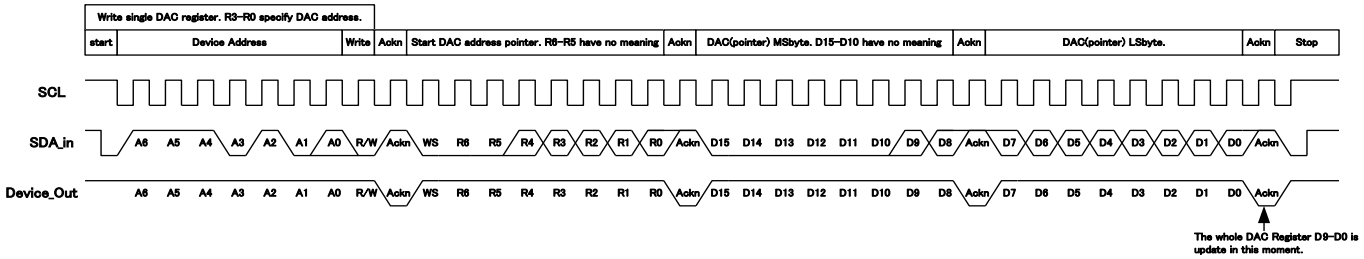


Figure 4. Output voltage setting (Single mode)

(ii) Multi mode timing chart

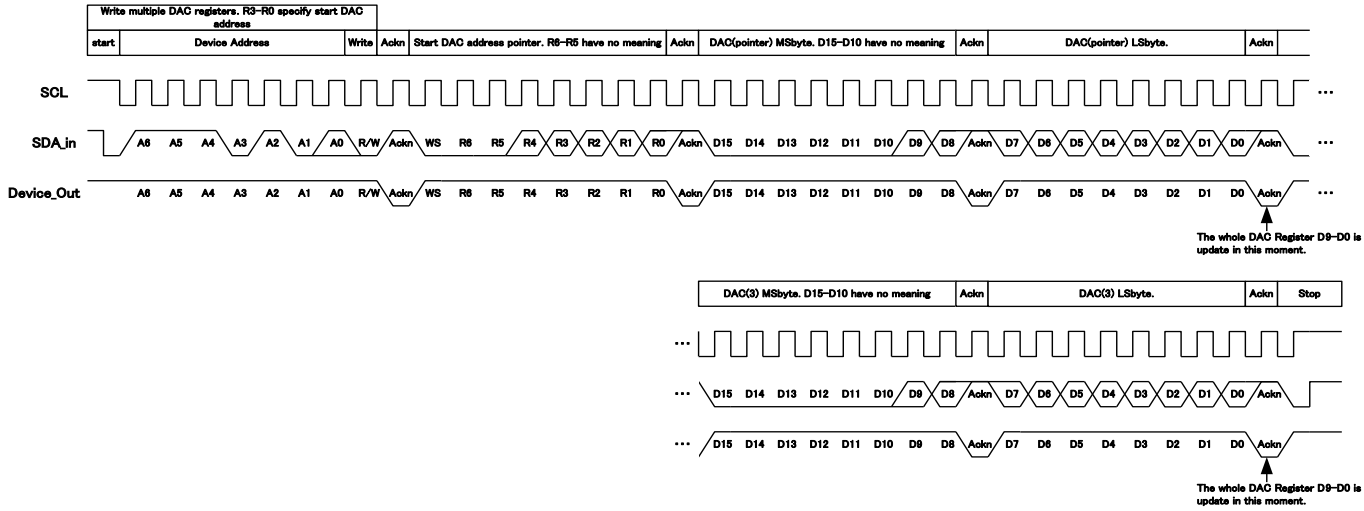


Figure 5. Output voltage setting (Multi mode)

■Device address

Device address A6 to A1 are specific to the IC and should be set as follows: （A6 to A0）=111010(A0).

A0 can be set by external. It is pulled-up inside so that in open state, it turns to”0”. If setting to ”1”, connect to VDD.

■Command interface

Use I²C BUS for command interface with host. Writing or reading by specifying 1 byte select address, along with slave address. I²C BUS Slave mode format is shown below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	DATA	A	P

S : START condition

Slave Address : After slave address (7bit), send total 8bit data with either READ mode (H) or WRITE mode (L). （MSB first）

A : Acknowledge

Added acknowledge bit per byte in sending and receiving data.
If the data is sent/ received properly, “L” is send/ received.
Sending or Receiving ”H” means lack of acknowledge.

Select Address : Use 1 byte select address.

DATA : Data byte. Sending/ Receiving data. （MSB first）

P : STOP condition

The case where writing 3FCh to DAC1（Single mode）

S	Slave Address	A	Select Address	A	Register1 DATA0	A	Register1 DATA1	A	P
(EX.)	E8h or EAh		01h		03h		FCh		


: Slave from master


: Master from slave

The case where writing 3FCh from DAC0 to DAC3 (Multi mode)

S	Slave Address	A	Select Address	A	Register0 DATA0	A	Register0 DATA1	A	Register1 DATA0	A	Register1 to 3 DATA0,DATA1	A	P
(EX.)E8h or EAh			00h		03h		FCh		03h				


: Slave from master


: Master from slave

■Double Register switching function

When setting Low of MODE pin, it is able to switch BANK A or BANK B by changing High/Low of BKSEL pin.
During BKSEL=Low, connect BANK A to DAC.
During BKSEL=High, connect BANK B to DAC.

■DAC output switching function by LD pin
During MODE pin = High setting, depending on LD pin condition, DAC output is able to switch.

・In case LD=Low, write a data to a register of a specified address and DAC output outputs the data written to the register.
(Refer to Figure 6: DAC output switching operation by LD pin (i).)

・In case LD=High, write a data to a register of a specified address and DAC output maintains the previous data setting. In this condition, if LD pin switches from High to Low, all DAC output (OUT0 to OUT11) outputs synchronously a data, written to a register.
(Refer to Figure 6: DAC output switching operation by LD pin (ii).)

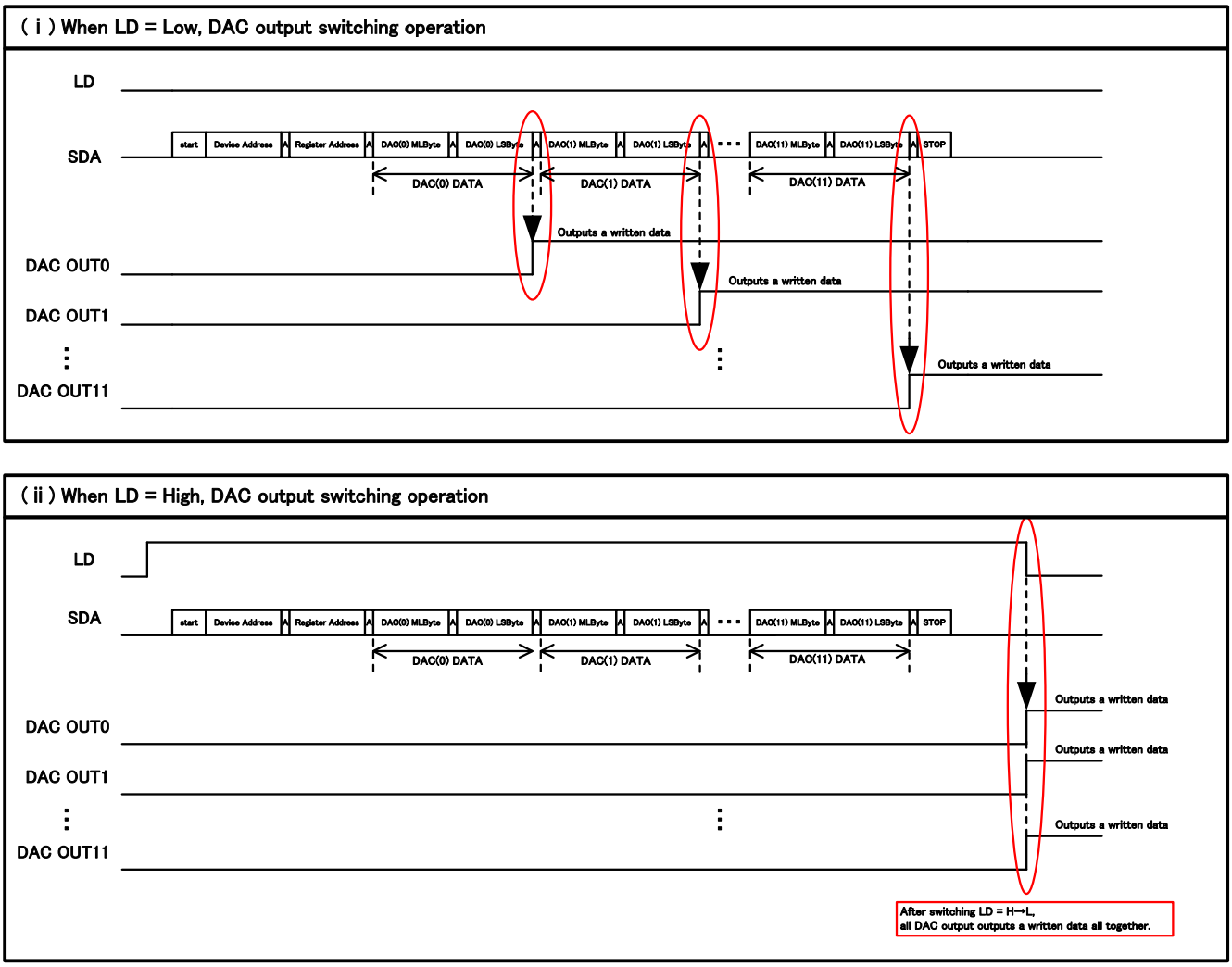


Figure 6. DAC output switching operation by LD pin

■Register address

BANK A and BANK B register addresses are configured by the chart below.

Register name	BANK A					Initial Value	Register name	BANK B					Initial Value
	R4	R3	R2	R1	R0			R4	R3	R2	R1	R0	
Register 0 BANK A	0	0	0	0	0	000h	Register 0 BANK B	1	0	0	0	0	000h
Register 1 BANK A	0	0	0	0	1	000h	Register 1 BANK B	1	0	0	0	1	000h
Register 2 BANK A	0	0	0	1	0	000h	Register 2 BANK B	1	0	0	1	0	000h
Register 3 BANK A	0	0	0	1	1	000h	Register 3 BANK B	1	0	0	1	1	000h
Register 4 BANK A	0	0	1	0	0	000h	Register 4 BANK B	1	0	1	0	0	000h
Register 5 BANK A	0	0	1	0	1	000h	Register 5 BANK B	1	0	1	0	1	000h
Register 6 BANK A	0	0	1	1	0	000h	Register 6 BANK B	1	0	1	1	0	000h
Register 7 BANK A	0	0	1	1	1	000h	Register 7 BANK B	1	0	1	1	1	000h
Register 8 BANK A	0	1	0	0	0	000h	Register 8 BANK B	1	1	0	0	0	000h
Register 9 BANK A	0	1	0	0	1	000h	Register 9 BANK B	1	1	0	0	1	000h
Register 10 BANK A	0	1	0	1	0	000h	Register 10 BANK B	1	1	0	1	0	000h
Register 11 BANK A	0	1	0	1	1	000h	Register 11 BANK B	1	1	0	1	1	000h

For Register address, lower 5bit (R4 to R0) at 2nd byte will be used. R6 to R5 is “Don’t Care.”

(2) Power On Reset

At VDD input, it generates Reset signal and initialize serial I/F and each register.

(3) UVLO (Under Voltage Lock Out)

When VDD and VCC falls under the setting value, Under Voltage Lock Out function is activated and output will be Hi-Z.
If VDD UVLO is operated, initialize a register.
If VCC UVLO is operated, NOT initialize a register.

(4) TSD(Thermal Shut Down)

The TSD circuit turns output Hi-z when the chip temperature reaches or exceeds approximately 175°C in order to prevent thermal destruction or thermal runaway. When the chip returns to a specified temperature, the circuit resets.
The TSD circuit is designed only to protect the IC itself. Application thermal design should ensure operation of the IC below the junction temperature of approximately 150°C.

Power supply sequence

Activate VDD before VCC to avoid a malfunction due to undefined logic in LOGIC circuit. Inputs serial data after canceling Power on Reset.
In case power supply turns OFF, it is recommended after VCC OFF, VDD OFF ,or VCC and VDD OFF synchronously.
If VDD turns OFF before VCC OFF, output condition may not be stable because of LOGIC circuit instability.
Please demonstrate and test fully on an application board.

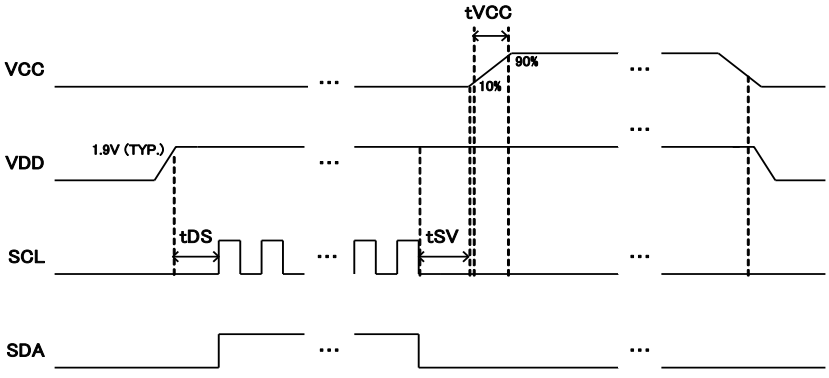


Figure 7. Power supply sequence

Power supply sequence typical value

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Serial Input Timing	t_{DS}	100	-	-	µs	
VCC Input Timing	t_{SV}	10	-	-	µs	
VCC Rising Time	t_{VCC}	1	-	-	ms	

I²C Timing

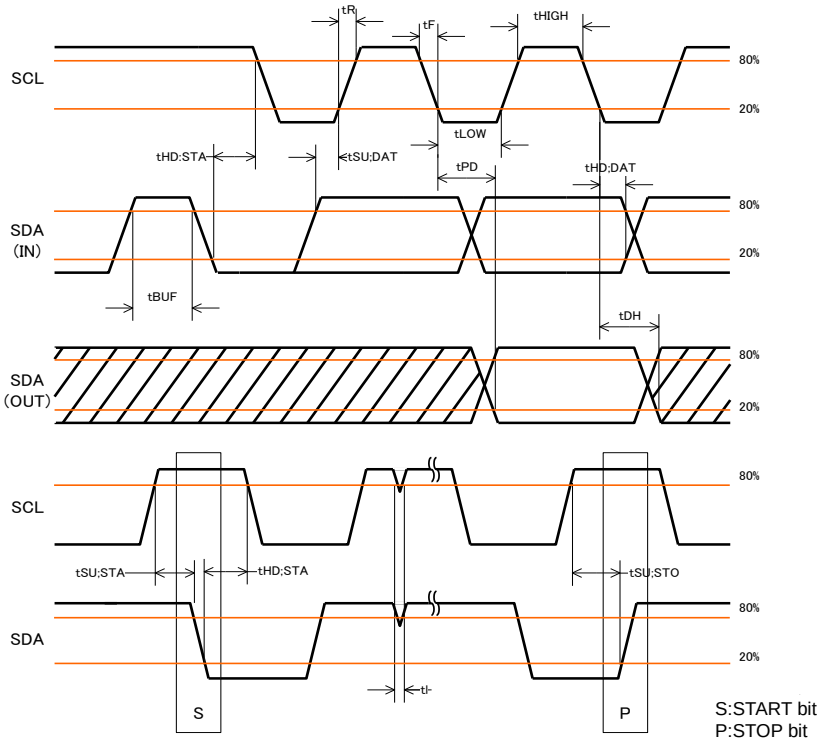


Figure 8. I²C timing

・Timing rule

PARAMETER	SYMBOL	NORMAL mode			FAST mode			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
SCL frequency	f_{SCL}	-	-	100	-	-	400	kHz
SCL"H" time	t_{HIGH}	4.0	-	-	0.6	-	-	µs
SCL"L" time	t_{LOW}	4.7	-	-	1.2	-	-	µs
Rising time	t_R	-	-	1.0	-	-	0.3	µs
Falling time	t_F	-	-	0.3	-	-	0.3	µs
Start condition holding time	$t_{HD;STA}$	4.0	-	-	0.6	-	-	µs
Start condition set-up time	$t_{SU;STA}$	4.7	-	-	0.6	-	-	µs
SDA holding time	$t_{HD;DAT}$	200	-	-	100	-	-	ns
SDA set-up time	$t_{SU;DAT}$	200	-	-	100	-	-	ns
Acknowledge delay time	t_{PD}	-	-	0.9	-	-	0.9	µs
Acknowledge hold time	t_{DH}	-	0.1	-	-	0.1	-	µs
Stop condition set-up time	$t_{SU;STO}$	4.7	-	-	0.6	-	-	µs
BUS open time	t_{BUF}	4.7	-	-	1.2	-	-	µs
Noise spike width	t_I	-	0.1	-	-	0.1	-	µs

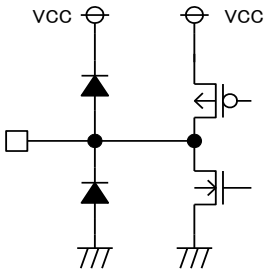
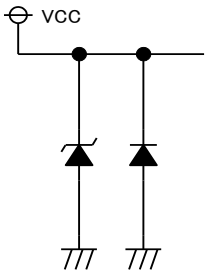
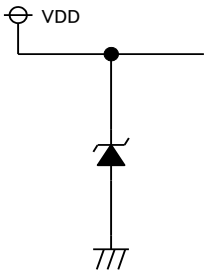
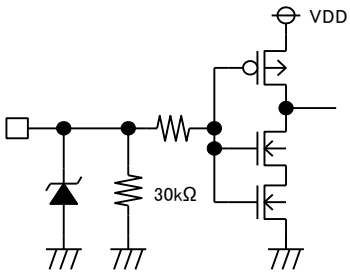
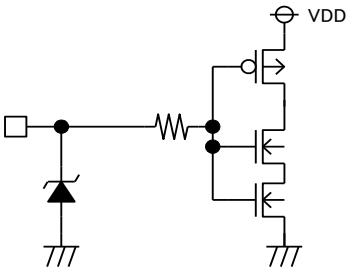
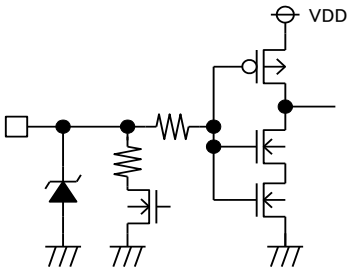
Gamma output setting

Relation between gamma output voltage (OUT0 to OUT11) and DAC setting value is shown as below.

$$Output\ voltage\ (OUT0\ to\ OUT11) = \frac{DAC\ setting\ value}{1024} \times VCC$$

DAC setting value range is 0 to 1023.
Gamma output OUT0 to OUT11 is outputted after VCC UVLO release. During UVLO detection, output is Hi-Z.

I/O Equivalent circuits

1.OUT5, 2.OUT4, 3.OUT3, 4.OUT2 5.OUT1, 6.OUT0, 19.OUT11, 20.OUT10 21.OUT9, 22.OUT8, 23.OUT7, 24.OUT6	7.VCC	9.VDD
		
10.MODE, 13.LD, 16.A0, 17.BKSEL	14.SCL	15.SDA
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

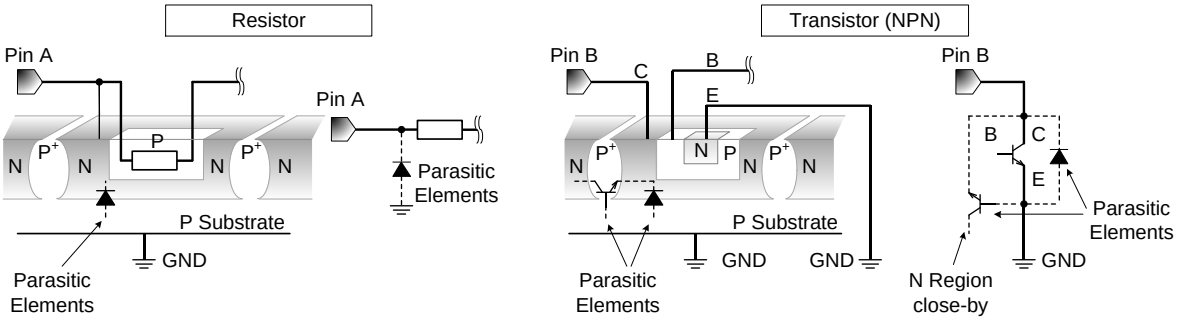


Figure 9. Example of monolithic IC structure

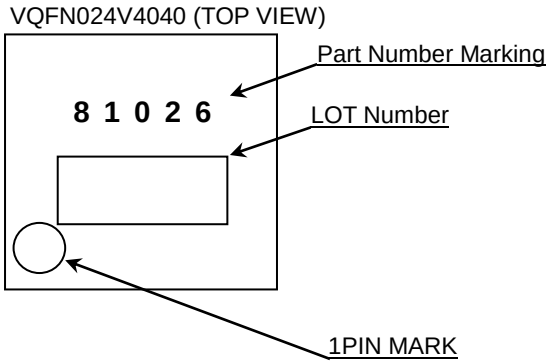
13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

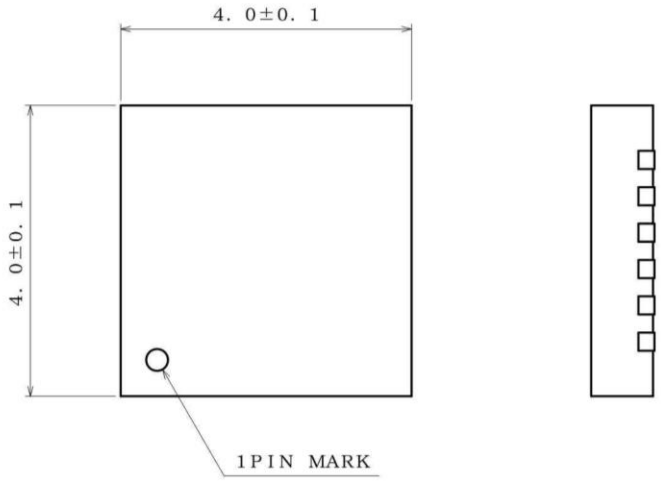
B D 8 1 0 2 6 M U V	-	E 2
Part number	Package MUV: VQFN024V4040	Packaging and forming specification E2: Embossed tape and reel

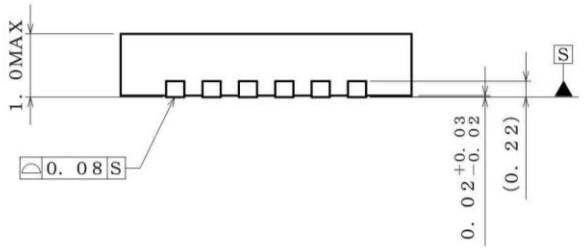
Marking Diagram

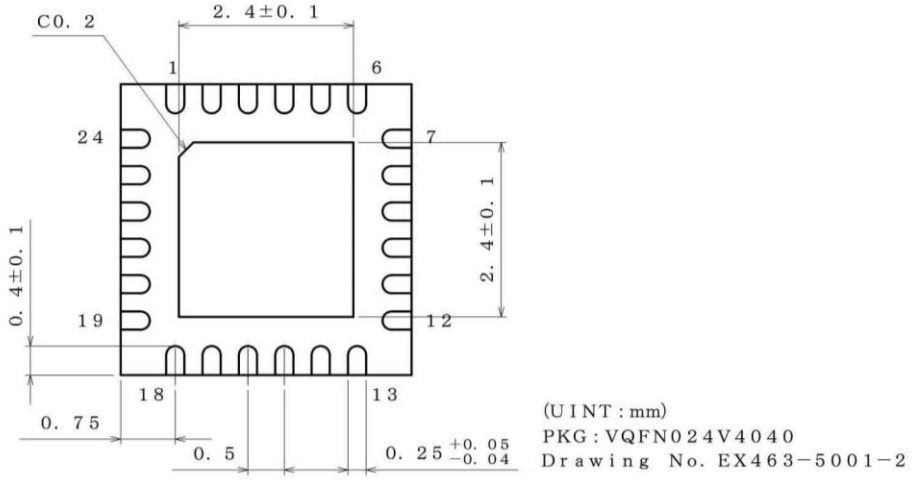


Physical Dimension, Tape and Reel Information

Package Name	VQFN024V4040

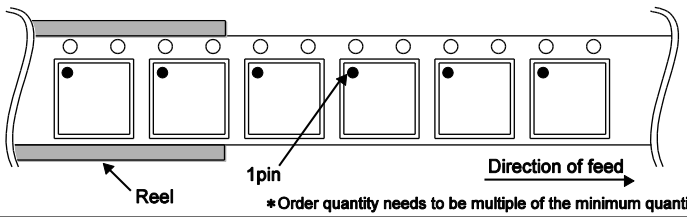






<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
19.Feb.2016	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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