

5ch System Motor Driver

BD8203EFV

General Description

BD8203EFV is a 5ch system motor driver for CD/DVD. A linear BTL mode can be adopted for all 5ch to reduce noise. It has a Built-in 5V regulator, a changeable regulator, and a general-purpose operational amplifier. Designed best for car audio systems.

Features

- Linear BTL method is implemented for the actuator driver and the DC motor driver to reduce noise.
- Loading driver 1ch
- Built-in regulator 2ch (1ch output changeable)
- MUTE function and Standby function
- Built-in general-purpose operational amplifier 1ch
- Built-in internal operational amplifier for the voltage detection between driver outputs and for VC standard

Applications

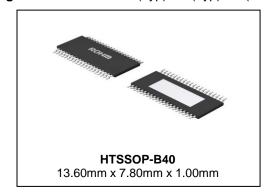
Car Audio

Key Specifications

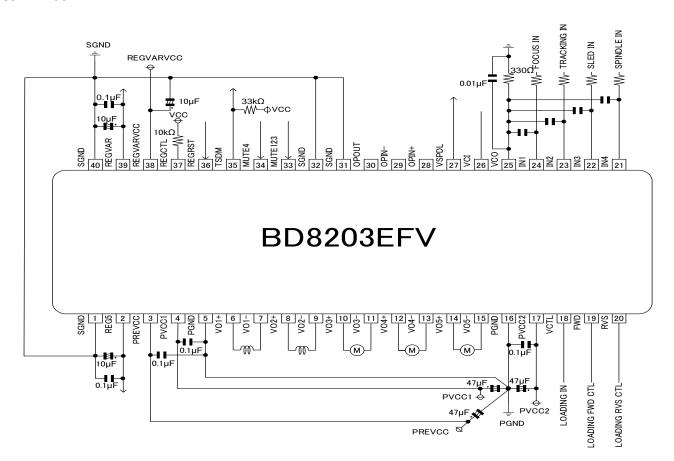
- Power Supply Voltage Range:
 Driver Part Pre Steps and Regulator1 7.5V to 14V
 Driver Part Power Steps 4.5V to VPREVCC V
 Power Steps of Two Regulators 4.5V to VPREVCC V
- Standby-on Current: 1mA(Max)
 Operating Temperature Range: -40°C to +85°C

Package

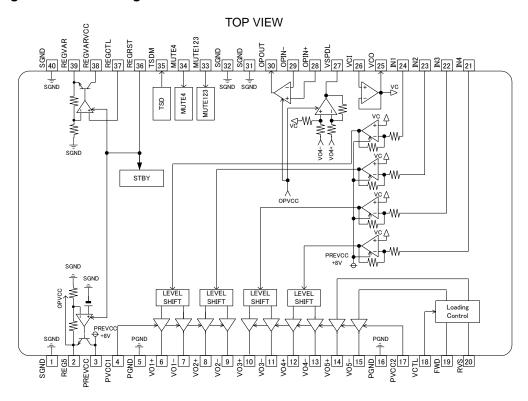
W(Typ) x D(Typ) x H(Max)



Typical Application Circuit



Block Diagram and Pin Configuration



Pin Description

| n Des | cription | | | | |
|-------|----------|---|-----|-----------|--|
| No. | Symbol | Description | No. | Symbol | Description |
| 1 | SGND | Signal GND | 21 | IN4 | CH4(SPDL)input |
| 2 | REG5 | REG5V Output | 22 | IN3 | CH3(SLD)input |
| 3 | PREVCC | PRE part, REG circuit, power supply terminal(+8V) | 23 | IN2 | CH2(TRK)input |
| 4 | PVCC1 | Power supply 1 | 24 | IN1 | CH1(FCS) input |
| 5 | PGND | Power GND | 25 | VCO | Standard voltage (VC) output |
| 6 | VO1+ | CH1(FCS) Positive output | 26 | VCI | Standard voltage (VC) input |
| 7 | VO1- | CH1(FCS) Negative output | 27 | VSPDL | Voltage detection value output between VO4 outputs |
| 8 | VO2+ | CH2(TRK) Positive output | 28 | OPIN+ | General purpose Op Amp non-reversing input |
| 9 | VO2- | CH2(TRK) Negative output | 29 | OPIN- | General purpose Op Amp reversing input |
| 10 | VO3+ | CH3(SLD) Positive output | 30 | OPOUT | General purpose Op Amp output |
| 11 | VO3- | CH3(SLD) Negative output | 31 | SGND | Signal GND |
| 12 | VO4+ | CH4(SPDL) Positive output | 32 | SGND | Signal GND |
| 13 | VO4- | CH4(SPDL) Negative output | 33 | MUTE123 | MUTE CH1,2,3 |
| 14 | VO5+ | CH5(LOAD) Positive output | 34 | MUTE4 | MUTE CH4(SPDL) |
| 15 | VO5- | CH5(LOAD) Negative output | 35 | TSDM | Thermal shutdown flag output |
| 16 | PGND | Power GND | 36 | REGRST | REG Reset input |
| 17 | PVCC2 | Power supply 2 | 37 | REGCTL | REGVAR Output changeability input terminal |
| 18 | VCTL | CH5(LOAD) Voltage control input | 38 | REGVARVCC | REGVAR Tr power supply terminal |
| 19 | FWD | CH5(LOAD) FWD input | 39 | REGVAR | REGVAR output |
| 20 | RVS | CH5(LOAD) RVS input | 40 | SGND | Signal GND |

Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Limit | Unit |
|-----------------------------|-------------------------------------|-------------------|------|
| Power Supply Voltage | VPREVCC, VPVCC1, VPVCC2, VREGVARVCC | 15 | V |
| Input Terminal Voltage1 | V _{IN1} (Note 1) | VPREVCC | V |
| Input Terminal Voltage2 | V _{IN2} (Note 2) | V _{REG5} | V |
| Output Terminal Voltage | V _{OUT} (Note 3) | V_{REG5} | V |
| Operating Temperature Range | Topr | -40 to +85 | °C |
| Storage Temperature | Tstg | -55 to +150 | °C |
| Junction Temperature | Tjmax | 150 | °C |
| Power Dissipation | Pd (Note 4) | 4.7 | W |

(Note 1) Input terminal 1 : REGRST (Note 2) Input terminal 2 : REGCTL, MUTE123, MUTE4, VCI, RVS, FWD, IN1, IN2, IN3, IN4, OPIN+, OPIN-, VCTL (Note 3) Output terminal : VCO, TSDM, VSPDL

(Note 4) Ta =25°C, Standard board mounting

(70mm x 70mm x 1.6mm, 4 glass epoxy layer substrate, 70mm x 70mm of the back copper foil area)

Reduce power by 34.6mW for each degree above 25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to +85°C)

(Set the power supply voltage taking allowable dissipation into considerations.)

| Parameter | Symbol | Min | Тур | Max | Unit |
|--|----------------|-----|-----|---------|------|
| Driver Part Pre Steps and Regulator 1 Power-Supply Voltage | VPREVCC | 7.5 | 8 | 14 | V |
| Driver Part Power Steps Power-Supply Voltage | VPVCC1, VPVCC2 | 4.5 | 8 | VPREVCC | V |
| Power Steps of Two Regulators Power-Supply Voltage | VREGVARVCC | 4.5 | 5 | VPREVCC | V |

Electrical Characteristics

(Unless otherwise specified, VPREVCC=VPVCC1=VPVCC2=8V, VREGVARVCC=5V, VVCO=1.65V, Ta=25°C)

| Parameter | | Symbol | MIN | TYP | MAX | Unit | Conditions |
|--------------------------|--|---------------------|------|-----|------|------|-------------------------------|
| Circuit Current | Quiescent Current | lq | - | 37 | 55 | mA | MUTE123=MUTE4=H, FWD=RVS=L |
| | Standby-on Current | I _{STBY} | - | - | 1 | mA | Standby mode(REGRST = L) |
| | Input Offset Voltage | VIOBTL | -5 | 0 | +5 | mV | |
| | Output Offset Voltage | Vofbtl | -75 | - | +75 | mV | |
| BTL Driver | Output Saturation Voltage (Vertical Harmony) | Vosatbtl | - | 1.5 | 2.3 | V | I _L =500mA |
| | Input Output Gain | G_{VBTL} | 16.8 | 18 | 19.2 | dB | |
| | Input Impedance | RZINBTL | 20 | 40 | 80 | kΩ | |
| | Slew Rate | V _{SLBTL} | 1.0 | - | - | V/µs | |
| | Input Offset Voltage | V _{IOOP1} | -10 | - | +10 | mV | |
| | Input Bias Voltage | I _{BOP1} | -300 | - | - | nΑ | |
| | H Level Output Voltage | V _{OHOP1} | 4 | - | - | V | |
| General-purpose | L Level Output Voltage | V _{OLOP1} | - | - | 0.2 | V | |
| Operational Amplifier | Output Sink Current Ability | ISINKOP1 | 2 | - | - | mA | |
| • | Output Source Current Ability | I _{SOUOP1} | 2 | - | - | mA | |
| | Range of Same Phase Input | V _{ICMOP1} | 0 | | 3.8 | V | V _{REG5} =5.0V |
| | Slew Rate | V _{SLOP1} | 0.5 | - | - | V/µs | |

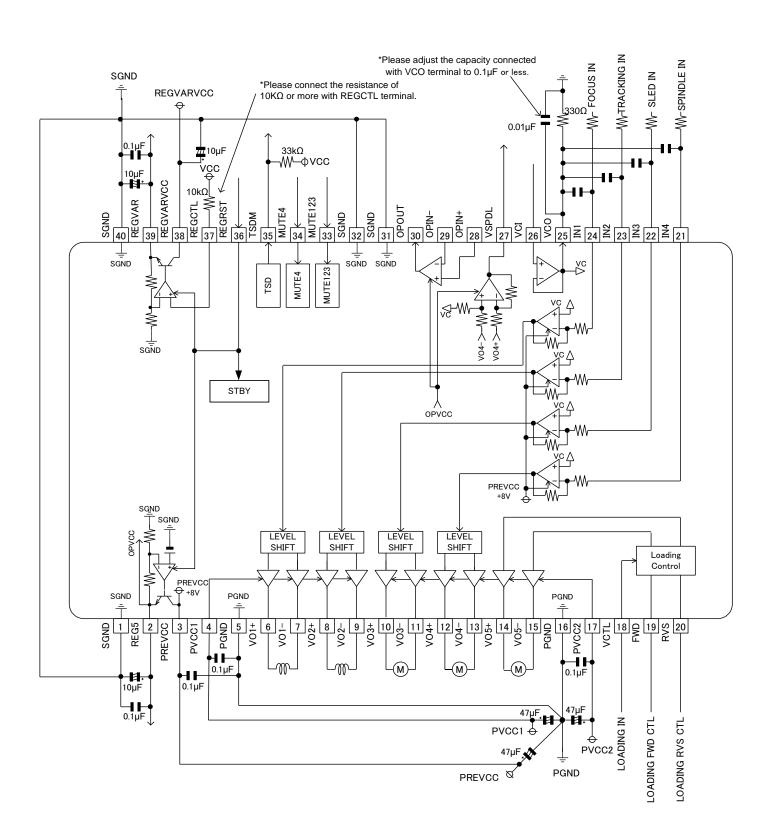
Electrical Characteristics – continued

(Unless otherwise specified, VPREVCC=VPVCC1=VPVCC2=8V, VREGVARVCC=5V, VVC0=1.65V, Ta=25°C)

| (Unless otherwi | se specified, V _{PREVCC} =V _{PVCC1} =V _F | | | | | | |
|------------------------------|---|---------------------------|------------------------------|------|---------------------|----------|--|
| | Parameter | Symbol | MIN | TYP | MAX | Unit | Conditions |
| | Output Offset Voltage | V000P2 | -50 | - | +50 | mV | V _{VO4+} = V _{VO4-} = 3.4V |
| Operational | H Level Output Voltage | V _{OHOP2} | 4 | - | - | V | |
| Amplifier for the | L Level Output Voltage | V _{OLOP2} | - | - | 0.2 | V | |
| Voltage | Output Sink Current Ability | ISINKOP2 | 2 | - | - | mA | |
| Detection between | Output Source Current Ability | I _{SOUOP2} | 2 | - | - | mA | |
| Driver Outputs | Range of Same Phase Input | VICMOP2 | 0 | | 6.8 | V | V _{REG5} =5.0V |
| | Input Output Gain | G _{VOP2} | -6.2 | -5 | -3.8 | dB | |
| | Slew Rate | V _{SLOP2} | 0.5 | - | - | V/µs | |
| | Output Offset Voltage | V000P3 | -10 | - | +10 | mV | |
| | Input Bias Voltage | І ворз | -300 | - | - | nA | |
| Internal | H level Output Voltage | V _{OHOP3} | 3.5 | - | - | V | |
| Operational | L level Output Voltage | V _{OLOP3} | - | - | 0.2 | V | |
| Amplifier for VC Standard | Output Sink Current Ability | ISINKOP3 | 0.5 | - | - | mA | |
| | Output Source Current Ability | I _{SOUOP3} | 10 | - | - | mA | |
| | Range of Same Phase Input | V _{ICMOP3} | 1.1 | - | 3.5 | V | V _{REG5} =5.0V BTL range of operation |
| | Input Terminal Inflow Current | I _{INLD} | - | 27 | 55 | μΑ | V _{FWD} ,V _{RVS} =3.3V |
| | VCTL Terminal Inflow Current | INVCTL | -1 | - | - | μA | V _{VCTL} =2V |
| Loading Driver | Output Offset Voltage | Vofld | -50 | 0 | +50 | mV | |
| Loading Driver | Output Saturation Voltage H | Vohld | - | 1.1 | 1.4 | V | I _L =500mA |
| | Output Saturation Voltage L | Volld | - | 0.45 | 0.8 | V | IL=500mA |
| | Input Output Gain | GVLD | 7.5 | 9.0 | 10.5 | dB | V _{VCTL} =1V |
| | REG5 Terminal Output Voltage | Voreg5 | 4.75 | 5.0 | 5.25 | V | I _L =100mA |
| Regulator 1 | REG5 Terminal Output Current Ability | I _{REG5_I} | 100 | - | - | mA | |
| | Load Change Regulation | $V_{\text{REG5_LOAD}}$ | -80 | - | - | mV | I _L =0mA to 100mA |
| | Input Change Regulation | V _{REG5_LINE} | -20 | - | +30 | mV | VPREVCC=7.5V to 9V, IL=100mA |
| | Range of REGVAR Output Voltage Setting | Vregvarr | 0.5 | - | 4.1 | V | I _L =100mA |
| | REGVAR Terminal Output Current Ability | I _{REGVAR_I} | 100 | - | - | mA | |
| D 11 0 | REGVAR Terminal Output Voltage | VREGVAR | 3.4 | 3.6 | 3.8 | V | IL=100mA,VREGCTL=3.3V |
| Regulator 2 (Output | Input Output Gain | G _{V2} | - | 1.09 | - | V/V | |
| Changeability) | Load Change Regulation Input Change Regulation | VREGVAR_LOAD VREGVAR_LINE | -80 -20 | - | +30 | mV mV | IL=0mA to 100mA VREGCTL=3.3V, VREGVARVCC=4.5V to 5.5V, |
| | Range of REGVARVCC Voltage | V _{REGVAR_ON} | V _{REGVAR} +0.9V | - | V _{PREVCC} | V | I _L =100mA |
| | REGCTL Terminal Input Current | IREGCTL_I | -1 | - | - | μA | VREGCTL=3.3V |
| | Input Voltage of Input Terminal H | VIHFUN | 2.0 | - | VPREVCC | V | MUTE123,MUTE4,RVS,FWD |
| | Input Voltage of Input Terminal L | VILFUN | - | - | 0.8 | V | MUTE123,MUTE4,RVS,FWD |
| | TSDM Terminal L Output Voltage | V _{OL_TSDM} | - | - | 0.4 | V | R _{TSDM} =33kΩ Pull-up3.3V |
| - <i>.</i> : | VCO Drop Mute Voltage | VMVco | 0.4 | 0.7 | 1 | V | |
| Function | PREVCC Drop Mute Voltage | VMPREVcc | 3.4 | 3.8 | 4.2 | V | |
| | REGRST Terminal Reset ON Voltage | V _{RESON1} | - | - | 0.8 | V | Turning OFF of regulator 1 and regulator 2 |
| | REGRST Terminal Reset OFF Voltage | VRESOFF | 2.0 | - | VPREVCC | V | Turning ON of regulator 1 and regulator 2 |

Application Information

1. Standard Example Application Circuit



Functional Description

Table for operation (VPREVCC=VPVCC1=VPVCC2=8V, VREGVARVCC=5V, VVCO=1.65V)

| Table 101 Obstation (VFREVOCE-VFVCC)-VFVCCZ-OV, VREGVARVOCE-OV, VVCC-1.00V) | | | | | | | | | | | |
|---|---------|-------|------|------|---------|---------|-----------------------|---------------|---------|---------|--|
| Input | | | | | Output | | | | | | |
| REGRST | MUTE123 | MUTE4 | FWD | RVS | REG5 | REGVAR | Operational amplifier | VO1 to VO3 | VO4 | VO5 | |
| Low | - | - | | - | STANDBY | STANDBY | STANDBY | STANDBY | STANDBY | STANDBY | |
| High | Low | Low | ı | ı | ON | ON | ON | OFF | OFF | | |
| High | High | Low | - | - | ON | ON | ON | ON | OFF | | |
| High | Low | High | ı | 1 | ON | ON | ON | OFF | ON | | |
| High | High | High | - | - | ON | ON | ON | ON | ON | | |
| High | • | - | Low | Low | ON | ON | ON | | | OFF | |
| High | - | - | High | Low | ON | ON | ON | | | Forward | |
| High | - | - | Low | High | ON | ON | ON | | | Reverse | |
| High | - | - | High | High | ON | ON | ON | | | Brake | |

(1) BTL Driver Control

BTL driver's ON/OFF can control with MUTE123 and MUTE4 terminal.

| | Input | | Output made | VO1(FCS), VO2(TRK), | \/O4/CDDL\ | |
|--------|---------|-------|----------------|---------------------|------------------|--|
| REGRST | MUTE123 | MUTE4 | Output mode | VO3(SLD) | VO4(SPDL) | |
| Low | - | - | STANDBY | Hi-Z | Hi-Z | |
| High | Low | Low | ALL OFF | Hi-Z(M) (Note 1) | Hi-Z(M) (Note 1) | |
| High | High | Low | FCS, TRK, SLD, | ON | Hi-Z(M) (Note 1) | |
| High | Low | High | SPDL ON | Hi-Z(M) (Note 1) | ON | |
| High | High | High | ALL ON | ON | ON | |

(Note 1) V_{VO1+} = V_{VO1-} = V_{PVCC1}/2 [V] (Typ), V_{VO2+} = V_{VO2-} = V_{PVCC1}/2 [V] (Typ)

 $V_{VO3+} = V_{VO3-} = (V_{PVCC2}-0.7)/2 [V] (Typ),$

 $V_{VO4+} = V_{VO4-} = [[(V_{PVCC2}-0.7)/2] \times 15.6 + V_{VCO} \times 20] / (15.6 + 20) [V] (Typ) at Hi-Z(M).$

(Example) $V_{VO4+} = V_{VO4-} \approx 2.53 \text{ [V](Typ)}$ at $V_{PVCC2} = 8 \text{[V]}, V_{VCO} = 1.65 \text{[V]}$

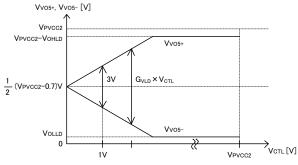
(2) Loading Driver

Only VCTL, FWD, and RVS terminal individually controls the load. (This is not controlled by turning ON/OFF the MUTE123 and MUTE4 terminal) It operates according to the truth table below

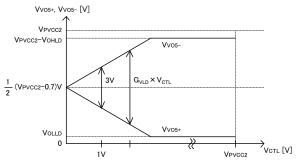
| op o. a.co | operates associating to the train table below. | | | | | | | | | |
|------------|--|---|---|---------|--|-----------------------------|-----------------------------|--|--|--|
| REGRST | Input EEGRST VCTL(Pin18) FWD(Pin19) RVS(Pin20) | | | | Voltage between outputs | VO5+(Pin14) | VO5-(Pin15) | | | |
| Low | - | - | - | STANDBY | 0 | Hi-Z | Hi-Z | | | |
| High | (Note 2) | L | L | OFF | 0 | Hi-Z(M) ^(Note 3) | Hi-Z(M) ^(Note 3) | | | |
| High | (Note 2) | Н | L | Forward | $G_{\text{VLD}} \times V_{\text{CTL}}$ | Н | L | | | |
| High | (Note 2) | L | Н | Reverse | G _{VLD} x V _{CTL} | L | Н | | | |
| High | (Note 2) | Н | Н | Brake | 0 | M (Note 4) | M (Note 4) | | | |

(Note 2) VCTL (Pin18) is an arbitrary value of 0- REG5 (= 5.0[V](Typ)).

(Note 3) $V_{VO5+} = V_{VO5-} = (V_{PVCC2}-0.7)/2[V]$ (Typ) at Hi-Z(M). (Note 4) $V_{VO5+} = V_{VO5-} = (V_{PVCC2}-0.7)/2[V]$ (Typ) at M.

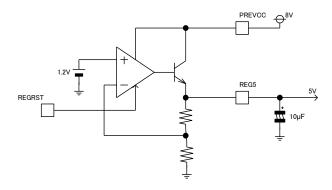


When Forward mode is set



When Reverse mode is set

(3) 5V Regulator 1

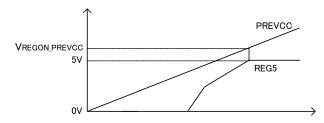


(a) Regulator 1 Control

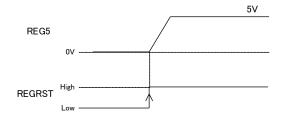
ON/OFF of regulator 1 can be controlled by REGRST terminal.

| REGRST | Regulator 1 | | |
|--------|-------------|--|--|
| Low | OFF | | |
| High | ON | | |

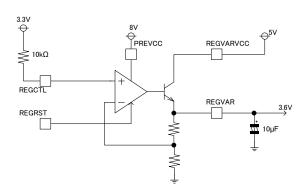
(b) Vcc - Vout Characteristic



(c) Timing Chart



(4) 3.6V Changeable Regulator 2

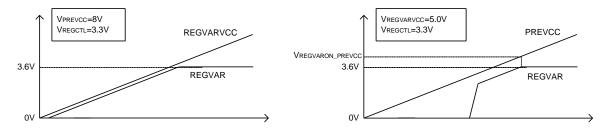


(a) Regulator 2 Controls

ON/OFF of regulator 2 can be controlled by REGRST terminal.

| REGRST | Regulator 2 | | |
|--------|-------------|--|--|
| Low | OFF | | |
| High | ON | | |

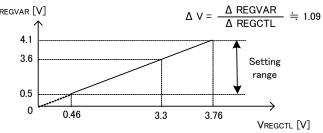
(b) Vcc - Vout Characteristics



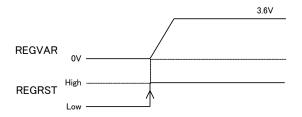
(c) VREGCTL - VOUT Characteristic

REGVAR can be set through REGCTL terminal.

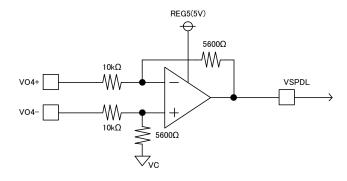
The range of REGVAR of the output voltage setting is 0.5-4.1V (At VREGVARVCC=5V (Typ)).



(d) Timing Chart

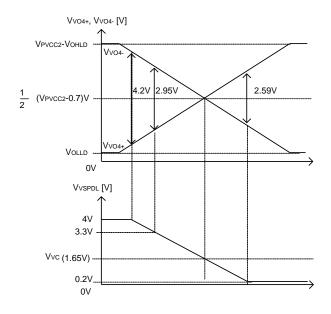


(5) OPAMP for the Voltage Detection between Driver Outputs



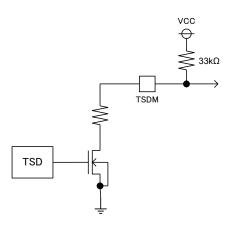
The voltage difference between VO4+, VO4- of the BTL driver for VSPDL is measured and outputted to VSPDL terminal.

$$V_{VSPDL} = \frac{5600}{10k} \ \left(V_{VO4-} - V_{VO4+} \right) + V_{VC}$$



(6) Thermal Shutdown Flag Output Function TSDM = Hi-Z (normal operation)

When thermal shutdown is activated, TSDM terminal becomes Low, all driver outputs (VO1-VO5) and regulator outputs (REG5, REGVAR) are turned OFF (output Hi-Z).



| Thermal shutdown | TSDM |
|------------------|------|
| OFF | Hi-Z |
| ON | Low |

(7) Power Supply Drop Mute and VC Drop Mute Function

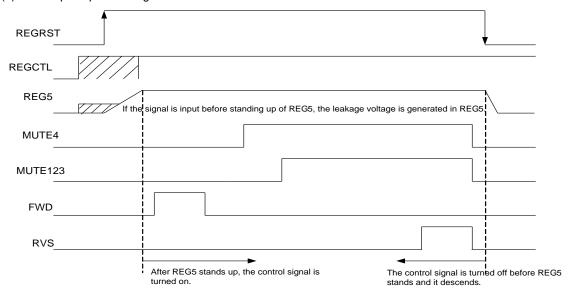
Power supply drop mute functions at VPREVCC<VMPREVCC(3.8V Typ). At this condition all driver outputs (VO1-VO5) are turned OFF (output Hi-Z).

VC drop mute functions at V_{VCO}<V_{MVCO}(0.7V Typ). At this condition driver outputs (VO1-VO4) also are turned OFF (output Hi-Z).

Mute function list (REGRST=MUTE123=MUTE4=FWD=High at the mode state of turning ON)

| THE TOTAL PROPERTY. | t (120101-10012120-100121-11011 at the mode date of tarning on) | | | | | | | | |
|---------------------|---|---------------------|-------------|------------|-----|--|--|--|--|
| Thermal shutdown | PREVCC | VCO | REG5,REGVAR | VO1 to VO4 | VO5 | | | | |
| OFF | > V _{MPREVCC} | > V _{MVCO} | ON | ON | ON | | | | |
| ON | - | • | OFF | OFF | OFF | | | | |
| OFF | < V _{MPREVCC} | - | ON | OFF | OFF | | | | |
| OFF | > V _{MPREVCC} | < V _{MVCO} | ON | OFF | ON | | | | |

(8) Start-up Sequence Regulations



Terminal \times where the destination of hanging the diode on the power supply side is REG5 must defend the above-mentioned sequence so as not to impress the voltage more than the voltage of REG5 terminal.

Please insert in the cereal and use the limit resistance for the terminal when you impress the voltage more than the voltage of REG5 terminal.

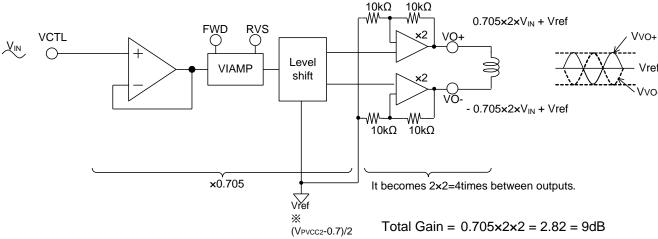
(Limit resistance 10kO or more is inserted in the cereal about REGCTL terminal.)

(Limit resistance 10kO or more is inserted in the cereal about REGCTL terminal. **Terminal where destination of hanging diode on power supply side is REG5

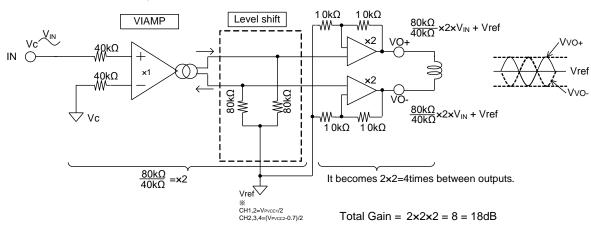
REGCTL, MUTE123, MUTE4, VCI, RVS, FWD, IN1, IN2, IN3, IN4, OPIN+, OPIN-, VCTL

Method of Calculating Gain

(a) Loading



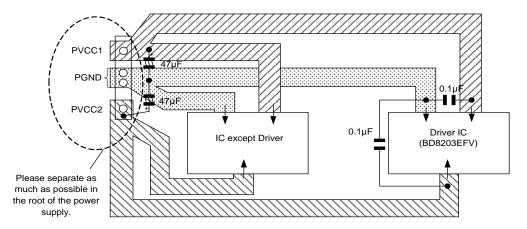
(b) Focus, Tracking, Sled, Spindle



- Noise Measures
 - The cause of PWM driver's noise is the following.
 - A. Noise from VCC and GND line
 - B. Radiation noise

Measures of A

- ① Because a high current is generated by the PWM, Lower wiring impedance at driver's power supply (PVCC) and GND line (PGND) is recommended. This can be achieved by separating the power supply line of other devices from the main supply to eliminate the common impedance, and connecting it to another line.
- ② Use electrolytic capacitor with low ESR to power supply pin (PVCC1, PVCC2, PREVCC) of drivers and GND pin (PGND) to make it stable. Please connect the ceramic capacitor with a high frequency characteristic directly to the pin (or as close as possible to the IC).



3 There is a method of inserting LC filter in the power supply line or GND line, when the first two measures are not sufficient to solve the noise problem.

(Example)

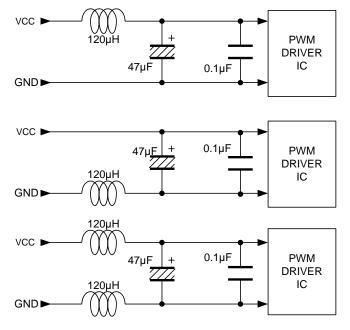


Figure 1. LC Filter Chart

④ In addition, there is a technique of adding a capacitor of about 2200pF (arbitrary capacitance) between each output and GND in the PWM driver. In this case, the wiring for GND must not be common with other signals.

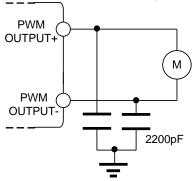
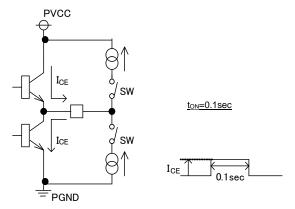
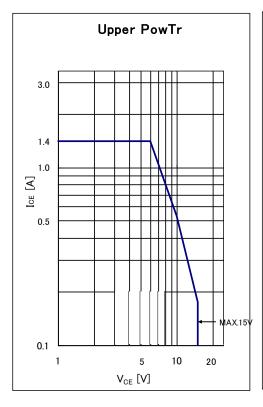


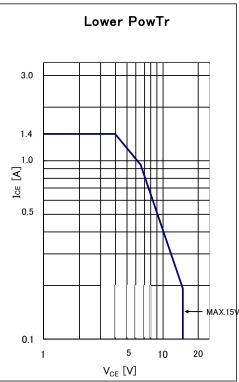
Figure 2. Snubber Circuit

3. ASO

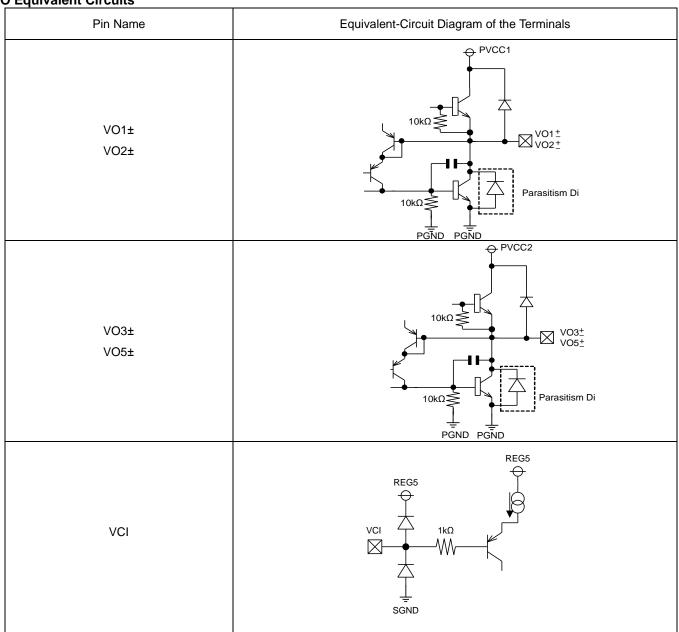
Pin 6 to Pin 15 ASO Data (TON = 0.1sec) $V_{PREVCC} = V_{PVCC1} = V_{PVCC2} = 15V$ $Ta = 25^{\circ}C$



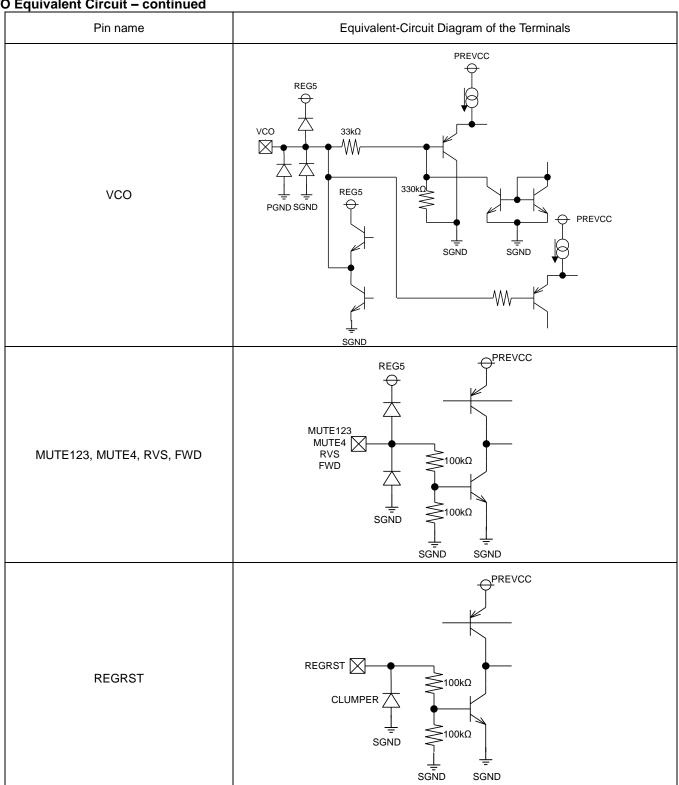




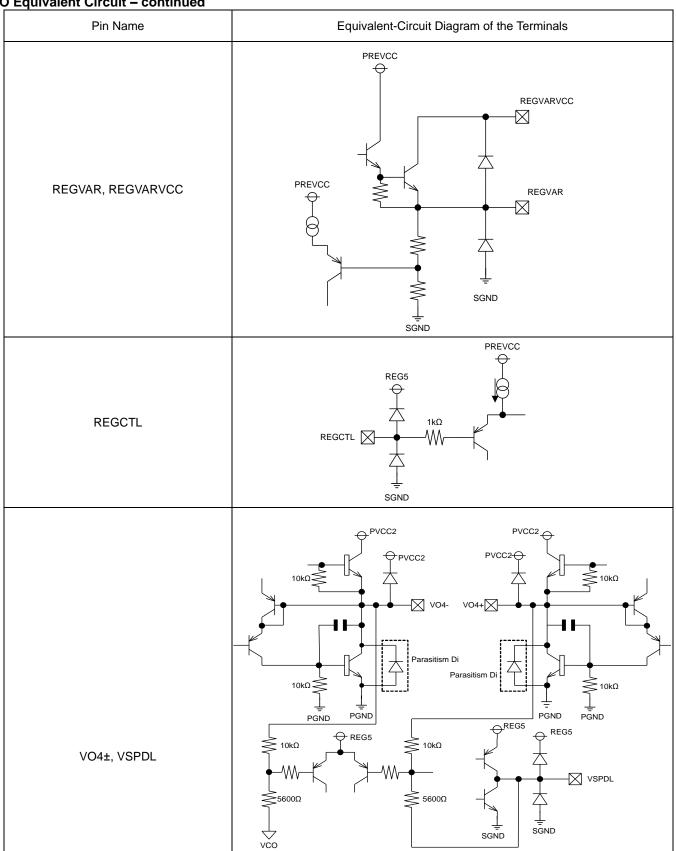
I/O Equivalent Circuits



I/O Equivalent Circuit - continued

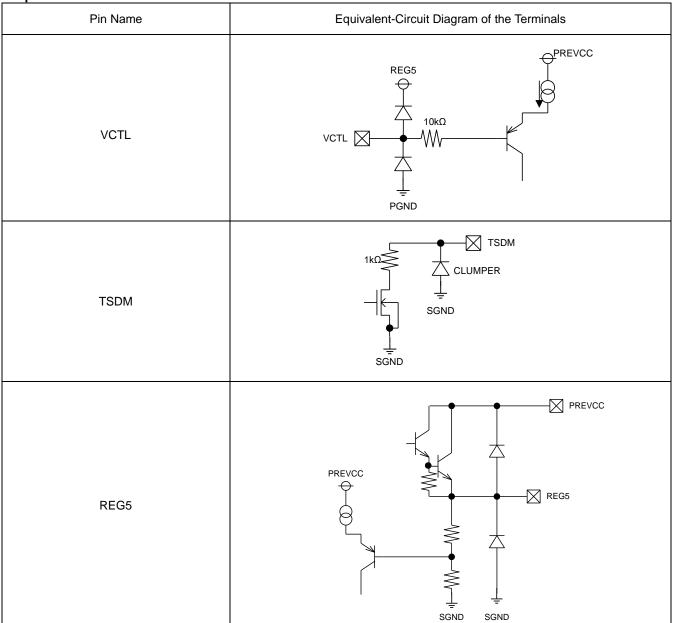


I/O Equivalent Circuit - continued



| Pin Name | Equivalent-Circuit Diagram of the Terminals | |
|--------------|---|--|
| IN1, 2, 3, 4 | PREVCC P | |
| OPIN + - | OPIN+ REG5 SGND REG5 REG5 SGND SGND | |
| OPOUT | REG5 PREG5 OPOUT SGND SGND | |

I/O Equivalent Circuit - continued



(Note) Resistance in the above-mentioned equivalent-circuit diagram of the terminals is 25°C, and a value at typical.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

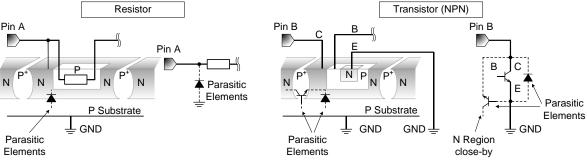


Figure 3. Example of monolithic IC structure

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

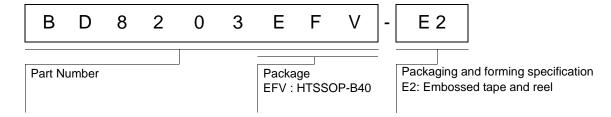
15. Capacitor Between Output and Ground

If a large capacitor is connected between the output pin and ground pin, current from the charged capacitor can flow into the output pin and may destroy the IC when the VCC or IN pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than 0.1 µF between output and ground.

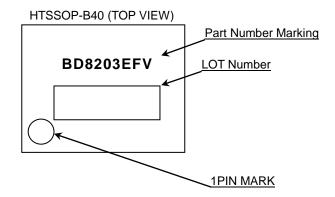
16. About the capacitor between the outputs

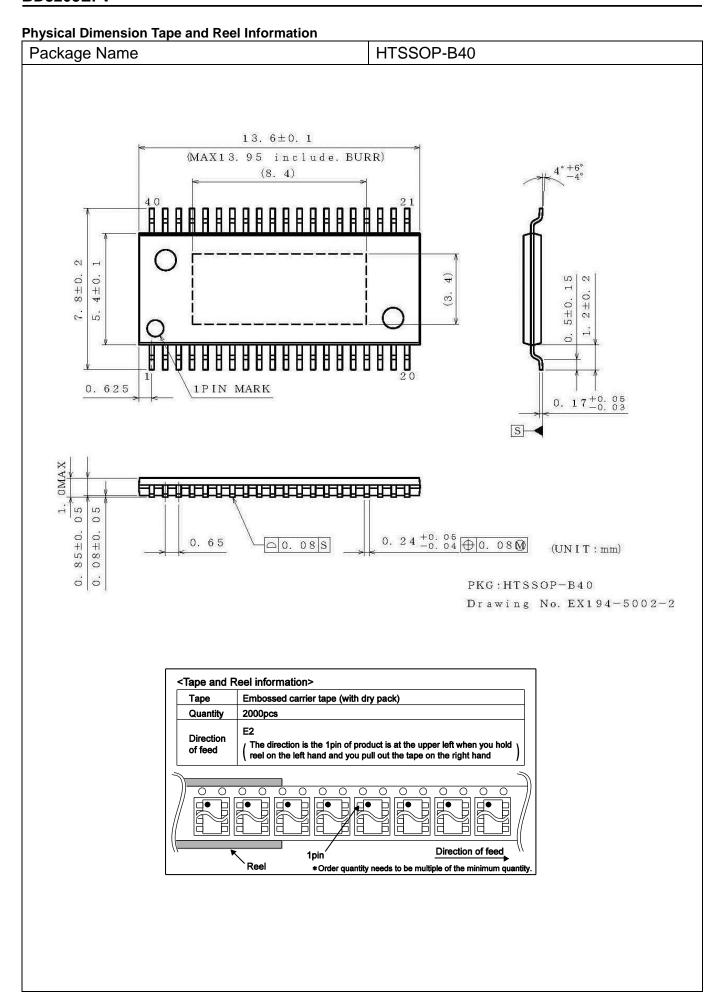
The output current increases with reference to the change between the outputs when the capacitor is connected between the driver outputs. Therefore, please add bypass capacitor $(0.1\mu F)$ as nearest as possible to the power supply (PVCC) and GND(PGND) of this IC as the route of the output current. Please select the value of the capacitor which will have no effect on the IC's normal characteristics, it is possible to pull out capacity at the low temperature happening to the electrolytic capacitor more than the capacity value of the capacitor between the outputs.

Ordering Information



Marking Diagram





Revision History

| Date | Revision | Changes |
|-------------|----------|-------------|
| 04.Nov.2015 | 001 | New Release |

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|---|---------|----------|------------|----------|
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