

1 Channel High Side Switch ICs

# 2.5A Current Limit High Side Switch ICs

## BD82044FVJ

### General Description

BD82044FVJ is a Single Channel High Side Switch IC employing N-channel power MOSFET with low on resistance and low supply current for the power supply line of universal serial bus (USB).

This IC has a built-in over current detection circuit, thermal shutdown circuit, under voltage lockout and soft start circuits.

### Features

- Over-Current Protection : 2.5A
- Control Input Logic : Active-High
- Output Discharge Function
- Reverse Current Protection when Power Switch Off
- Thermal Shutdown
- Open-Drain Fault Flag Output
- Under-Voltage Lockout
- OCP Fast Response
- Soft-Start Circuit
- ESD Protection
- UL : File No.E243261
- IEC 60950-1 CB scheme approval

### Applications

- USB hub in consumer appliances, PC, PC peripheral equipment, and so forth

### Key Specifications

- Input Voltage Range: 2.7V to 5.5V
- ON Resistance: (VIN=5V) 72mΩ(Typ)
- Over Current Threshold: 2.5A
- Standby Current: 0.01μA (Typ)
- Operating Temperature Range: -40°C to +85°C

### Package

TSSOP-B8J

W(Typ) x D(Typ) x H(Max)

3.00mm x 4.90mm x 1.10mm



### Typical Application Circuit

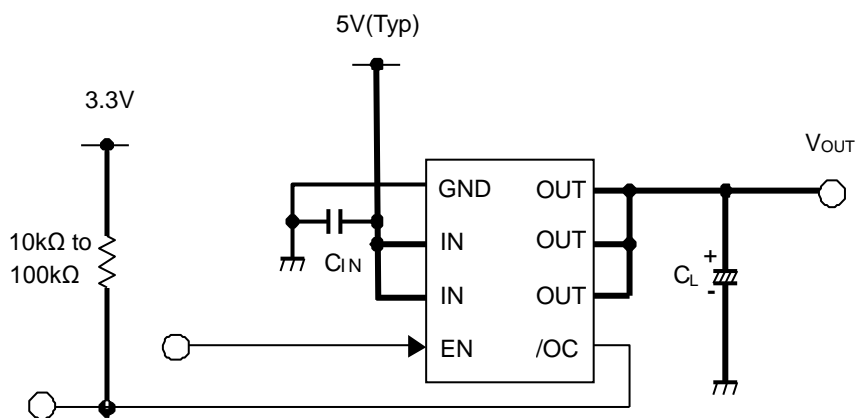
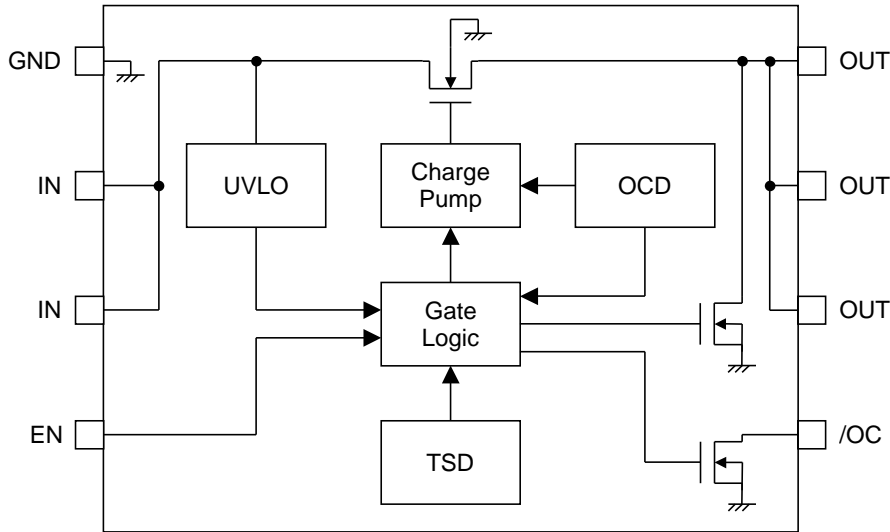


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Block Diagram



Pin Configuration

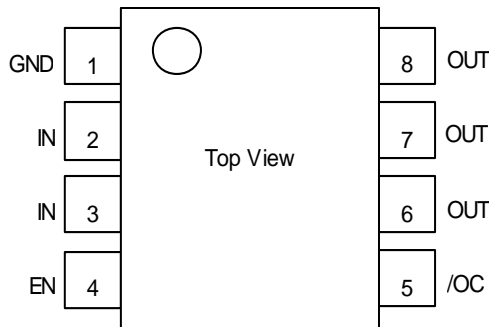


Figure 3. Pin Configuration (TOP VIEW)

Pin Descriptions

Pin No.	Symbol	I/O	Function
1	GND	-	Ground
2, 3	IN	I	Power supply input Input terminal to the power switch and power supply input terminal of the internal circuit Short these pins externally
4	EN	I	Enable input Active high power on switch High level input > 2.0V, Low level input < 0.8V
5	/OC	O	Error flag output Low when over-current or thermal shutdown is activated Open drain output
6, 7, 8	OUT	O	Power switch output Short these pins externally

**Absolute Maximum Ratings**( $T_a=25^{\circ}\text{C}$ )

Parameter	Symbol	Rating	Unit
IN Supply Voltage	$V_{IN}$	-0.3 to +6.0	V
EN Input Voltage	$V_{EN}$	-0.3 to +6.0	V
/OC Voltage	$V_{/OC}$	-0.3 to +6.0	V
/OC Sink Current	$I_{/OC}$	5	mA
OUT Voltage	$V_{OUT}$	-0.3 to +6.0	V
Storage Temperature	$T_{stg}$	-55 to +150	$^{\circ}\text{C}$
Power Dissipation	$P_d$	0.58 (Note 1)	W

(Note 1) Mounted on 70mm x 70mm x 1.6mm glass epoxy board. Reduce 4.7mW per  $1^{\circ}\text{C}$  above  $25^{\circ}\text{C}$

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Recommended Operating Ratings**

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
IN Operating Voltage	$V_{IN}$	2.7	5.0	5.5	V
Operating Temperature	$T_{opr}$	-40	-	+85	$^{\circ}\text{C}$

**Electrical Characteristics** ( $V_{IN}=5\text{V}$ ,  $T_a=25^{\circ}\text{C}$ , unless otherwise specified.)DC Characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Operating Current	$I_{DD}$	-	110	150	$\mu\text{A}$	$V_{EN}=5\text{V}$ , $V_{OUT}=\text{open}$
Standby Current	$I_{STB}$	-	0.01	5	$\mu\text{A}$	$V_{EN}=0\text{V}$ , $V_{OUT}=\text{open}$
EN Input Voltage	$V_{ENH}$	2.0	-	-	V	High input
	$V_{ENL}$	-	-	0.8	V	Low input
EN Input Leakage	$I_{EN}$	-1	0.01	+1	$\mu\text{A}$	$V_{EN}=0\text{V}$ or $5\text{V}$
On Resistance	$R_{ON}$	-	72	90	m $\Omega$	$I_{OUT}=0.5\text{A}$
		-	74	93		$I_{OUT}=1.0\text{A}$
		-	78	98		$I_{OUT}=1.5\text{A}$
		-	84	105		$I_{OUT}=2.0\text{A}$
Reverse Leak Current	$I_{REV}$	-	-	1	$\mu\text{A}$	$V_{OUT}=5.5\text{V}$ , $V_{IN}=0\text{V}$
Over-Current Threshold	$I_{TH}$	2.05	2.50	2.80	A	Current Load Slew rate 100A/s
Short Circuit Output Current	$I_{SC}$	1.20	1.60	2.00	A	$V_{OUT}=0\text{V}$ , $C_L=100\mu\text{F}$ RMS
Output Discharge Resistance	$R_{DISC}$	-	55	100	$\Omega$	$I_{OUT}=1\text{mA}$ , $V_{EN}=0\text{V}$
/OC Output Low Voltage	$V_{/OC}$	-	-	0.4	V	$I_{/OC}=1\text{mA}$
/OC Output Leak Current	$I_{L/OC}$	-	0.01	1	$\mu\text{A}$	$V_{/OC}=5\text{V}$
UVLO Threshold	$V_{TUVH}$	2.1	2.3	2.5	V	$V_{IN}$ increasing
	$V_{TUVL}$	2.0	2.2	2.4	V	$V_{IN}$ decreasing

AC Characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Output Rise Time	$t_{ON1}$	-	0.3	10	ms	$R_L=10\Omega$
Output Turn-on Time	$t_{ON2}$	-	0.5	20	ms	
Output Fall Time	$t_{OFF1}$	-	2	10	$\mu\text{s}$	
Output Turn-off Time	$t_{OFF2}$	-	4	20	$\mu\text{s}$	
/OC Delay Time	$t_{/OC}$	4	7	15	ms	

Measurement Circuit

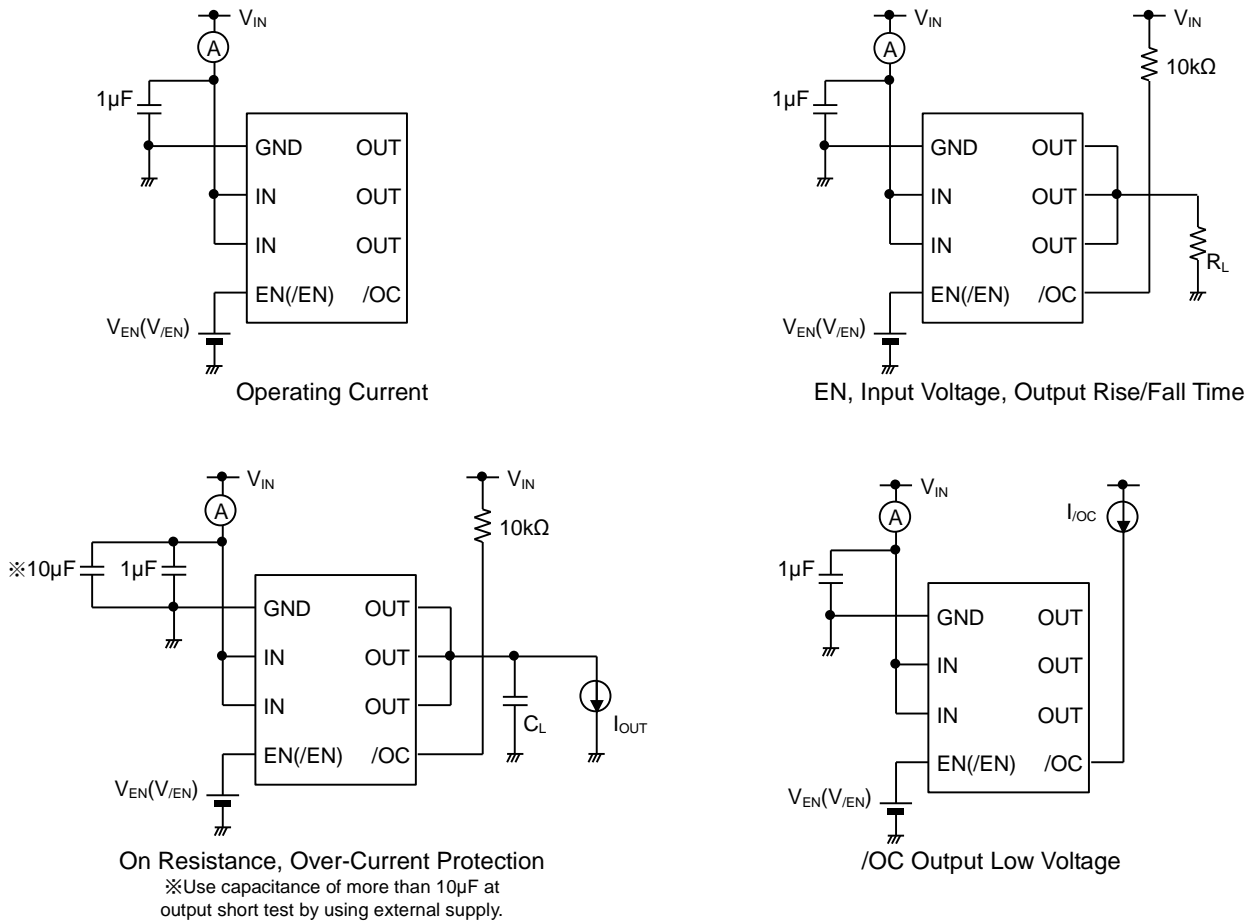


Figure 4. Measurement Circuit

Timing Diagram

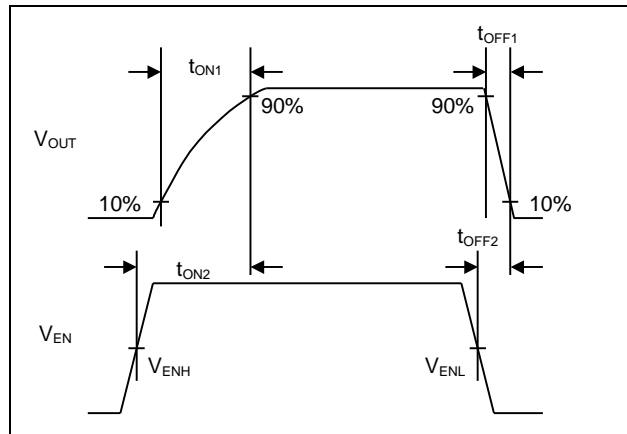


Figure 5. Output Rise/Fall Time

Typical Performance Curves

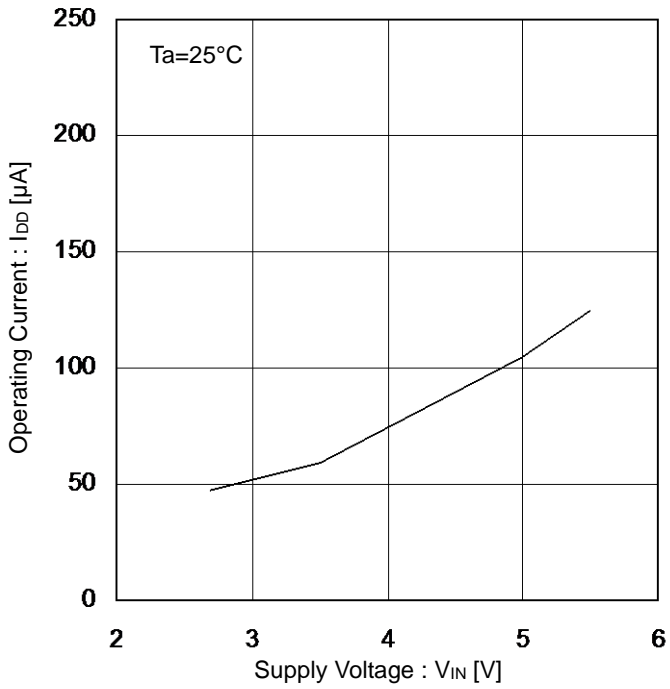


Figure 6. Operating Current vs Supply Voltage  
EN Enable

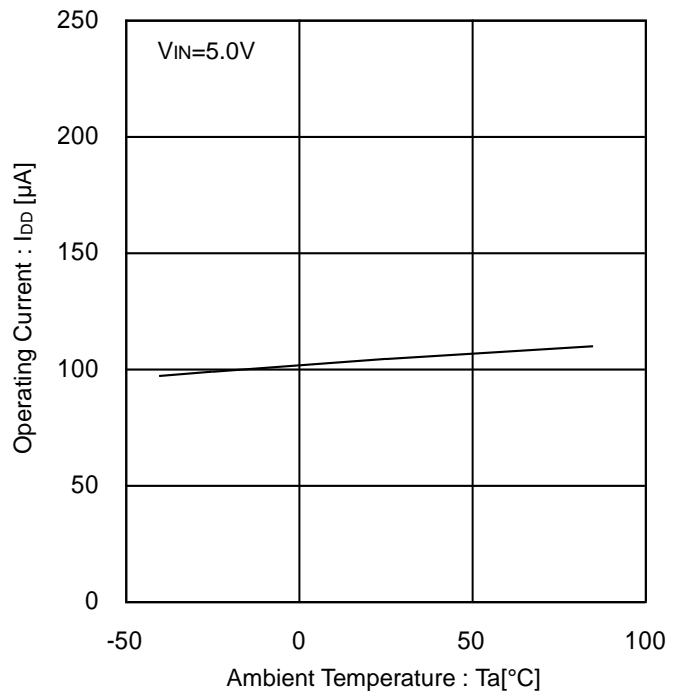


Figure 7. Operating Current vs Ambient Temperature  
EN Enable

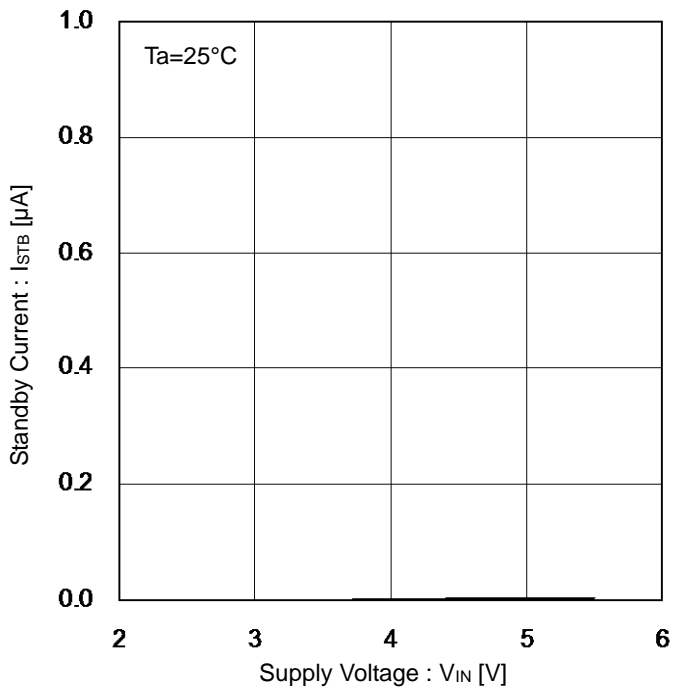


Figure 8. Standby Current vs Supply Voltage  
EN Disable

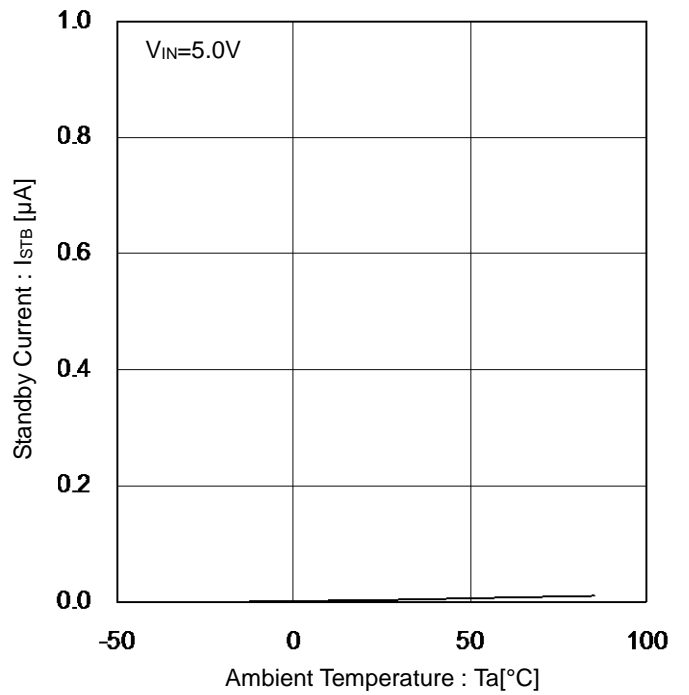


Figure 9. Standby Current vs Ambient Temperature  
EN Disable

Typical Performance Curves - continued

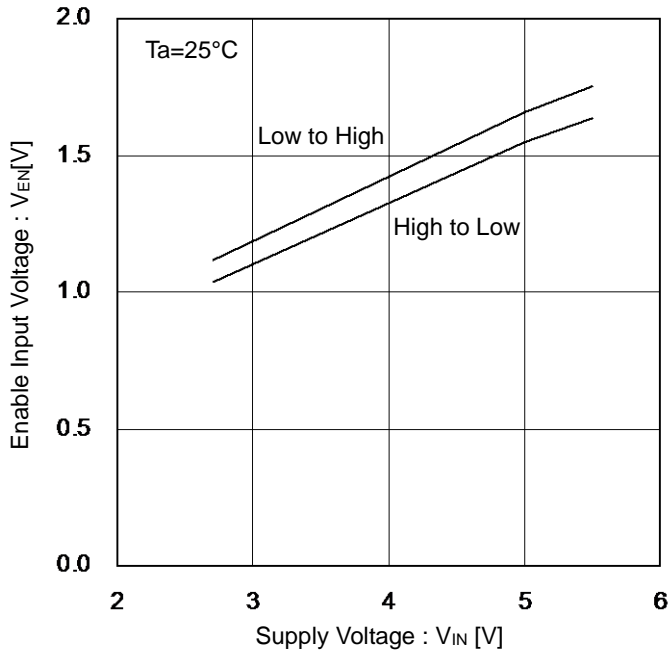


Figure 10. EN Input Voltage vs Supply Voltage

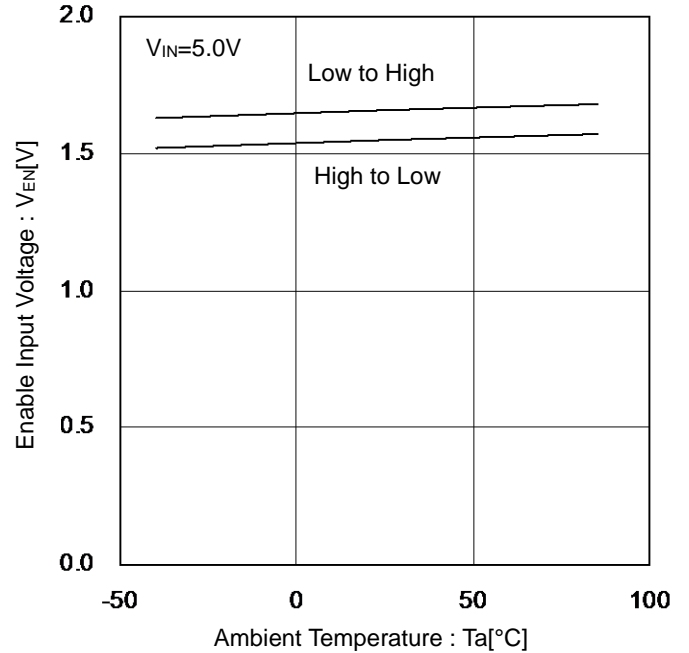


Figure 11. EN Input Voltage vs Ambient Temperature

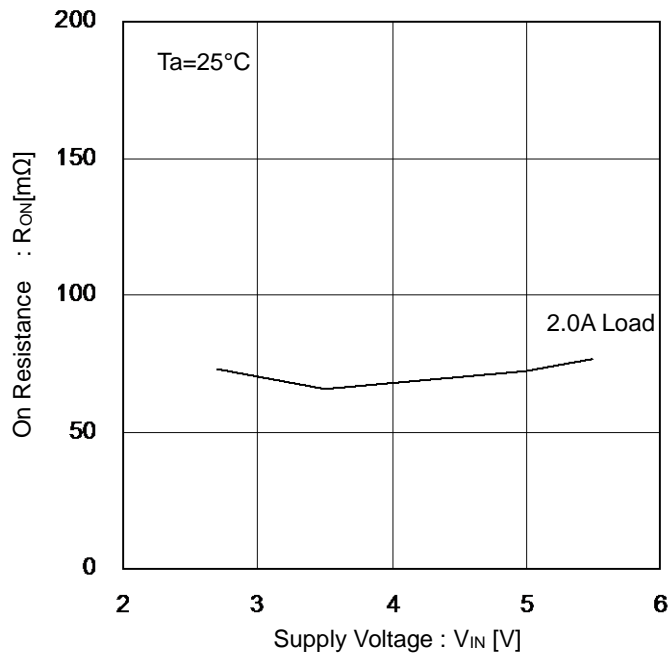


Figure 12. On Resistance vs Supply Voltage

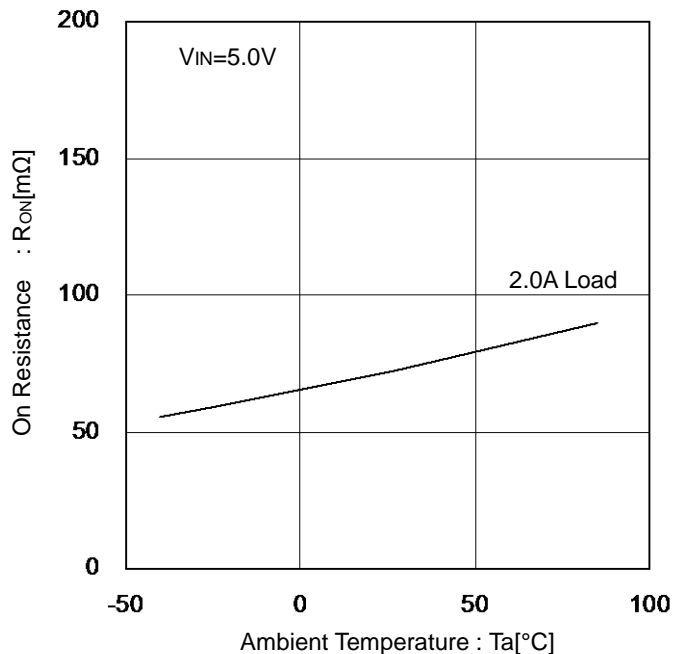


Figure 13. On Resistance vs Ambient Temperature

Typical Performance Curves - continued

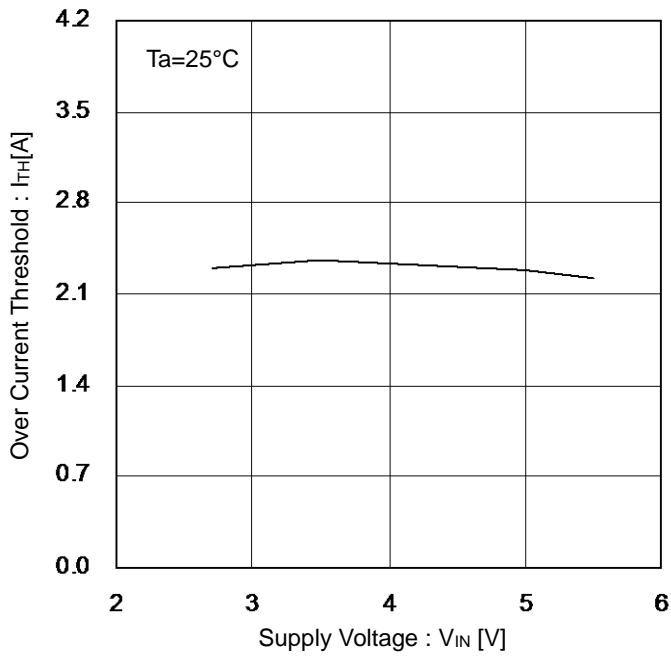


Figure 14. Over-Current Threshold vs Supply Voltage

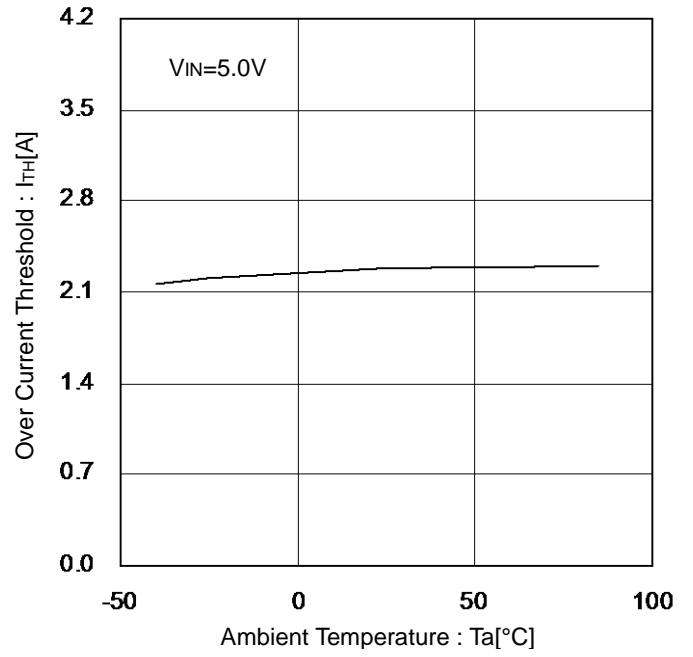


Figure 15. Over-Current Threshold vs Ambient Temperature

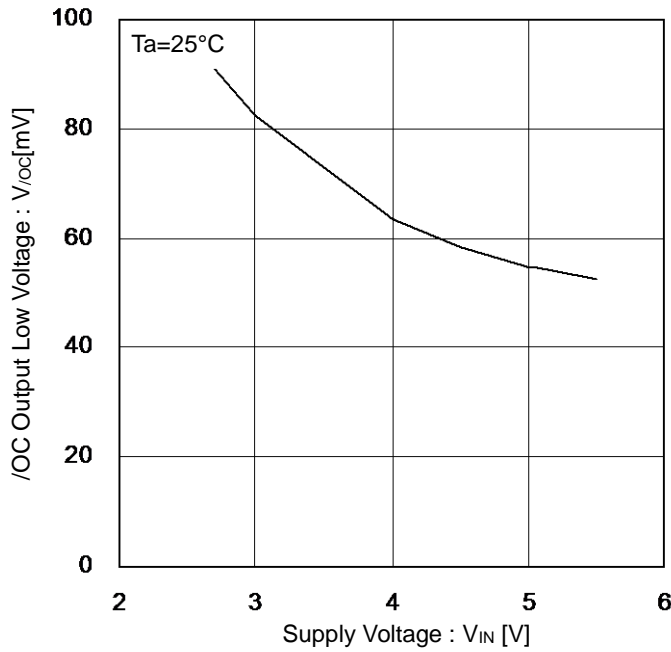


Figure 16. /OC Output Low Voltage vs Supply Voltage

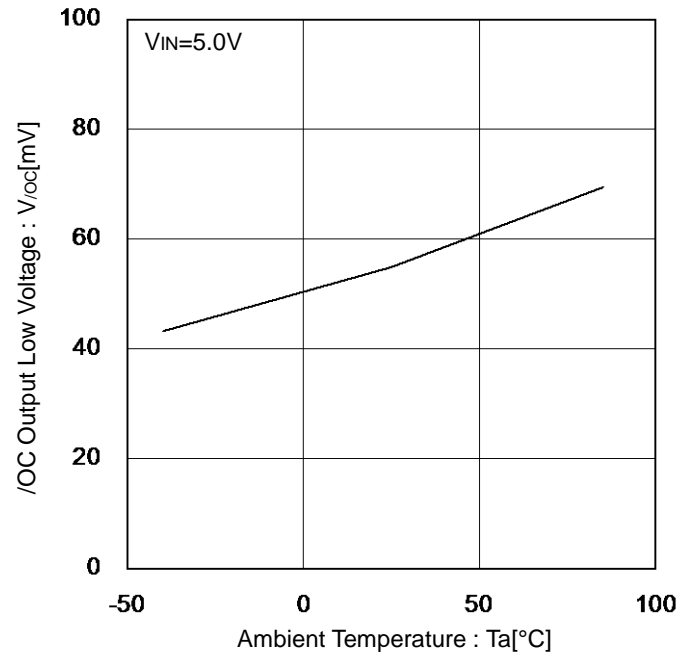


Figure 17. /OC Output Low Voltage vs Ambient Temperature

Typical Performance Curves - continued

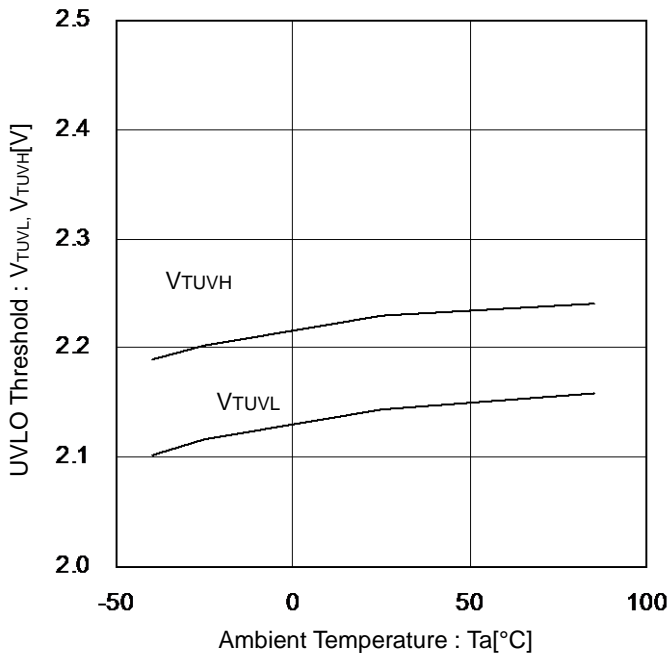


Figure 18. UVLO Threshold vs Ambient Temperature

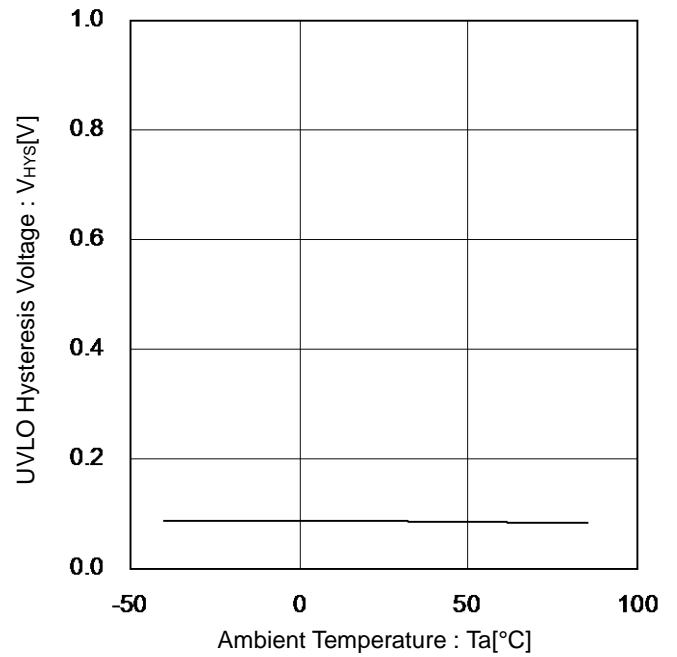


Figure 19. UVLO Hysteresis Voltage vs Ambient Temperature

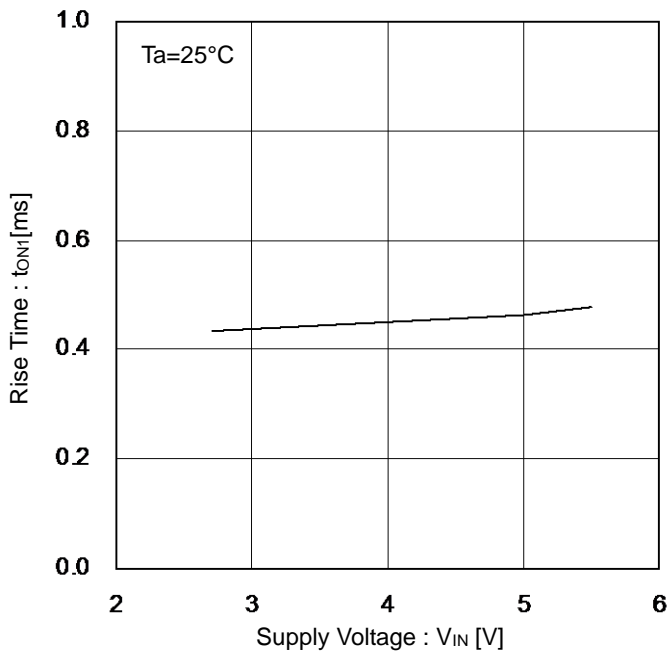


Figure 20. Output Rise Time vs Supply Voltage

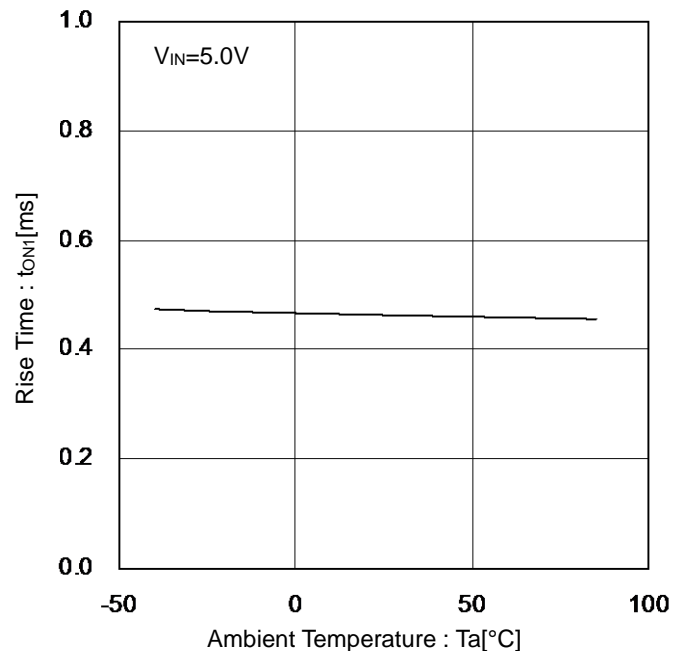


Figure 21. Output Rise Time vs Ambient Temperature



Typical Performance Curves - continued

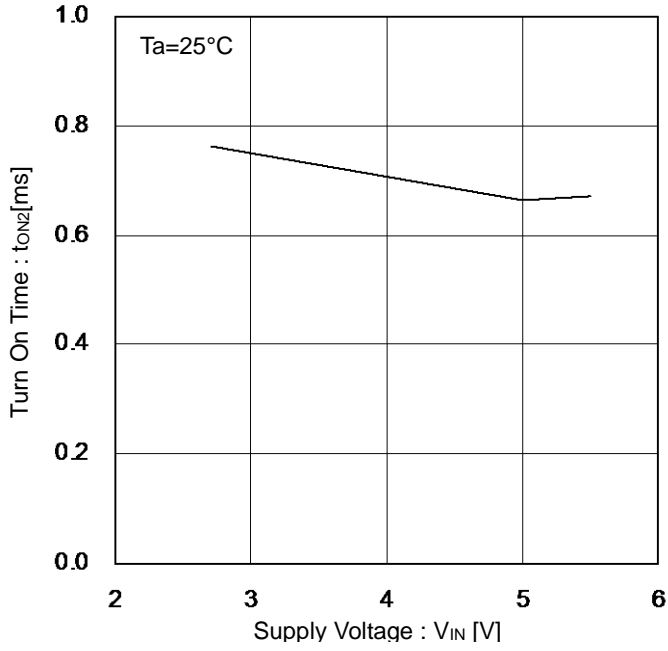


Figure 22. Output Turn-on Time vs Supply Voltage

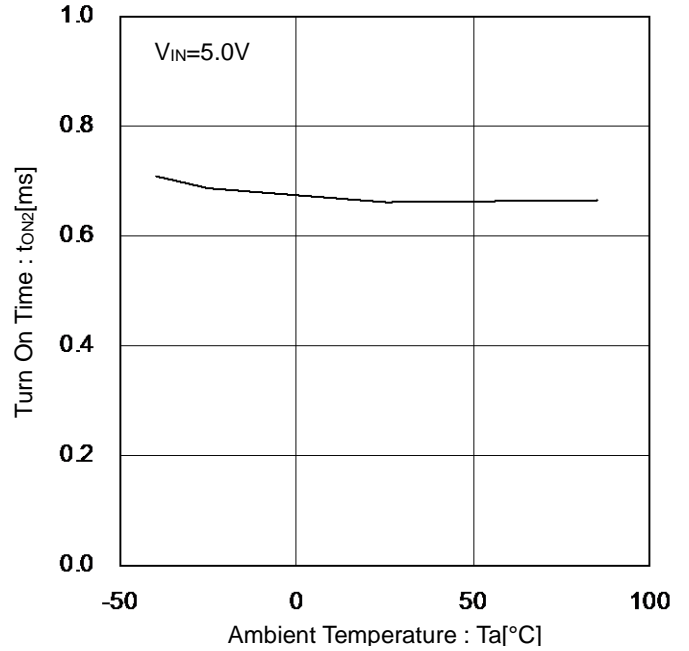


Figure 23. Output Turn-on Time vs Ambient Temperature

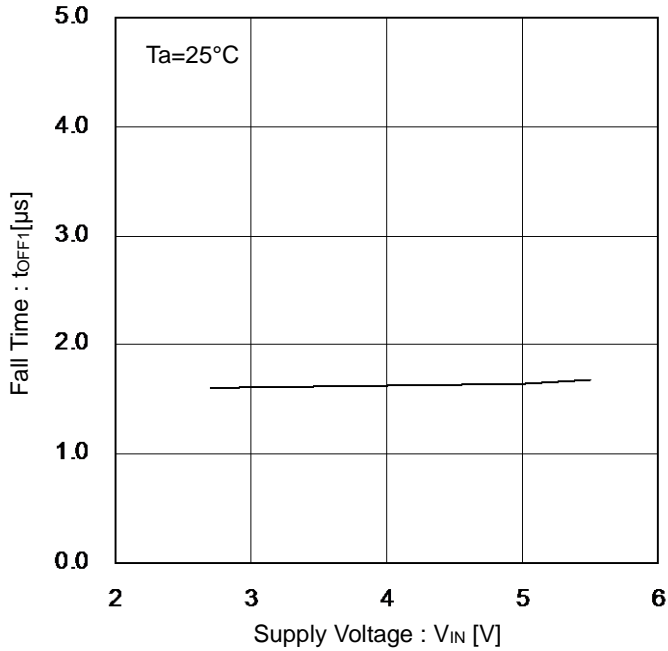


Figure 24. Output Fall Time vs Supply Voltage

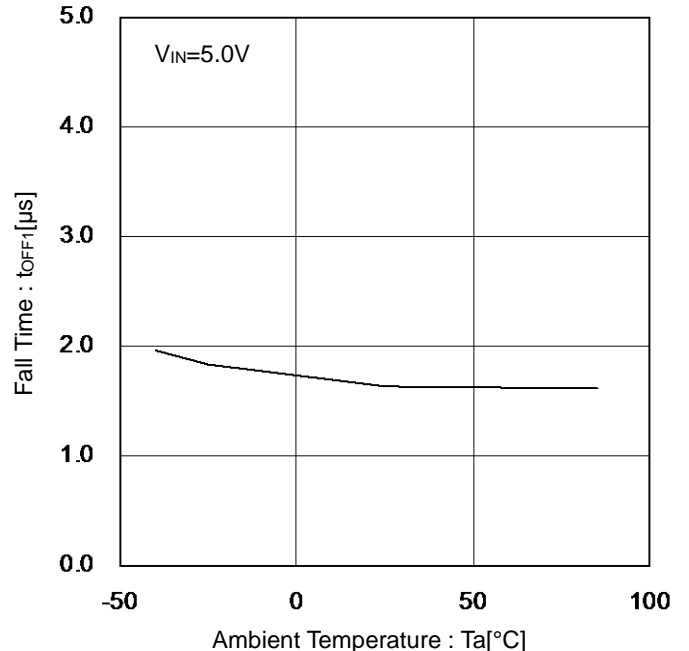


Figure 25. Output Fall Time vs Ambient Temperature

Typical Performance Curves - continued

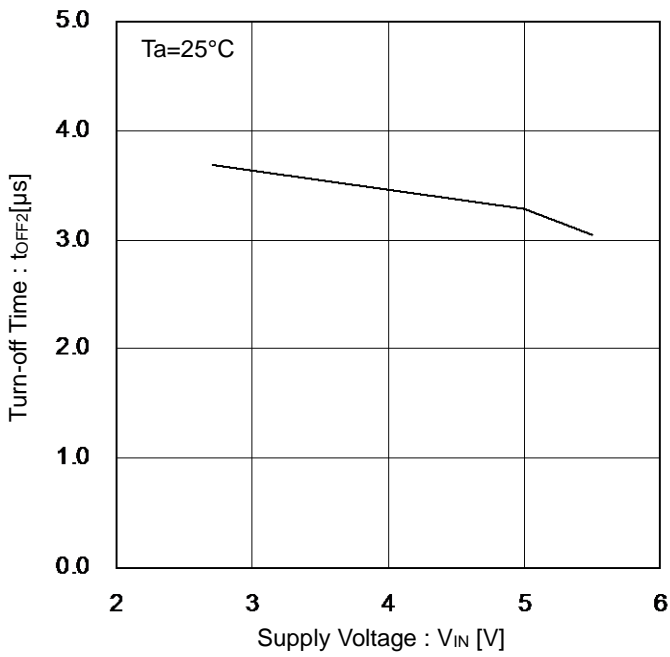


Figure 26. Output Turn-off Time vs Supply Voltage

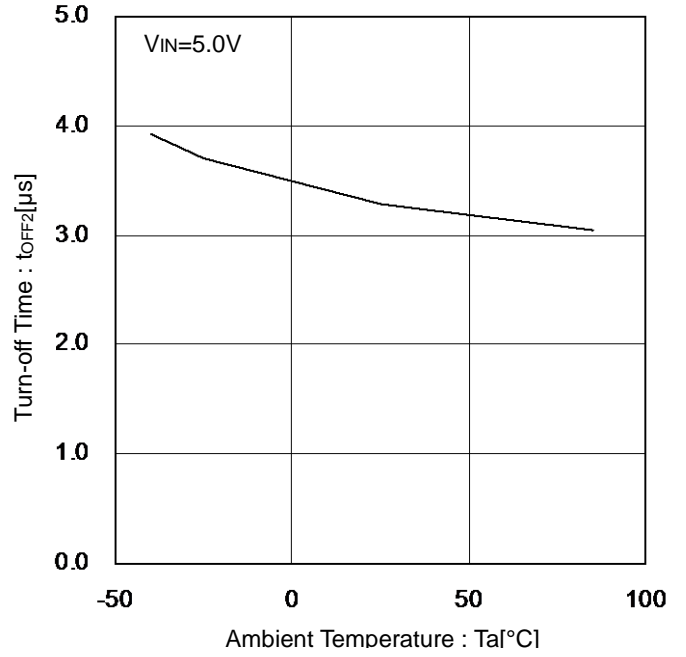


Figure 27. Output Turn-off Time vs Ambient Temperature

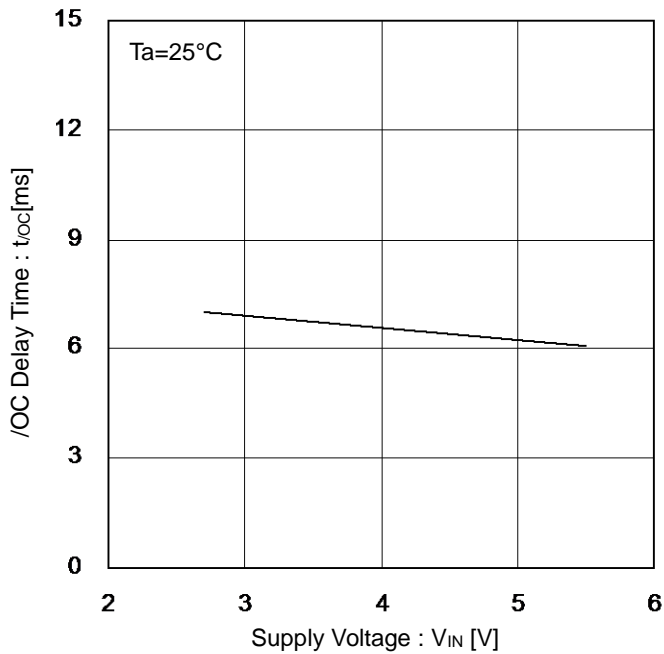


Figure 28. /OC Delay Time vs Supply Voltage

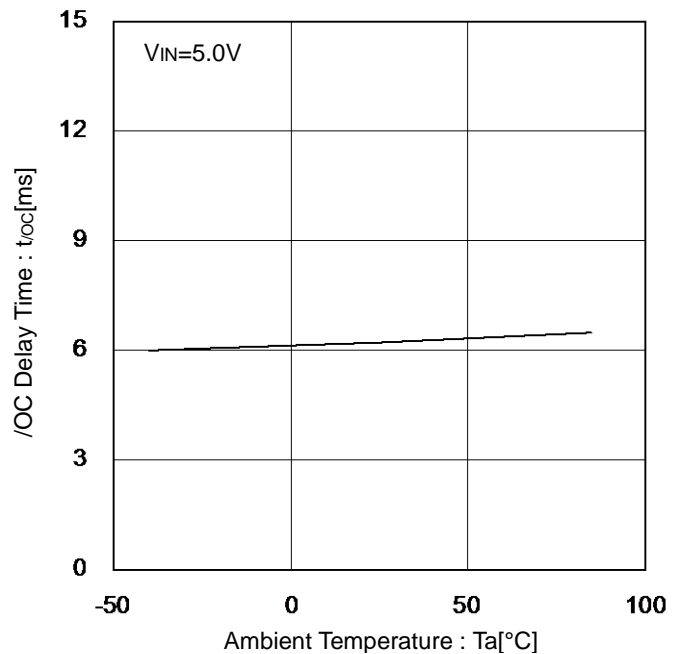


Figure 29. /OC Delay Time vs Ambient Temperature

Typical Performance Curves - continued

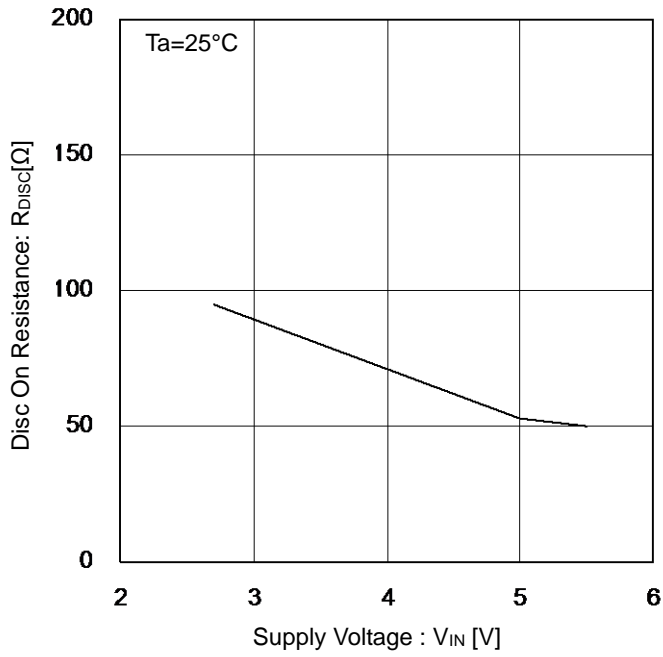


Figure 30. Discharge On Resistance vs Supply Voltage

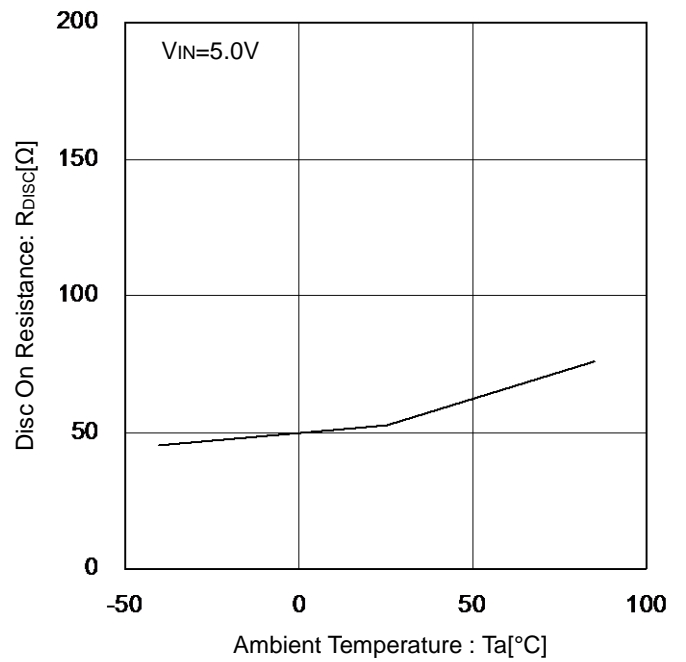
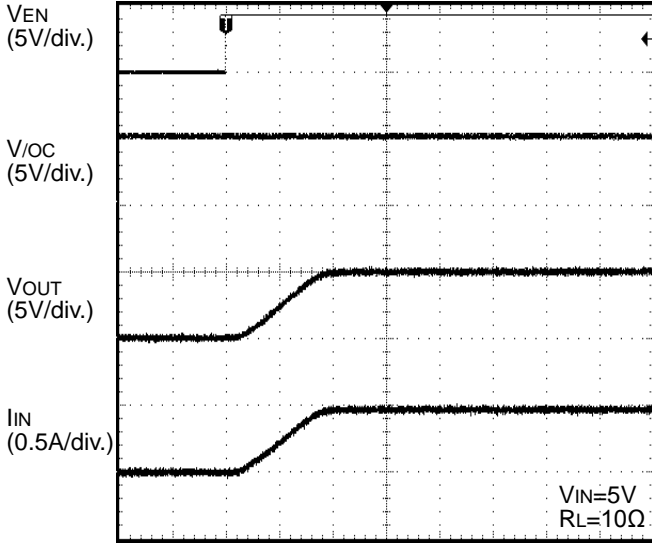
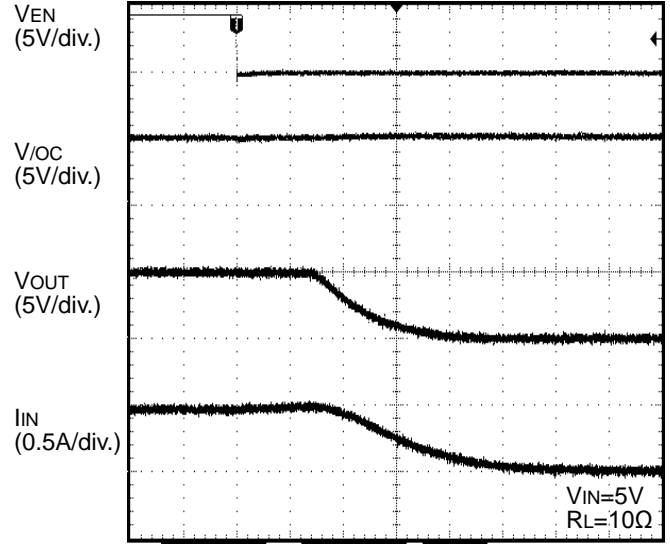


Figure 31. Discharge On Resistance vs Ambient Temperature

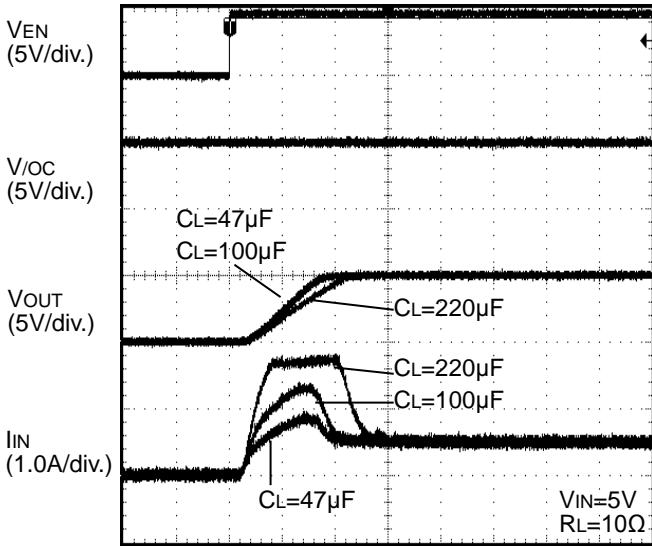
Typical Wave Forms (BD82044FVJ)



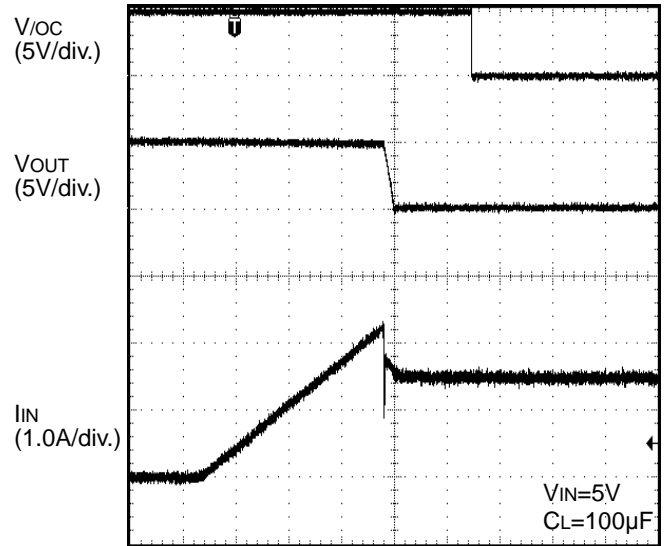
TIME(0.4ms/div.)  
Figure 32. Output Rise Characteristic



TIME(1μs/div.)  
Figure 33. Output Fall Characteristic

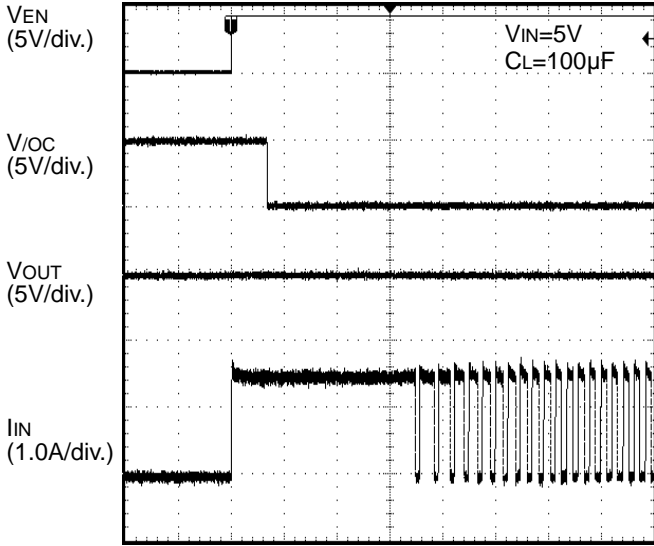


TIME(0.4ms/div.)  
Figure 34. Inrush Current Response

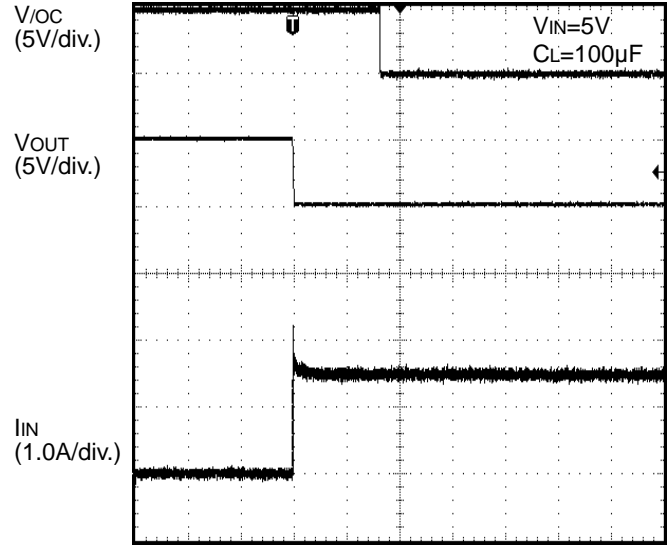


TIME(4ms/div.)  
Figure 35. Over-Current Response Ramped Load

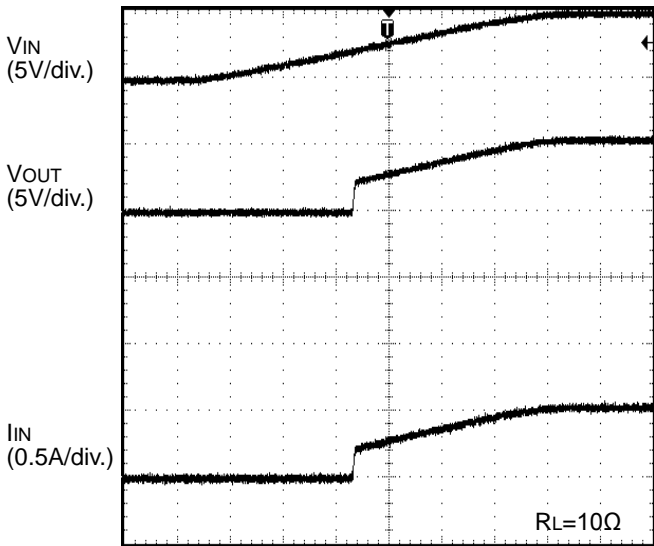
Typical Wave Forms (BD82044FVJ)



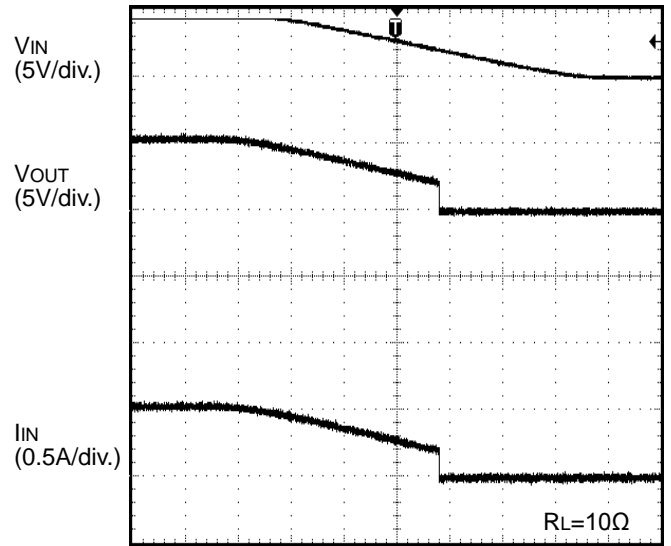
TIME(10ms/div.)  
Figure 36. Over-Current Response  
Enable to Shortcircuit



TIME(4ms/div.)  
Figure 37. Over-Current Response  
1ΩLoad Connected at Enable



TIME(10ms/div.)  
Figure 38. UVLO Response  
Increasing  $V_{IN}$



TIME(10ms/div.)  
Figure 39. UVLO Response  
Decreasing  $V_{IN}$

## Typical Application Circuit

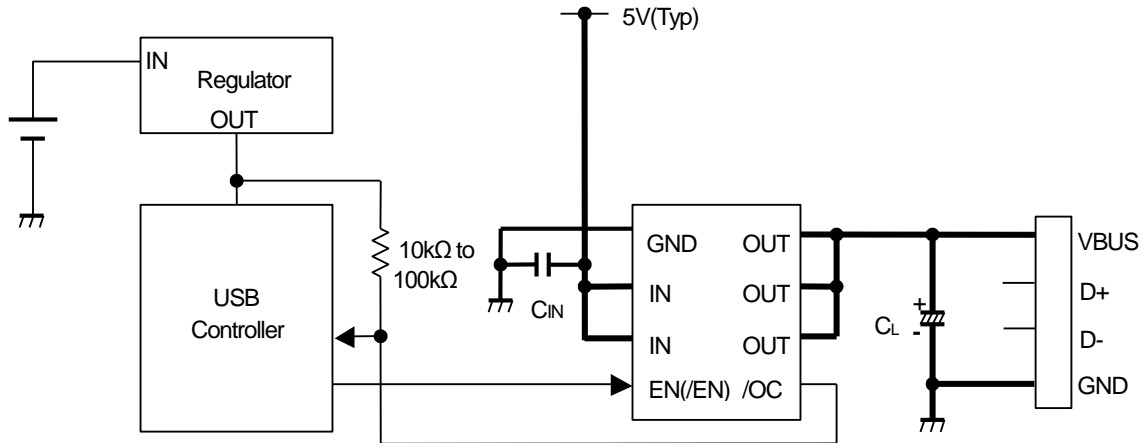


Figure 40. Typical Application Circuit

## Application Information

IN terminal supply internal circuit of IC and input of power switch. Therefore ringing of power line causes bad influences on IC operations. In order to avoid this case, it is recommended to connect a low ESR bypass capacitor (1 $\mu$ F or higher) as close to between IN and GND terminal as possible. When excessive current flows due to output short-circuit or so, ringing occurs because of inductance between power source line to IC may exert a bad influence upon IC. In order to decrease voltage fluctuations from power source line to IC, connect a low ESR capacitor in parallel with C<sub>IN</sub>. 10 $\mu$ F to 100 $\mu$ F or higher is effective.

Pull up /OC output by resistance 10k $\Omega$  to 100k $\Omega$ .

Set up a value for C<sub>L</sub> which satisfies the application.

This system connection diagram does not guarantee operation as the intended application.

When using the circuit with changes to the external circuit values, make sure to leave an adequate margin for external components including static and transitional characteristics as well as the design tolerance of the IC.

## Functional Description

### 1. Switch Operation

IN terminal and OUT terminal are connected to the drain and the source of switch MOSFET respectively. The IN terminal is also used as power source input to internal control circuit.

When the switch is turned on from EN control input, the IN terminal and OUT terminal are connected by a 72m $\Omega$ (Typ) switch. In ON status, the switch is bidirectional. Therefore, when the potential of OUT terminal is higher than that of the IN terminal, current flows from OUT terminal to IN terminal.

Since the parasitic diode between the drain and the source of switch MOSFET is canceled, current flow from OUT to IN is prevented during off state. Output Discharge Function operates at off state.

### 2. Thermal Shutdown Circuit (TSD)

If over current would continue, the temperature of the IC would increase drastically. If the junction temperature reaches beyond 135 $^{\circ}$ C(Typ) during the condition of over-current detection, thermal shutdown circuit operates and turns power switch off and outputs error flag (/OC). Then, when the junction temperature decreases below 115 $^{\circ}$ C(Typ), power switch is turned on and error flag (/OC) is cancelled. Unless the cause of the increase of the chip's temperature is removed or the output of power switch is turned off, this operation repeats.

The thermal shutdown circuit operates when the switch is on (EN signal is active).

### 3. Over Current Detection (OCD)

The over current detection circuit (OCD) limits current (I<sub>sc</sub>) and outputs error flag (/OC) when current flowing in each switch MOSFET exceeds a specified value. There are three cases when the OCD circuit is activated. The OCD operates when the switch is on (EN signal is active).

- (1) When the switch is turned on while the output is in short-circuit status, the switch gets in current limit status immediately.
- (2) When the output short-circuits or when high current load is connected while the switch is on, very large current will flow until the over-current limit circuit reacts. When this happens, the over-current limit circuit is activated and the current limitation is carried out.
- (3) When the output current increases gradually, current limitation does not work until the output current exceeds the over-current detection value. When it exceeds the detection value, current limitation is carried out.

#### 4. Under-Voltage Lockout (UVLO)

UVLO circuit prevents the switch from turning on until  $V_{IN}$  exceeds 2.3V(Typ). If  $V_{IN}$  drops below 2.2V(Typ) while the switch is still on, then the UVLO will shut off the power switch. UVLO has a hysteresis of 100mV(Typ).

Under-voltage lockout circuit works when the switch is on (EN signal is active). And While UVLO works, Output Discharging Function operates.

#### 5. Error Flag (/OC) Output

Error flag output is an N-MOS open drain output. Upon detection of over current or thermal overrun, the output level becomes low.

Over current detection has a delay filter. This delay filter prevents current detection flags from being sent during instantaneous events such as surge current due to switching or hot plug. If fault flag output is unused, /OC pin should be connected to open or ground line.

#### 6. Output Discharge Function

When the switch is turned off from disable control input or UVLO function, the 55Ω(Typ.) discharge circuit between OUT and GND turns on. By turning on this switch, electric charge at capacitive load is discharged. But when the voltage of IN declines extremely, then the OUT pin becomes Hi-Z without UVLO function.

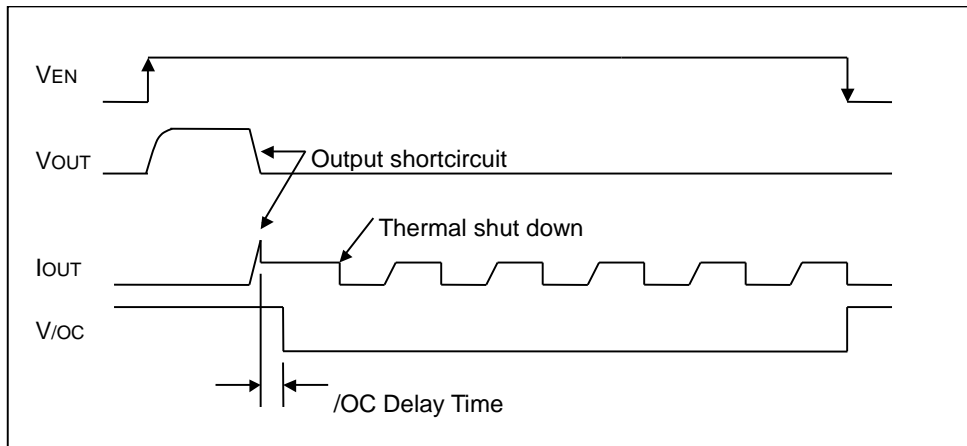


Figure 41. Over-Current Detection, Thermal Shutdown Timing.

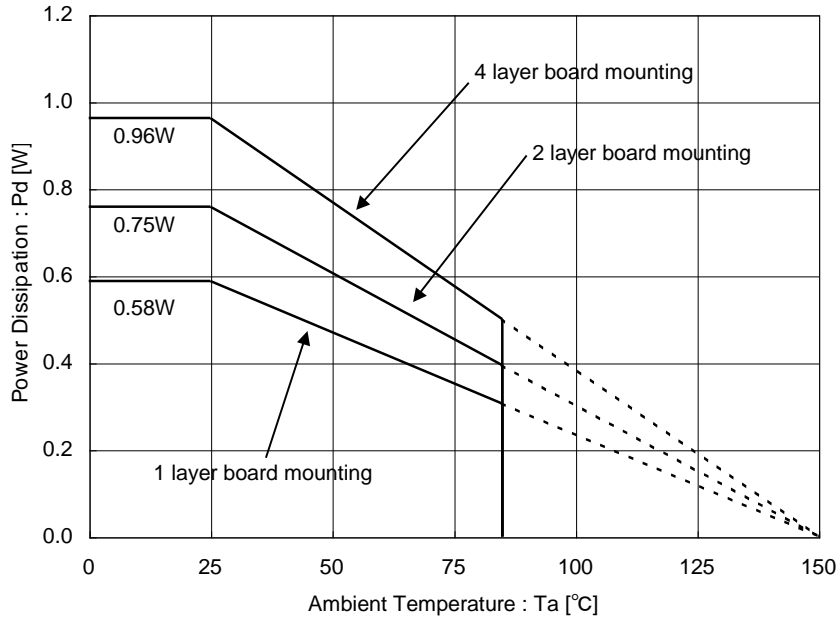
**Power Dissipation**

The power dissipation depends on output load, ambient temperature and PCB layout. The device has current capacity of 2.0A. Power dissipation can be calculated using the output current and the RON of the power switch as below.

$$P_d = R_{ON} \times I_{OUT}^2$$

The derating curve is shown below

TSSOP-B8J(MSOP-8 JEDEC standard)



Note: IC is Mounted on 70mmx70mmx1.6mm glass-epoxy PCB.

Derating is 4.7mW/°C above Ta=25°C(when 1layer board mounting).

Figure 42. Power Dissipation Curve (Pd-Ta Curve)

**I/O Equivalent Circuit**

Symbol	Pin No.	Equivalent Circuit
EN	4	
/OC	5	
OUT	6,7,8	



## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes - continued

## 12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin\ A$  and  $GND > Pin\ B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin\ B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

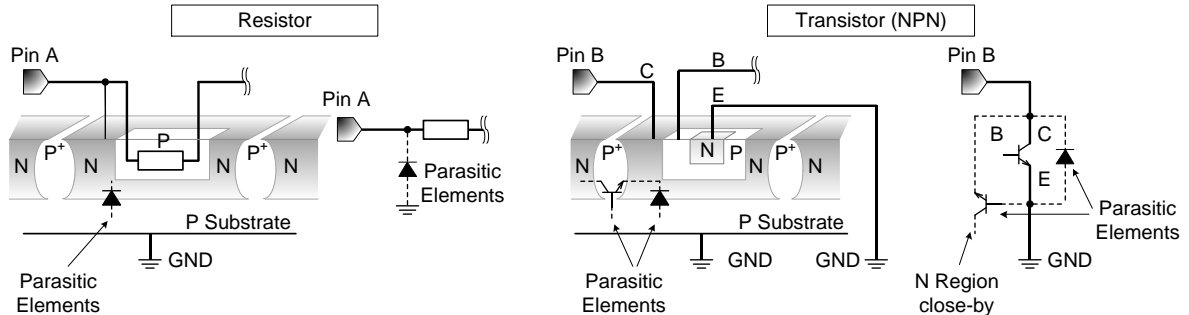


Figure 43. Example of monolithic IC structure

## 13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

## 14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF all output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

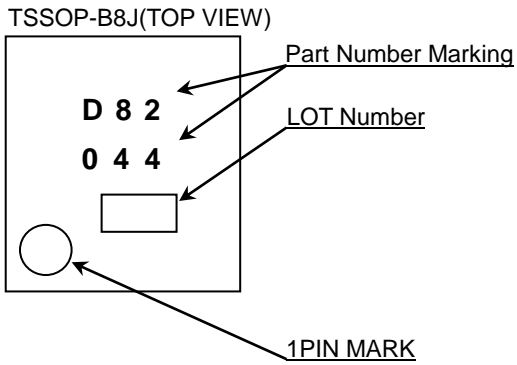
## 15. Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation ( $P_d$ ) in actual states of use.

Ordering Information

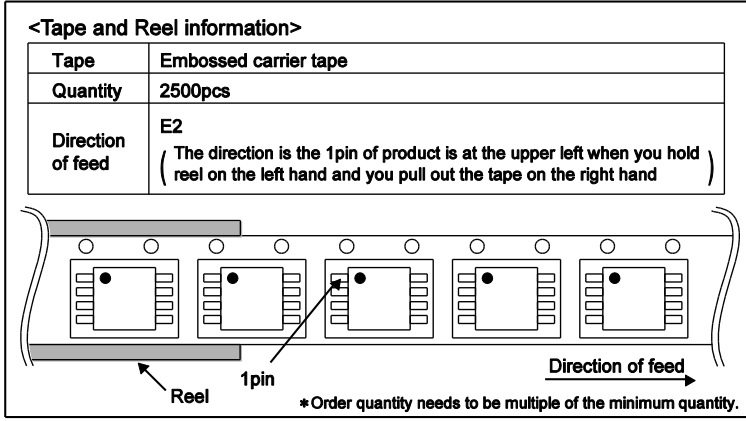
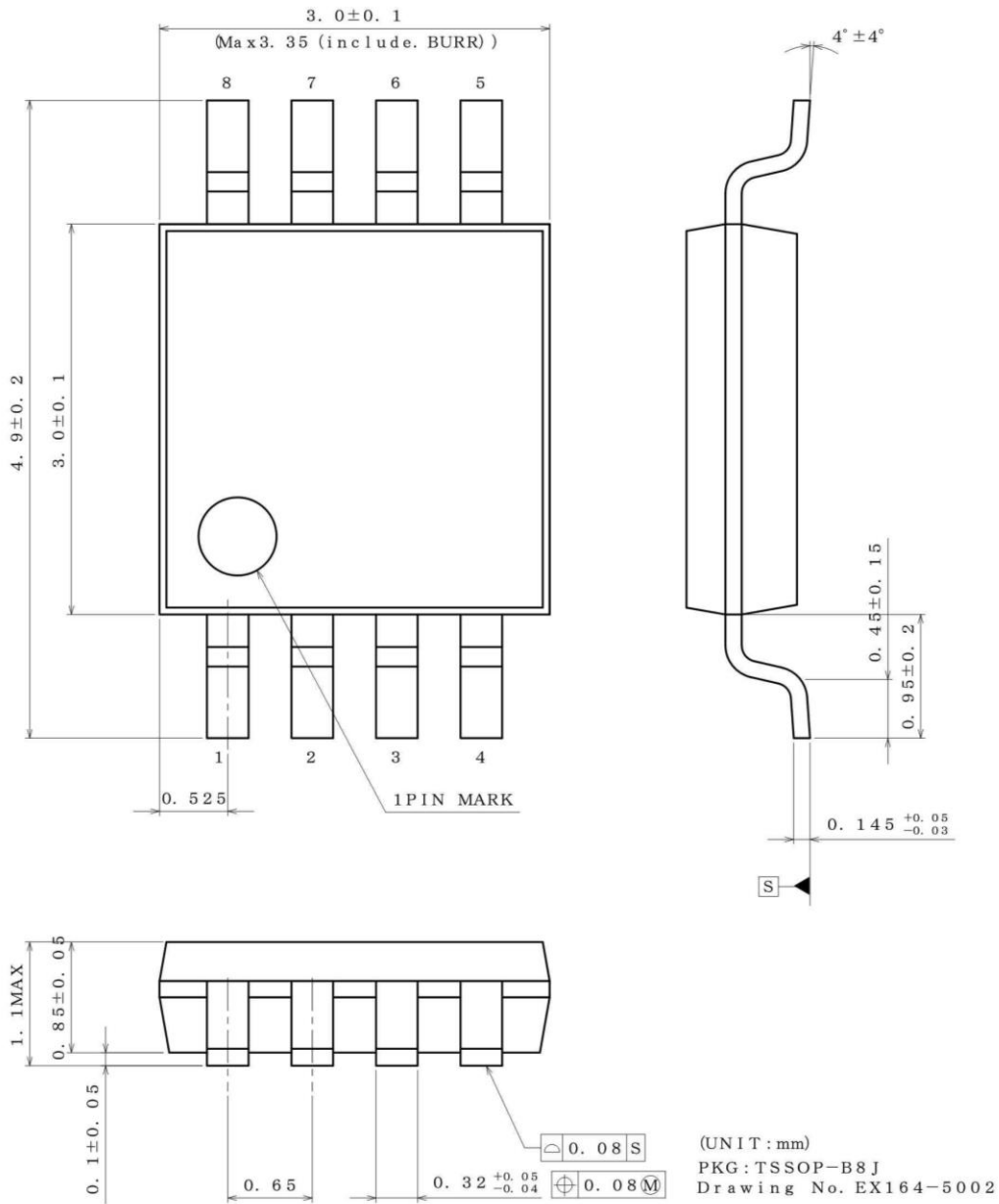
B D 8 2 0 4 4 F V J		-		G E2	
Part Number		Package FVJ: TSSOP-B8J (MSOP-8 Jedec)		G: Halogen free package	
				Packaging and forming specification E2: Embossed tape and reel	

Marking Diagram



Physical Dimension, Tape and Reel Information

Package Name	TSSOP-B8J
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## Revision History

Date	Revision	Changes
06.JAN.2014	0001	Target Specification
05.FEB.2014	001	Release
26.MAY.2014	002	UL, CB recognized.
21.DEC.2015	003	Revise CB File No. Add Functional Description(6.Output Discharge Function)

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
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- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

### Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
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### Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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