LDO Regulators with Watchdog Timer and Voltage Detector

200 mA Output LDO Regulator for Automotive with WDT and Voltage Detector

BD820F50EFJ-C

General Description

BD820F50EFJ-C is a regulator with a high withstand voltage of 45 V. And it integrates a reset (RESET) that monitors its output and a watchdog timer (WDT).
The quiescent current is low while the output current is 200 mA.
The reset signal is output when the output of the regulator falls below 4.2 V (Typ).
The reset delay time and watchdog monitor time can be adjusted by the external capacitor.

Key Specifications

- Wide Temperature Range (Tj): -40 °C to +150 °C
- Wide Input Voltage Range: -0.3 V to +45 V
- Low Quiescent Current: 6 µA (Typ)
- Output Current Capability: 200 mA (Max)
- Output Voltage: 5.0 V (Typ)

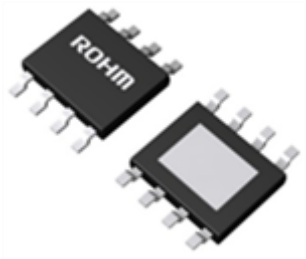
Package

	W (Typ) x D (Typ) x H (Max)
HTSOP-J8	4.90 mm x 6.00 mm x 1.00 mm

Feature

- AEC-Q100 Qualified(Note 1)
- Qualified for Automotive Applications
- Low ESR Ceramic Capacitors Applicable for Output
- Low Dropout Voltage: PDMOS Output Transistor
- Integrated Power On and Under-voltage Reset
- Adjustable Reset Delay Time and Watchdog Time by External Capacitor
- Integrated Over Current Protection (OCP)
- Integrated Thermal Shutdown (TSD)

(Note 1) Grade 1



HTSOP-J8

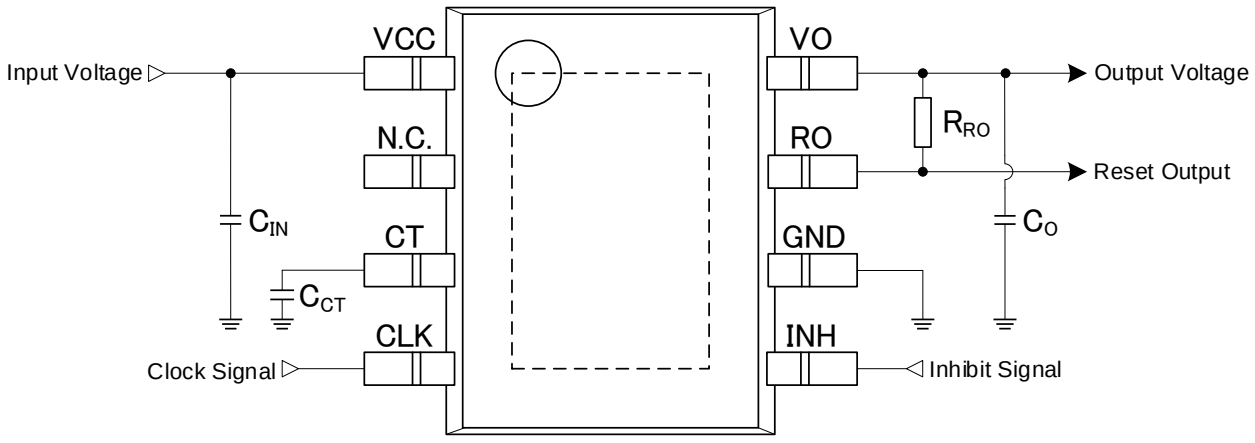
Applications

- Power Train System
- Body Control Unit
- Car Audio System
- Car Navigation System

Typical Application Circuit

- External Components
  Capacitor(Note 2) : 0.1 µF ≤ C_{IN} (Min), 6 µF ≤ C_{OUT} (Min), 0.047 µF ≤ C_{CT} ≤10 µF
  Resistor: 5.1 kΩ (Min) ≤ R_{RO}

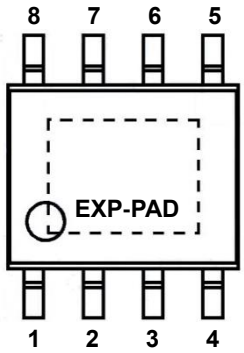
(Note 2) Electrolytic, tantalum and ceramic capacitors can be used.



Contents

Pin Configurations

HTSOP-J8
(TOP VIEW)

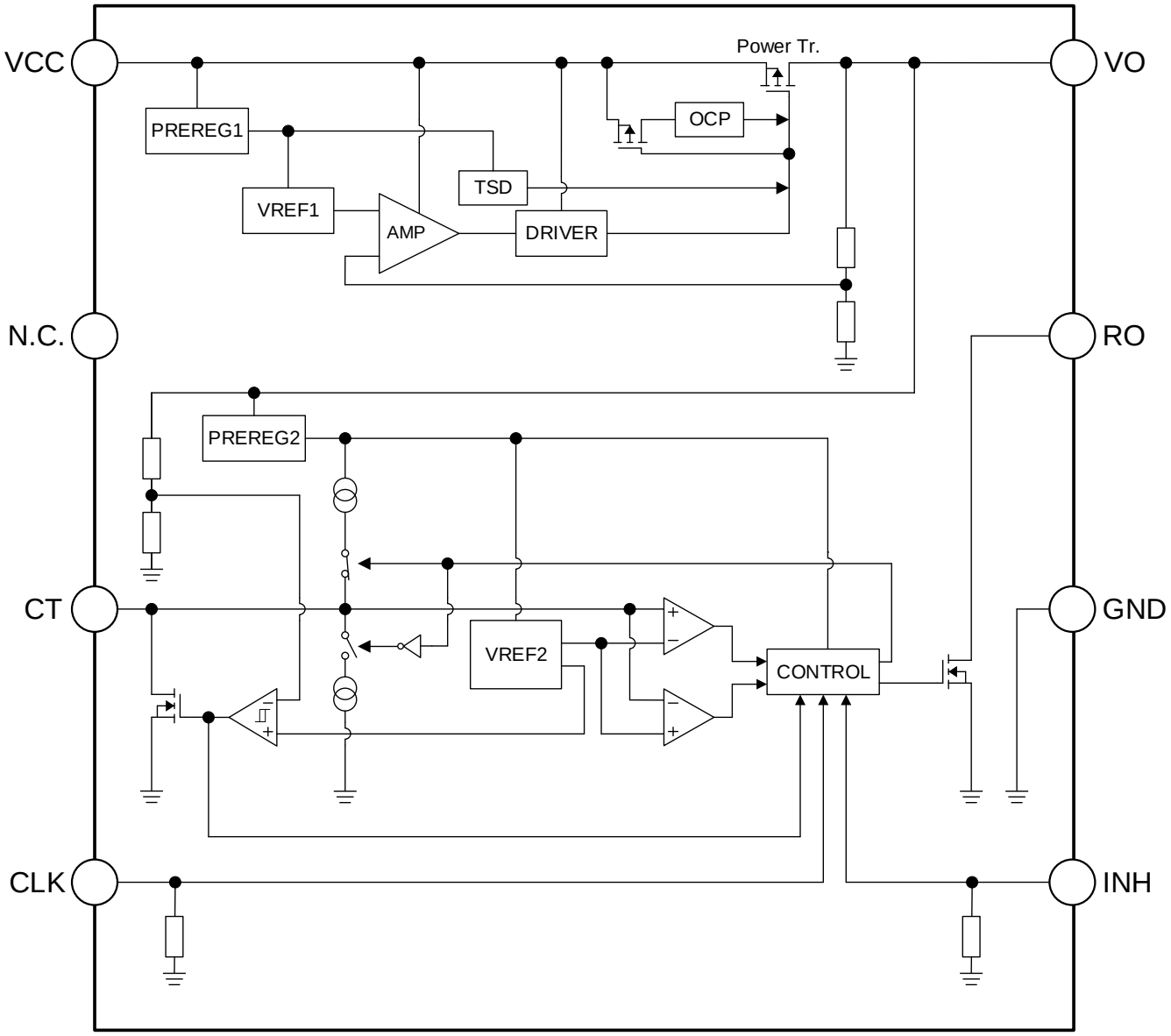


Pin Descriptions

Pin No.	Pin Name	Function	Descriptions
1	VCC	Input	This pin is an input of IC to supply the input voltage. It is necessary to connect a capacitor which is 0.1 µF (Min) or higher between VCC pin and GND. The detailed selecting guide is described in Selection of External Components.
2	N.C.	-	This pin is not connected to the chip. It can keep open or it's also possible to connect to GND(Note 1).
3	CT	Setting of RESET Delay Time and WDT Monitor Time	This pin sets RESET Delay Time and WDT Monitor Time. It is necessary to connect a capacitor which is from 0.047 µF (Min) to 10 µF (Max) between the CT pin and GND. The detail of a selection is described in WDT and RESET Function of Electrical Characteristics.
4	CLK	CLK Signal Input from Microcomputer	This pin is an input of CLK signal(Note 2) from Microcomputer. Pull-down resisters are implemented in IC. If this pin is open, the input state is kept as low.
5	INH	Control WDT ON/OFF	This pin enables or disables WDT by High/Low input(Note 2). High Voltage: WDT function is turned OFF. Low Voltage: WDT function is turned ON. Pull-down resisters are implemented in IC. The input state is low (WDT function is turned ON) if this pin is open.
6	GND	Ground	This is Ground pin. It shall be connect to the lowest potential.
7	RO	RESET Output	This pin outputs RESET. An output construction is made by Open-drain and Open-collector. It should connect a resister which is 5.1 kΩ (Min) or higher between VO pin and RO pin to pull-up. It is also possible to pull-up via resistor to any voltage below the maximum rating. If RESET function is unnecessary, it can keep open.
8	VO	Output	This pin outputs 5 V (Typ) as the ouput of a regulator IC. In order to operate stable, it is necessary to connect a capacitor which is 6 µF (Min) or higher between VO pin and GND. The detailed selecting guide is described in Selection of External Components.
EXP-PAD	EXP-PAD	Heat Dissipation	Since EXP-PAD on the back side is connected to the IC substrate, so it should connect to external Ground node.

(Note 1) If Pin No.2 is shorted to GND, Pin No.2 will be adjacent to Pin No.1 VCC on the board layout.
If adjacent pins are expected to be shorted, please confirm if there is any problem with the actual application.
(Note 2) CLK Input High/Low Level Voltage which is described in WDT and RESET Function of Electrical Characteristics should be supplied to the CLK pin.
INH Input High/Low Level Voltage which is also described in WDT and RESET Function of Electrical Characteristics should be supplied to the INH pin.
It is not allowed to supply the input state keeping the midpoint potential voltage.

Block Diagram



Description of Blocks

Block Name	Function	Description of Blocks
PREREG1	Internal Power Supply for LDO	To provide Power Supply for Internal Circuit of LDO
PREREG2	Internal Power Supply for WDT/RESET	To provide Power Supply for Internal Circuit of WDT and RESET
VREF1	Reference Voltage for LDO	To generate the Reference Voltage for LDO
VREF2	Reference Voltage for WDT/RESET	To generate the Reference Voltage for WDT and RESET
AMP	Error Amplifier	The Error Amplifier amplifies the difference between the divided feedback voltage and the reference voltage, then it regulates Power Tr. via DRIVER.
DRIVER	Output MOSFET Driver	To drive the Output MOSFET (Power Tr.)
TSD	Thermal Shutdown Protection	In case maximum power dissipation is exceeded or the ambient temperature is higher than the Maximum Junction Temperature, overheating causes the chip temperature (Tj) to rise. The TSD protection circuit detects this and forces the output to turn off in order to protect the device from overheating. When the junction temperature decreases to low, the output turns on automatically.
OCP	Over Current Protection	If the output current increases higher than the maximum Output Current, the output current is limited by Over Current Protection in order to protect the device from a damage caused by an over current. In this operating condition, the output voltage may decrease because the output current is limited. If an abnormality state is removed and the output current value returns normally, the output voltage also returns to normal state.
CONTROL	WDT + RESET Control	To control Reset Delay and Watchdog Time depending on each state of CT voltage, INH voltage and CLK signal.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage(Note 1)	V_{CC}	-0.3 to +45.0	V
CT Voltage	V_{CT}	-0.3 to +7.0 (≤ V_O + 0.3)	V
CLK Voltage	V_{CLK}	-0.3 to +7.0	V
INH Voltage	V_{INH}	-0.3 to +7.0	V
RO Voltage	V_{RO}	-0.3 to +20.0	V
Output Voltage	V_O	-0.3 to +20.0 (≤ V_{CC} + 0.3)	V
Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation and thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Do not exceed Tjmax.

Thermal Resistance(Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 4)	2s2p(Note 5)	
HTSOP-J8				
Junction to Ambient	θ_{JA}	130	34	°C/W
Junction to Top Characterization Parameter(Note 3)	Ψ_{JT}	15	7	°C/W

(Note 2) Based on JESD51-2A(Still-Air), using a BD820F50EFJ-C Chip.

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 6) This thermal via connects with the copper pattern of all layers.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage*(Note 1)*	V_{IN}	5.9*(Note 2)*	-	42.0	V
Start-up Voltage*(Note 3)*	$V_{IN\ START-UP}$	3.0	-	-	V
Output Current	I_O	0	-	200	mA
Input Capacitor	C_{IN}	0.1	-	-	µF
Output Capacitor	C_O	6	-	1000	µF
Output Capacitor Equivalent Series Resistance	ESR (C_O)	-	-	5	Ω
CT Capacitor	C_{CT}	0.047	0.1	10	µF
RO Pull-up Resister	R_{RO}	5.1	-	-	kΩ
Operating Temperature	Ta	-40	-	+125	°C

(Note 1) Do not exceed Tjmax.

(Note 2) This voltage is the minimum input voltage that can operate with the maximum output current, e.g.) Io = 200 mA. If the actual required output current is smaller than 200 mA, the minimum input voltage can be also eased as lower. In this case, the dropout voltage should be considered depending on the output current value.

(Note 3) This voltage is the minimum input voltage to be able to start operating an internal circuit of IC. However, in the case of the input voltage becomes lower than “the output voltage + the dropout voltage”, the output voltage becomes V_{CC}-ΔVd, because Low dropout regulator can’t regulate as of the output voltage which is higher than the input voltage.

Electrical Characteristics

For All Function

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{CC} = 13.5 V, I_O = 0 mA, the typical value is defined at Tj = +25 °C

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Circuit Current (+25 °C)	I_{CC1}	-	5	12	μA	I_O = 0 mA, Tj = +25 °C V_{INH} = 5 V
Circuit Current (-40 °C to +125 °C)	I_{CC2}	-	5	18	μA	I_O = 0 mA, -40 °C ≤ Tj ≤ +125 °C V_{INH} = 5 V
Circuit Current (-40 °C to +125 °C)	I_{CC3}	-	6	-	μA	I_O = 0 mA, -40 °C ≤ Tj ≤ +125 °C V_{INH} = GND

LDO Function

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{CC} = 13.5 V, I_O = 0 mA, the typical value is defined at Tj = +25 °C

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Output Voltage	V_{O1}	4.90	5.00	5.10	V	6 V ≤ V_{CC} ≤ 40 V, 0 mA ≤ I_O ≤ 100 mA
Output Voltage	V_{O2}	4.90	5.00	5.10	V	8 V ≤ V_{CC} ≤ 26 V, I_O ≤ 200 mA
Minimum Dropout Voltage	ΔVd	-	0.40	0.80	V	V_{CC} = 4.75V (= V_O x 0.95), I_O = 200 mA
Ripple Rejection	R.R.	50	70	-	dB	f = 120 Hz, ein = 1 Vrms, I_O = 100 mA
Line Regulation	Reg.I	-	10	30	mV	8 V ≤ V_{CC} ≤ 16 V
Load Regulation	Reg.L	-	10	30	mV	10 mA ≤ I_O ≤ 100 mA
Thermal Shutdown	T_{TSD}	-	175	-	°C	Tj at TSD ON
Over Current Protection	I_{OCP}	201	600	-	mA	

Electrical Characteristics - continued

Reset, WDT Function

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{CC} = 13.5 V, I_O = 0 mA, the typical value is defined at Tj = +25 °C

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Reset Detection Voltage	V_{RT}	4.09	4.20	4.31	V	
Reset Detection Hysteresis	V_{RHY}	25	60	100	mV	
Reset Low Voltage	V_{RO_L}	-	-	0.4	V	3 V ≤ V_O ≤ V_{RT}, R_{RO} = 5.1 kΩ
CT Upper-side Threshold	V_{CTH}	-	0.80	-	V	
CT Lower-side Threshold	V_{CTL}	-	0.40	-	V	
CT Charge Current	I_{CT_C}	-	4.0	-	μA	V_{CT} = 0.20 V
CT Discharge Current	I_{CT_D}	-	1.0	-	μA	V_{CT} = 1.00 V
Delay Time L→H	t_D	12	20	28	ms	C_{CT} = 0.1 μF *(Note 1)*
WDT Monitor Time	t_{WH}	24	40	56	ms	C_{CT} = 0.1 μF *(Note 1)*
WDT Reset Time	t_{WL}	6	10	14	ms	C_{CT} = 0.1 μF *(Note 1)*
Minimum Operation Voltage	V_{OPR}	1	-	-	V	V_{RO} < 0.5 V, R_{RO} = 5.1 kΩ
CLK Input Current	I_{CLK}	1.5	5	15	μA	V_{CLK} = 5 V
CLK Input Pulse Width	t_{PCLK}	3	-	-	μs	
CLK Input High Level Voltage	V_{HCLK}	V_O × 0.8	-	V_O	V	
CLK Input Low Level Voltage	V_{LCLK}	0	-	V_O × 0.3	V	
INH Input Current	I_{INH}	1.5	5	15	μA	V_{INH} = 5 V
INH Input High Level Voltage	V_{HINH}	V_O × 0.8	-	V_O	V	
INH Input Low Level Voltage	V_{LINH}	0	-	V_O × 0.3	V	

(Note 1) t_D, t_{WH}, and t_{WL} can be adjustable by changing the CT pin capacitance value. (0.047 μF to 10 μF available)

t_D [s] = 0.2 x C_{CT} [F] x 10^6 The accuracy of adjustment: Typical value+35 %+1 ms, -40 %
t_{WH} [s] = 0.4 x C_{CT} [F] x 10^6 The accuracy of adjustment: Typical value±40 %
t_{WL} [s] = 0.1 x C_{CT} [F] x 10^6 The accuracy of adjustment: Typical value±40 %

The capacitance which is lower than or equal to 0.047 μF can be also used for C_{CT}, if wider deviation of t_D can be accepted because of an effect by internal delay.
In addition, the deviation of the external component, (e.g.) capacitance, DC bias, and temperature characteristic, is not considered in these formula.

Typical Performance Curves

Unless otherwise specified, V_{CC} = 13.5 V, I_O = 0 mA, V_{INH} = 5V

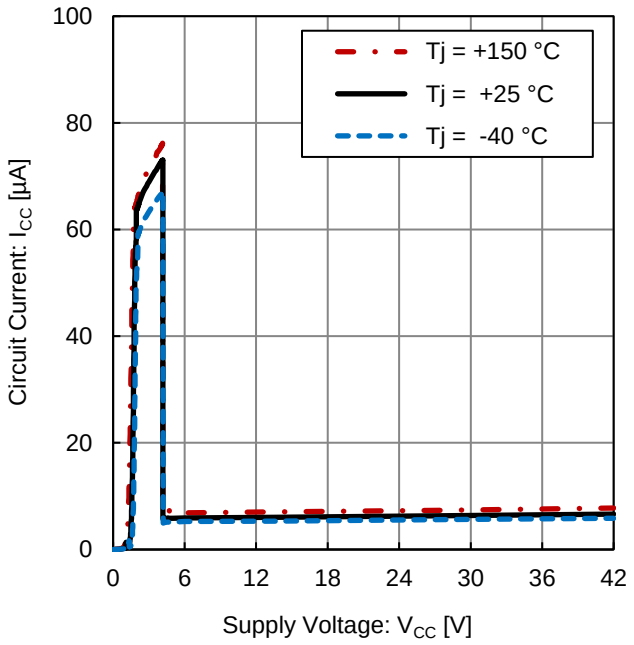


Figure 1. Circuit Current vs Supply Voltage

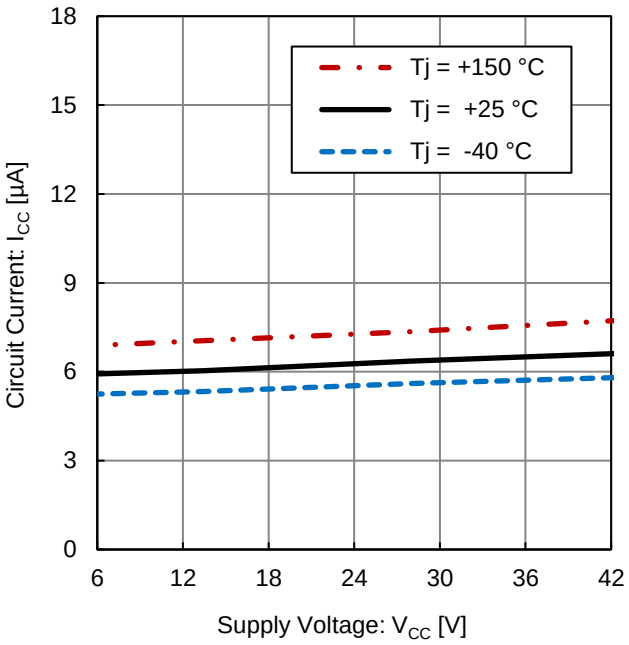


Figure 2. Circuit Current vs Supply Voltage

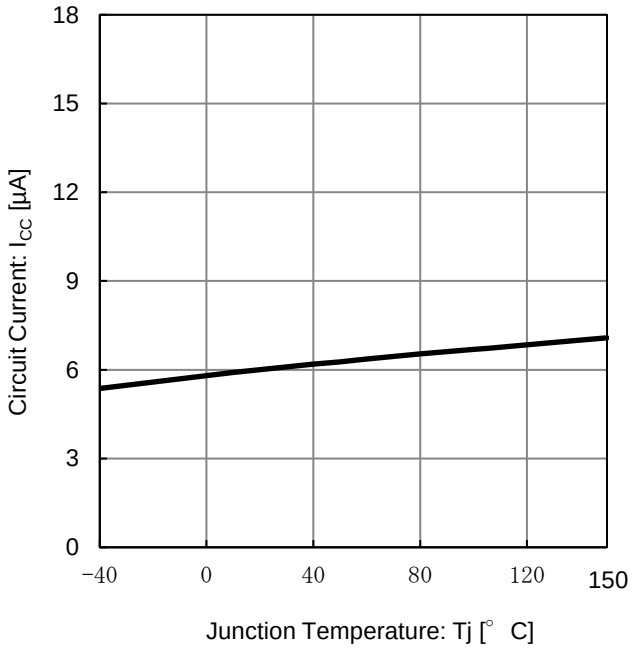


Figure 3. Circuit Current vs Junction Temperature

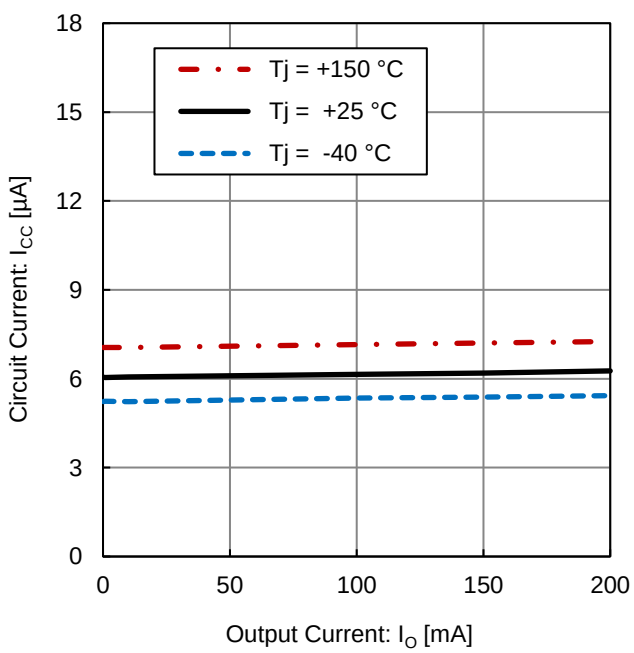


Figure 4. Circuit Current vs Output Current

Typical Performance Curves – continued

Unless otherwise specified, V_{CC} = 13.5 V, I_O = 0 mA, V_{INH} = 5V

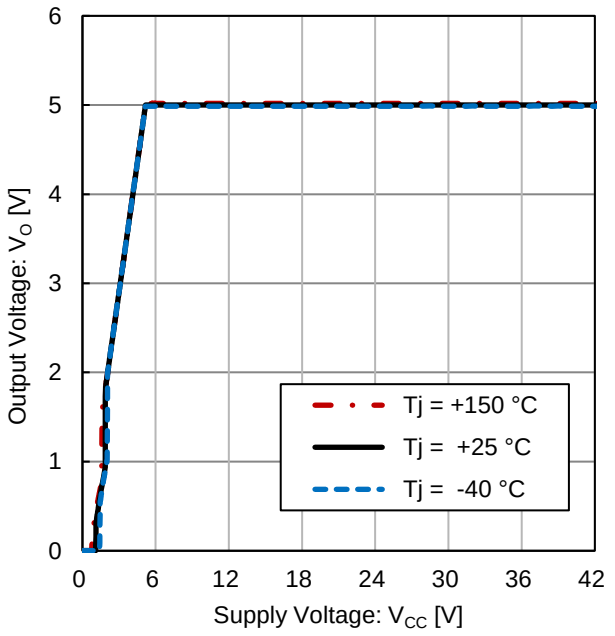


Figure 5. Output Voltage vs Supply Voltage

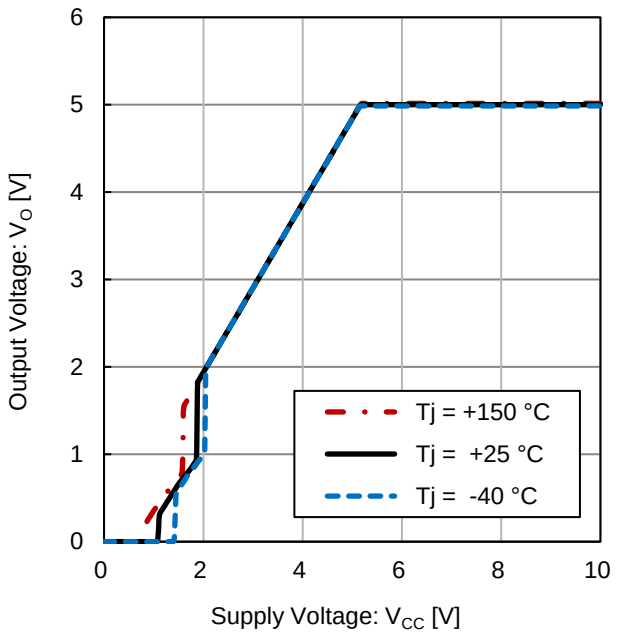


Figure 6. Output Voltage vs Supply Voltage

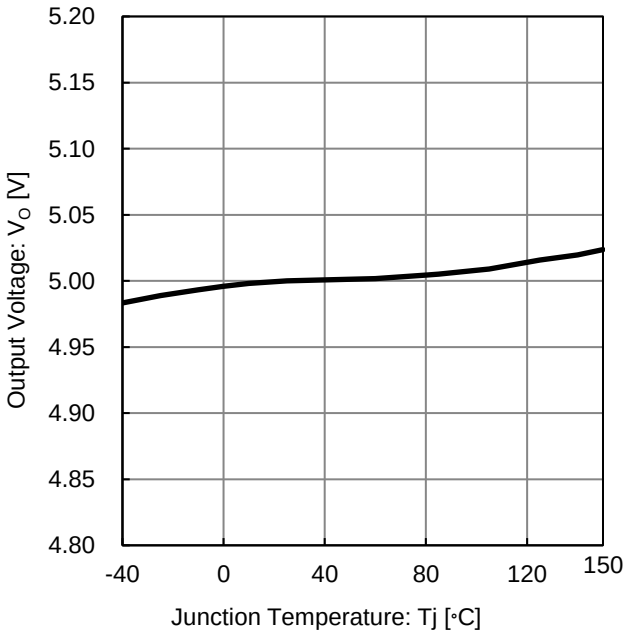


Figure 7. Output Voltage vs Junction Temperature

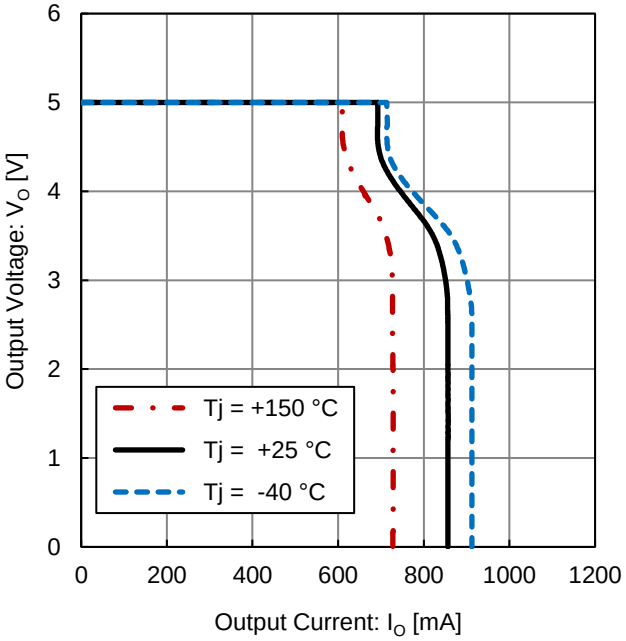


Figure 8. Output Voltage vs Output Current

Typical Performance Curves – continued

Unless otherwise specified, V_{CC} = 13.5 V, I_O = 0 mA, V_{INH} = 5V

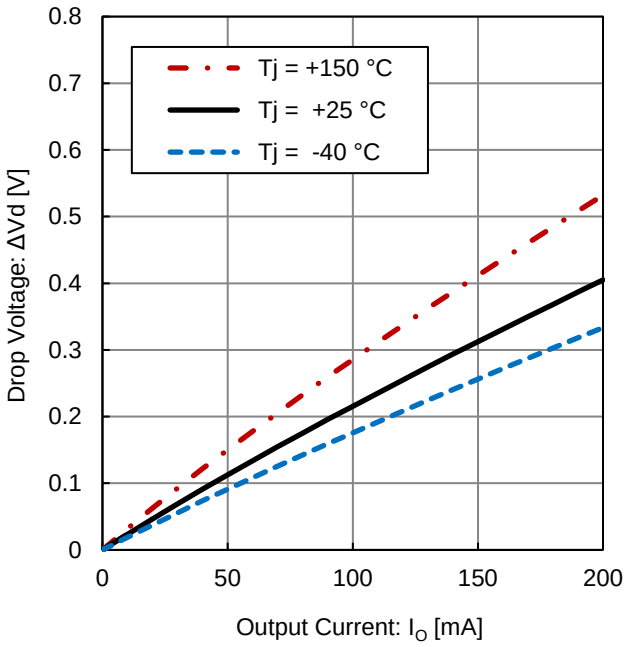


Figure 9. Drop Voltage vs Output Current
(V_{CC} = 4.75 V)

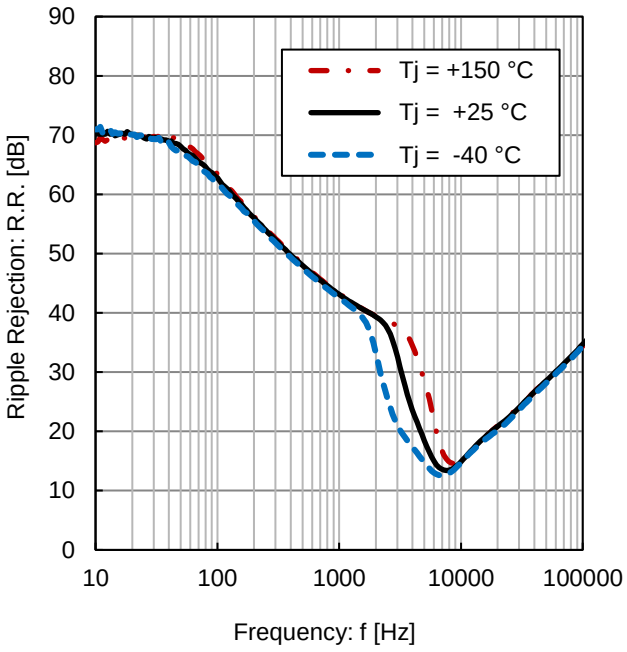


Figure 10. Ripple Rejection vs Frequency
(ein = 1 Vrms, I_O = 100 mA)

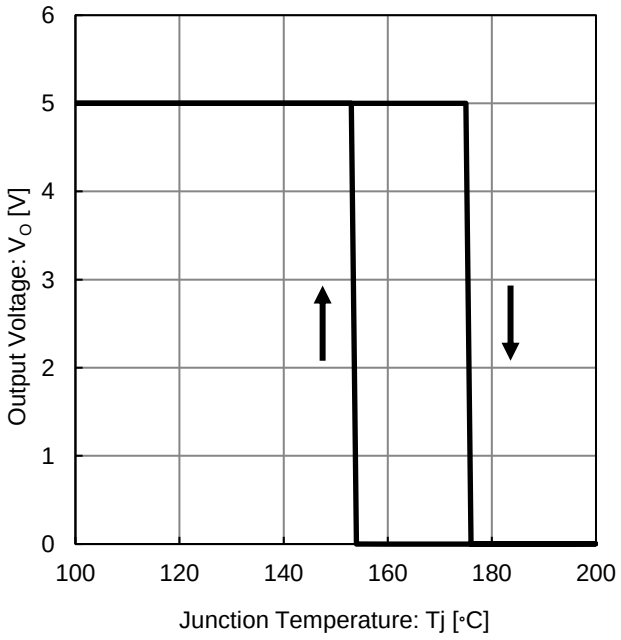


Figure 11. Output Voltage vs Junction Temperature

Typical Performance Curves – continued

Unless otherwise specified, V_{CC} = V_O =5 V, I_O = 0 mA, V_{INH} = 5 V, C_{CT} = 0.1 µF, R_{RO} = 5.1 kΩ

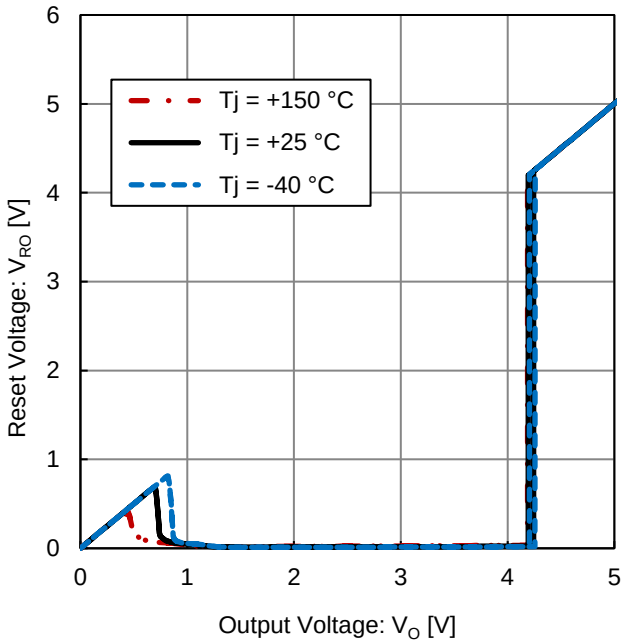


Figure 12. Reset Voltage vs Output Voltage

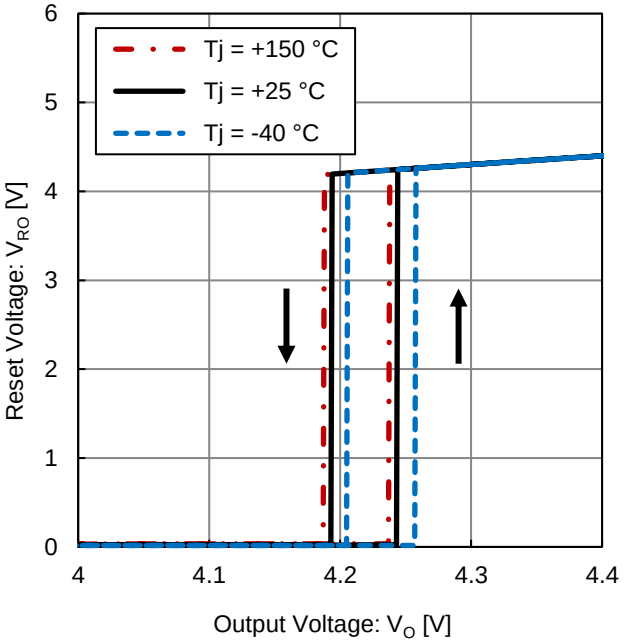


Figure 13. Reset Voltage vs Output Voltage

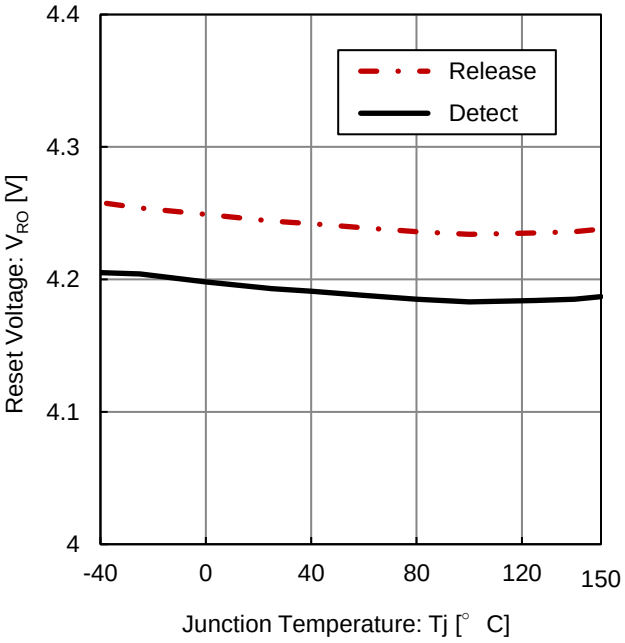


Figure 14. Reset Voltage vs Junction Temperature

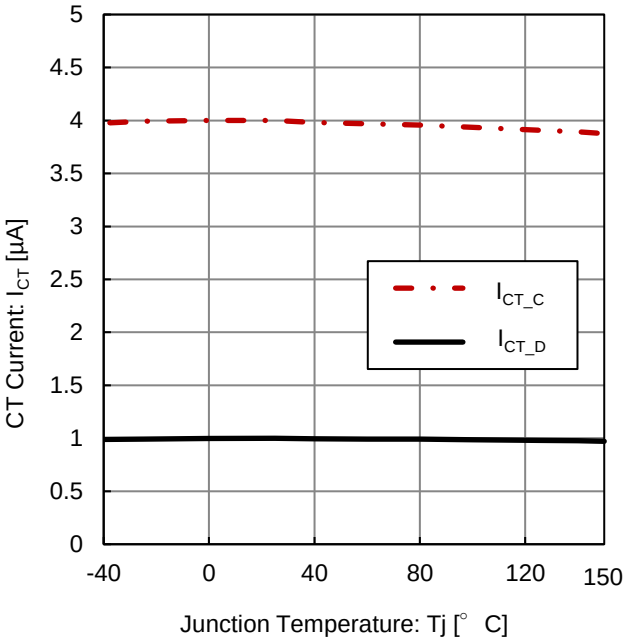


Figure 15. CT Current vs Junction Temperature
(I_{CT_C}: V_{CT} = 0.20 V, V_{INH} = Open
I_{CT_D}: V_{CT} = 1.00 V, V_{INH} = Open)

Typical Performance Curves – continued

Unless otherwise specified, V_{CC} = V_O =5 V, I_O = 0 mA, C_{CT} = 0.1 µF, R_{RO} = 5.1 kΩ

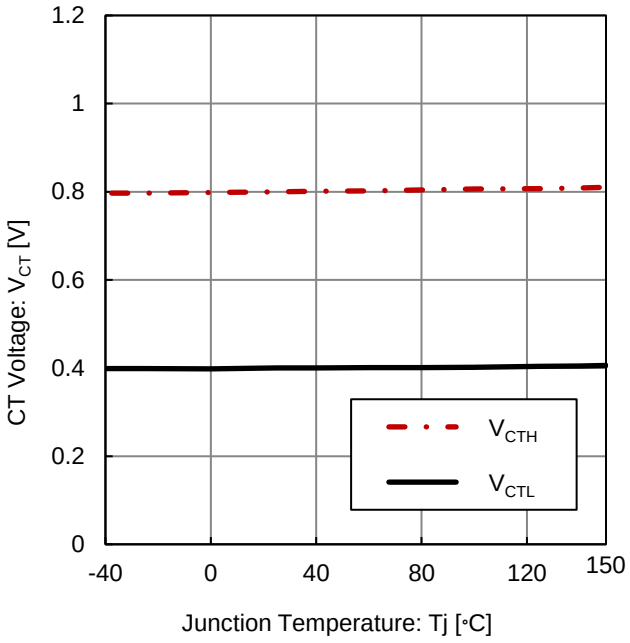


Figure 16. CT Voltage vs Junction Temperature

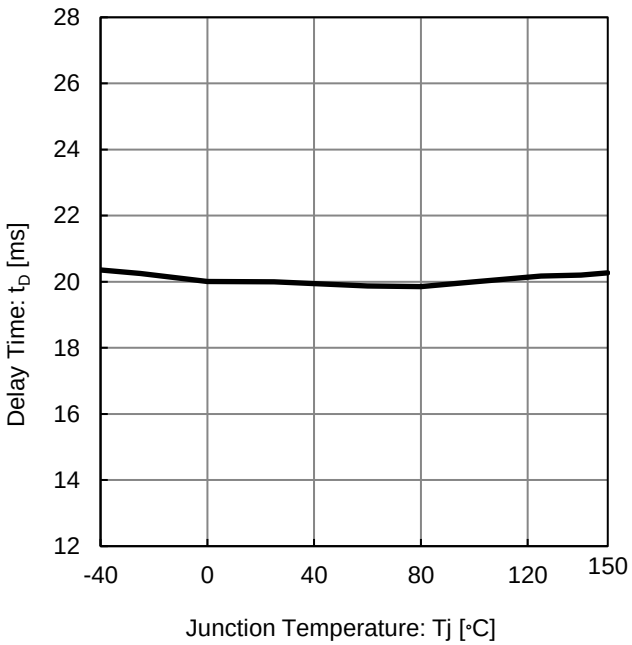


Figure 17. Delay Time vs Junction Temperature

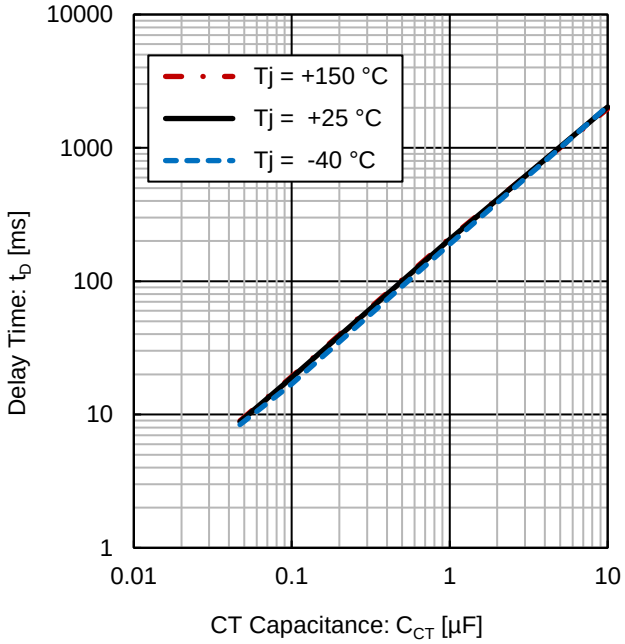


Figure 18. Delay Time vs CT Capacitance

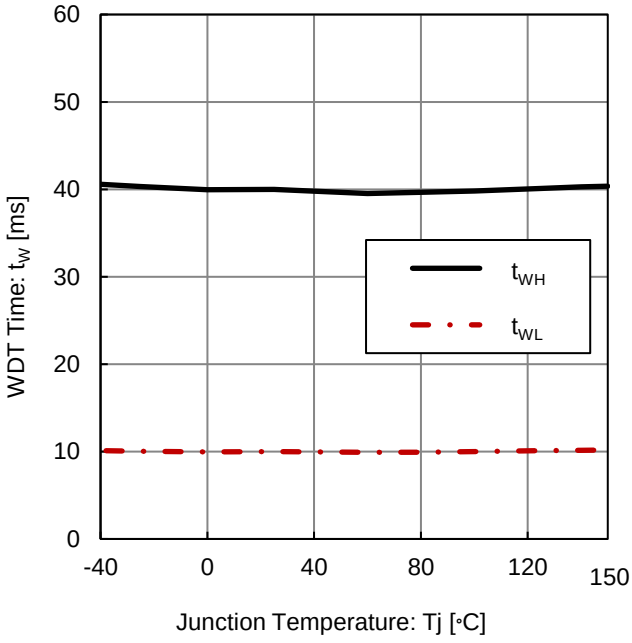


Figure 19. WDT Time vs Junction Temperature

Typical Performance Curves – continued

Unless otherwise specified, V_{CC} = V_O =5 V, I_O = 0 mA, C_{CT} = 0.1 µF, R_{RO} = 5.1 kΩ

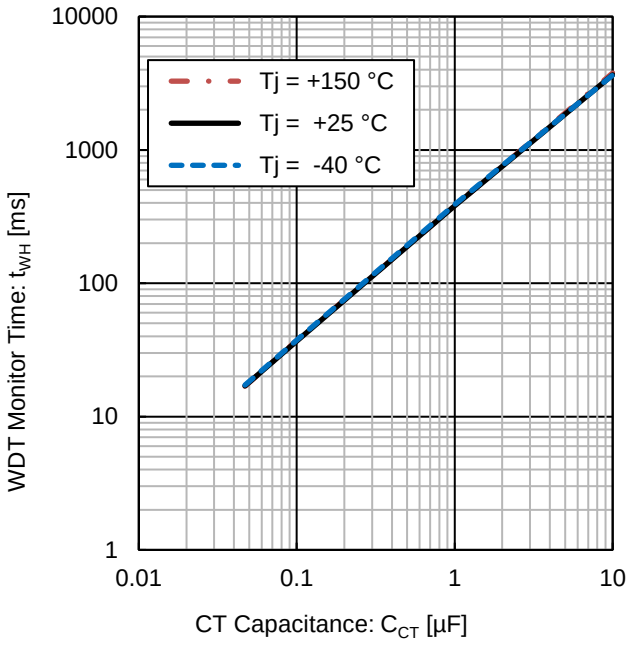


Figure 20. WDT Monitor Time vs CT Capacitance

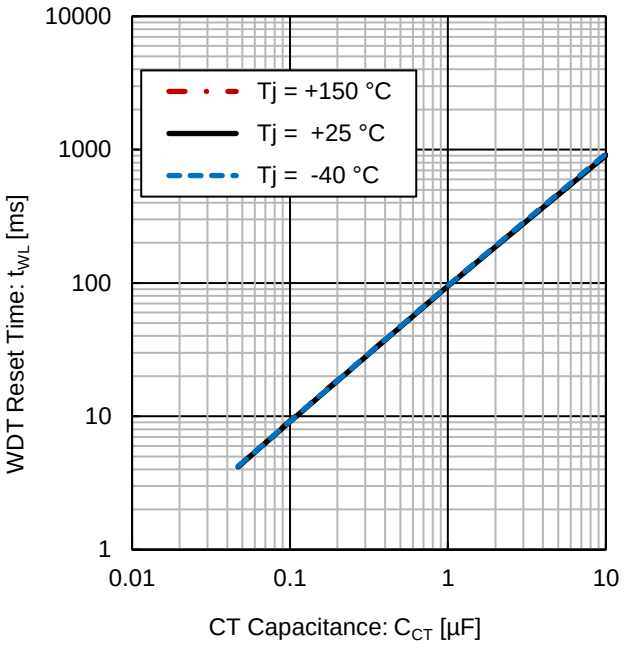


Figure 21. Delay Time vs CT Capacitance

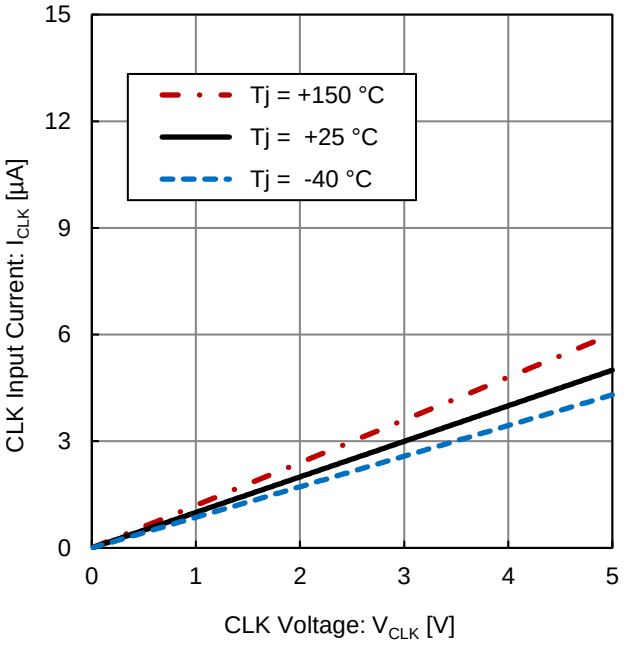


Figure 22. CLK Input Current vs CLK Voltage

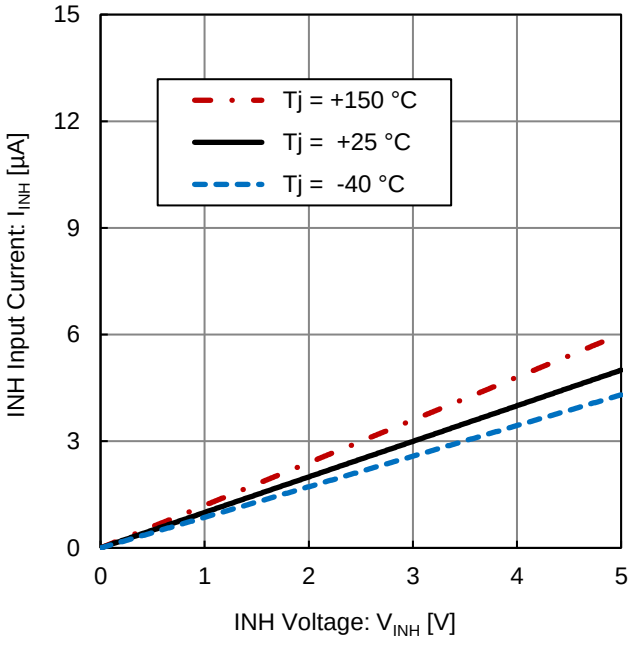


Figure 23. INH Input Current vs INH Voltage

Typical Performance Curves – continued

Unless otherwise specified, V_{CC} = V_O =5 V, I_O = 0 mA, C_{CT} = 0.1 µF, R_{RO} = 5.1 kΩ

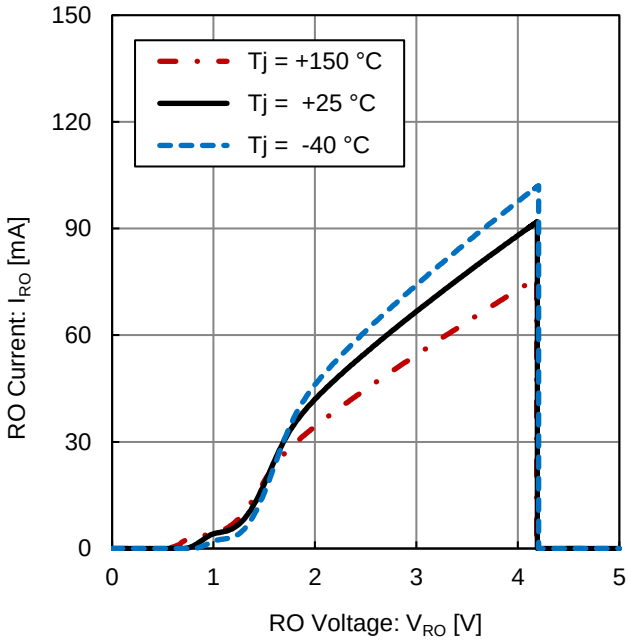
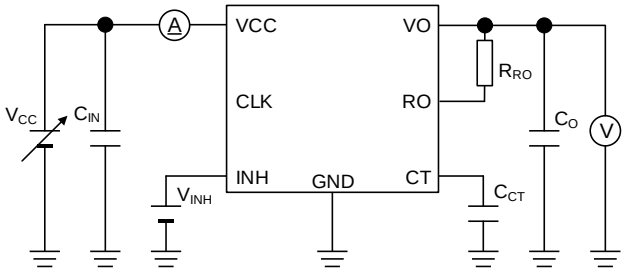
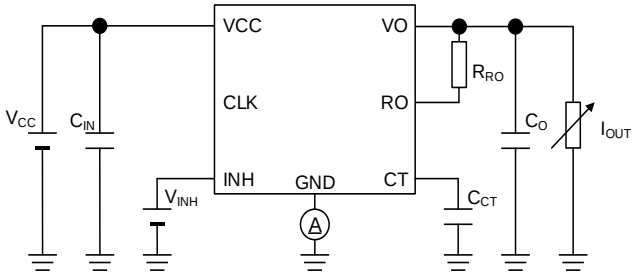


Figure 24. RO Current vs RO Voltage

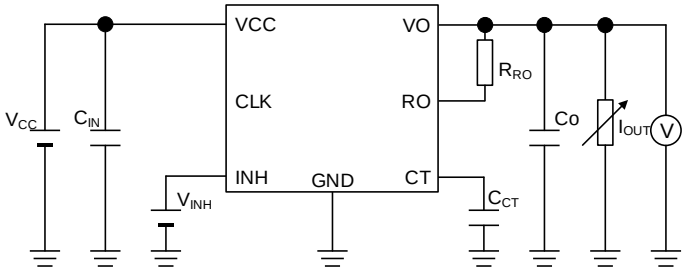
Measurement Circuit for Typical Performance Curves



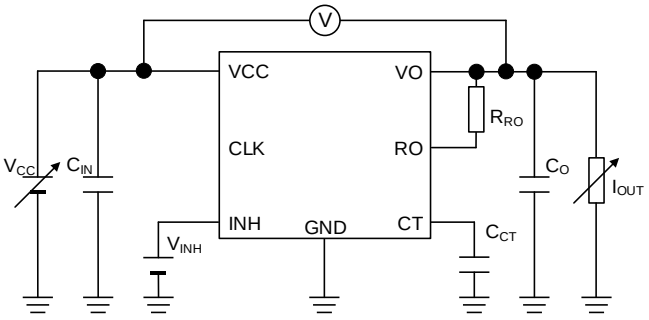
Measurement Setup for
Figure 1, 2, 3, 5, 6, 7, 11



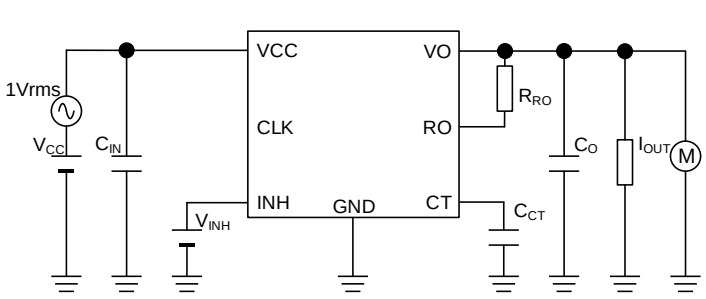
Measurement Setup for
Figure 4



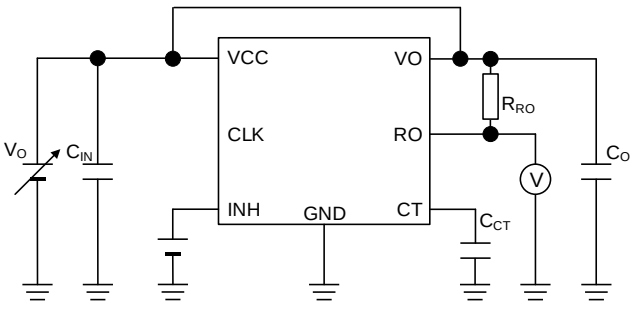
Measurement Setup for
Figure 8



Measurement Setup for
Figure 9

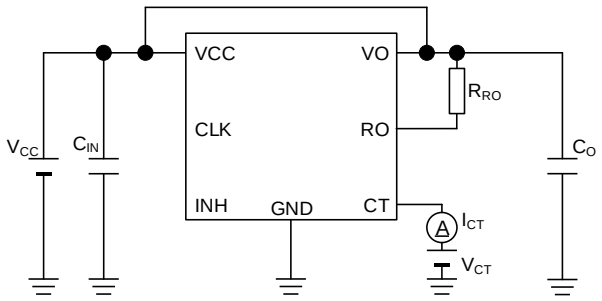


Measurement Setup for
Figure 10

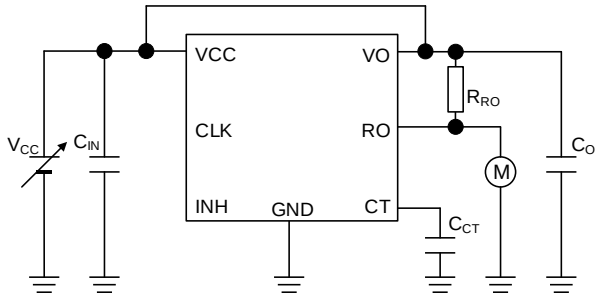


Measurement Setup for
Figure 12, 13, 14

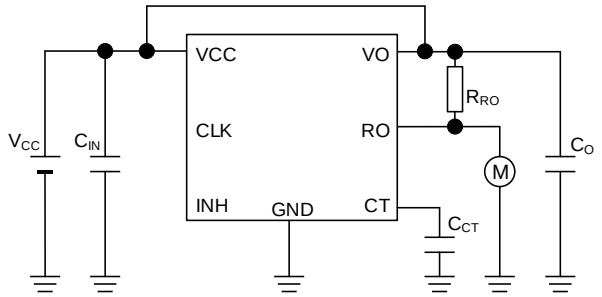
Measurement Circuit for Typical Performance Curves - Continued



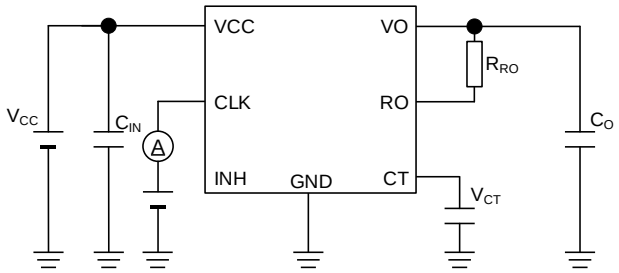
Measurement Setup for
Figure 15, 16
,



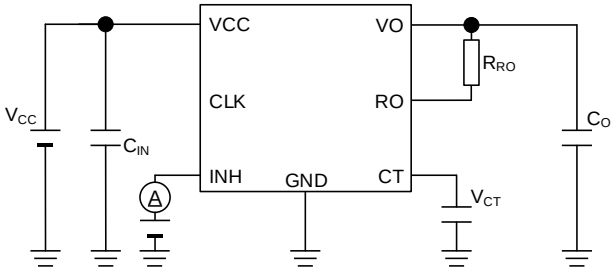
Measurement Setup for
Figure 17, 18



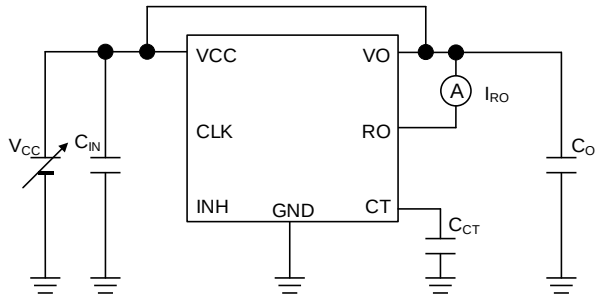
Measurement Setup for
Figure 19, 20, 21



Measurement Setup for
Figure 22



Measurement Setup for
Figure 23



Measurement Setup for
Figure 24

Timing Chart

VCC ON/OFF

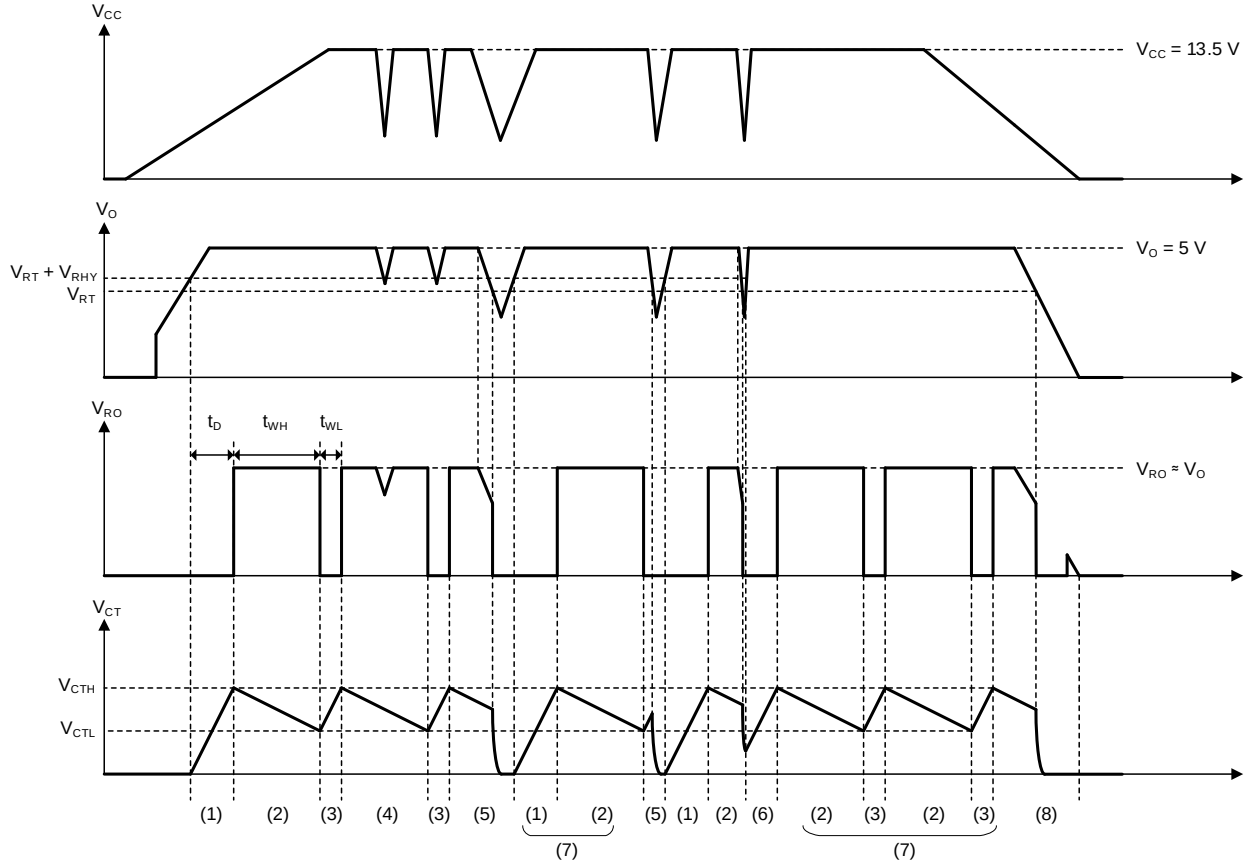


Figure 25. Timing Chart 1

This page shows the detail of the RESET and Watchdog Timer operation. (Without CLK signal input)

(1) Watchdog Timer (WDT) and RESET of BD820F50EFJ-C starts operating when the output voltage becomes higher than RESET detection voltage (V_{RT}) + RESET detection hysteresis (V_{RHY}), i.e. the reset state caused by low output is removed. When it starts, CT voltage rises up by charging the internal constant current to the external capacitor, C_{CT}. If CT voltage reaches to high side threshold voltage, V_{CTH}, RO outputs H state. The voltage level of H state is defined by the pull-up voltage via resistor at the RO pin. This time period described in Timing Chart as (1) is called Delay Time L→H (t_D).

(2) When V_{CT} reaches V_{CTH}, the constant current state of CT is switched from charging to dis-charging. After that, if the electron charged in C_{CT} is dis-charged and then V_{CT} reaches to low side threshold voltage, V_{CTL}, RO outputs L state. This time period described in Timing Chart as (2) is called WDT Monitor Time (t_{WH}).

(3) After (2), when V_{CT} reaches V_{CTL}, the constant current state of CT is switched again from dis-charging to charging. Then, if the electron charged to C_{CT} and V_{CT} reaches V_{CTH} again, RO outputs H state. This time period described in Timing Chart as (3) is called WDT Reset Time (t_{WL}).

(4) When VO voltage changes in the range $V_O > V_{RT}$, RESET function judges the state as not abnormal because VO voltage is still higher than the threshold voltage of RESET Detection Voltage, so RO keeps H state.

(5) If VO voltage changes across the threshold voltage of V_{RT}, the constant current state of CT is forced to be changed as dis-charging in order to dis-charge the electron at C_{CT}. Whichever either H or L of RO state, it happens independently. RESET function judges the state as abnormal because VO voltage is lower than RESET Detection Voltage, and then RO outputs L state.

VCC ON/OFF - Continued

(6) If the time period of changing VO voltage in (5) condition is too short, and if CT voltage cannot reach to V_{CTL} at once before going back VO voltage to across V_{RT} + V_{RHY}, the forced CT dis-charging state is canceled and turns back the state of (1) or (3). This short glitch time is about 100 µs at the condition CT capacitance is 0.1 µF. The current of forced CT discharging is defined by the internal pull-down resistor which is typically 500 Ω, so the glitch time has a dependency on the CT capacitance and V_{CT} voltage at when VO comes back higher than V_{RT} + V_{RHY}. Therefore, in this case, there is a possibility that Delay Time L→H (t_D) becomes shorter depending on the situation of V_{CT} voltage.
In order to avoid this abnormal operation which becomes shorter Delay Time L→H (t_D), if there is a possibility to change VO voltage rapidly in very short time, consider to ease the condition which causes the problem depending on the transient input changes or load current changes. For example, to limit VO voltage changes caused by fast transient of the load current, the bigger and proper output capacitor should be implemented. The limitation of the input transient changes slower than 100 µs helps to decrease the transient VO voltage changes.

(7) When RO outputs L, and V_{CT} also becomes L state which is lower than V_{CTL} via after (5) operation, and then, if VO voltage becomes higher than V_{RT} + V_{RHY}, WDT and RESET function restarts operating continuously as following transition, (1)→(2)→(3)→(2)→(3)→….

(8) When VO voltage becomes lower than V_{RT} and then falls to low, the constant current of CT keeps its state of dis-charging in order to make CT voltage completely low. In this case, RO can keep L output state until VO voltage becomes lower than or equal to 1 V (V_{OPR}), i.e. during the condition that $V_{OPR} < V_O < V_{RT}$.

Each period time of t_D, t_{WH} and t_{WL} can be adjusted by CT capacitance, C_{CT}.

It can be calculated by following formulas.

$$t_D[s] \approx \frac{V_{CTH}[V] \times C_{CT}[F]}{I_{CT\_C}[A]}$$

$$t_{WH}[s] \approx \frac{|V_{CTH} - V_{CTL}|[V] \times C_{CT}[F]}{I_{CT\_D}[A]}$$

$$t_{WL}[s] \approx \frac{|V_{CTL} - V_{CTH}|[V] \times C_{CT}[F]}{I_{CT\_C}[A]}$$

However, the calculated value using these formulas is just a rough estimation. Therefore the value for the CT capacitance shall be designed by the ratio calculation compared the actual value to the value at the condition of C_{CT} = 0.1 µF described in the Electrical Characteristics – Reset, WDT Function.

Timing Chart - Continued

CLK ON/OFF

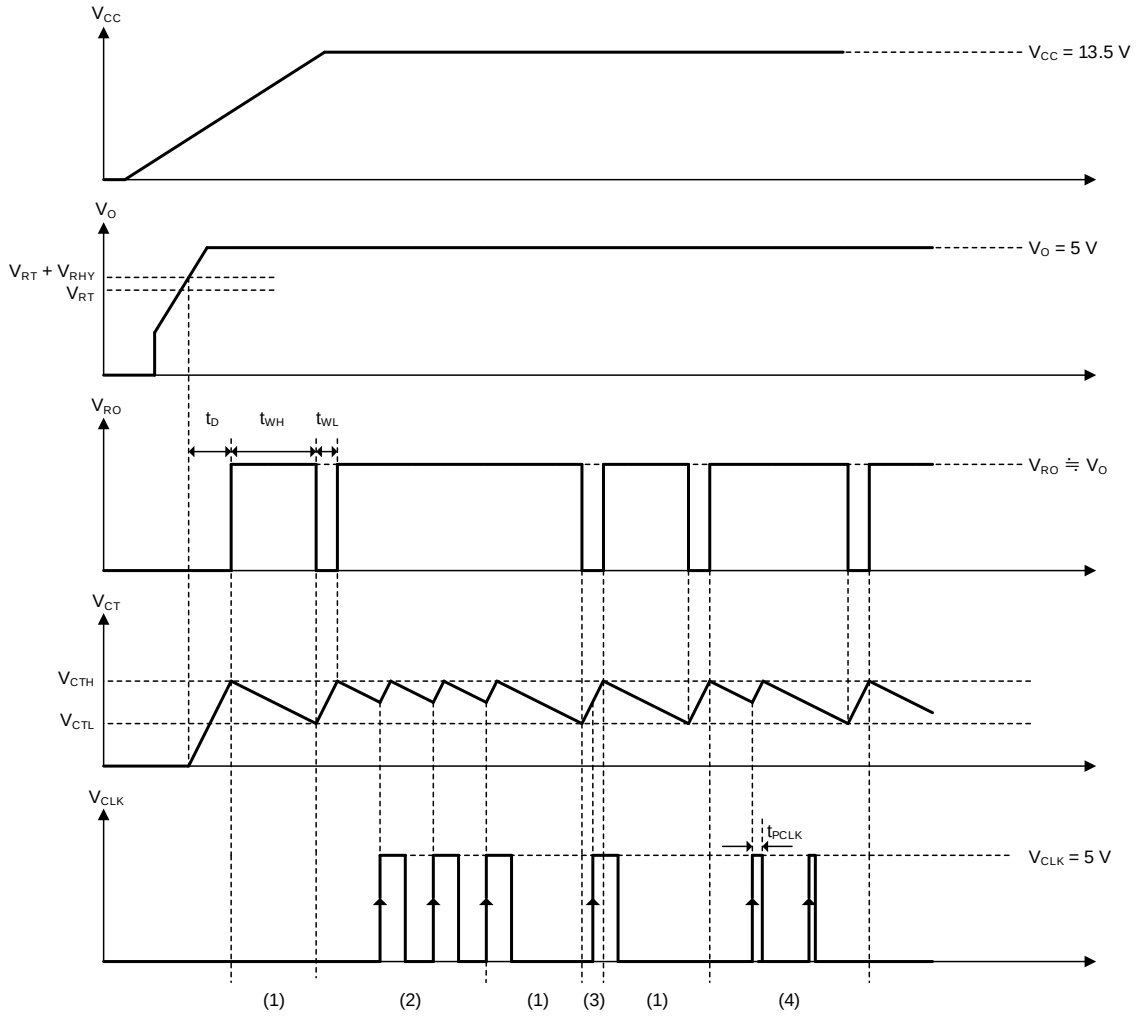


Figure 26. Timing Chart 2

A WDT behavior on the CLK inputs is described here.

CLK inputs is acceptable only while RO outputs H, i.e. during t_{WH}, for BD820F50EFJ-C.
When RO outputs L, i.e. during t_{WL}, t_D and so on, CLK inputs is not allowed.

(1) While RO outputs H, if the input of a rising edge to the CLK pin is not supplied, a dis-charge state at CT kept. If this state continues until V_{CT} reaches V_{CTL}, then the output of RO switches from H to L. This state is Timeout Failure that WDT does not detect the rising edge of CLK inputs during the period defined by C_{CT} capacitance.

(2) While RO outputs H, if the rising edge supplies to the CLK pin, WDT detects this rising edge and then it changes the dis-charging state at CT to a charging state. Then V_{CT} reaches to V_{CTH} by charging constant current to C_{CT}, CT state changes back to the dis-charging. RO can keep H output if CLK signal inputs with constant timing that CT state is the dis-charging as described (2).

(3) While RO outputs L, even if the rising edge supplies to the CLK pin, WDT does not detect the edge.

(4) The pulse width of CLK inputs, i.e. t_{PCLK}, must be always longer than or equal to 3 μs. Otherwise there is a possibility that CLK pulse cannot change CT state.

Timing Chart - Continued

INH ON/OFF 1

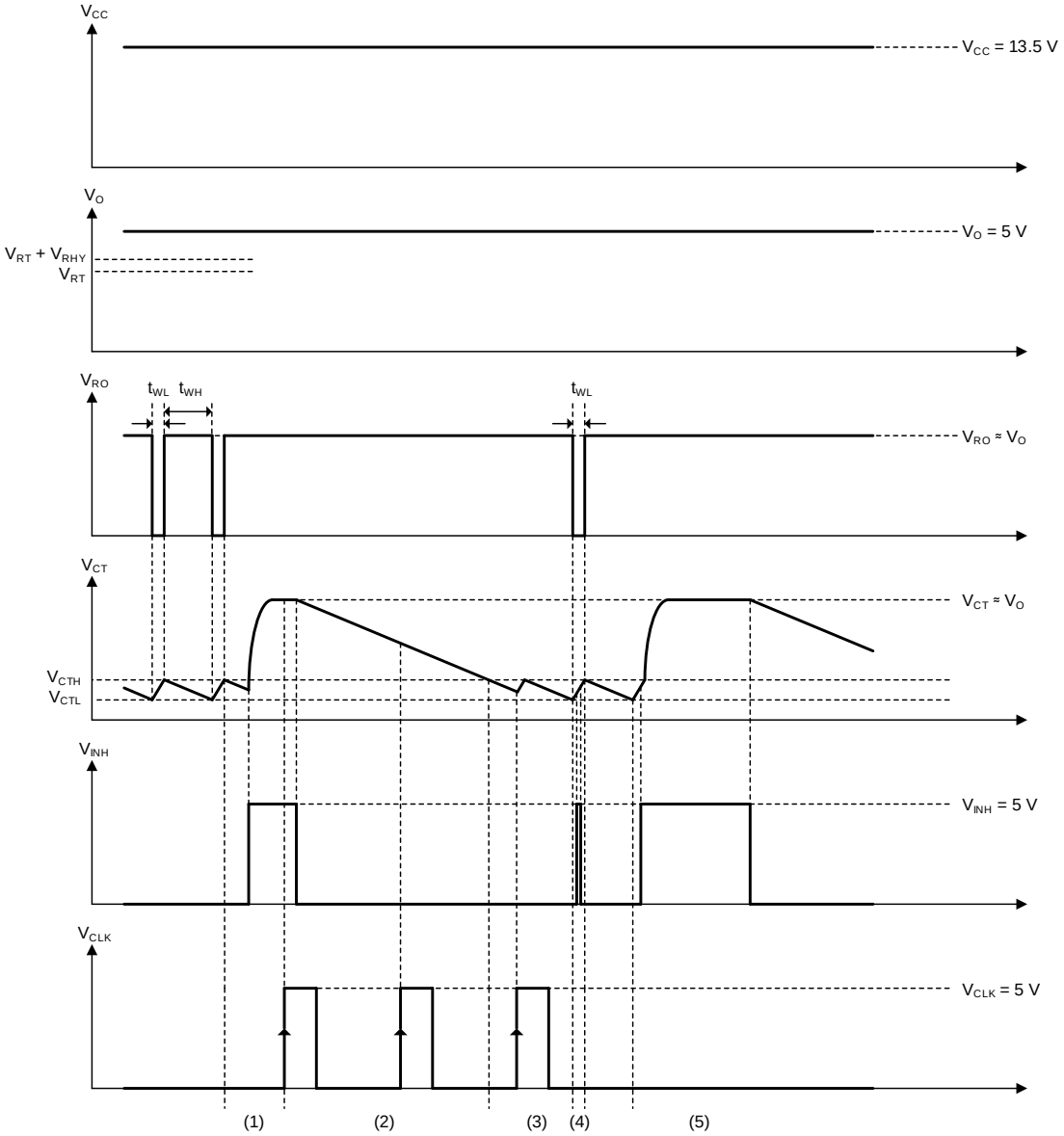


Figure 27. Timing Chart 3

A disabled WDT behavior on the INH inputs is described here.

INH function expects to use for writing to Micro Computer while stopping WDT function in the factory, so it is not designed to use RESET function with activating INH in the normal operation. Therefore, it cannot use for the normal operation with the limitation of WDT function, i.e. only using the function of LDO + RESET.

(1) If the H input(around V_O voltage) supplies to the INH pin, the CT pin is pulled up to the VO pin voltage internally. Since V_{CT} is maintained at higher voltage than or equal to V_{CTL}, it means WDT does not operate during the condition that $V_{RT} < V_O$, so RO can keep H output state.

(2) The charged electron of C_{CT} is dis-charged by CT Discharge Current(I_{CT_D}) when the INH pin is supplied L input or it keeps open. Even if the rising edge supplies to the CLK pin while the condition that $V_{CT} > V_{CTH}$, WDT does not detect this edge.

(3) WDT detects the rising edge during the condition that $V_{CTH} > V_{CT} > V_{CTL}$.

(4) While CT charging state, even if the H input supplies to INH, WDT is designed not to detect it. WDT only detects the INH signal while CT state is the dis-charging.

(5) If the electron charged to C_{CT} and V_{CT} reaches V_{CTH} while maintaining the INH pin at H, and if the constant current state of CT is switched from charging to dis-charging, WDT detects the INH signal. The CT pin is pulled up to the VO pin voltage same as (1), then RO can keep H output state.

Timing Chart - Continued

INH ON/OFF 2

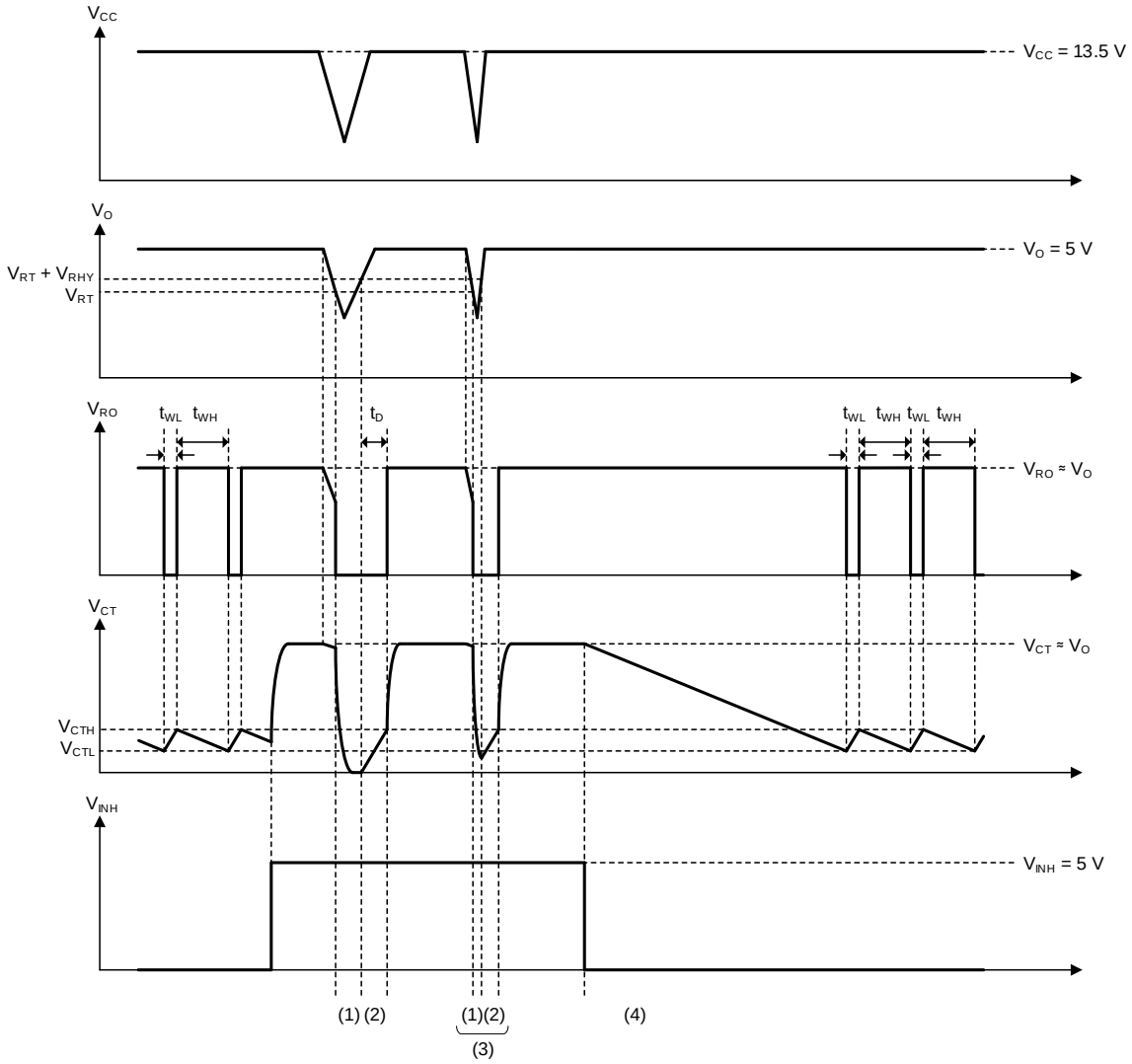


Figure 28. Timing Chart 4

(1) If the VO pin voltage changes across the threshold voltage of V_{RT}, while CT is pulled up to the VO pin voltage by INH signal, the constant current state of CT is forced to be changed as dis-charging in order to dis-charge the electron at C_{CT}. The RESET function judges the state as abnormal because VO voltage is lower than RESET detection voltage, therefore RO outputs L state.

(2) RESET and WDT starts operating when the output voltage becomes higher than V_{RT} + V_{RHY}, after RO output and the CT pin voltage become L by behavior of (1). If the electron charged to C_{CT} and V_{CT} reaches V_{CTH}, RO outputs H state. This (2) is t_D.

(3) As same as described in Timing Chart 1 (6), if the time period of changing VO voltage in (2) condition is too short, and if CT voltage cannot reach to V_{CTL} at once before going back VO voltage to across V_{RT}+V_{RHY}, the forced CT dis-charging state is canceled and turns back the state of (2). In this case, there is a possibility that t_D becomes shorter. This abnormal operation should be taken care when INH function uses for writing to Micro Computer while stopping WDT function in the factory.

(4) If the INH pin is supplied L input or it keeps open, the constant current state of CT changes from dis-charging to charging, WDT and RESET function operates continuously as following transition, $t_{WL} \rightarrow t_{WH} \rightarrow t_{WL} \rightarrow t_{WH} \rightarrow t_{WL}$….

Application and Implementation

Notice: The following information is given as a reference or hint for the application and the implementation. Therefore it does not guarantee its operation on the specific function, accuracy or external components in the application. In the application, it shall be designed with sufficient margin by enough understanding about characteristics of the external components, e.g. capacitor, and also by appropriate verification in the actual operating conditions.

Selection of External Components

Input Pin Capacitor

If the battery is placed far from the regulator or the impedance of the input-side is high, higher capacitance is required for the input capacitor in order to prevent the voltage-drop at the input line. The input capacitor and its capacitance should be selected depending on the line impedance which is between the input pin and the smoothing filter circuit of the power supply. Therefore the proper capacitance value which is selected by the consideration of the input impedance is different each application. Generally, the capacitor with capacitance value of 0.1 µF (Min) with good high frequency characteristic is recommended for this regulator.

In addition, to prevent an influence to the regulator's characteristic from the deviation or the variation of the external capacitor's characteristic, all input capacitors mentioned above is recommended to have a good DC bias characteristic and a temperature characteristic, e.g. approximately ±15 %, with being satisfied high absolute maximum voltage rating based on EIA standard. This capacitor must be placed close to the input pin and it's better to be mounted on the same board side of the regulator.

Output Pin Capacitor

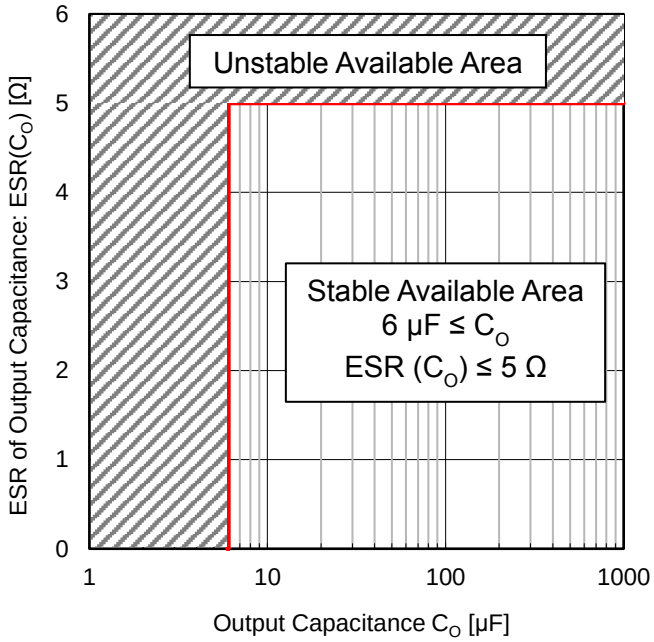
The output capacitor is mandatory for the regulator in order to realize stable operation. The output capacitor with capacitance value ≥ 6 µF (Min) and ESR up to 5 Ω (Max) must be required between the output pin and the GND pin.
A proper selection of appropriate both the capacitance value and ESR for the output capacitor can improve the transient behavior of the regulator and can also keep the stability with better regulation loop. The correlation of the output capacitance value and ESR is shown in the graph on the next page as the output capacitor's capacitance value and the stability region for ESR. As described in this graph, this regulator is designed to be stable with ceramic capacitors as of MLCC, with the capacitance value from 6 µF to 1000 µF and with ESR value within almost 0 Ω to 5 Ω. The frequency range of ESR can be generally considered as within about 10 kHz to 100 kHz.

Note that the provided the stable area of the capacitance value and ESR in the graph is obtained under a specific set of conditions which is based on the measurement result in single IC on our board with a resistive load. In the actual environment, the stability is affected by wire impedance on the board, input power supply impedance and also loads impedance, therefore please note that a careful evaluation of the actual application, the actual usage environment and the actual conditions should be done to confirm the actual stability of the system.

Generally, in the transient event which is caused by the input voltage fluctuation or the load fluctuation beyond the gain bandwidth of the regulation loop, the transient response ability of the regulator depends on the capacitance value of the output capacitor. Basically the capacitance value of ≥ 6 µF (Min) for the output capacitor is recommended as shown in the table on Output Capacitance C_{OUT}, ESR Available Area, however using bigger capacitance value can be expected to improve better the transient response ability in a high frequency. Various types of capacitors can be used for this high capacity of the output capacitor which includes electrolytic capacitor, electro-conductive polymer capacitor and tantalum capacitor. Noted that, depending on the type of capacitors, its characteristics which is ESR (≤ 5 Ω) absolute value range, a temperature dependency of capacitance value and increased ESR at cold temperature needs to be taken into consideration.

In addition, the same consideration should be taken as the input pin capacitor, to prevent an influence to the regulator's characteristic from the deviation or the variation of the external capacitor's characteristic, all output capacitors mentioned above is recommended to have a good DC bias characteristic and a temperature characteristic, e.g. approximately ±15 %, with being satisfied high absolute maximum voltage rating based on EIA standard. This capacitor must be placed close to the output pin and it's better to be mounted on the same board side of the regulator.

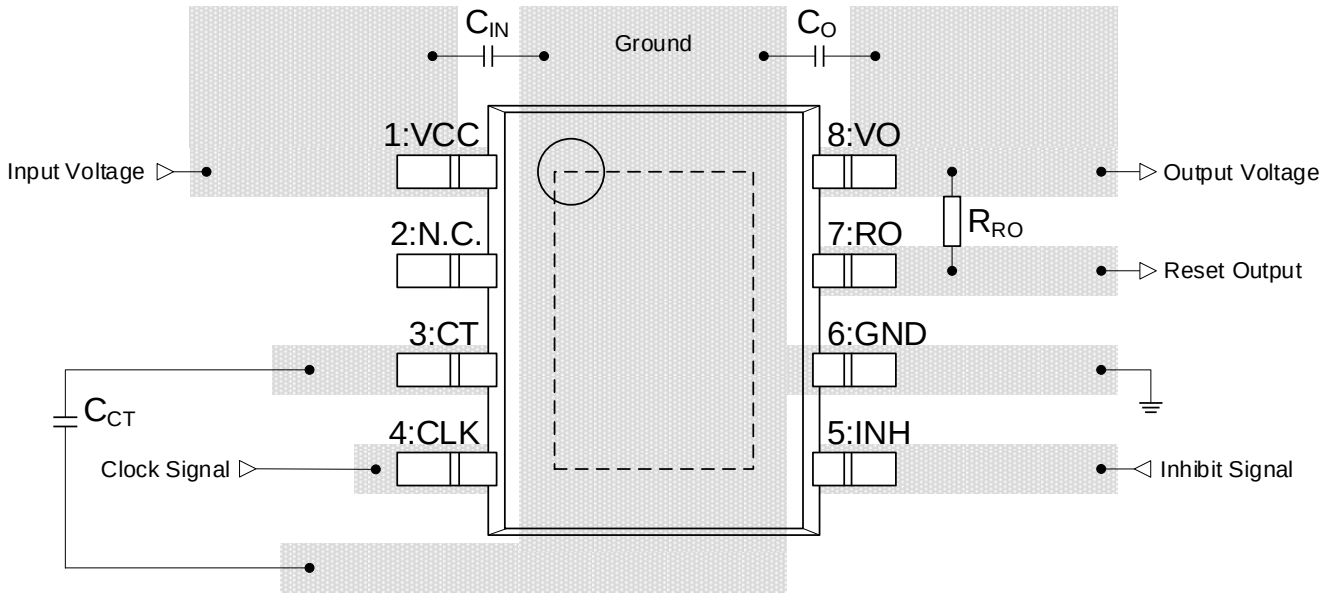
Application and Implementation - continued



Output Capacitance C_O, ESR Available Area
(-40 °C ≤ Tj ≤ +150 °C, 5.9 V ≤ V_{CC} ≤ 45 V, V_{INH} = 5 V, I_O = 0 mA to 200 mA)

Application and Implementation – continued

Typical Application and Layout Example



Parameter	Symbol	Reference Value for Application
Output Current	I_O	0 mA ≤ I_O ≤ 200 mA
Output Capacitor	C_O	6 µF ≤ C_O ≤ 1000 µF
ESR of Output Capacitor Capacitor	ESR (C_O)	ESR ≤ 5 Ω
Input Voltage	V_{CC}	5.9 V to 42.0 V
Input Capacitor*(Note 1)*	C_{IN}	0.1 µF ≤ C_{IN}
CT Pin Capacitor	C_{CT}	0.047 µF ≤ C_{CT} ≤ 10 µF
RO Pull-up Resistor	R_{RO}	5.1 kΩ ≤ R_{RO}

(Note 1) If the influence of the impedance at the power supply line cannot be ignored, the input capacitance value should be adjusted.

Application and Implementation - continued

Surge Voltage Protection for Linear Regulators

The following shows some helpful Tips to protect ICs from possible inputting surge voltage which exceeds absolute maximum ratings.

Positive surge to the input

If there is any potential risk that positive surges higher than absolute maximum ratings, (e.g.) 45 V, is applied to the input, a Zener Diode should be inserted between the VCC and the GND to protect the device as shown in Figure 29.

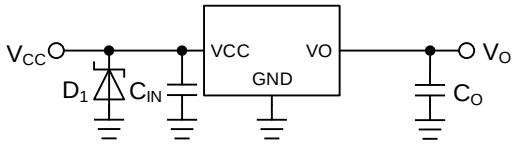


Figure 29. Surges Higher than 45 V is Applied to the Input

Negative surge to the input

If there is any potential risk that negative surges below the absolute maximum ratings, (e.g.) -0.3 V, is applied to the input, a Schottky Diode should be inserted between the VCC and the GND to protect the device as shown in Figure 30.

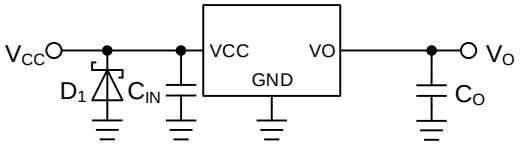


Figure 30. Surges Lower than -0.3 V is Applied to the Input

Reverse Voltage Protection for Linear Regulators

A linear regulator which is one of the integrated circuit (IC) operates normally in the condition that higher input voltage is always supplied than the output voltage. However, there is a possibility to happen the abnormal situation in specific conditions which is the output voltage becomes higher than the input voltage. A reverse polarity connection between the input and the output might be occurred or a certain inductor component can also cause a polarity reverse conditions. If the countermeasure is not implemented, it may cause damage to the IC. The following shows some helpful Tips to protect ICs from the reverse voltage occasion.

Protection Against Reverse Input /Output Voltage

In the case that MOS FET is used for the pass transistor, a parasitic body diode between the drain-source generally exists. If the output voltage becomes higher than the input voltage, and then if the voltage difference exceeds V_F of the body diode, a reverse current flows as from the output to the input through the body diode as shown in Figure 31. The current flows in the parasitic body diode is not limited in the protection circuit because it is the parasitic element, therefore too much reverse current may cause damage to degrade or destroy the semiconductor elements of the regulator.

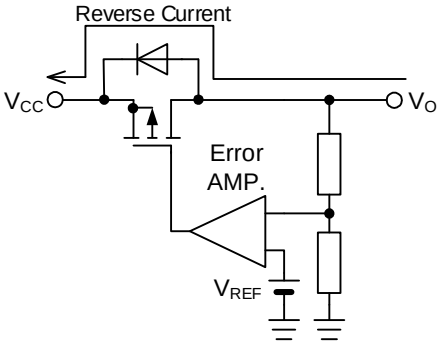


Figure 31. Reverse Current Path in a MOS Linear Regulator

Protection Against Reverse Input/Output Voltage – continued

An effective solution for this problem is to implement an external bypass diode in order to prevent the reverse current flow inside the IC as shown in Figure 32. Note that the bypass diode must be turned on prior to the internal body diode of the IC. This external bypass diode should be chosen as being lower forward voltage V_F than the internal body diode. It should to be selected a diode which has a rated reverse voltage greater than the IC's input maximum voltage and also which has a rated forward current greater than the anticipated reverse current in the actual application.

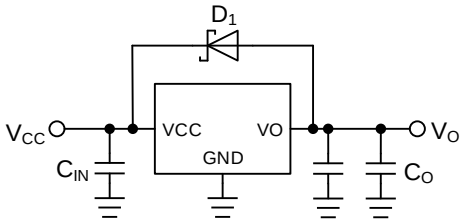


Figure 32. Bypass Diode for Reverse Current Diversion

A Schottky barrier diode which has a characteristic of low forward voltage (V_F) can meet to the requirement for the external diode to protect the IC from the reverse current, however it also has a characteristic that the leakage (I_R) caused by the reverse voltage is bigger than other diodes. Therefore, it should be taken into the consideration to choose it because if the leak current is large, it may cause increase of the current consumption simply, or raise of the output voltage in the light-load current condition. The I_R characteristic of Schottky diode has positive temperature characteristic, which the details shall be checked with the datasheet of the products, and the careful confirmation of behavior in the actual application is mandatory.

Even in the condition when the input/output voltage is inverted, if the VCC pin can be open as shown in Figure 33, or if the VCC pin can become high-impedance condition as designed in the system, it cannot damage or degrade the parasitic element. It's because a reverse current via the pass transistor becomes extremely low. In this case, therefore, the protection external diode is not necessary.

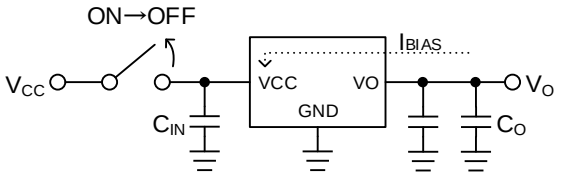


Figure 33. Open V_{CC}

Protection Against Input Reverse Voltage

When the input of the IC is connected to the power supply, accidentally if plus and minus are routed in reverse, or if there is a possibility that the input may become lower than the GND pin, a large current passes via the internal electrostatic breakdown prevention diode between the input pin and the GND pin as shown in Figure 34, thus it may cause to destroy the IC.

An implementation of a Schottky barrier diode or a rectifier diode connected in series to the power supply line as shown in Figure 35 is the simplest solution to prevent this problem. However, it increases a power loss calculated as $V_F \times I_{CC}$, and it also causes the voltage drop as a forward voltage V_F at the power supply line to the input of the IC.
Generally since the Schottky barrier diode has lower V_F, so it contributes to rather smaller power loss than rectifier diodes. If IC has load currents, the required input current to the IC is also bigger. In this case, this external diode generates heat more, therefore it should be taken into the consideration of a selection for diode with enough margin in power dissipation. On the other hands, in the reverse connection condition, a reverse current passes this diode, however, it can be negligible because its small amount.

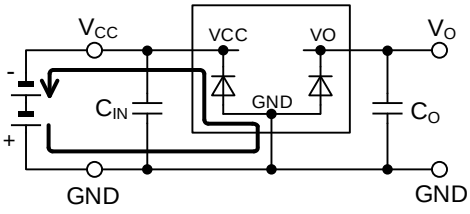


Figure 34. Current Path in Reverse Input Connection

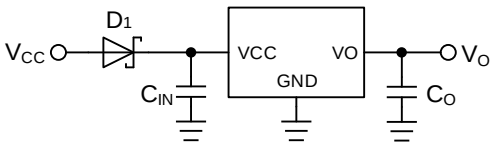


Figure 35. Protection against Reverse Polarity 1

Protection Against Input Reverse Voltage - continued

Figure 36 shows a circuit in which a P-channel MOSFET is connected in series to the power. The body diode (parasitic element) is located in the drain-source junction area of the MOSFET. The drop voltage in a forward connection is calculated from the On state resistance of the MOSFET and the output current I_O. Therefore, it is smaller than the drop voltage by the diode as shown in Figure 35 and results in less of a power loss. No current flows in a reverse connection where the MOSFET remains off in Figure 36.

If the gate-source voltage exceeds maximum rating of MOSFET gate-source junction with derating curve in consideration, reduce the gate-source junction voltage by connecting resistor voltage divider as shown in Figure 37.

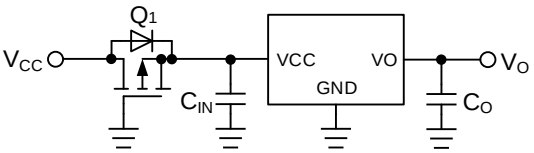


Figure 36. Protection against Reverse Polarity 2

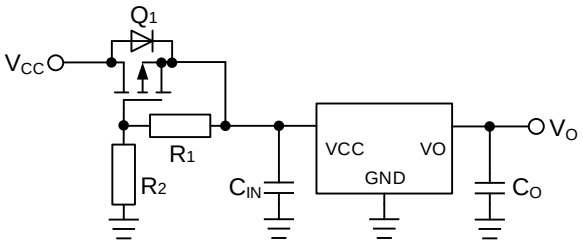


Figure 37. Protection against Reverse Polarity 3

Protection Against Reverse Output Voltage when Output Connect to an Inductor

If the output load is inductive, electrical energy accumulated in the inductive load is released to the ground at the moment that the output voltage is turned off. IC integrates ESD protection diodes between the IC output and ground pins, which a large current may flows in such condition finally resulting on destruction of the IC. To prevent this situation, connect a Schottky barrier diode in parallel to the diode as shown in Figure 38.

Further, if a long wire is in use for the connection between the output pin of the IC and the load, confirm that the negative voltage is not generated at the VO pin when the output voltage is turned off by observation of the waveform on an oscilloscope, since it is possible that the load becomes inductive. An additional diode is required for a motor load that is affected by its counter electromotive force, as it produces an electrical current in a similar way.

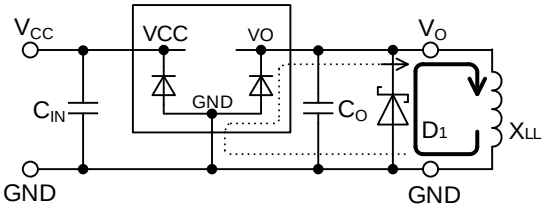


Figure 38. Current Path in Inductive Load (Output: Off)

Power Dissipation

HTSOP-J8

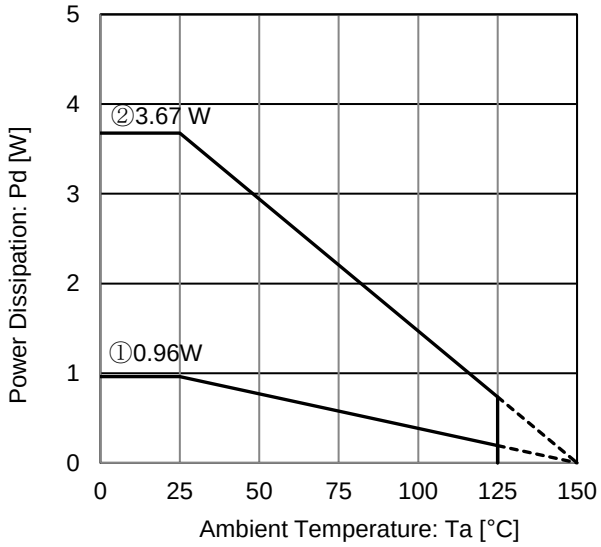


Figure 39. HTSOP-J8 Package Data

IC mounted on ROHM standard board based on JEDEC.
① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB:
74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB:
74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 130 °C/W, Ψ_{JT} (top center) = 15 °C/W
Condition②: θ_{JA} = 34 °C/W, Ψ_{JT} (top center) = 7 °C/W

Thermal Design

This product exposes a frame on the back side of the package for thermal efficiency improvement.
Within this IC, the power consumption is decided by the dropout voltage condition, the load current and the circuit current. The power dissipation changes by ambient temperature. Refer to power dissipation curves illustrated in Figure 39 when using the IC in an environment of Ta ≥ 25 °C. Even if the ambient temperature Ta is at 25 °C, depending on the input voltage and the load current, chip junction temperature can be very high. Consider the design to be Tj ≤ Tjmax = 150 °C in all possible operating temperature range.
Should by any condition the maximum junction temperature Tjmax = 150 °C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Because this value may be different from actual use environment, caution is required. Verify the application and allow sufficient margins in the thermal design by using the following formula to calculate the junction temperature Tj.
Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature Tj by ambient temperature.

$$Tj = Ta + P_C \times \theta_{JA} \ [°C]$$

where

Tj	is Junction Temperature
Ta	is Ambient Temperature
P_C	is Power Consumption
θ_{JA}	is Thermal Impedance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature Tj by top center of case's (mold) temperature.

$$Tj = T_T + P_C \times \Psi_{JT} \ [°C]$$

where

Tj	is Junction Temperature
T_T	is Top Center of Case's (mold) Temperature
P_C	is Power Consumption
Ψ_{JT}	is Thermal Impedance (Junction to Top Center of Case)

The following method is used to calculate the power consumption Pc (W).

$$Pc = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC} \ [W]$$

where

P_C	is Power Consumption
V_{CC}	is Supply Voltage
V_O	is Output Voltage
I_O	is Load Current
I_{CC}	is Circuit Current

Calculation Example

If V_{CC} = 13.5 V, V_O = 5.0 V, I_O = 100 mA, I_{CC} = 6 μA, the power consumption P_C can be calculated as follows:

$$\begin{aligned} P_C &= (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC} \\ &= (13.5V - 5.0\ V) \times 100\ mA + 13.5\ V \times 6\ \mu A \\ &= 0.85\ W \end{aligned}$$

At the ambient temperature Tamax = 85°C, the thermal impedance (Junction to Ambient) θ_{JA} = 34.0 °C/W(4-layer PCB)

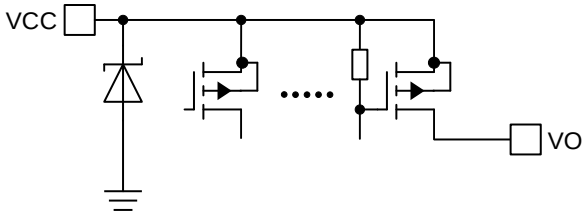
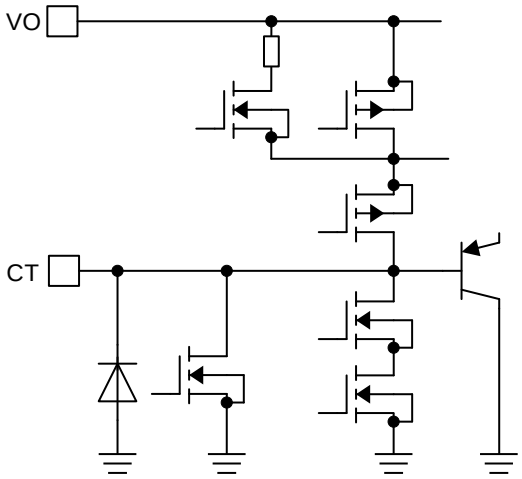
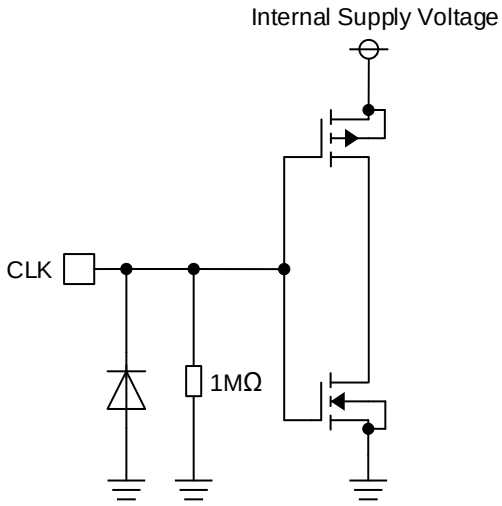
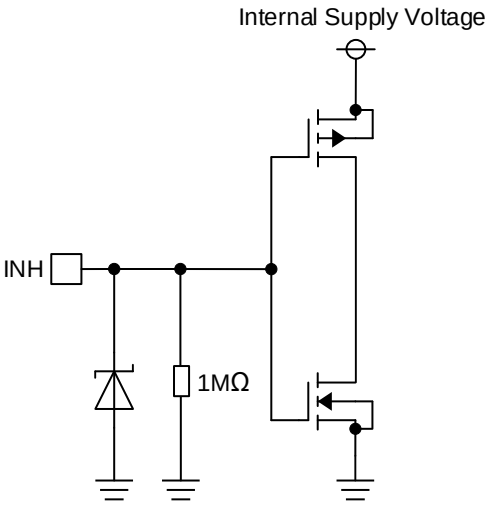
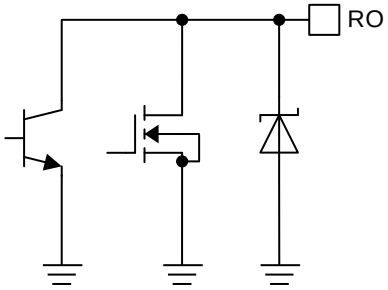
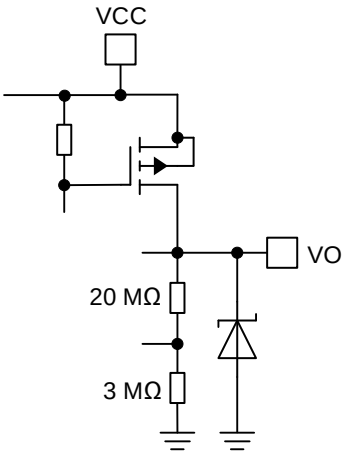
$$\begin{aligned} Tj &= Tamax + P_C \times \theta_{JA} \\ &= 85\ °C + 0.85\ W \times 34.0\ °C/W \\ &= 113.9\ °C \end{aligned}$$

When operating the IC, the top center of case's (mold) temperature T_T = 108 °C, Ψ_{JT} = 7 °C/W(4-layer PCB)

$$\begin{aligned} Tj &= T_T + P_C \times \Psi_{JT} \\ &= 108\ °C + 0.85\ W \times 7\ °C/W \\ &= 113.95\ °C \end{aligned}$$

If margin is not secured by the calculation mentioned above, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad for optimum thermal performance.

I/O Equivalence Circuit(Note 1)

1. VCC	3. CT
	
4. CLK	**5. INH**
	
7. RO	**8. VO**
	

(Note 1) Resistance value is Typical.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Thermal Consideration
   The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. The amount of heat generation depends on the voltage difference between the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating. If Junction temperature is over Tjmax (=150 °C), IC characteristics may be worse due to rising chip temperature. Heat resistance in specification is measurement under PCB condition and environment recommended in JEDEC. Ensure that heat resistance in specification is different from actual environment.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

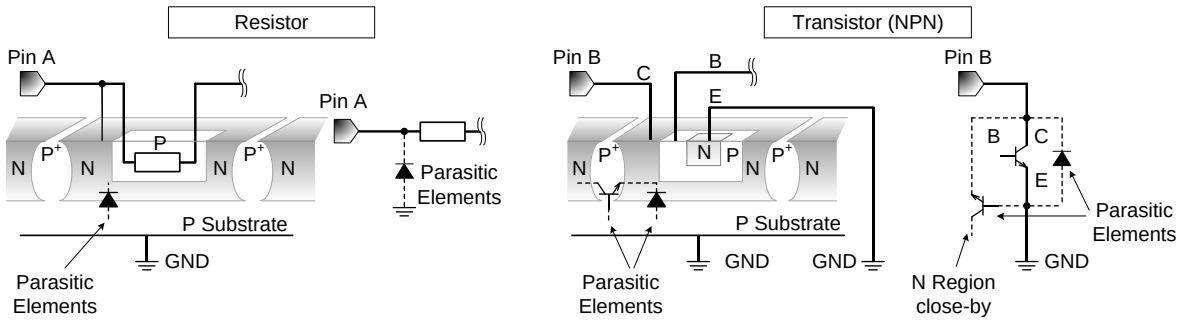


Figure 40. Example of IC Structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

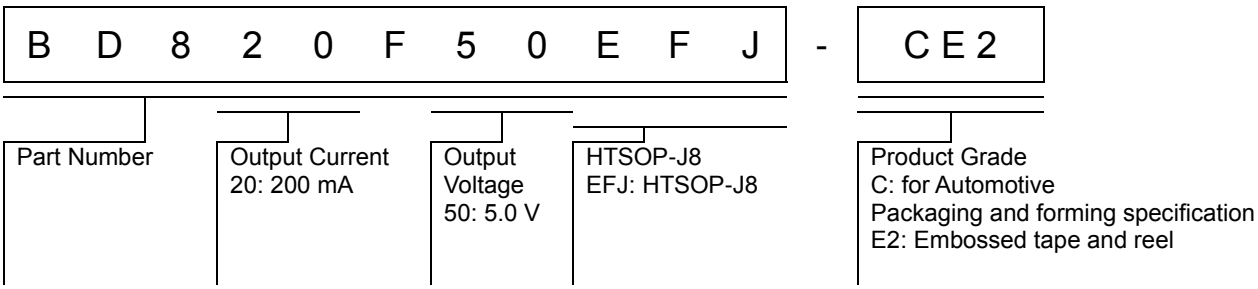
13. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

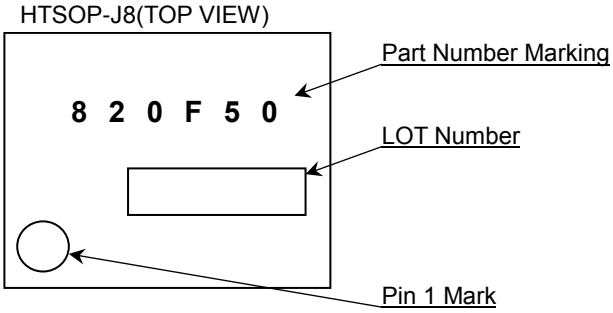
14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

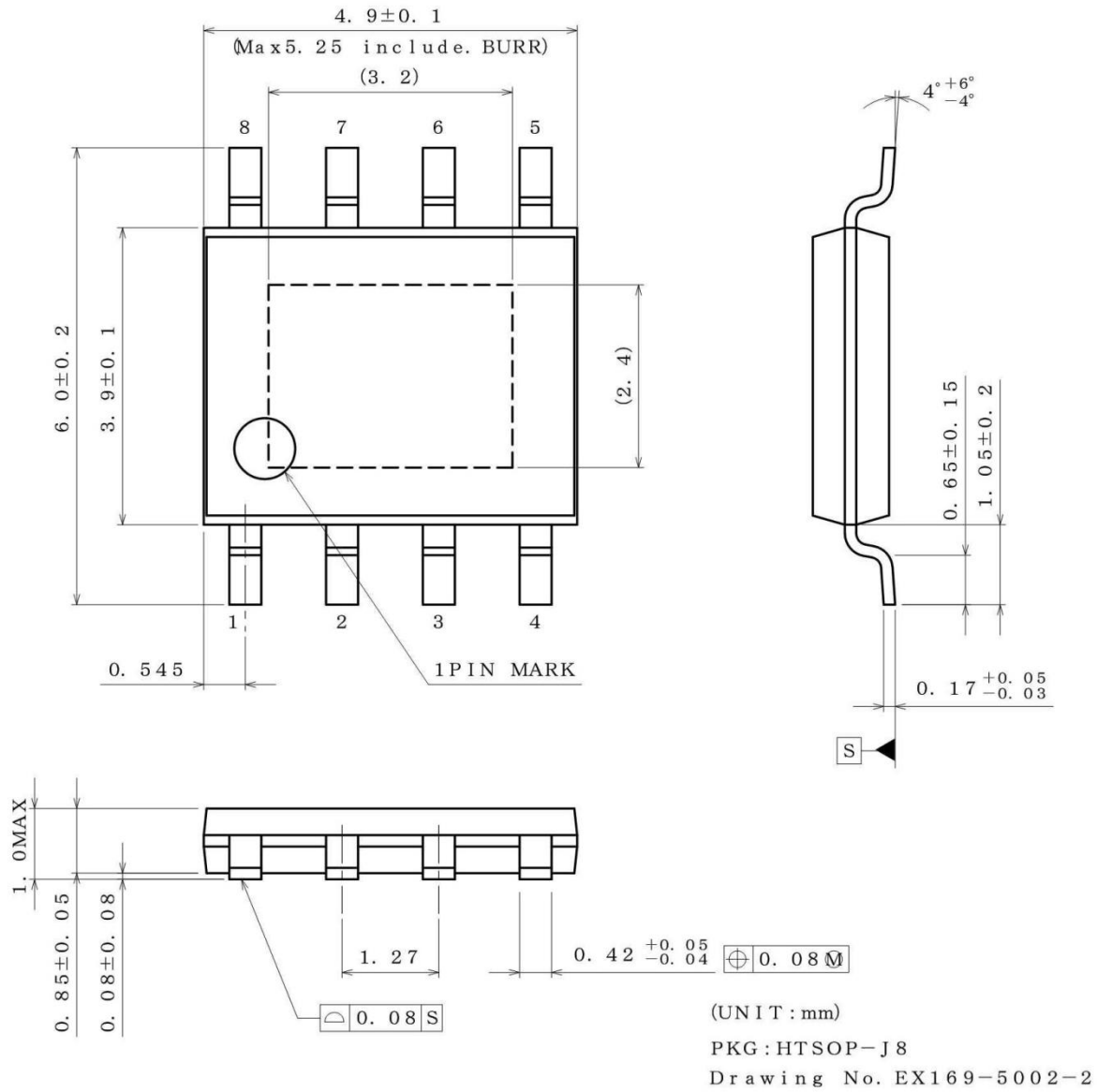


Marking Diagram



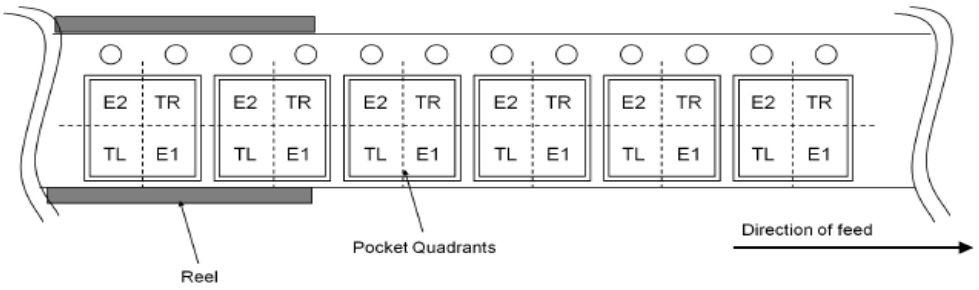
Physical Dimension and Packing Information

Package Name	HTSOP-J8



<Tape and Reel information>

Tape	**Embossed carrier tape**
Quantity	**2500pcs**
Direction of feed	**E2** **(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)**



Revision History

Date	Revision	Changes
17.Dec.2018	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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