System Motor Driver Series for CD･DVD･BD Player

9ch System Motor Driver For Car AV

BD8256EFV-M

General Description

BD8256EFV-M is a 9ch motor driver developed for driving coil actuator (3ch), sled motor (2ch), a loading motor, and a three-phase motor for spindle. This chip has a built-in 2ch LVDS (Low Voltage Differential Signaling) output for spherical aberration. This can drive the motor and coil of blu-ray drive.
It has a built-in Serial Peripheral Interface (SPI) with a max clock frequency of 35MHz, for interfacing with the Micro-controller.

Features

- Built-in Serial Peripheral Interface(SPI)
- High efficiency at 180° PWM for spindle driver
- Built-in 2-channel stepping motor driver for sled
- Built-in actuator over current protection circuit
- Built-in loading driver short-circuit protection
- AEC-Q100 Qualified

Applications

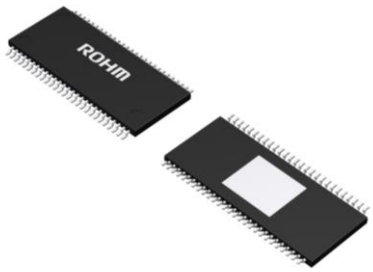
- Car navigation
- Car AV

Key Specifications

- Ron(Spindle): 1.0Ω(Typ)
- Ron(Loading): 1.5Ω(Typ)
- Power Supply Voltage Range: 4.5V to 10.5V

Package

	W(Typ) × D(Typ) × H(Max)
HTSSOP-B54	18.50mm × 9.50mm × 1.00mm



HTSSOP-B54

Typical Application Circuit

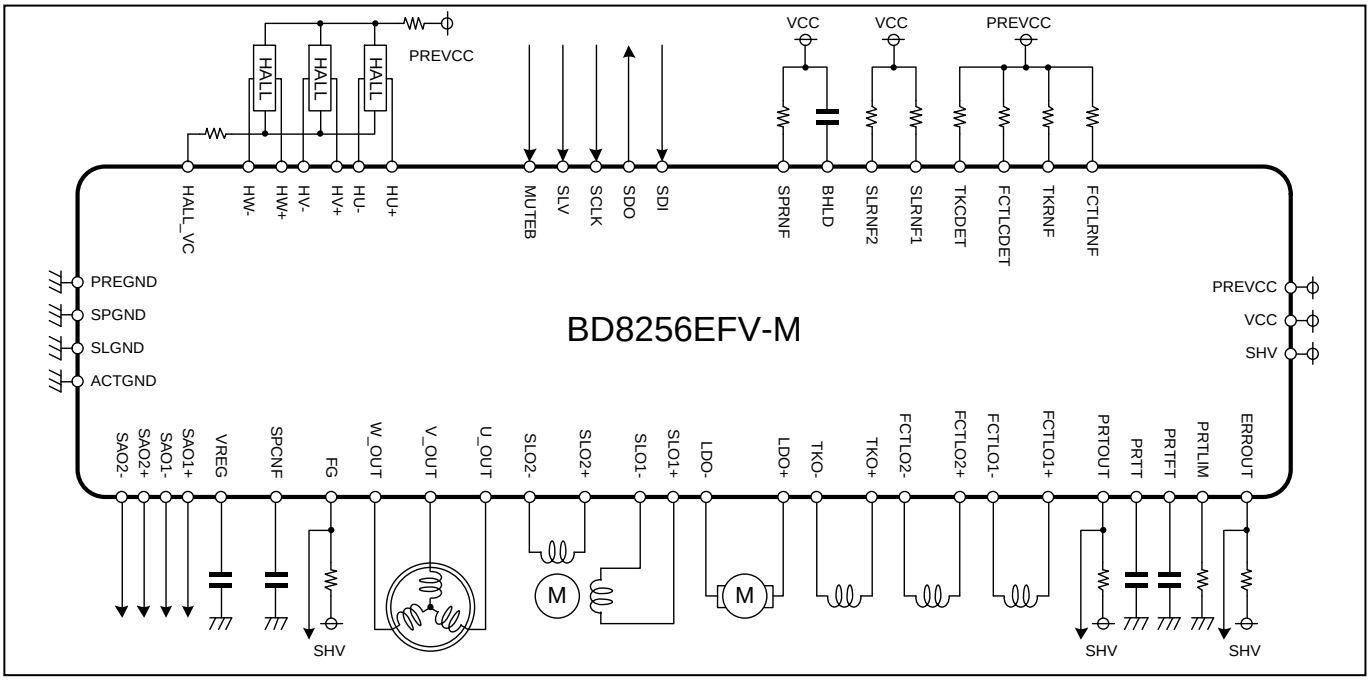


Figure 1. Typical Application Circuit

Pin Configuration (TOP VIEW)

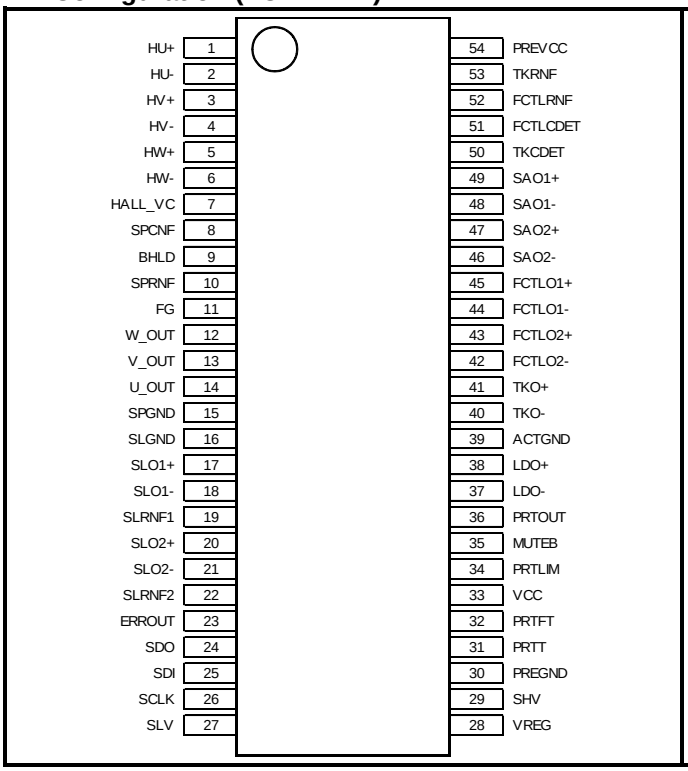


Figure 2. Pin configuration

Block Diagram

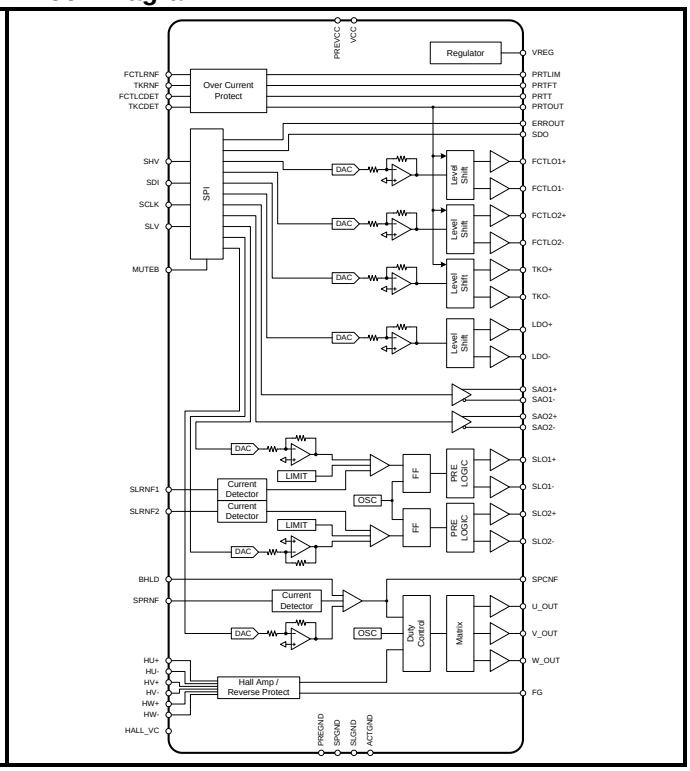


Figure 3. Block diagram

Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	HU+	Hall amp. U positive input	28	VREG	Inside power supply for SPI logic
2	HU-	Hall amp. U negative input	29	SHV	Power supply for SDO output
3	HV+	Hall amp. V positive input	30	PREGND	Pre block ground
4	HV-	Hall amp. V negative input	31	PRTT	Protect time setting for tracking
5	HW+	Hall amp. W positive input	32	PRTFT	Protect time setting for focus and tilt
6	HW-	Hall amp. W negative input	33	VCC	Power supply for pre driver and loading
7	HALL_VC	Hall bias	34	PRTLIM	Limit setting for actuator protect
8	SPCNF	Spindle driver loop filter	35	MUTEB	Mute input
9	BHLD	Spindle current bottom hold	36	PRTOUT	Protect output
10	SPRNF	Spindle power supply and current sense	37	LDO-	Loading driver negative output
11	FG	FG output	38	LDO+	Loading driver positive output
12	W_OUT	Spindle driver W output	39	ACTGND	Actuator and loading power ground
13	V_OUT	Spindle driver V output	40	TKO-	Tracking driver negative output
14	U_OUT	Spindle driver U output	41	TKO+	Tracking driver positive output
15	SPGND	Spindle power ground	42	FCTLO2-	Focus tilt driver 2 negative output
16	SLGND	Sled power ground	43	FCTLO2+	Focus tilt driver 2 positive output
17	SLO1+	Sled driver 1 positive output	44	FCTLO1-	Focus tilt driver 1 negative output
18	SLO1-	Sled driver 1 negative output	45	FCTLO1+	Focus tilt driver 1 positive output
19	SLRNF1	Sled 1 power supply and current sense	46	SAO2-	Sphere aberration 2 negative output
20	SLO2+	Sled driver 2 positive output	47	SAO2+	Sphere aberration 2 positive output
21	SLO2-	Sled driver 2 negative output	48	SAO1-	Sphere aberration 1 negative output
22	SLRNF2	Sled 2 power supply and current sense	49	SAO1+	Sphere aberration 1 positive output
23	ERROUT	Serial data error output	50	TKCDET	Current detect for tracking drive
24	SDO	Serial data output	51	FCTLCDET	Current detect for focus tilt drive
25	SDI	Serial data input	52	FCTLRNF	Focus tilt power supply and current sense
26	SCLK	Serial clock input	53	TKRNF	Tracking power supply and current sense
27	SLV	Serial slave input	54	PREVCC	Pre driver power supply

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Pre Power supply voltage	V_{VCC}	15	V
Power MOS power supply voltage	V_{SPRNF},V_{SLRNF1},V_{SLRNF2}	15	V
PWM control / BTL power supply voltage	V_{PREVCC},V_{TKRNF},$V_{FCTLRNF}$	7	V
Serial Output power supply	V_{SHV}	7	V
Input pin voltage 1	V_{IN1} (1)	15	V
Input pin voltage 2	V_{IN2} (2)	7	V
Output pin voltage 1	V_{OUT1} (3)	15	V
Output pin voltage 2	V_{OUT2} (4)	7	V
Power Consumption	Pd	2.0 (5)	W
Operating temperature range	Topr	-40 to +90	°C
Storage temperature range	Tstg	-55 to +150	°C
Junction temperature	Tjmax	150	°C

(1) BHLD, SPCNF
(2) HU+, HU-, HV+, HV-, HW+, HW-, HALL_VC, PRTFT, PRTT, SLV, SCLK, SDI, TKCDET, FCTLCDET, MUTEB
(3) FG, U_OUT, V_OUT, W_OUT, SLO1+, SLO1-, SLO2+, SLO2-, ERROUT, PRTLIM, PRTOUT, LDO+, LDO-
(4) SDO, VREG, FCTLO1+, FCTLO1-, FCTLO2+, FCTLO2-, TKO+, TKO-, SAO1+, SAO1-, SAO2+, SAO2-
(5) Ta=25°C, PCB (70mm × 70mm × 1.6mm, glass epoxy standard board) mounting.
Derated by 16mW/°C when operating above 25°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

Recommended Operating Ratings (Ta = -40°C to +90°C)

Parameter	Symbol	Limits			Unit
		Min.	Typ	Max.	
Pre /Loading driver power supply voltage (6)	V_{VCC}	4.5	8	10.5	V
Spindle driver power supply voltage (6)(7)	V_{SPRNF}	-	V_{VCC}	-	V
Sled motor driver power supply voltage (6)(7)	V_{SLRNF1}, V_{SLRNF2}	-	V_{VCC}	-	V
PWM control power supply voltage (6)	V_{PREVCC}	4.5	5	5.5	V
Actuator driver power supply voltage (6)	$V_{FCTLRNF}$, V_{TKRNF}	4.5	5	V_{PREVCC}	V
Serial output power supply (6)	V_{SHV}	3.0	3.3	3.6	V

(6) Consider power consumption when deciding power supply voltage.
(7) Set the voltage same as V_{VCC}.

Electrical Characteristics (Unless otherwise specified, Ta=25°C, V_{VCC}=V_{SPRNF}=V_{SLRNF1}=V_{SLRNF2}=8V, V_{PREVCC}=V_{TKRNF}=$V_{FCTLRNF}$=5V, V_{SHV}=3.3V, R_{SPRNF}=0.33Ω, R_{SLRNF}=0.56Ω)

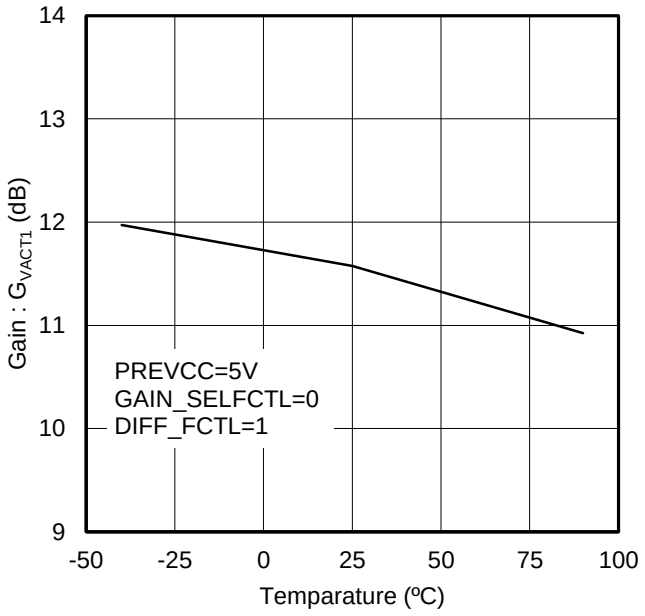
Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ	Max.		
Circuit Current						
PREVCC Quiescent Current	I_{Q1}	-	18	30	mA	MUTEB=High
VCC Quiescent Current	I_{Q2}	-	7	14	mA	SPI=72h FE, 70h FE
PREVCC Standby Current	I_{ST1}	-	3	6	mA	MUTEB=Low
VCC Standby Current	I_{ST2}	-	1	2	mA	
Spindle Driver						
Hall Bias Voltage	V_{HB}	0.45	0.9	1.35	V	IHB=10mA
Input Bias Current	I_{HIB}	-	0.5	3	μA	
Input Level	V_{HIM}	50	-	-	mVpp	
Common Mode Input Range	V_{HICM}	1.5	-	3.8	V	
Input Dead Zone (One Side)	V_{DZSP}	0	10	40	mV	
Input-Output Gain	gm_{SP}	0.98	1.24	1.50	A/V	R_{SPRNF}=0.33Ω, R_L=2Ω
Output ON Resistance (Total Sum)	R_{ONSP}	-	1	1.8	Ω	IL=500mA
Output limit Current	I_{LIMSP}	0.85	1.06	1.27	A	R_{SPRNF}=0.33Ω
PWM Frequency	f_{OSC}	-	100	-	kHz	R_L=2Ω
FG Output Low Level Voltage	V_{FGL}	-	0.1	0.3	V	33KΩ pull-up(3.3V)
Sled Motor Driver						
Input Dead Zone (One Side)	V_{DZSL}	5	15	30	mV	
Input-Output Gain	gm_{SL}	0.84	1.10	1.36	A/V	$R_{SLRNF1,2}$=0.56Ω, R_L=8Ω
Output ON Resistance (Total sum)	R_{ONSL}	-	2.2	3.3	Ω	IL=500mA
Output Limit Current	I_{LIMSL}	0.79	0.93	1.07	A	$R_{SLRNF1,2}$=0.56Ω
PWM Frequency	f_{OSC}	-	100	-	kHz	R_L=8Ω
Actuator Driver						
Output Offset Voltage	V_{OFACT}	-50	0	50	mV	Low Gain mode, R_L=8Ω
Output ON Resistance	R_{ONACT}	-	1.5	2.0	Ω	IL=500mA
Voltage Gain 1	G_{VACT1}	10.5	11.7	12.9	dB	Low Gain mode, R_L=8Ω
Voltage Gain 2	G_{VACT2}	16.4	17.7	18.9	dB	High Gain mode, R_L=8Ω
Loading Driver						
Output Offset Voltage	V_{OFLD}	-100	0	100	mV	Low Gain mode, R_L=8Ω
Output ON Resistance	R_{ONLD}	-	1.5	2.5	Ω	IL=500mA
Voltage Gain 1	G_{VLD1}	15.2	17.2	19.2	dB	Low Gain mode, R_L=8Ω
Voltage Gain 2	G_{VLD2}	16.7	18.7	20.7	dB	High Gain mode, R_L=8Ω
Actuator Protection Circuit						
PRTT/PRTF Default Voltage	V_{PRTREF}	1.00	1.06	1.12	V	
PRTT/PRTF Protect Detection Voltage	V_{PRTDET}	2.77	2.95	3.13	V	
PRTLIM Voltage	V_{PRTLIM}	500	530	560	mV	
Detection Input Offset Voltage	V_{OFDET}	-5	0	5	mV	
Protect Sign Output						
PRTOUT Low Level Output Voltage	V_{OL1}	-	0.1	0.3	V	33kΩ pull-up(3.3V)
ERROUT Low Level Output Voltage	V_{OL2}	-	0.1	0.3	V	33kΩ pull-up(3.3V)
Logic Inputs (SDI,SCLK,SLV,MUTEB)						
Low Level Input Voltage	V_{INL}	-	-	0.5	V	
High Level Voltage	V_{INH}	2.2	-	-	V	
High Level Current (SDI,SCLK,MUTEB)	I_{INH}	-	33	66	μA	SDI,SCLK,MUTEB=3.3V
Low Level Current (SLV)	I_{INL}	-60	-30	-	μA	SLV=0V
Function						
VCC Drop Mute Voltage	V_{MVCC}	3.4	3.8	4.2	V	
LVDS Output						
Difference Movement Output Voltage	V_{OD}	250	-	950	mV	R_L=100Ω
Offset Voltage	V_{OC}	0.95	1.25	1.55	V	R_L=100Ω
TSD						
TSD Junction Temperature(1)	T_{TSD}	150	175	200	°C	
TSD Hysteresis Temperature(1)	T_{HYS}	-	25	-	°C	

(1) These items are specified by design,not tested during production

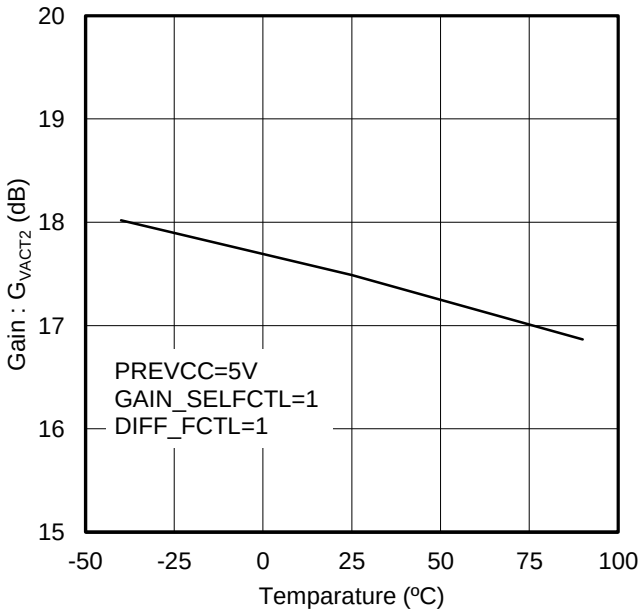
Electrical Characteristics (Unless otherwise specified, Ta=-40°C~90°C, V_{VCC}=V_{SPRNF}=V_{SLRNF1}=V_{SLRNF2}=8V, V_{PREVCC}=V_{TKRNF}=$V_{FCTLRNF}$=5V, V_{SHV}=3.3V, R_{SPRNF}=0.33Ω, R_{SLRNF}=0.56Ω)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ	Max.		
Circuit Current						
PREVCC Quiescent Current	I_{Q1}	-	18	36	mA	MUTEB=High
VCC Quiescent Current	I_{Q2}	-	7	14	mA	SPI=72h FE, 70h FE
PREVCC Standby Current	I_{ST1}	-	3	6	mA	MUTEB=Low
VCC Standby Current	I_{ST2}	-	1	2	mA	
Spindle Driver						
Hall Bias Voltage	V_{HB}	0.45	0.9	1.35	V	IHB=10mA
Input Bias Current	I_{HIB}	-	0.5	3	μA	
Input Level	V_{HIM}	50	-	-	mVpp	
Common Mode Input Range	V_{HICM}	1.5	-	3.8	V	
Input Dead Zone (One Side)	V_{DZSP}	0	10	45	mV	
Input-Output Gain	gm_{SP}	0.85	1.24	1.63	A/V	R_{SPRNF}=0.33Ω, R_L=2Ω
Output ON Resistance (Total Sum)	R_{ONSP}	-	1	1.8	Ω	IL=500mA
Output limit Current	I_{LIMSP}	0.85	1.06	1.27	A	R_{SPRNF}=0.33Ω
PWM Frequency	f_{OSC}	-	100	-	kHz	R_L=2Ω
FG Output Low Level Voltage	V_{FGL}	-	0.1	0.3	V	33KΩ pull-up(3.3V)
Sled Motor Driver						
Input Dead Zone (One Side)	V_{DZSL}	3	15	35	mV	
Input-Output Gain	gm_{SL}	0.84	1.10	1.36	A/V	$R_{SLRNF1,2}$=0.56Ω, R_L=8Ω
Output ON Resistance (Total sum)	R_{ONSL}	-	2.2	3.3	Ω	IL=500mA
Output Limit Current	I_{LIMSL}	0.79	0.93	1.07	A	$R_{SLRNF1,2}$=0.56Ω
PWM Frequency	f_{OSC}	-	100	-	kHz	R_L=8Ω
Actuator Driver						
Output Offset Voltage	V_{OFACT}	-50	0	50	mV	Low Gain mode, R_L=8Ω
Output ON Resistance	R_{ONACT}	-	1.5	2.0	Ω	IL=500mA
Voltage Gain 1	G_{VACT1}	9.4	11.7	13.5	dB	Low Gain mode, R_L=8Ω
Voltage Gain 2	G_{VACT2}	15.4	17.7	19.5	dB	High Gain mode, R_L=8Ω
Loading Driver						
Output Offset Voltage	V_{OFLD}	-110	0	110	mV	Low Gain mode, R_L=8Ω
Output ON Resistance	R_{ONLD}	-	1.5	2.5	Ω	IL=500mA
Voltage Gain 1	G_{VLD1}	14.1	17.2	19.5	dB	Low Gain mode, R_L=8Ω
Voltage Gain 2	G_{VLD2}	15.6	18.7	21.0	dB	High Gain mode, R_L=8Ω
Actuator Protection Circuit						
PRTT/PRTF Default Voltage	V_{PRTREF}	0.98	1.06	1.14	V	
PRTT/PRTF Protect Detection Voltage	V_{PRTDET}	2.65	2.95	3.25	V	
PRTLIM Voltage	V_{PRTLIM}	490	530	570	mV	
Detection Input Offset Voltage	V_{OFDET}	-7	0	7	mV	
Protect Sign Output						
PRTOUT Low Level Output Voltage	V_{OL1}	-	0.1	0.3	V	33kΩ pull-up(3.3V)
ERROUT Low Level Output Voltage	V_{OL2}	-	0.1	0.3	V	33kΩ pull-up(3.3V)
Logic Inputs (SDI,SCLK,SLV,MUTEB)						
Low Level Input Voltage	V_{INL}	-	-	0.5	V	
High Level Voltage	V_{INH}	2.2	-	-	V	
High Level Current (SDI,SCLK,MUTEB)	I_{INH}	-	33	75	μA	SDI,SCLK,MUTEB=3.3V
Low Level Current (SLV)	I_{INL}	-75	-30	-	μA	SLV=0V
Function						
VCC Drop Mute Voltage	V_{MVCC}	3.4	3.8	4.2	V	
LVDS Output						
Difference Movement Output Voltage	V_{OD}	250	-	950	mV	R_L=100Ω
Offset Voltage	V_{OC}	0.95	1.25	1.55	V	R_L=100Ω

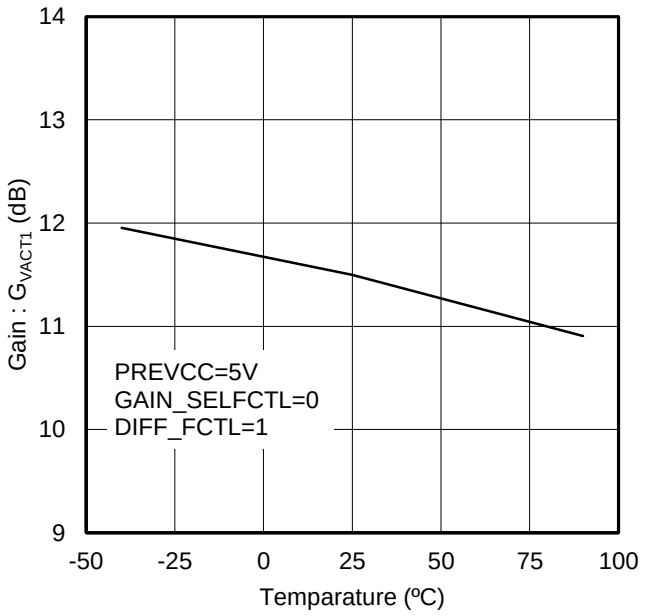
Typical Performance Curves



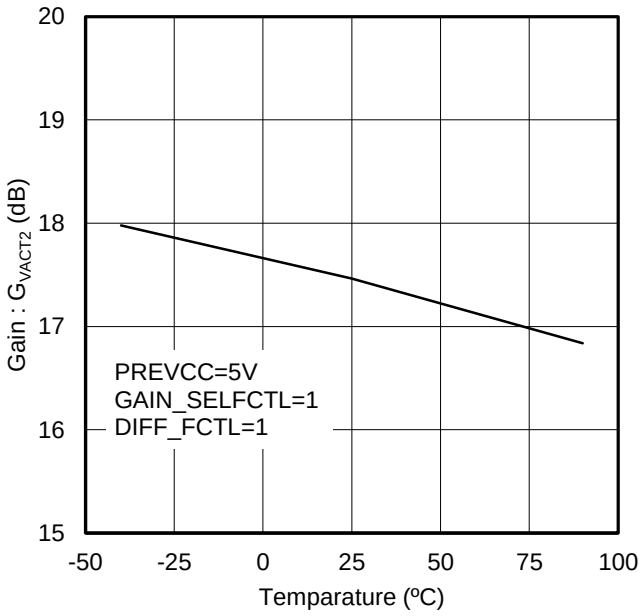
FCTL1 Voltage gain 1 (Low gain mode)



FCTL1 Voltage gain 2 (High gain mode)

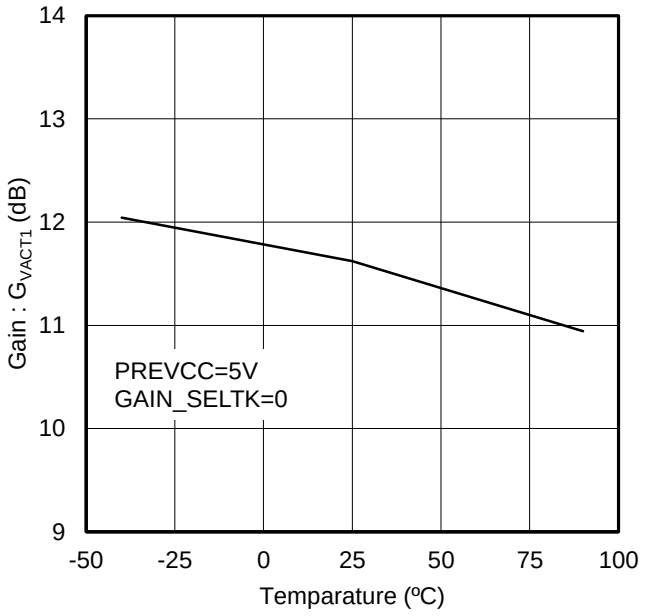


FCTL2 Voltage gain 1 (Low gain mode)

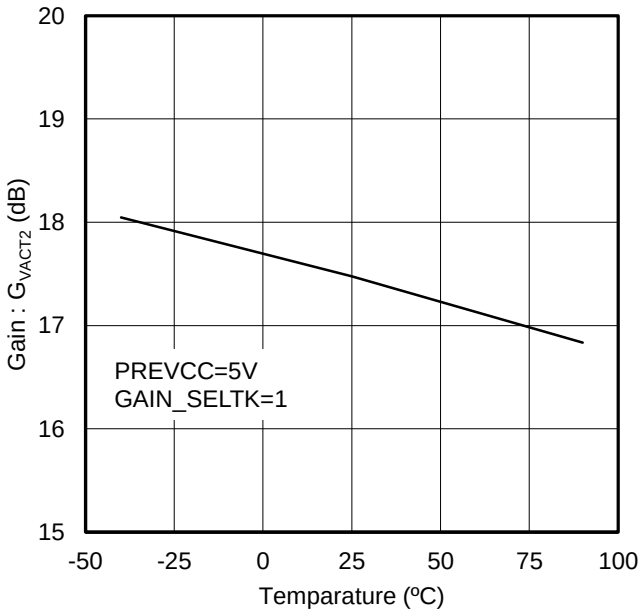


FCTL2 Voltage gain 2 (High gain mode)

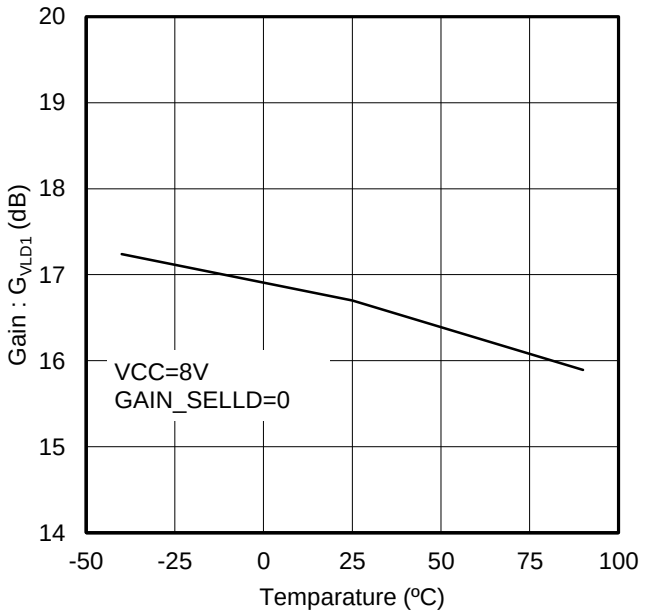
Typical Performance Curves - continued



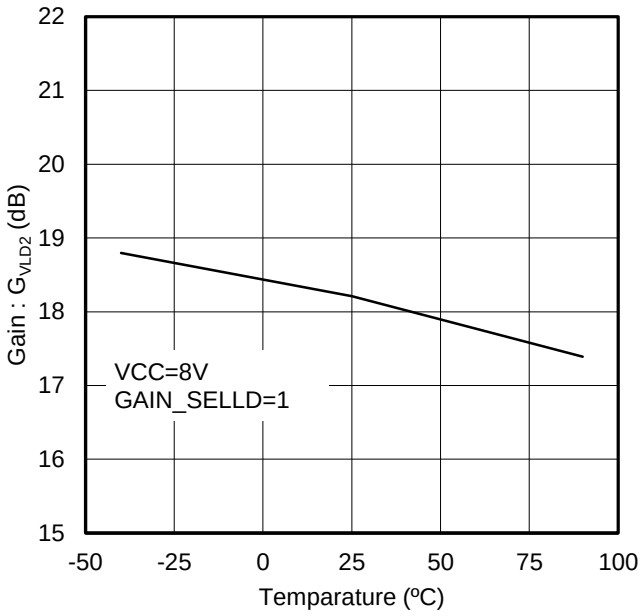
TK Voltage gain 1 (Low gain mode)



TK Voltage gain 2 (High gain mode)



LD Voltage gain 1 (Low gain mode)



LD Voltage gain 2 (High gain mode)

Description of Blocks

■ Serial Peripheral Interface (SPI)

16 bit serial interfaces (SLV, SCLK, SDI, SDO) are provided to perform setting of operations and output levels. SPI communication is performed while SLV terminal is in Low. SDI data are sent to internal shift register at the rising edge of SCLK terminal. Shift register data are loaded into 12 bit internal shift register at the rising edge of SLV terminal according to the address map. Readout operation is performed when readout bit is set to 1. Then state is read out at the falling edge of SCLK terminal and output to SDO terminal.

◆ Input-Output Timing

Figure 4 shows write/read timing of the serial ports.

Minimum timing of each item is as shown in the table below. In order to prevent increase in delay of SPI input/output timing, wiring between SLV/SCLK/SDI/SDO and the microcomputer should be as short as possible to minimize the wiring capacitance.

Symbol	Item	Min	Typ	Max	Unit
A	SDI setup time *	9	-	-	ns
B	SDI hold time *	9	-	-	ns
C	Setup SLV to SCLK rising edge *	9	-	-	ns
D	SCLK high pulse width *	10	-	-	ns
E	SCLK low pulse width *	10	-	-	ns
F	Setup SCLK rising edge to SLV *	9	-	-	ns
G	SLV pulse width *	15	-	-	ns
H	SDO delay time *	-	-	10	ns
I	SDO hold time *	2	-	-	ns
J	SDO OFF time *	-	-	20	ns
K	SCLK frequency	-	-	35	MHz

* Guaranteed Design Items

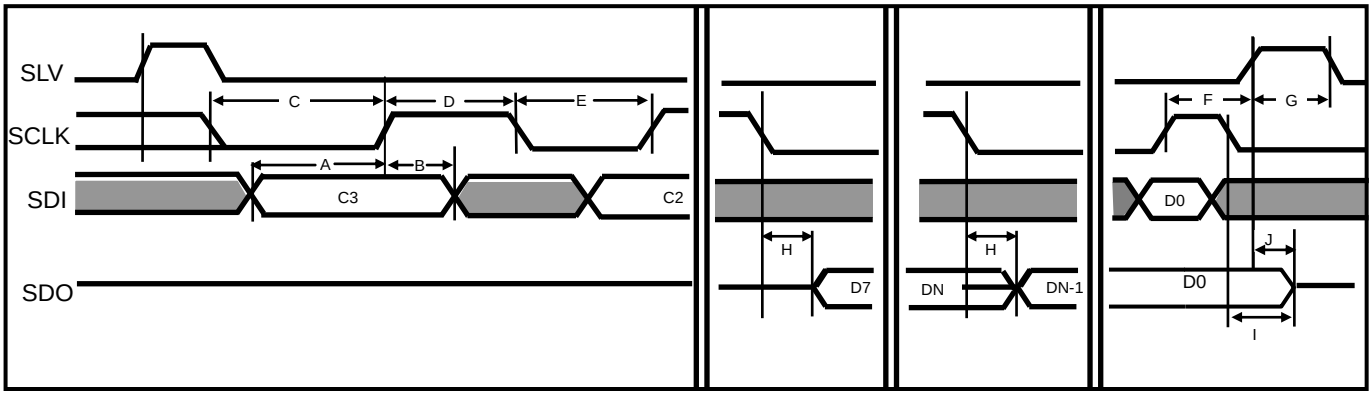


Figure 4. SPI Input Timing

◆ DAC Register

1. Input / Output Sequence
Enter the register address in the SDI input on the first 4 bits and data for a specific DAC voltage in the next 12 bits.
When specified as REG=02h (address for focus), REG 77h data is output to the SDO.
When specified as REG≠02h (address for non-focus), SDO becomes Hi-Z.

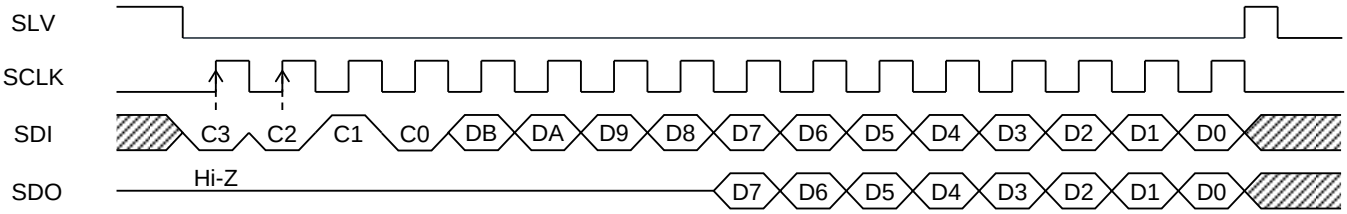


Figure 5. 12bit Write / 8bit Read Sequence (when specified as REG=02h)

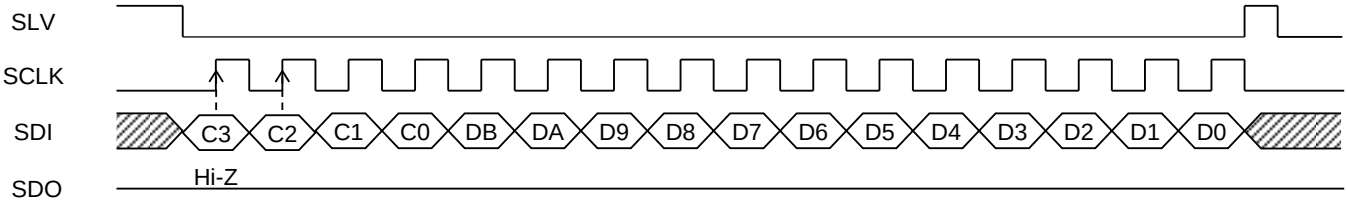


Figure 6. 12bit Write Sequence (when specified as REG≠02h, C3, C2≠1, 1)

2. Address Map (hereinafter register address is referred to as REG)

DAC Register Address Map

REG	NAME	R/W	DB	DA	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Reset **
00h	N/A	-	-	-	-	-	-	-	-	-	-	-	-	-	-
01h	DFCTL1	W	11	10	9	8	7	6	5	4	3	2	1	0	B
02h	DFCTL2	W	11	10	9	8	7	6	5	4	3	2	1	0	B
03h	DTK	W	11	10	9	8	7	6	5	4	3	2	1	0	B
04h	DSL1	W	11	10	9	8	7	6	5	4	3	2	1 *	0 *	B
05h	DSL2	W	11	10	9	8	7	6	5	4	3	2	1 *	0 *	B
06h	DSA1	W	11	-	-	-	-	-	-	-	-	-	-	-	B
07h	DSA2	W	11	-	-	-	-	-	-	-	-	-	-	-	B
08h	DSP	W	11	10	9	8	7	6	5	4	3	2	1	0	B
09h	DLD	W	11	10	9	8	7	6	5	4	3	2	1	0	B
0Ah	N/A	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0Bh	N/A	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Default : 0
* : fixed at 0
** : refer to P.15 about reset
- : not affected even when data is written

◆ Control register

1. Input / Output Sequence

When writing data to the control register, enter the register address in the first 7 bits of the SDI input, then set the 1bit R/W to 0 and enter the data of each setting in the last 8 bits. SDO is Hi-Z when R/W=0.

When reading data from the control register, enter the register address in the first 7 bits of the SDI input, then set the 1 bit R/W to 1. The last 8 bits are ignored. When R/W=1, 8-bit data of specified address is output to the SDO.

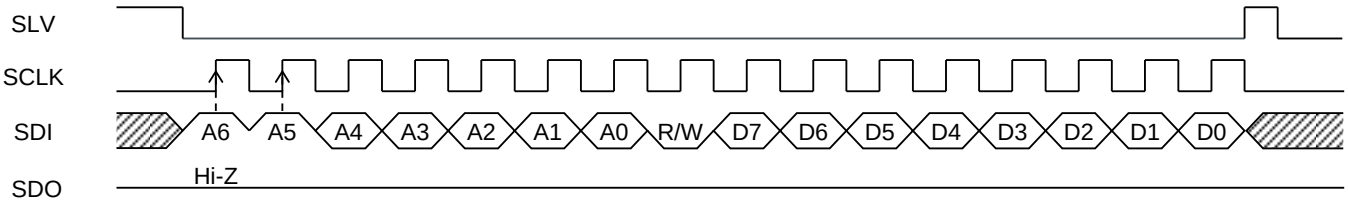


Figure 7. Control Register 8 bit Write Sequence (A6, A5=1,1, R/W= 0)

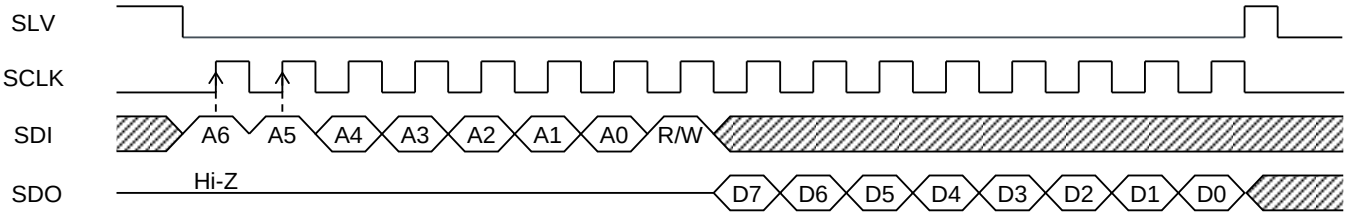


Figure 8. Control Register 8 bit Read Sequence (A6, A5=1,1, R/W= 1)

2. Address Map

Control Register Address Map

REG	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
70h	OUTPUT _EN1	R/W	FCTL1 _OUTEN	FCTL2 _OUTEN	TK _OUTEN	SL _OUTEN	SA _OUTEN	SP _OUTEN	LD _OUTEN	N/A
71h	-	-	-	-	-	-	-	-	-	-
72h	POWER _SAVE1	R/W	FCTL1 _PSB	FCTL2 _PSB	TK _PSB	SL _PSB	SA _PSB	SP _PSB	LD _PSB	N/A
73h	-	-	-	-	-	-	-	-	-	-
74h	DRIVER _SET	R/W	N/A	SP _BRAKE	GAIN _SELFCTL	GAIN _SELTK	DIFF _FCTL	LD _BRAKE	GAIN _SELLD	N/A
75h	RESET	W	RST _DAC	RST _CTLREG	RST _PKTERR	RST _PKTSTOP	RST _OCP	RST _SHORT	N/A	N/A
76h	PKT _TIME	R/W	N/A	N/A	PKTSTOP _TIME1	PKTSTOP _TIME0	N/A	N/A	N/A	N/A
77h	STATUS _FLAG1	R	ALL _ERR	OCP _FCTL	OCP _TK	SHORT _LD	TSD	PKT _ERR	PKT _STOP	UVLO _VCC
78h	TEST0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79h	TEST1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	N/A	N/A	N/A
7Ah	TEST2	R/W	N/A	N/A	Reserved	N/A	Reserved	Reserved	Reserved	N/A
7Bh	RST _CHECK	R/W	RST _CHECKA	RST _CHECKB	N/A	N/A	N/A	N/A	N/A	N/A
7Ch	-	-	-	-	-	-	-	-	-	-
7Dh	-	-	-	-	-	-	-	-	-	-
7Eh	-	-	-	-	-	-	-	-	-	-
7Fh	-	-	-	-	-	-	-	-	-	-

Write access to "Reserved" bits should be made by "0" input.

Read access to "N/A" bits will return "0".

3. Details of Control Registers
Functions of each register are as shown below.

・ REG 70h OUTPUT_EN1 (Read / Write)
Each driver output settings (Hi-Z/Active) can be changed in REG 70h.

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	FCTL1_OUTEN	0	FCTL1 Output Enable	Disable	Enable	A
6	FCTL2_OUTEN	0	FCTL2 Output Enable	Disable	Enable	A
5	TK_OUTEN	0	TK Output Enable	Disable	Enable	A
4	SL_OUTEN	0	SL1,SL2 Output Enable	Disable	Enable	A
3	SA_OUTEN	0	SA1,SA2 Output Enable	Disable	Enable	A
2	SP_OUTEN	0	SP Output Enable	Disable	Enable	A
1	LD_OUTEN	0	LD Output Enable	Disable	Enable	A
0	N/A	0	-	-	-	-

・ REG 71h -

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	-	-	-	-	-	-
6	-	-	-	-	-	-
5	-	-	-	-	-	-
4	-	-	-	-	-	-
3	-	-	-	-	-	-
2	-	-	-	-	-	-
1	-	-	-	-	-	-
0	-	-	-	-	-	-

・ REG 72h POWER_SAVE1 (Read / Write)
Power save mode settings for each block can be set in REG 72h.
Power save mode makes the output Hi-Z and turns OFF the internal circuit to reduce the current consumption.

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	FCTL1_PSB	0	FCTL1 Block Power Save	Enable	Disable	A
6	FCTL2_PSB	0	FCTL2 Block Power Save	Enable	Disable	A
5	TK_PSB	0	TK Block Power Save	Enable	Disable	A
4	SL_PSB	0	SL1,SL2 Block Power Save	Enable	Disable	A
3	SA_PSB	0	SA1,SA2 Block Power Save	Enable	Disable	A
2	SP_PSB	0	SP Block Power Save	Enable	Disable	A
1	LD_PSB	0	LD Block Power Save	Enable	Disable	A
0	N/A	0	-	-	-	-

・ REG 73h -

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	-	-	-	-	-	-
6	-	-	-	-	-	-
5	-	-	-	-	-	-
4	-	-	-	-	-	-
3	-	-	-	-	-	-
2	-	-	-	-	-	-
1	-	-	-	-	-	-
0	-	-	-	-	-	-

・ REG 74h DRIVER_SET (Read / Write)

Operation mode settings of the driver can be changed in REG 74h.

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	N/A	0	-	-	-	-
6	SP_BRAKE	0	SP Brake Mode	Short Brake	Reverse Brake	A
5	GAIN_SELFCTL	0	Gain Select FCTL	Low Gain	High Gain	A
4	GAIN_SELTK	0	Gain Select TK	Low Gain	High Gain	A
3	DIFF_FCTL	0	Differential FCTL Control Mode	Differential Control	Independent Control	A
2	LD_BRAKE	0	LD Brake Mode	LD Output Active	LD Output Short Brake	A
1	GAIN_SELLD	0	Gain Select LD	Low Gain	High Gain	A
0	N/A	0	-	-	-	-

<Bit 6> Short brake/reverse brake can be selected as spindle brake mode.
<Bit 5> Low/high gain mode of the focus/tilt driver's gain can be selected.
<Bit 4> Low/high gain mode of the tracking driver's gain can be selected.
<Bit 3> Differential/independent drive of the focus and tilt driver can be selected. See page 18 for more information.
<Bit 2> Short brake mode (both positive & negative output low) can be activated when loading output is "Active".
<Bit 1> Low/high gain mode of the loading driver's gain can be switched.

・ REG 75h RESET (Write)

Resister settings and latched error flag can be reset in REG 75h.

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	RST_DAC	0	DAC Reset	Normal	Reset	E
6	RST_CTLREG	0	Control Register Reset	Normal	Reset	E
5	RST_PKTERR	0	Packet Bit Counts Error Reset	Normal	Reset	E
4	RST_PKTSTOP	0	No Packet Input Error Reset	Normal	Reset	E
3	RST_OCP	0	Actuator Overcurrent Protection Latch Off Reset	Normal	Reset	E
2	RST_SHORT	0	LD Supply/Ground-Fault Protection Latch Off Reset	Normal	Reset	E
1	N/A	0	-	-	-	-
0	N/A	0	-	-	-	-

<Bit 7>Reset all DAC register value to 0.
<Bit 6>Reset all control register value to default.
<Bit 5>Reset packet bit counts error flag register value to 0.
<Bit 4>Reset no packet input error flag register value to 0.
<Bit 3>Reset actuator overcurrent protection flag register value to 0.
<Bit 2>Reset loading supply/ground-fault protection flag register value to 0.

・ REG 76h PKT_TIME (Read / Write)

In REG 76h, you can specify or disable wait time until error operation in case of no SPI input.

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	N/A	0	-	-	-	-
6	N/A	0	-	-	-	-
5	PKTSTOP_TIME1	0	SPI Packet Watchdog Timer Operation Time Selection	(00)=Disabled, (01)=1ms, (10)=100µs, (11)=30µs		A
4	PKTSTOP_TIME0	0				A
3	N/A	0	-	-	-	-
2	N/A	0	-	-	-	-
1	N/A	0	-	-	-	-
0	N/A	0	-	-	-	-

・ REG 77h STATUS_FLAG (Read)

REG 77h outputs each protection state flag

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	ALL_ERR	0	All Error Flags	Normal	Abnormal	*
6	OCP_FCTL	0	FCTL Overcurrent Detection Flag (FCTL1, 2, TK Output Hi-Z)	Normal	Abnormal	C
5	OCP_TK	0	TK Overcurrent Detection Flag (FCTL1, 2, TK Output Hi-Z)	Normal	Abnormal	C
4	SHORT_LD	0	LD Supply/Ground-Fault Protection Detection Flag (LD Output Hi-Z)	Normal	Abnormal	C
3	TSD	0	TSD Detection Flag (All Output Hi-Z)	Normal	Abnormal	F
2	PKT_ERR	0	Number of Packet Bits Error Flag (Flag Only)	Normal	Abnormal	C
1	PKT_STOP	0	Packet Watchdog Timer (All Output Hi-Z)	Normal	Abnormal	C
0	UVLO_VCC	0	VCC Low Voltage Fault Flag (All Output Hi-Z)	Normal	Abnormal	D

<Bit7> *How to reset: ALL_ERR outputs all the error flags (OCP_FCTL, OCP_TK, SHORT_LD, TSD, PKT_ERR, PKT_STOP, UVLO_VCC). Therefore, reset conditions are depending on each flags.

・ REG 78h TEST0 (Read / Write)

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	Reserved	0	-	-	-	D
6	Reserved	0	-	-	-	D
5	Reserved	0	-	-	-	D
4	Reserved	0	-	-	-	D
3	Reserved	0	-	-	-	D
2	Reserved	0	-	-	-	D
1	Reserved	0	-	-	-	D
0	Reserved	0	-	-	-	D

・ REG 79h TEST1 (Read / Write)

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	Reserved	0	-	-	-	F
6	Reserved	0	-	-	-	F
5	Reserved	0	-	-	-	F
4	Reserved	0	-	-	-	F
3	Reserved	0	-	-	-	F
2	N/A	0	-	-	-	-
1	N/A	0	-	-	-	-
0	N/A	0	-	-	-	-

・ REG 7Ah TEST2 (Read / Write)

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	N/A	0	-	-	-	-
6	N/A	0	-	-	-	-
5	Reserved	0	-	-	-	F
4	N/A	0	-	-	-	-
3	Reserved	0	-	-	-	F
2	Reserved	0	-	-	-	F
1	Reserved	0	-	-	-	F
0	N/A	0	-	-	-	-

・ REG 7Bh RST_CHECK (Read / Write)
REG 7Bh is the flag confirming reset completion of registers listed in page 15.

Bit	Name	Default	Function	Set "0"	Set "1"	Reset
7	RST_CHECKA	0	Reset A Completion Check Flag	0	1	A
6	RST_CHECKB	0	Reset B Completion Check Flag	0	1	B
5	N/A	0	-	-	-	-
4	N/A	0	-	-	-	-
3	N/A	0	-	-	-	-
2	N/A	0	-	-	-	-
1	N/A	0	-	-	-	-
0	N/A	0	-	-	-	-

◆ Register Reset Operations

Type "A" : MODE Setting Bit (REG 70h, 72h, 74h, 76h, 7Bh[7])
Reset Conditions : VCC < 3.8V
or PREVCC < 3.8V
or VREG < 2.0V
or MUTEB < 0.5V
or RST_CTLREG(75h[6]) = 1

Type "B" : DAC Setting Bit (REG 01h~09h, 7Bh[6])
Reset Conditions : VCC < 3.8V
or PREVCC < 3.8V
or VREG < 2.0V
or MUTEB < 0.5V
or RST_DAC(75h[7]) = 1

Type "C" : Operational State (Latched) Output Bit (REG 77h[1,2,4,5,6])
Reset Conditions : VCC < 3.8V
or PREVCC < 3.8V
or VREG < 2.0V
or MUTEB < 0.5V
or RST_CTLREG (75h[6]) = 1
or RST_PKTERR (75h[5]) = 1 (for PKT_ERR(77h[2]))
or RST_PKTSTOP (75h[4]) = 1 (for PKT_STOP(77h[1]))
or RST_OCP (75h[3]) = 1 (for OCPFCTL(77h[6]) and OCPTK(77h[5]))
or RST_SHORT (75h[2]) = 1 (for SHORT_LD(77h[4]))

Type "D" : Operational State (Continuously Updated) Output Bit 1 (REG 77h[0])
Reset Conditions : PREVCC < 2.0V
or VREG < 1.2V
or MUTEB < 0.5V

Type "E" : Reset Setting Bit (REG 75h)
Reset Conditions : Self-reset (If set to 1, automatically returns to "0" following reset operation)

Type "F" : Operational State (Continuously Updated) Output Bit 2 (REG 77h[3])
Reset Conditions : VCC < 3.8V
or PREVCC < 3.8V
or VREG < 2.0V
or MUTEB < 0.5V

Reset Operations

Reset condition		DAC REG	Control REG															
								77h								7Bh	
		01h ~ 09h	70h	72h	74h	75h	76h	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6
Hard	VCC < 3.8V	○	○	○	○		○	○	○	○	○	○	○	○		○	○
	PREVCC < 2.0V	○	○	○	○		○	○	○	○	○	○	○	○	○	○	○
	PREVCC < 3.8V	○	○	○	○		○	○	○	○	○	○	○	○		○	○
	MUTEB < 0.5V	○	○	○	○		○	○	○	○	○	○	○	○	○	○	○
Soft	RST_SHORT 75h[2] = 1							*1			○						
	RST_OCP 75h[3] = 1							*1	○	○							
	RST_PKTSTOP 75h[4] = 1							*1						○			
	RST_PKTERR 75h[5] = 1							*1					○				
	RST_CTLREG 75h[6] = 1		○	○	○		○	*1								○	
	RST_DAC 75h[7] = 1	○						*1									○
Self reset						○											

*1 Reset conditions of REG 77h[7] are dependent upon REG 77h[6]-77h[0].

■ SPI Input / Output Terminal Processing

Provided with input terminals SLV, SCLK and SDI, and output terminal SDO, as serial interfaces. Input terminals SLV, SCLK and SDI have built-in 100kΩ (Typ) pull-up/pull-down resistor. Output terminal SDO is able to output the voltage set at SHV as high level voltage in 3-state CMOS output.

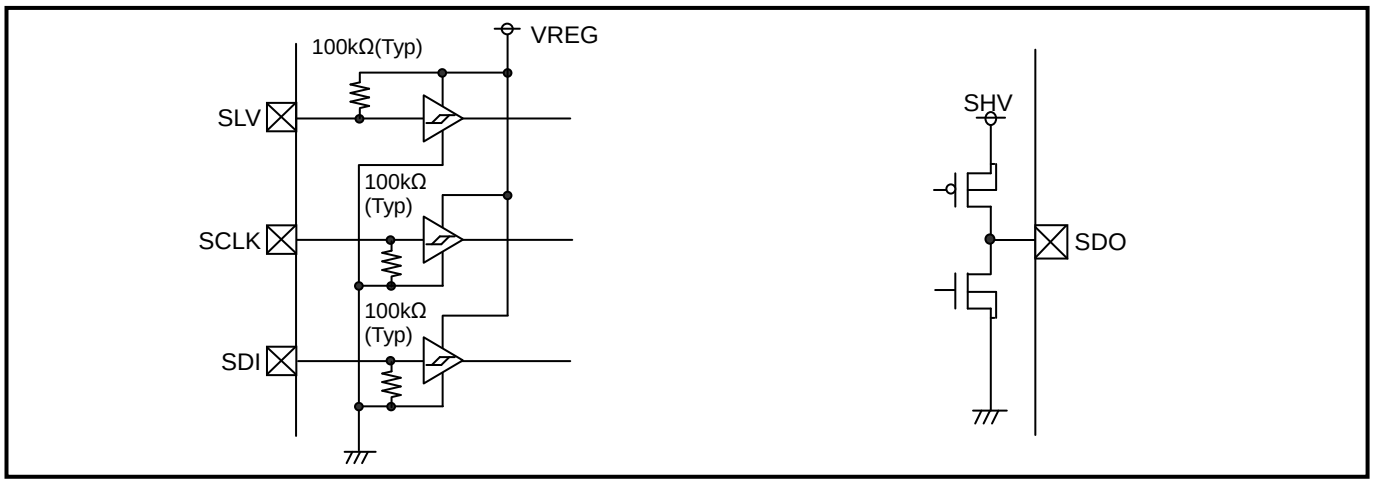


Figure 9. SPI Input / Output Terminal Processing

■ DAC and Gain Setting

◆ Actuator (FCTL1, FCTL2, TK)

Suppose that voltage difference between positive/negative outputs is V_{OUT}, V_{OUT} can be expressed as follows.

$$V_{OUT} = G_{VACT} \times V_{DAC}$$

Here, G_{VACT} value will be different as below depending upon gain mode settings.

Low Gain Mode (REG 74h[5] GAIN_SELFCTL, REG74h[4] GAIN_SELTK = 0 (Default))
G_{VACT1} = 3.85 times (11.7dB)

High Gain Mode (GAIN_SELFCTL, GAIN_SELTK = 1)
G_{VACT2} = 7.67 times (17.7dB)

V_{DAC}, the DAC output voltage, can be obtained from DAC register settings through the following equation.

MSB=0:

$$V_{DAC} = 1.0\times(bit[10]\times0.5^{1}+bit[9]\times0.5^{2}+bit[8]\times0.5^{3}+\ldots+bit[0]\times0.5^{11})$$

MSB=1::

$$V_{DAC} = (-1.0)\times(\hat{}bit[10]\times0.5^{1}+\hat{}bit[9]\times0.5^{2}+\hat{}bit[8]\times0.5^{3}+\ldots+\hat{}bit[0]\times0.5^{11}+0.5^{11})$$

DAC format (DFCTL1, DFCTL2, DTK)

REG	MSB Digital input (BIN) LSB	Hex	Dec	V_{DAC} [V]	V_{OUT} [V]*
01h(DFCTL1), 02h(DFCTL2), 03h(DTK)	1000_0000_0000	800h	-2048	-0.9995	-3.848
	1000_0000_0001	801h	-2047	-0.9995	-3.848
	1000_0000_0010	802h	-2046	-0.9990	-3.846
	1111_1111_1111	FFFh	-1	-0.0005	-0.002
	0000_0000_0000	000h	0	0	0.000
	0000_0000_0001	001h	+1	+0.0005	+0.002
	0111_1111_1110	7FEh	+2046	+0.9990	+3.846
	0111_1111_1111	7FFh	+2047	+0.9995	+3.848

* In low gain mode setting. Output voltage saturation is not taken into account in the table.

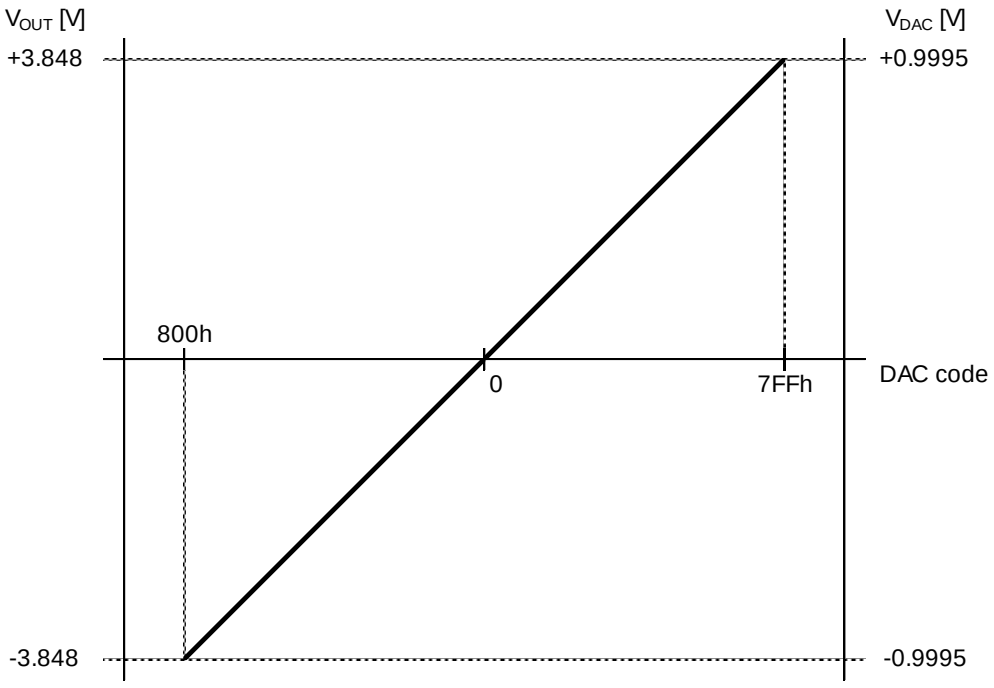


Figure 10. DAC Setting vs. V_{DAC}/V_{OUT} (in low gain mode)

◆ FCTL 1, FCTL 2 Differential Drive Mode

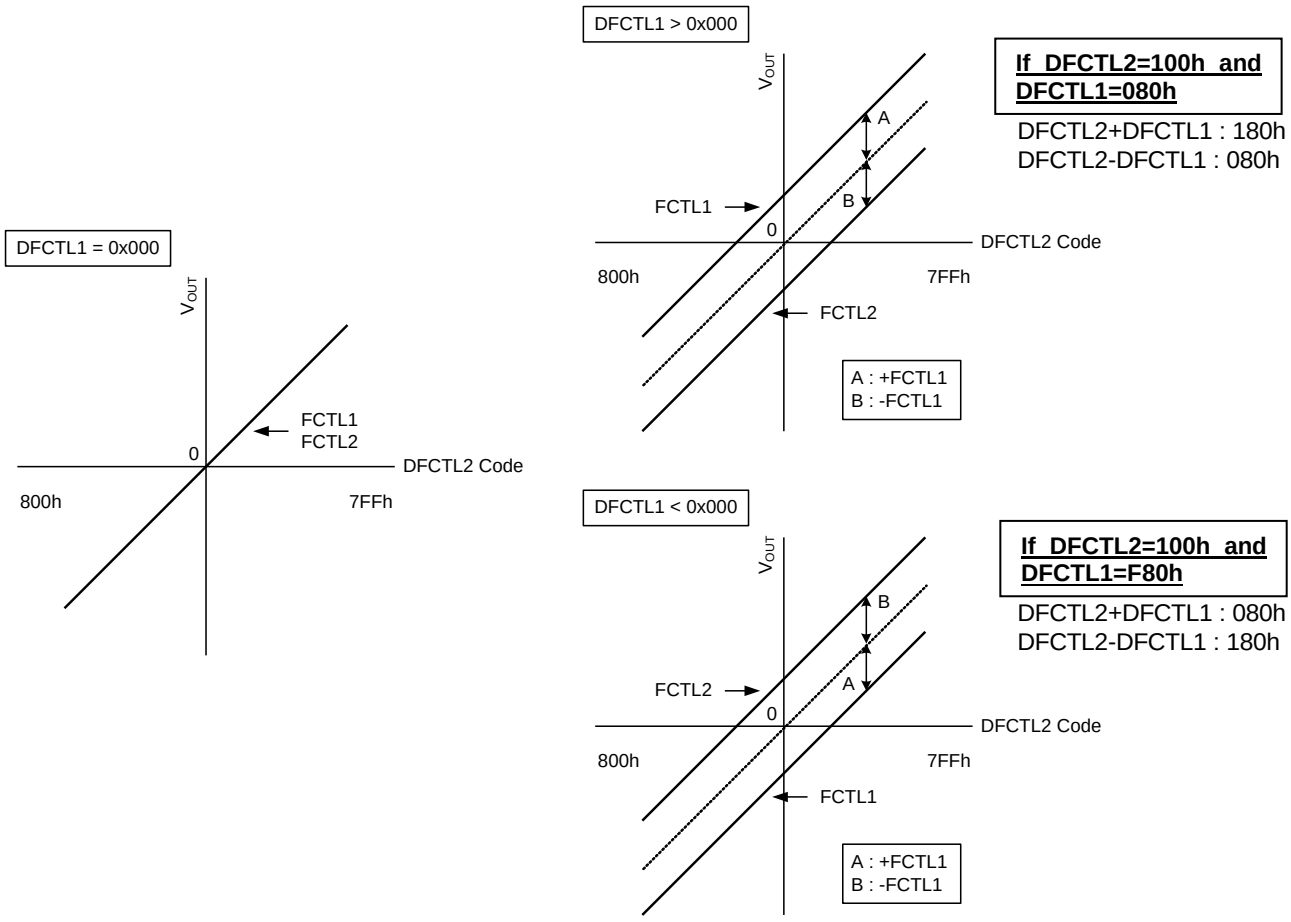
If you set REG 74h[3] DIFF_FCTL to 0, FCTL1 and FCTL2 turn into differential drive mode. In this mode, 12 bit data to be input into DAC of FCTL1 and FCTL2 will be the values obtained by the following equations. $DAC_{FCTL1, 2}$ shows 12-bit data to be input into respective DACs. Note that the DAC output voltage V_{DAC}, gain GV_{ACT} and output voltage V_{OUT} are to be in accordance with page 17.

DAC_{FCTL1} = DFCTL2 + DFCTL1

DAC_{FCTL2} = DFCTL2 – DFCTL1

Operation images during the differential drive mode are as shown below.

FCTL1, 2 Differential Operation Images when DIFF_FCTL=0



◆Loading (LD)

Suppose that voltage difference between positive/negative outputs is V_{OUT}, V_{OUT} can be expressed as follows.

$V_{OUT} = G_{VLD} \times V_{DAC}$

Here, G_{VLD} value will be different as below depending upon gain mode settings.

Low Gain Mode (REG 74h[1] GAIN_SELLD = 0 (Default))
G_{VLD1} = 7.24 times (17.2dB)

High Gain Mode (GAIN_SELLD =1)
G_{VLD2} = 8.51 times (18.7dB)

V_{DAC}, the DAC output voltage, can be obtained from DAC register settings through the following equation.

MSB=0:

$V_{DAC} = 1.0 \times (bit[10] \times 0.5^1 + bit[9] \times 0.5^2 + bit[8] \times 0.5^3 + \ldots + bit[0] \times 0.5^{11})$

MSB=1 :

$V_{DAC} = (-1.0) \times (\wedge bit[10] \times 0.5^1 + \wedge bit[9] \times 0.5^2 + \wedge bit[8] \times 0.5^3 + \ldots + \wedge bit[0] \times 0.5^{11} + 0.5^{11})$

DAC format (DLD)

REG	MSB Digital input (BIN) LSB	Hex	Dec	V_{DAC} [V]	V_{OUT} [V]*
09h(DLD)	1000_0000_0000	800h	-2048	-0.9995	-7.236
	1000_0000_0001	801h	-2047	-0.9995	-7.236
	1000_0000_0010	802h	-2046	-0.9990	-7.233
	1111_1111_1111	FFFh	-1	-0.0005	-0.004
	0000_0000_0000	000h	0	0	0.000
	0000_0000_0001	001h	+1	+0.0005	+0.004
	0111_1111_1110	7FEh	+2046	+0.9990	+7.233
	0111_1111_1111	7FFh	+2047	+0.9995	+7.236

* In low gain mode setting. Output voltage saturation is not taken into account in the table.

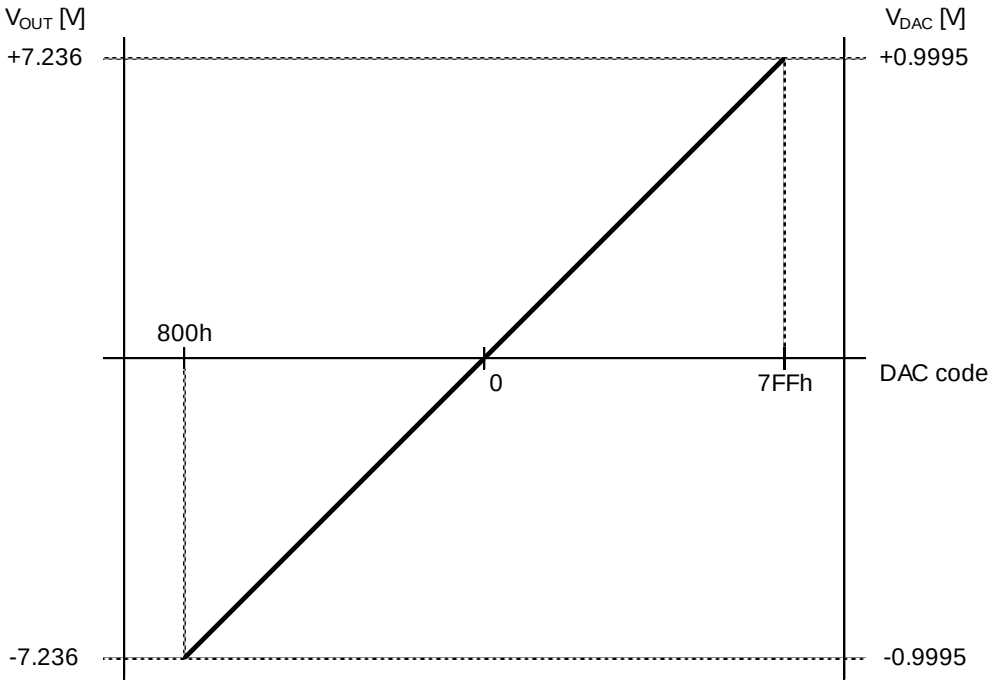


Figure 11. DAC Setting vs. V_{DAC}/V_{OUT} (in low gain mode)

◆ Sled (SL1, SL2)

Suppose that $I_{O\ PEAK}$ represents peak output current, $I_{O\ PEAK}$ can be expressed in the following ways.

$I_{O\ PEAK} = 0$ ($|V_{DAC}| < V_{DZSL}$)
$I_{O\ PEAK} = gm_{SL} \times |V_{DAC}|$ ($gm_{SL} \times |V_{DAC}| < I_{LIMSL}$)
$I_{O\ PEAK} = I_{LIMSL}$ ($gm_{SL} \times |V_{DAC}| > I_{LIMSL}$)

Where V_{DZSL} is input deadzone (single-sided) of 15mV (Typ). The gm_{SL} is output/input gain and I_{LIMSL} is output limit current, and they can be obtained respectively as follows.

$gm_{SL} = 0.616 / R_{SLRNF}$ [A/V]
$I_{LIMSL} = 0.52 / R_{SLRNF}$ [A]

V_{DAC}, the DAC output voltage, can be obtained from DAC register settings through the following equation.

MSB=0

$V_{DAC} = 1.0\times(bit[10]\times0.5^1+bit[9]\times0.5^2+bit[8]\times0.5^3+\ldots+bit[2]\times0.5^9)$

MSB=1

$V_{DAC} = (-1.0) \times (\hat{}bit[10]\times0.5^1+\hat{}bit[9]\times0.5^2+\hat{}bit[8]\times0.5^3+\ldots+\hat{}bit[2]\times0.5^9+0.5^9)$

DAC format (DSL1, DSL2)

REG	MSB Digital input (BIN) LSB	Hex	Dec	V_{DAC} [V]	$I_{O\ PEAK}$ [A]*
04h(DSL1), 05h(DSL2)	1000_0000_0000	800h	-2048	-0.9980	-1.098
	1000_0000_0100	804h	-2044	-0.9980	-1.098
	1111_1110_0000	FE0h	-32	-0.0156	-0.017
	1111_1110_0100	FE4h	-28	-0.0137	0
	1111_1111_1100	FFCh	-4	0.0020	0
	0000_0000_0000	000h	0	0	0
	0000_0000_0100	004h	+4	+0.0020	0
	0000_0001_1100	01Ch	+28	+0.0137	0
	0000_0010_0000	020h	+32	+0.0156	+0.017
	0111_1111_1000	7F8h	+2040	+0.9961	+1.096
	0111_1111_1100	7FCh	+2044	+0.9980	+1.098

*Output voltage saturation and limit current setting are not taken into account in the table. Condition:R_{SLRNF}=0.56Ω

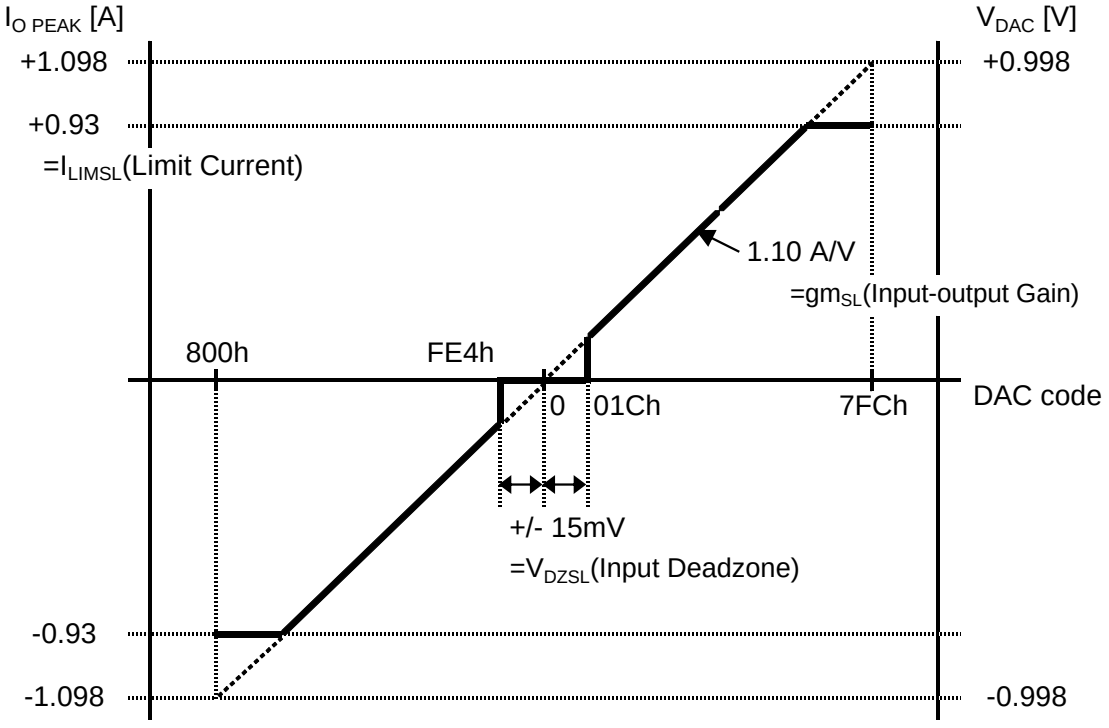


Figure 12. $I_{O\ PEAK}$ Characteristics (When set as R_{SLRNF}=0.56 Ω).

◆ Spindle (SP)

Suppose that $I_{O\ PEAK}$ represents peak output current, $I_{O\ PEAK}$ can be expressed in the following ways.

$I_{O\ PEAK} = 0$ ($|V_{DAC}| < V_{DZSP}$)
$I_{O\ PEAK} = gm_{SP} \times |V_{DAC}|$ ($gm_{SP} \times |V_{DAC}| < I_{LIMSP}$)
$I_{O\ PEAK} = I_{LIMSP}$ ($gm_{SP} \times |V_{DAC}| > I_{LIMSP}$)

Where V_{DZSP} is input deadzone (single-sided) of 10mV (Typ). The gm_{SP} is output/input gain and I_{LIMSP} is output limit current, and they can be obtained respectively as follows.

$gm_{SP} = 0.409 / R_{SPRNF}$ [A/V]
$I_{LIMSP} = 0.35 / R_{SPRNF}$ [A]

V_{DAC}, the DAC output voltage, can be obtained from DAC register settings through the following equation.

MSB=0 :

$V_{DAC} = 1.0\times(bit[10]\times0.5^1+bit[9]\times0.5^2+bit[8]\times0.5^3+\ldots+bit[0]\times0.5^{11})$

MSB=1 :

$V_{DAC} = (-1.0)\times(\hat{}bit[10]\times0.5^1+\hat{}bit[9]\times0.5^2+\hat{}bit[8]\times0.5^3+\ldots+\hat{}bit[0]\times0.5^{11}+0.5^{11})$

DAC format (DSP)

REG	MSB Digital input (BIN) LSB	Hex	Dec	V_{DAC} [V]	$I_{O\ PEAK}$ [A]※
08h(DSP)	1000_0000_0000	800h	-2048	-0.9995	-1.239
	1000_0000_0001	801h	-2047	-0.9995	-1.239
	1111_1110_1011	FEBh	-21	-0.0103	-0.013
	1111_1110_1100	FECh	-20	-0.0098	0
	1111_1111_1111	FFFh	-1	-0.0005	0
	0000_0000_0000	000h	0	0	0
	0000_0000_0001	001h	+1	+0.0005	0
	0000_0001_0100	014h	+20	+0.0098	0
	0000_0001_0101	015h	+21	+0.0103	+0.013
	0111_1111_1110	7FEh	+2046	+0.9990	+1.238
	0111_1111_1111	7FFh	+2047	+0.9995	+1.239

*Output voltage saturation and limit current setting are not taken into account in the table. Condition:R_{SPRNF}=0.33Ω

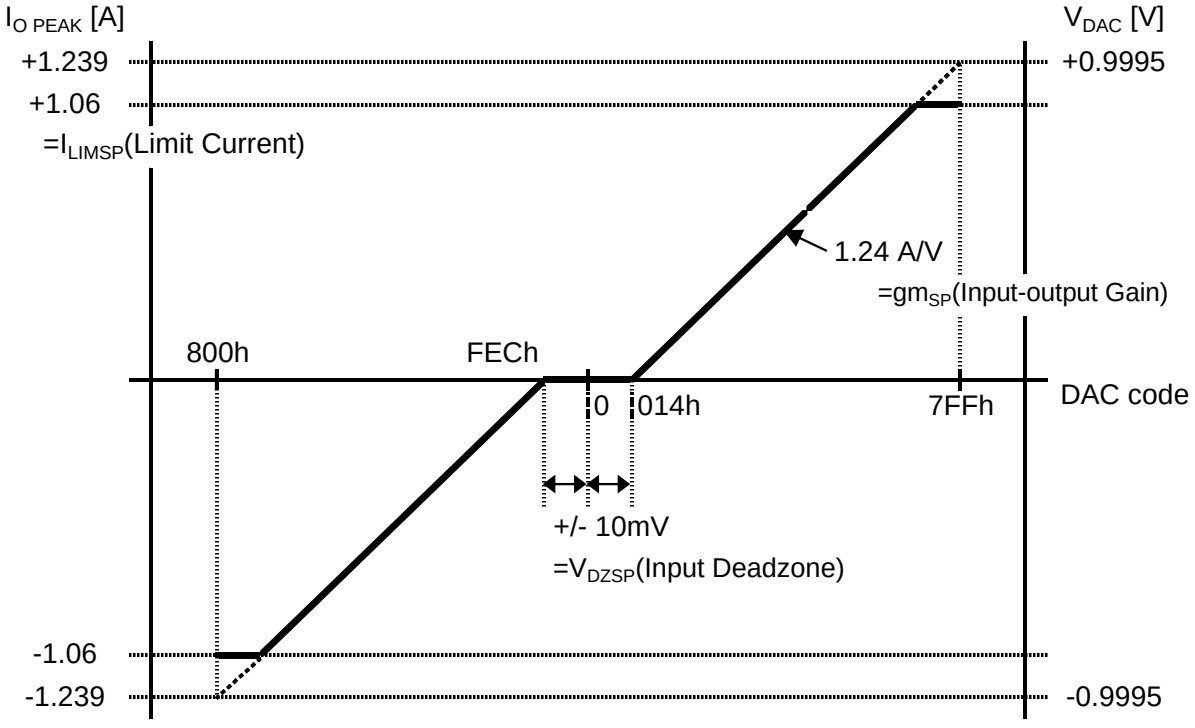


Figure 13. $I_{O\ PEAK}$ Characteristics (When set as R_{SPRNF}=0.33 Ω).

■ Description of Driver Operations

◆ LVDS for Spherical Aberration Driver (SA1, SA2)

LVDS for Spherical Aberration Driver delivers output corresponding to data stored in DSA1 and DSA2, in accordance with the table below.
SAO1+ and SAO1- correspond to DSA1, while SAO2+ and SAO2- to DSA2, and they can be controlled independently.
Recommended operation frequency of each output is 10 kHz or less.

DAC format (DSA1, DSA2)

REG	MSB Digital input (BIN) LSB	Hex	Dec	SAO+	SAO-
06h(DSA1), 07h(DSA2)	0 - - - _ - - - - _ - - - -	000h	0	L	H
	1 - - - _ - - - - _ - - - -	800h	-2048	H	L

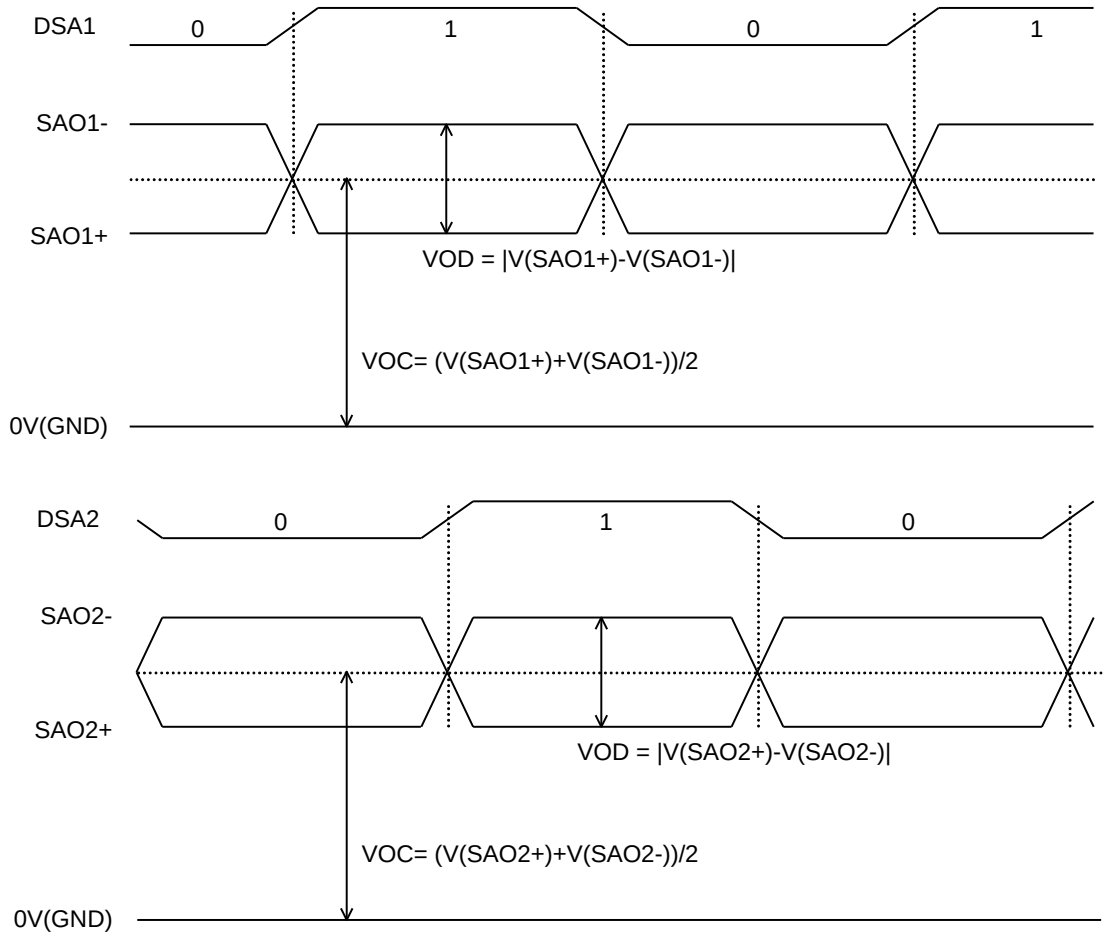


Figure 14. Timing Chart of LVDS for Spherical Aberration Driver

◆ Sled Motor Driver

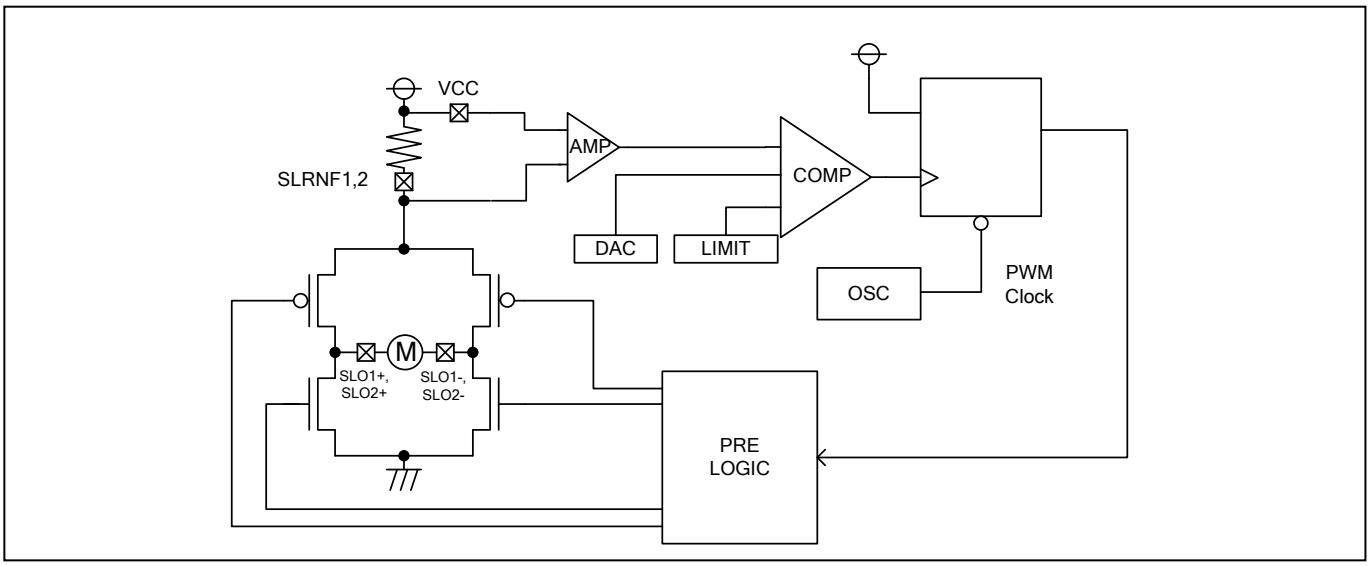


Figure 15. Sled motor driver block

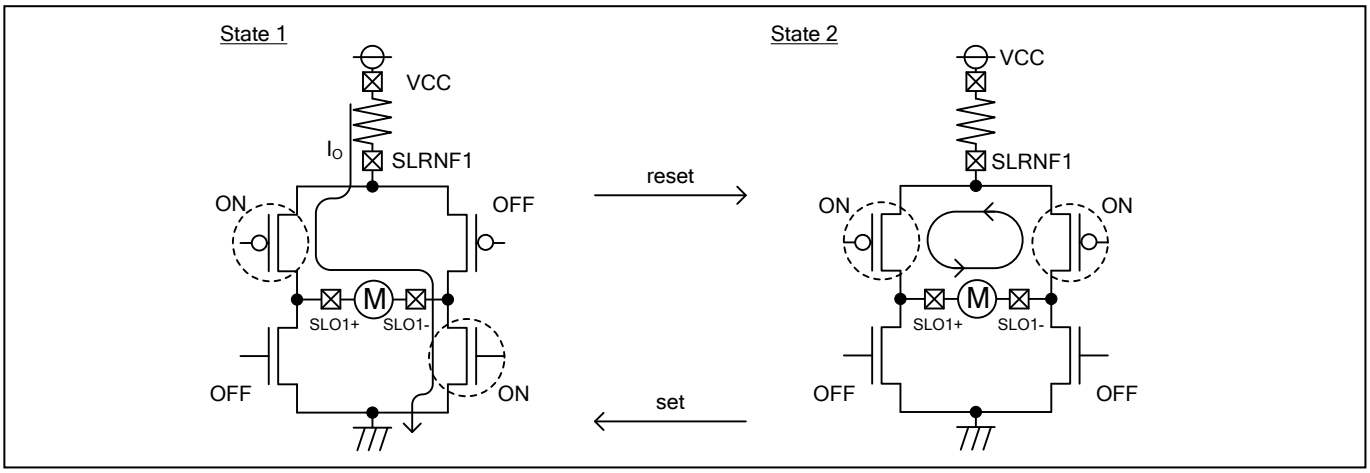


Figure 16. Current Paths in Set [State 1] and Reset [State 2]

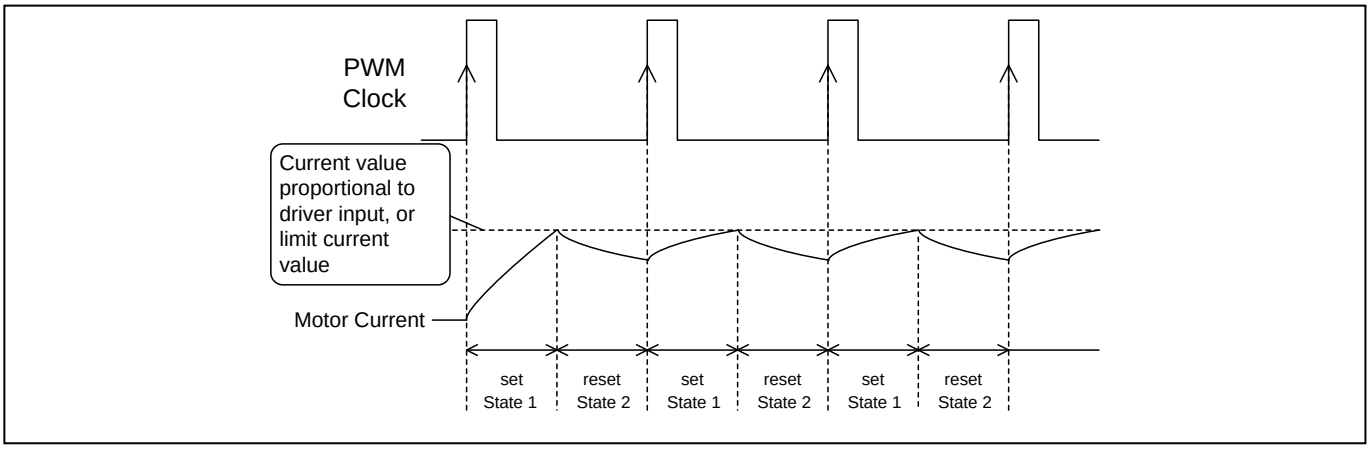


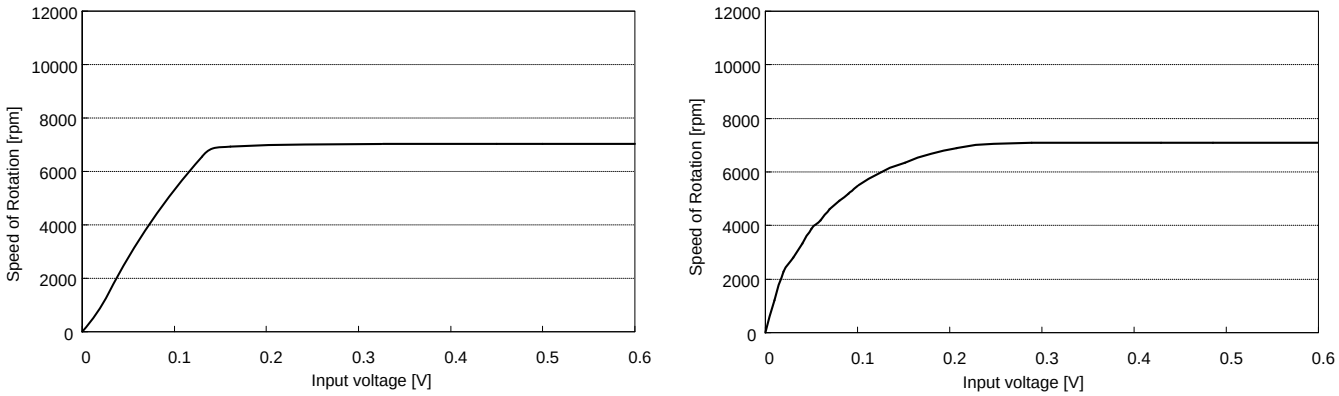
Figure 17. Sled Motor Driver Operation Timing Chart

Set [State1] : Output turned ON at the rise of PWM clock --> Load current supplied from VCC.
Reset [State2] : Output turned OFF when load current increases to reach current value proportional to input or limit current value --> Load current regenerated by L component of the motor through the path shown in State 2 diagram.

◆ Spindle Driver

1. Spindle Driver Input-Output Characteristics

Figure 18 shows input-output characteristics of the average current detection control and the peak current detection control. This IC controls output by detecting peak current. Linearity of the input/output characteristics is improved compared with the one in the average current detection method.

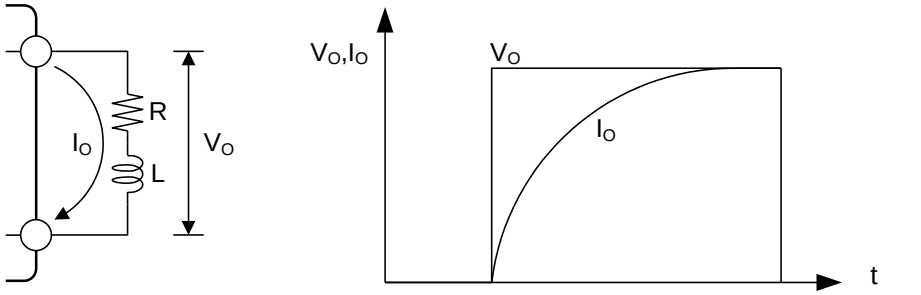


(a) Peak Current Control Method (BD8256EFV-M)

(b) Average Current Control Method

Figure 18. Spindle Driver Input-Output Characteristics

Difference in input/output characteristics due to control method can be explained as below.
Motor coil comprises not only pure inductance but also impedance component. Suppose that V_O represents peak value of output pulse, I_O, current which flows into the motor when output pulse is turned on, can be expressed in the following ways.

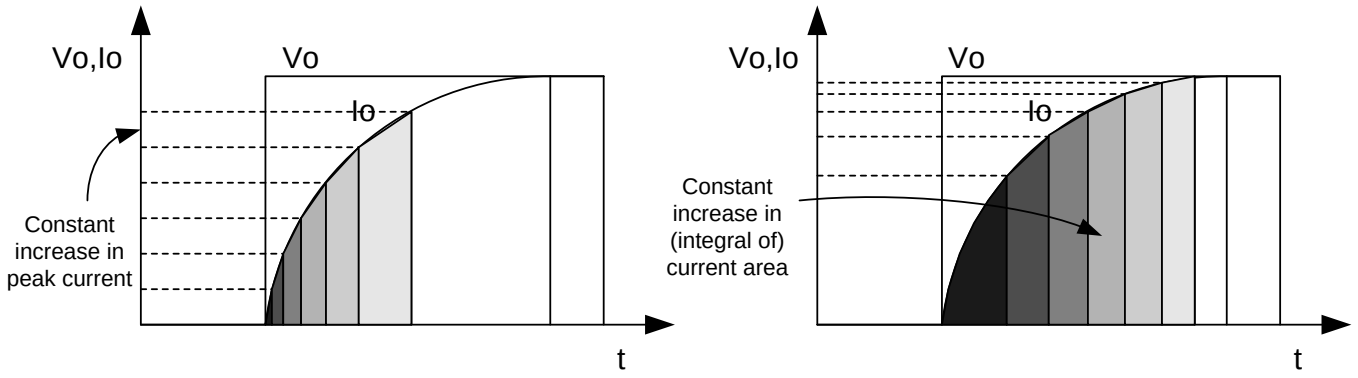


$$V_O = I_O(t) \times R + L \times \frac{dI_O(t)}{dt}$$

$$I_O = \frac{V_O}{R}(1 - e^{-\frac{R}{L}t})$$

Figure 19. Current Waveform Including Impedance Component

You can see from the above equation that motor current Io follows a curve of natural logarithm. If you try to express this as motor current characteristics as opposed to input voltage controlled by the respective methods, you will get Figure 20.
Spindle motor speed is proportional to motor current. In case of PWM driver, motor current is roughly equivalent to peak current because it includes regenerative current. In the peak current control, therefore, motor current (rotation speed) becomes proportional to input voltage.
In contrast, in the average current control, average value of supply current (integral of supply current) becomes proportional to input voltage. So motor current (rotation speed) as opposed to input voltage roughly follows a curve of natural logarithm (Figure 20. (b)). And therefore, you get higher gain in low speed range.



(a) Peak Current Control (b) Average Current Control

Figure 20. Input Voltage vs. Motor Current

2. Current Limit Operation.

Figure 21 shows the operation timing chart.

In this IC, flip-flop is activated based on a clock signal generated by the built-in triangular wave generator to generate PWM pulse. The spindle driver starts operation at the rising edge of internal clock. Short brake mode is activated if peak current defined by limit current or gain is detected, and no output pulse is delivered until next clock input. Both during limit current detection and usual peak current detection, it operates at PWM oscillating frequency generated by the same internal clock.

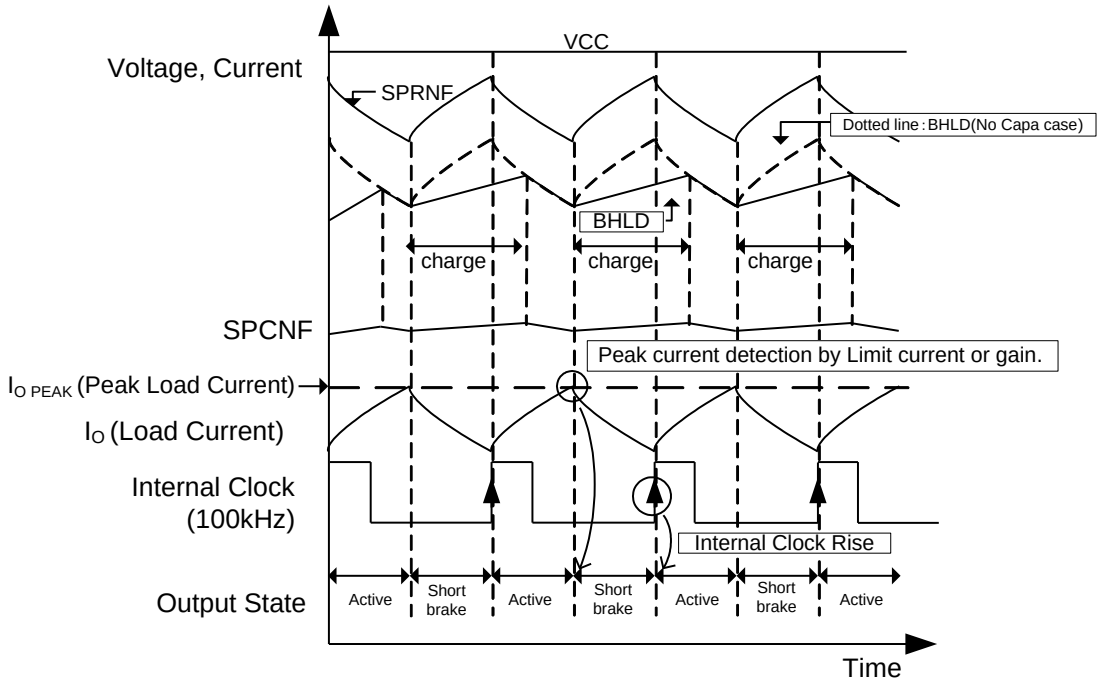


Figure 21. Spindle Driver Operation Timing Chart

3. Role of Capacitors of BHLD and SPCNF Terminals

Figure 22 shows a block diagram of the spindle driver.

In this IC, peak current control method is realized by monitoring Io, the load current flowing in the spindle motor, at SPRNF terminal, and holding the peak current in C_{BHLD}, the capacitor connected to BHLD terminal. Charging time of BHLD terminal is a time constant defined by capacity of C_{BHLD} and 200 kΩ (Typ) internal resistance.

C_{SPCNF}, the capacitor of SPCNF terminal, influences f_c, the cut-off frequency, of the spindle driver control loop. f_c can be expressed in the following formula. Where R_{OERR} is internal error amplifier output impedance of approximately 700 kΩ (Typ).

$$f_c = \frac{1}{2\pi C_{SPCNF} R_{OERR}}$$

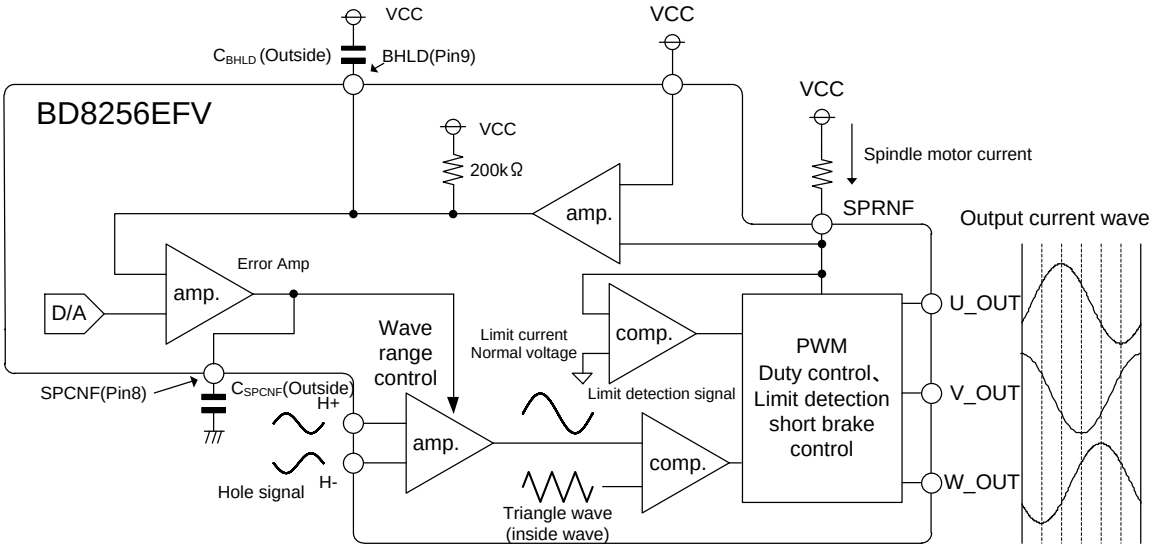


Figure 22. Spindle Driver Block Diagram

4. Spindle Hall Signal Setting

In this IC, as shown in Figure 22, low noise (silence) is realized by controlling output current into a sine wave. Hall signal amplified according to REG 08h DSP is used to control the output current. So, if amplitude of the hall signal is too small, amplitude of the output current will also be too small, and rotation speed will become too low. Therefore, make sure that input level of the hall signal be 50 mV (input level at hall amplifier: V_{HIM}) or greater as shown in Figure 23. Also make sure that waveform of the hall signal be as close as possible to sine wave.

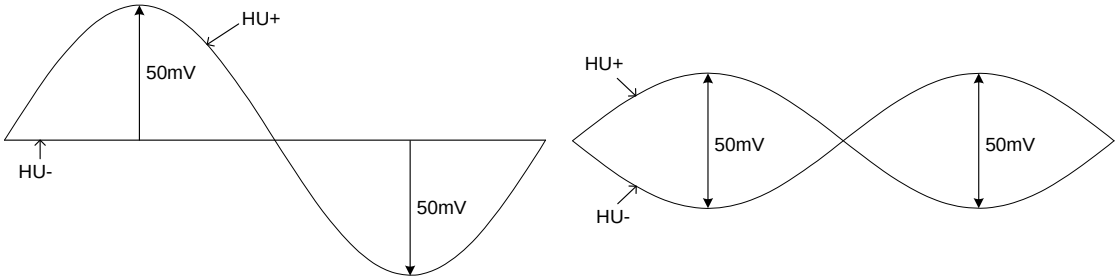


Figure 23. Minimum Amplitude of Hall Input (Example of HU+ and HU- Input).

5. Hall input (Pin 1 to Pin 6) / Hall bias (Pin 7) (Spindle)
Hall elements can be connected either in series or in parallel as shown in Figure 24.
Hall input voltage should be set within the range of 1.5 V to 3.8 V (In-phase input voltage range of hall amplifier: V_{HICM}).
If the Hall input range is not meeting the specification due to variation in characteristics of Hall elements, there is a setting to connect resistor parallel to a resistor.
Additionally, they can also be connected to GND instead of hall bias (Pin 7). In this case, GND should be set as PREGND (Pin 30) and the hall bias (Pin 7) to open.
For connection details, please refer to the page with Application Example.

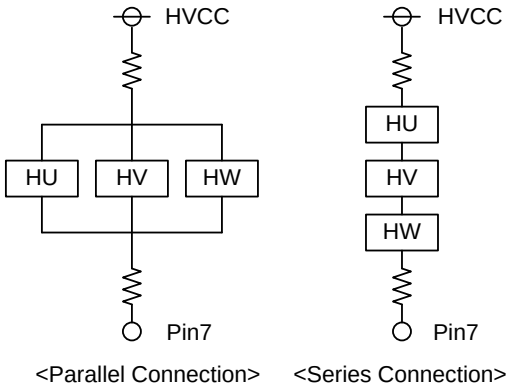


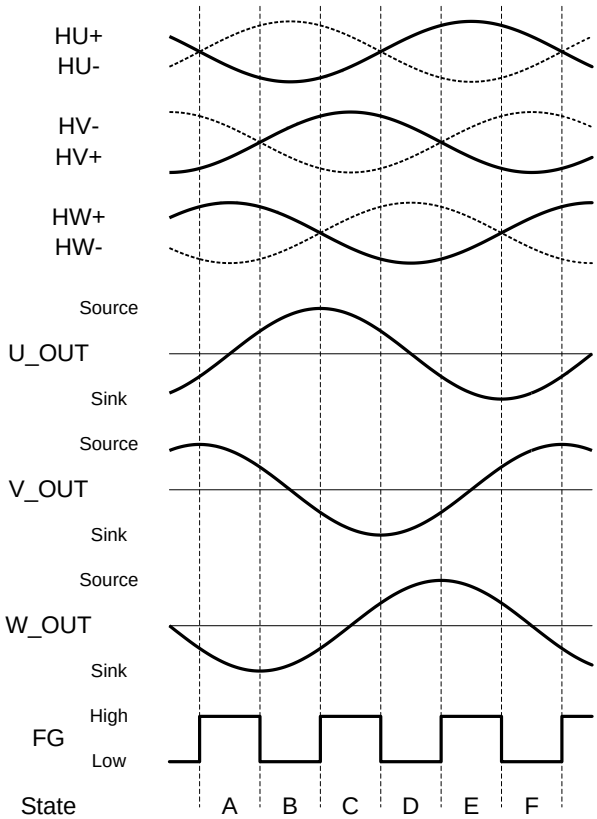
Figure 24. Example of Hall Elements Connection

6. FG Pulse
3FG is output to FG terminal. Pull-up resistor of FG is recommended to be 3.3 kΩ or less. If the resistance setting is higher than that, High logic of FG output can be reversed to become "Low" as soon as spindle output becomes Hi-Z.
Since FG pulse is generated from hall output signal, it can become unstable if the hall signal catches noise. Radiation noise on circuit patterns or flexible cables should be avoided as much as possible. Against any remaining noise, it is recommended to insert a capacitor (around 0.01 µF) between positive and negative sides of the hall signal.

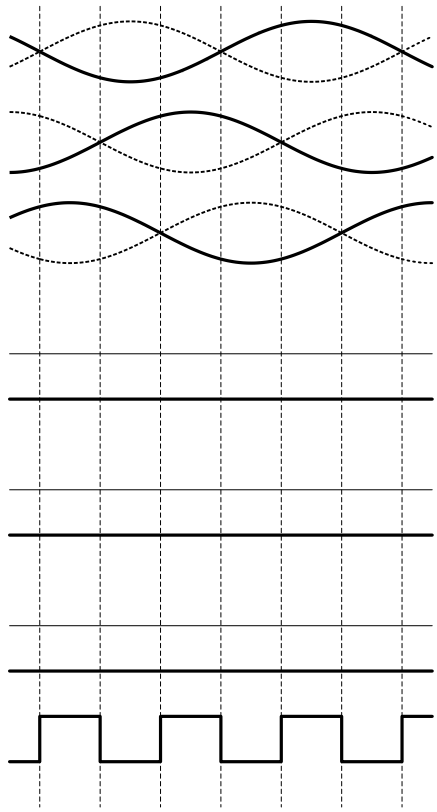
7. Reverse brake
When reverse brake is done coming from high speed, take note of the counter-electromotive force. Also, consider the speed of motor rotation to ensure sufficient output current when using the reverse brake.

8.Capacitor between SPVM-SPGND
There is change in voltage and current because of the steep drive PWM. The capacitor between SPVM-SPGND is placed in order to suppress the fluctuations due to the SPVM voltage. However, the effect is reduced if this capacitor is placed far from the IC due to the effect of line impedances. Therefore, this capacitor should be placed near the IC.

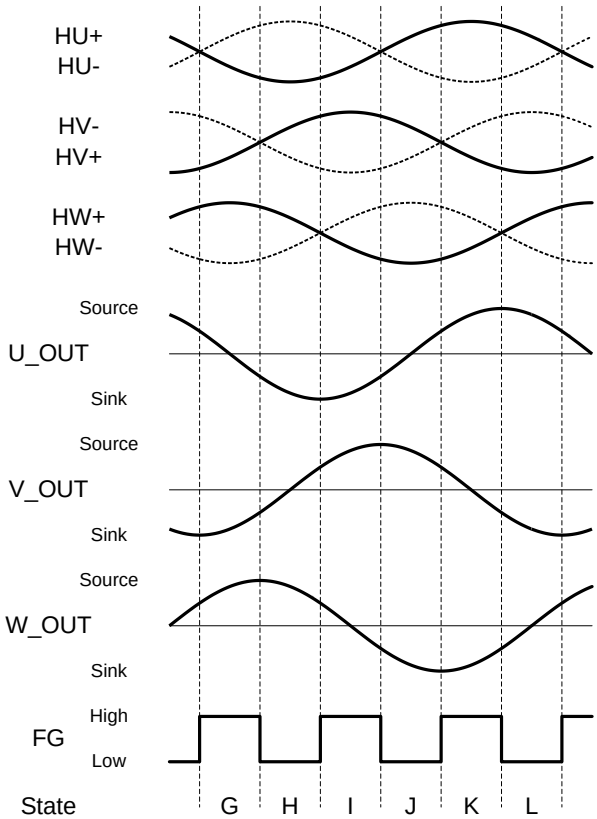
9. Spindle Dricer Input-Output Timing Chart



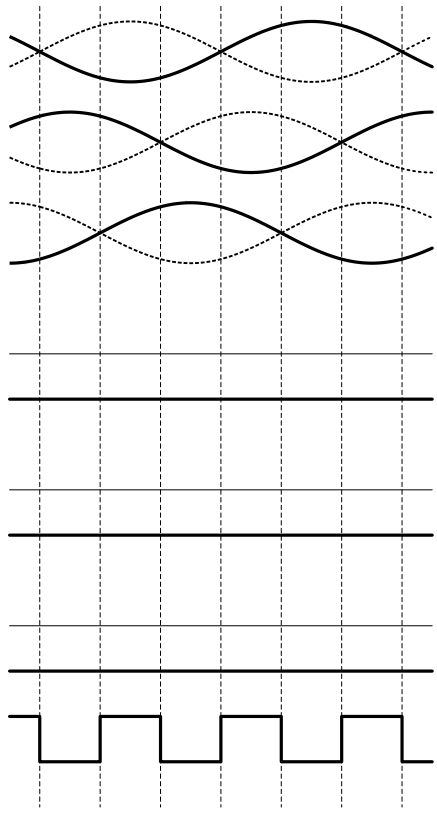
(a) Forward Mode
(DSP>000h)



(b) Short Brake Mode
(DSP<000h, REG 74h[6]=0)



(c) Reverse Brake Mode
(DSP<000h, REG 74h[6]=1)

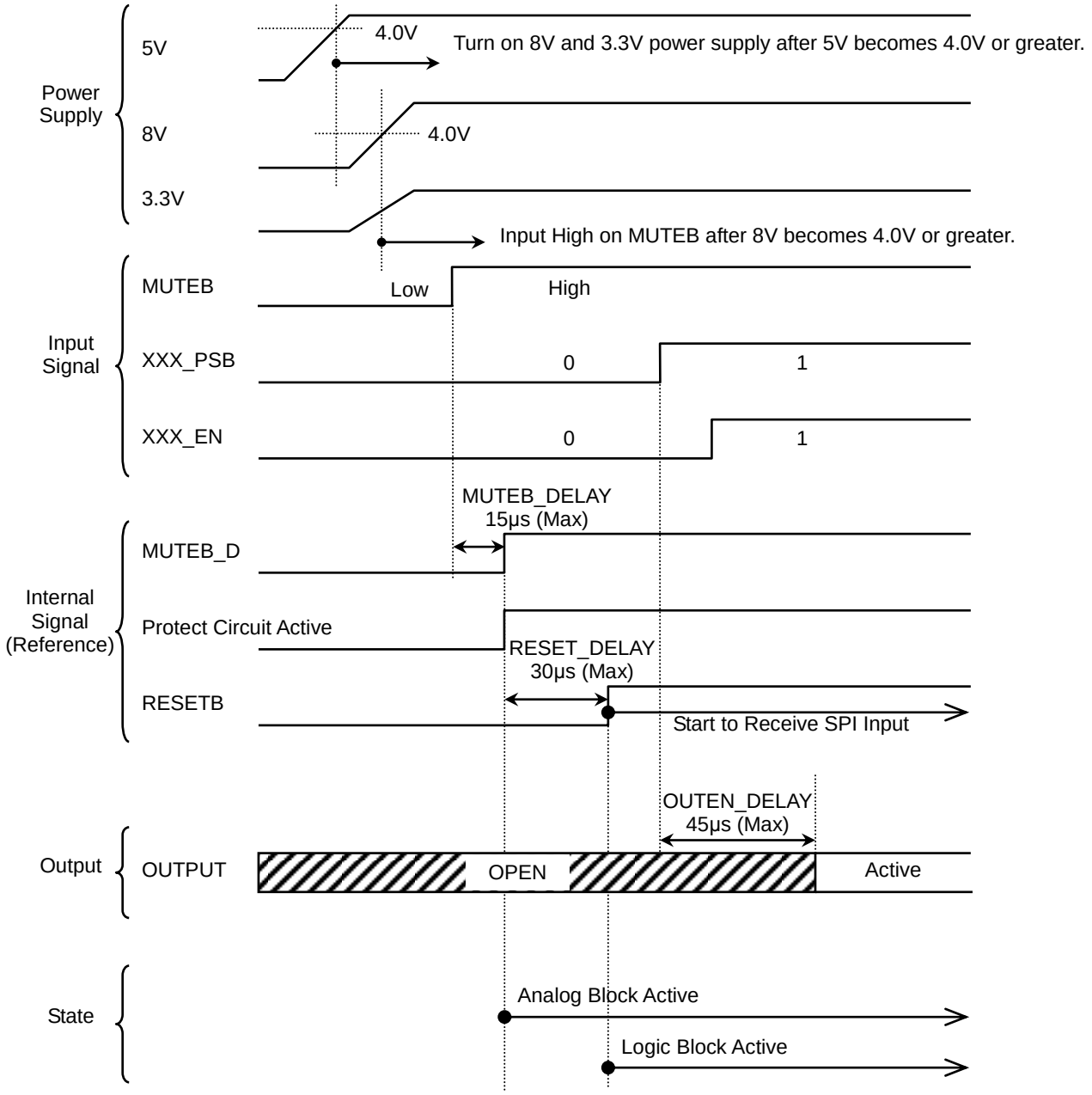


(b) Anti-reverse Mode
(DSP<000h, REG 74h[6]=1, after reverse detected)

Start-up Operation

1. Startup Signals
   - 5V Power supply : PREVCC, FCTLRNF, TKRNF
   - 8V Power supply : VCC, SPRNF, SLRNF1, SLRNF2
   - 3.3V Power supply : SHV
   - MUTEB (Input terminal) : Standby (Low) / Active (High) setting for whole IC
   - XXX_PSB (SPI control signal) : Power save (0) / Active (1) setting for control circuits of 9ch blocks
   - XXX_EN (SPI control signal) : Open (0) / Active (1) setting for output of 9ch blocks
   - MUTEB_D (Internal signal) : Standby / active control for analog block
     There may be 15 µs (Max) delay from MUTEB.
   - RESETB (Internal signal) : Reset /active control for SPI block and logic block

2. Start-up and Shut-down Sequences
   Make sure to turn on 5V power supply before 8V and 3.3V power supplys. Otherwise internal logic becomes indefinite and abnormal output may be produced. As long as 5V power is turned on first, either 8V or 3.3V may be turned on next. There are no special requirements on sequence of power shut down.
   .



Description of Functions

1. Output Voltage State (Spindle / Sled Motor)

	Spindle	Sled Motor
Under Input Dead Zone	Hi-Z	Short Brake
Under Current Limit Operation	Short Brake	Short Brake

2. PWM Oscillation Frequency (Spindle / Sled Motor)

PWM oscillation of the spindle and the sled motor is internally free-running. Oscillation frequency is 100 kHz (Typ).

3. UVLO

If VCC or PREVCC terminal voltage becomes 3.8 V (Typ) or less, or VREG terminal voltage becomes 2.0 V (Typ) or less, output of all channels turns OFF (Hi-Z).

* REG 77h[0] UVLO_VCC is set to "1" while UVLO is activated. And UVLO_VCC is reset to "0" if PREVCC terminal voltage becomes 2.0 V (Typ) or less, or VREG terminal voltage becomes 1.2 V (Typ) or less, but this is below the operational voltage range and some register state may be unsustainable depending on degree of voltage drop.

4. Thermal Shutdown

Thermal shutdown (over temperature protection circuit) is built-in in order to prevent thermal breakage of IC.

The package should be used within acceptable power dissipation, but in case where it is left beyond the acceptable power dissipation, junction temperature rises, and thermal shutdown is activated at 175℃ (Typ) and all the channel outputs are turned OFF (Hi-Z).

Then, when the junction temperature falls down to 150℃ (Typ), the channel outputs are turn ON again. Note that even though the thermal shut down is operating, IC may be overheated and end up broken if heat is continuously applied from outside.

* REG 77h[3] TSD is set to "1" while thermal shutdown is activated, but this condition is beyond the rated temperature and all register states may be unsustainable depending on degree of temperature rise.

5. Loading Supply/Ground-Fault Protection

This is the function to prevent breakage of output POWER MOS when there exist the conditions that may break the output POWER MOS if loading output is supply/ground-faulted.

- Supply-fault occurs when SINK-side POWER MOS is ON, and the supply-fault protection is performed if output terminal voltage of (Power Supply - 1 Vf) or greater and supply-fault current are detected at the same time. Here, the output is OFF-latched. Note that 1 Vf = 0.7V (Typ).
- Ground-fault occurs when SOURCE-side POWER MOS is ON, and the ground-fault protection is performed if ground-fault current is detected. Here, the output is OFF-latched. Note that the ground-fault detection current is dependent on the output voltage. See Figure 25.

* REG 77h[4] SHORT_LD is set to "1" if the loading supply/ground-fault protection is activated.
* You can reset the protection mode by resetting REG 75h[2] SHORT_RESET if the protection mode is activated and the output is OFF-latched.
* High frequency noise suppression filter is built in the supply/ground-fault protection circuit, but the supply/ground-fault protection may be activated against the noise of 10 μs (Typ) or greater.

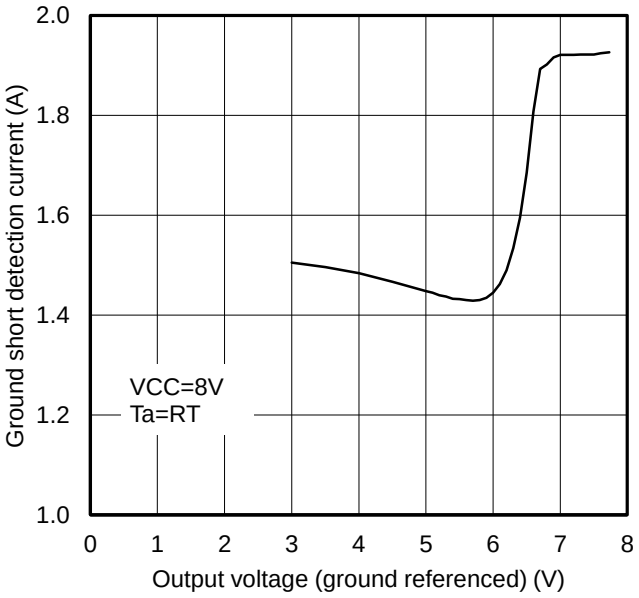


Figure 25. Output voltage vs Ground short detection current

6. Packet Bit Counts Error

Serial input signal of this IC consists of 16 bits in one packet. If counts of the SCLK rising during the period between falling and rising of SLV are anything but 16 times, it is determined as a erroneous packet and REG 77h[2] PKT_ERR is set to "1". Any data determined as an erroneous packet are nullified, and the registers maintain the state immediately before the error. Note that PKT_ERR remains at "1" even though the next 1 packet is sent and counts of the clock rising during the period between falling and rising of SLV are 16 times. But this error will not open (i.e. turn off) the output circuit.

7. Packet Watchdog Timer

If REG 76h[5,4] PKTSTOP_TIME is preset to anything but "00" and there is no valid packet (16 bits) rising of SLV within this preset time period, REG 77h[1] PKT_STOP will be set to "1" and all outputs will be OFF-latched (Hi-Z).

* You can reset the protection mode by resetting REG 75h[4] RST_PKTSTOP if the protection mode is activated and the output is OFF-latched.

8. ERROUT Terminal

If either the packet bit counts error or the packet watchdog timer is activated, this terminal switches to High as an error flag.

9. PRTOUT Terminal

Operational state of MUTEB, UVLO and actuator overcurrrent protection is output to PRTOUT terminal. Output conditions are as per the following table.

<table>
<tr><th>MUTEB</th><th>UVLO</th><th>Overcurrent Protection</th><th>PRTOUT</th></tr>
<tr><td rowspan="4">L</td><td rowspan="2">ON</td><td>ON</td><td rowspan="6">H*</td></tr>
<tr><td>OFF</td></tr>
<tr><td rowspan="2">OFF</td><td>ON</td></tr>
<tr><td>OFF</td></tr>
<tr><td rowspan="4">H</td><td rowspan="2">ON</td><td>ON</td></tr>
<tr><td>OFF</td></tr>
<tr><td rowspan="2">OFF</td><td>ON</td></tr>
<tr><td>OFF</td><td>L</td></tr>
</table>

*When connected with pull-up resistor.

10. VREG Terminal

VREG terminal is the regurator output for internal blocks. A 0.01µF compensating capacitor shall be connected across the VREG terminal. Any value less than 0.01µF, or no compensating capacitor will result in system instablity.

11. Actuator Overcurrent Protection (OCP: Over Current Protection)

This is the function to protect the actuator when overcurrent condition is detected over a preset time period.

PRTT, PRTFT	PRTOUT	Actuator Output
> 2.95V	H	Hi-Z (Protection Enabled)
< 2.95V	L	Active

Charges/discharges the capacitor with current proportional to load current based on the externally preset load current threshold as "0".

Time period until the protection is activated is subject to the value of the capacitors connected to PRTT and PRTFT terminals and the resistors connected to TKRNF, FCTLRNF, TKCDET, FCTLCDET and PRTLIM terminals. Default value of PRTT and PRTFT terminals is 1.06 V (Typ). The protection is activated at 2.95 V (Typ). (Be aware that the protection will be activated even at start-up or when recovered from stand-by, as long as voltage of 2.95 V or greater remains at PRTT or PRTFT terminal.)

The protection will be deactivated when voltage at PRTT and PRTFT terminals falls down to 1.1 V or less and REG 75h[3] RST_OCP is set to "1" at that timing.

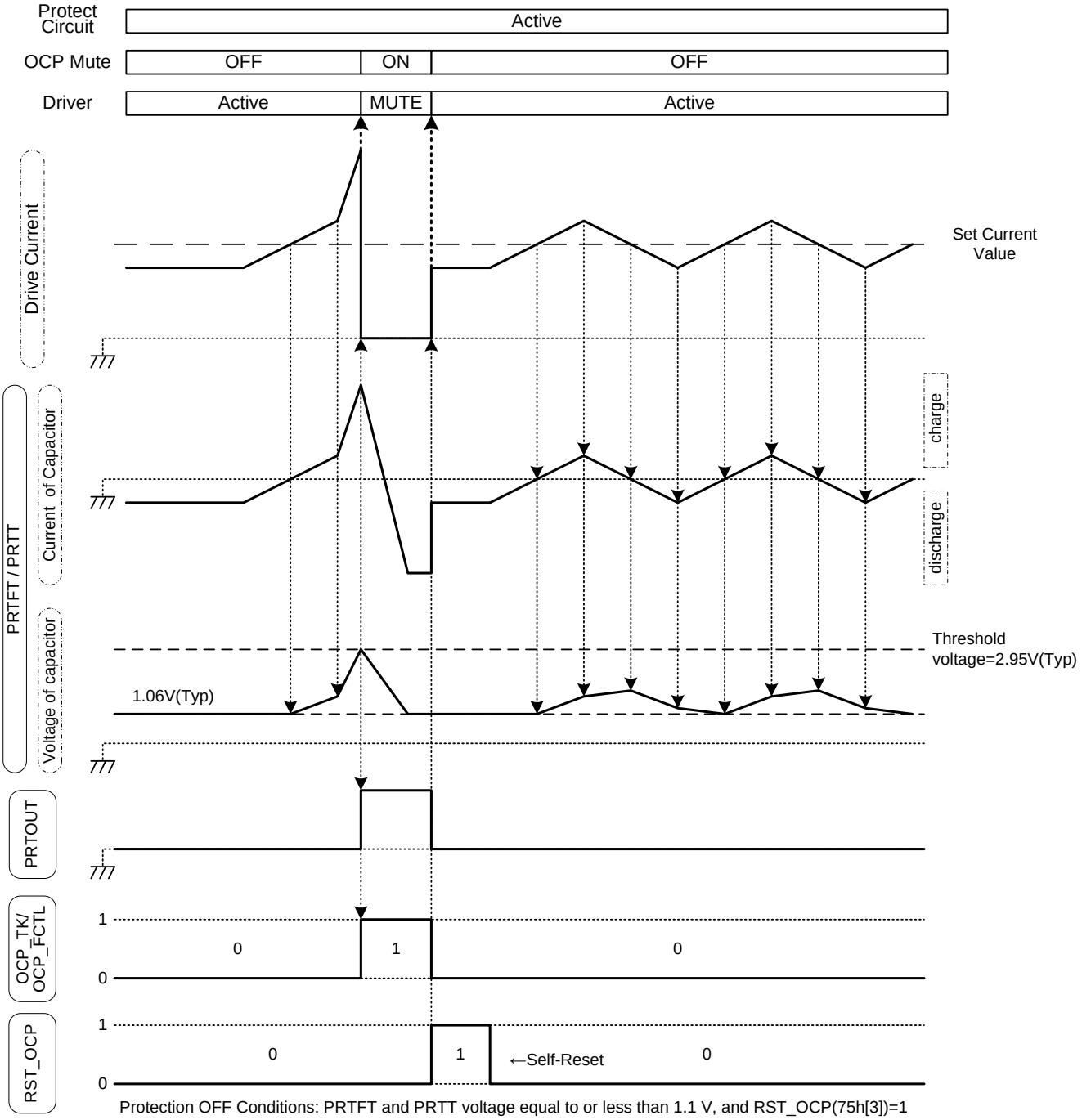


Figure 26. OCP Timing Chart

12. Example of Constants Setting for Actuator Overcurrent Protection Circuit

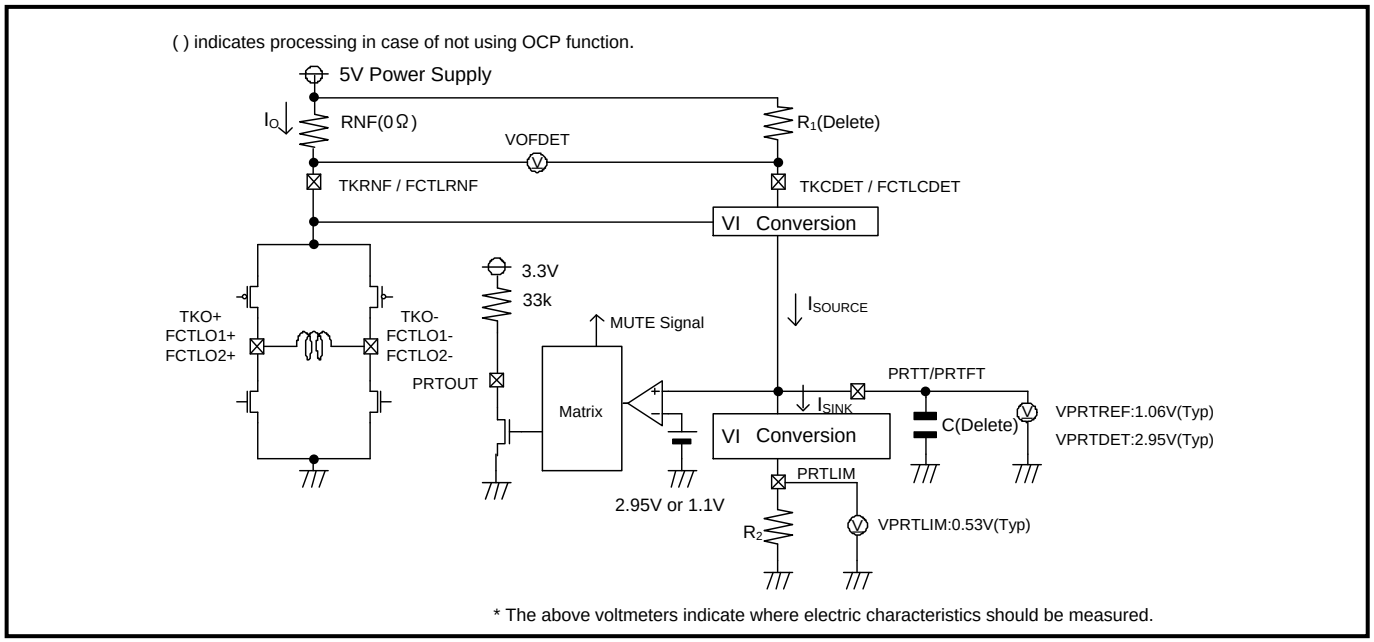


Figure 27. Overcurrent Protection Circuit Constants

Capacitor-recharging/discharging current I_{SINK} and I_{SOURCE} can be obtained respectively as follows.

$$I_{SINK} = \frac{VPRTLIM}{R_2},\ I_{SOURCE} = \frac{RNF \times I_O}{R_1}$$

Load current I_t (threshold current) which begins to detect overcurrent is the current where $I_{SINK}=I_{SOURCE}$, and can be obtained as follows.

$$I_{SINK} = I_{SOURCE}$$
$$\frac{VPRTLIM}{R_2} = \frac{RNF \times I_t}{R_1}$$
$$I_t = \frac{R_1}{R_2} \times \frac{VPRTLIM}{RNF}$$

$I_{SINK} < I_{SOURCE}$, so t_d, the time period until error detection flag is output, should be the time period until PRTFT/PRTT voltage becomes 2.95 V (Typ) and can be obtained as follows. ($V_d = VPRTDET - VPRTREF = 2.95 - 1.06 = 1.89V$)

$$C \times V_d = (I_{SOURCE} - I_{SINK}) \times t_d$$
$$t_d = \frac{C \times V_d}{I_{SOURCE} - I_{SINK}}$$
$$t_d = \frac{C \times V_d}{\frac{RNF \times I_O}{R_1} - \frac{VPRTLIM}{R_2}}$$

For example, suppose that t_d=100 ms, I_O=200 mA, I_t=100 mA, RNF=0.5 Ω and R_2=47 kΩ, R_1 and C can be obtained respectively as follows.

$$R_1 = \frac{R_2 \times RNF}{VPRTLIM} \times I_t = \frac{47k \times 0.5}{0.53} \times 100m = 4.4(k\Omega)$$
$$C = \frac{t_d}{V_d} \times \left(\frac{RNF \times I_o}{R_1} - \frac{VPRTLIM}{R_2} \right) = \frac{100m}{1.89} \times \left(\frac{0.5 \times 200m}{4.4k} - \frac{0.53}{47k} \right) = 0.61(\mu F)$$

Also, t_{dc}, the time period after activation of the protection until PRTFT/PRTT voltage goes down to the default voltage (1.06 V Typ) through discharge of C, can be obtained as follows.

$$C \times V_d = I_{sink} \times t_{dc}$$
$$\therefore t_{dc} = \frac{C \times Vd}{I_{SINK}} = \frac{C \times (VPRTDET - VPRTREF)}{I_{SINK}} = \frac{0.59 \times (2.95 - 1.06) \times 47k}{0.53} = 102(ms)$$

Noise Suppression

The following are possible causes of noise of the PWM driver.

A. Noise from power line or ground

B. Radiated noise

- Countermeasures against A -

(1) Reduce impedance in wiring for the driver's 8 V power supply (SPRNF, SLRNF 1, SLRNF 2, VCC), 5V power supply (FCTLRNF, TKRNF) and power GND (SPGND, SLGND, ACTGND) lines where high current flows. Make sure that they be separated from power supply lines of other devices at the root so that they do not have common impedance. (Figure 28)

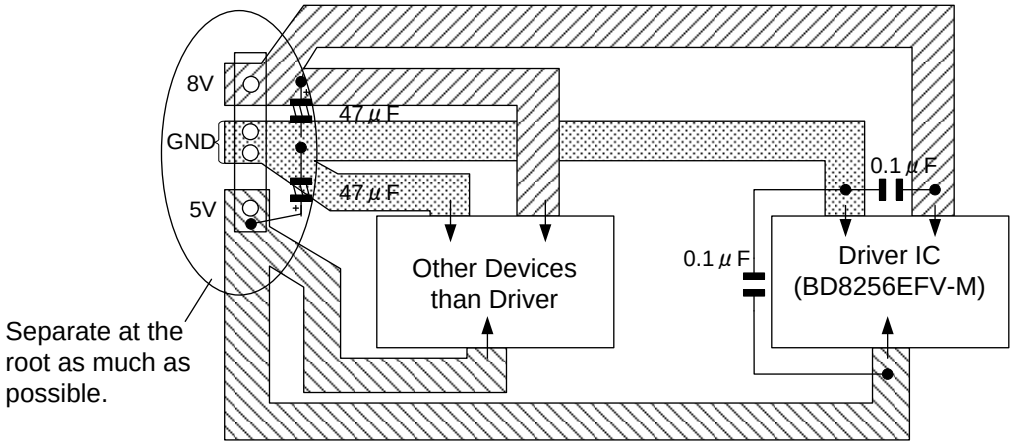


Figure 28. Pattern Example

(2) Provide a low ESR electrolytic capacitor between the power terminal and the ground terminal of the driver to achieve strong stabilization. Provide a ceramic capacitor with good high frequency property next to the IC.
Also provide a ceramic capacitor with good high frequency property between RNF and GND. (Figure 29)
Then power supply ripple due to PWM switching and spindle motor rotation can be reduced.

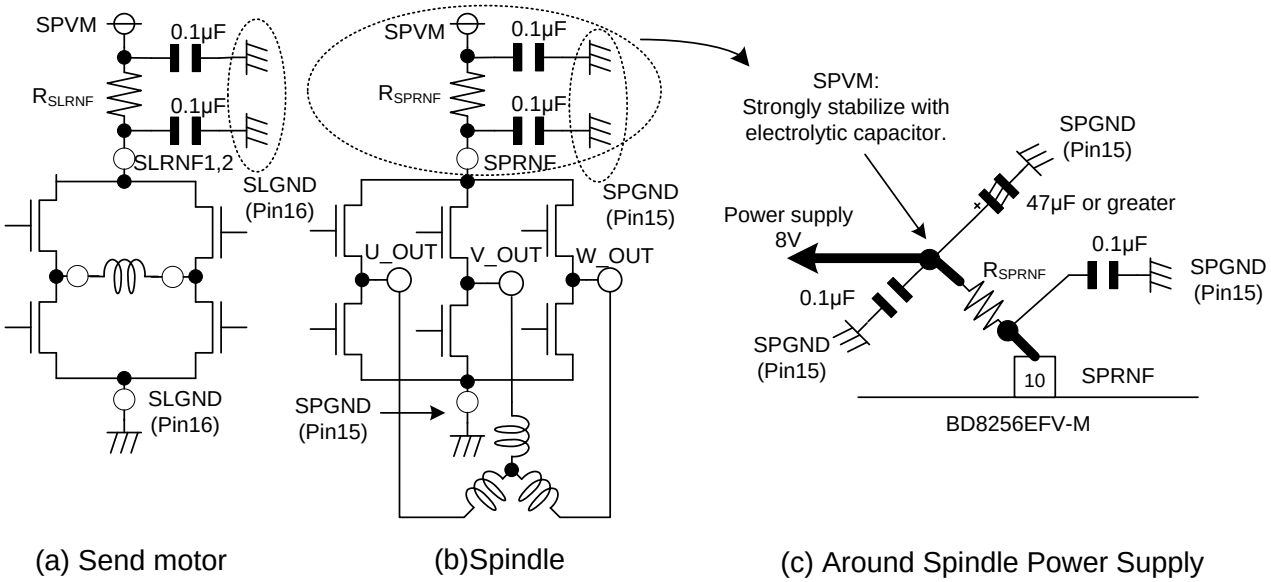


Figure 29. Position of Ceramic Capacitors

(3) If you could not improve the situation by (1) and (2), another way is to insert a LC filter in the power line or the ground line.

Example:

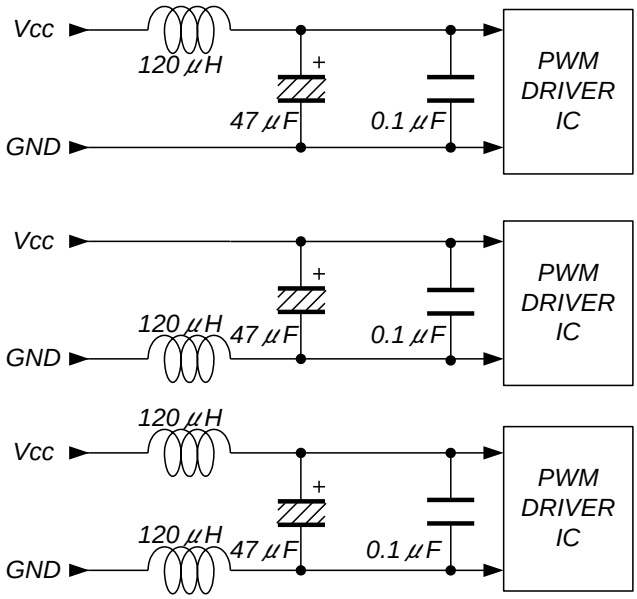


Figure 30. LC Filter Diagram

(4) Or you can also add a capacitor of around 2200 pF between each output and the ground. In this case, ensure that the GND wiring should not have any common impedance with other signals.

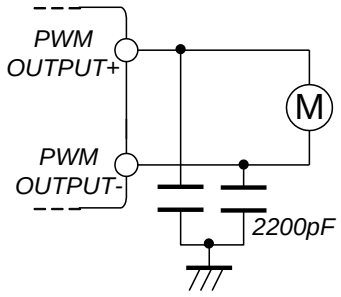


Figure 31. Snubber Circuit

- Countermeasures against B - See Figure 32 -
  - (1) Ensure certain distance between RF signal line and PWM-driven output line. If they must be located inevitably too close, shield the RF signal line with GND except the stable GND.
  - (2) Like in (1), flexible cable to the pickup should be shielded with GND in order to separate noise between the signal line and the actuator drive output line.
  - (3) Connect the motor system and the actuator system to separate flexible cables.
  - (4) As FG pulse is generated from hall signal, provide a shield with stable GND or other wire with low impedance between the PWM output and the hall signal so that noise is not radiated from the flexible cable and the board pattern.

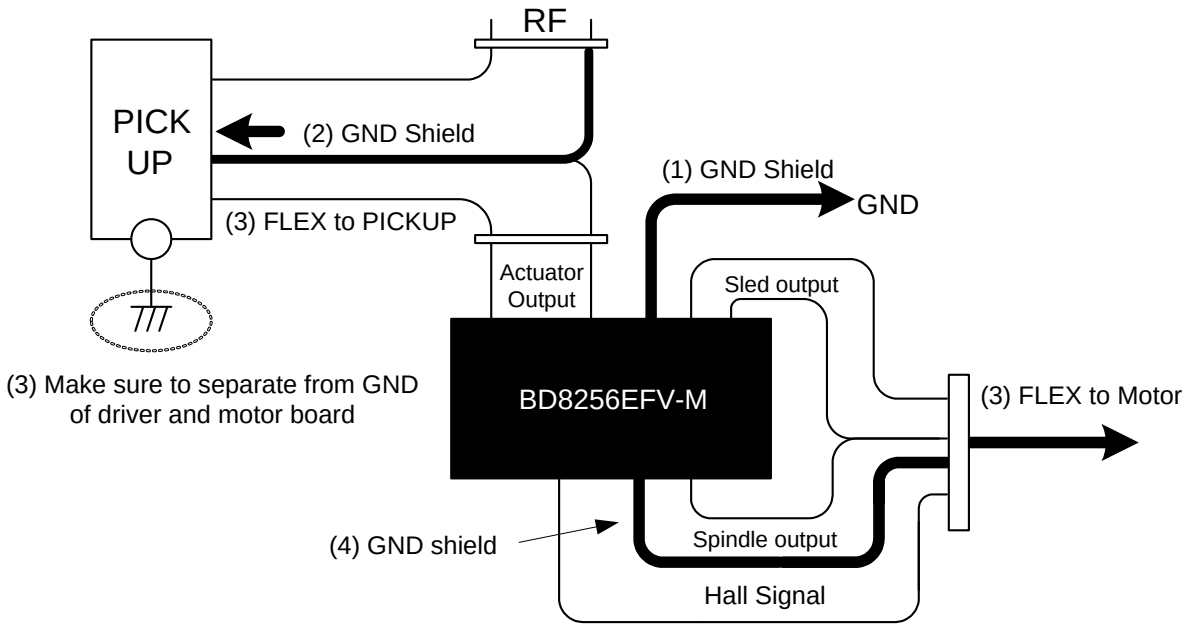


Figure 32. RF Noise Suppression

Power Supply and Ground *(○) is pin.

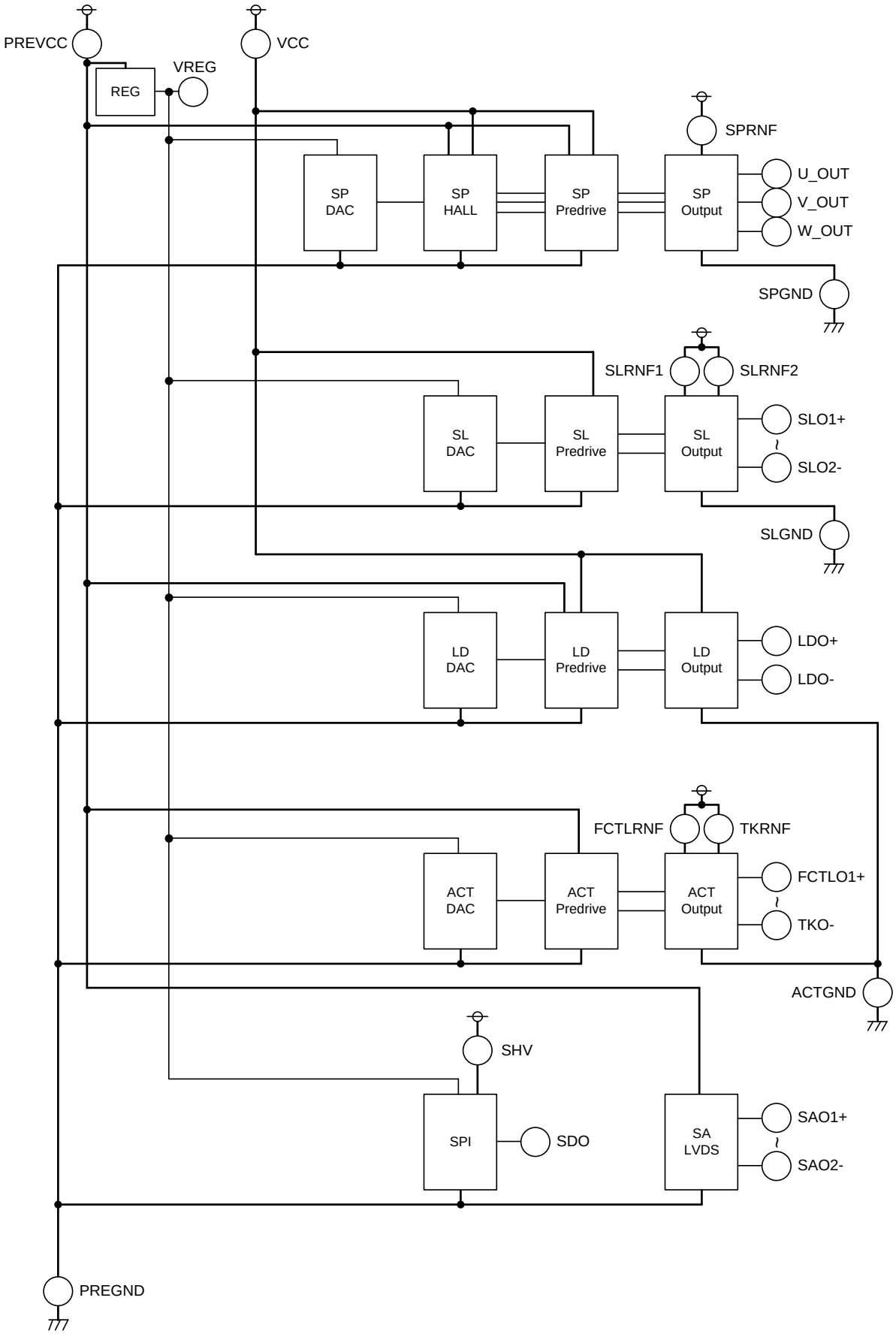


Figure 33. Power Supply and Ground

Application Example1

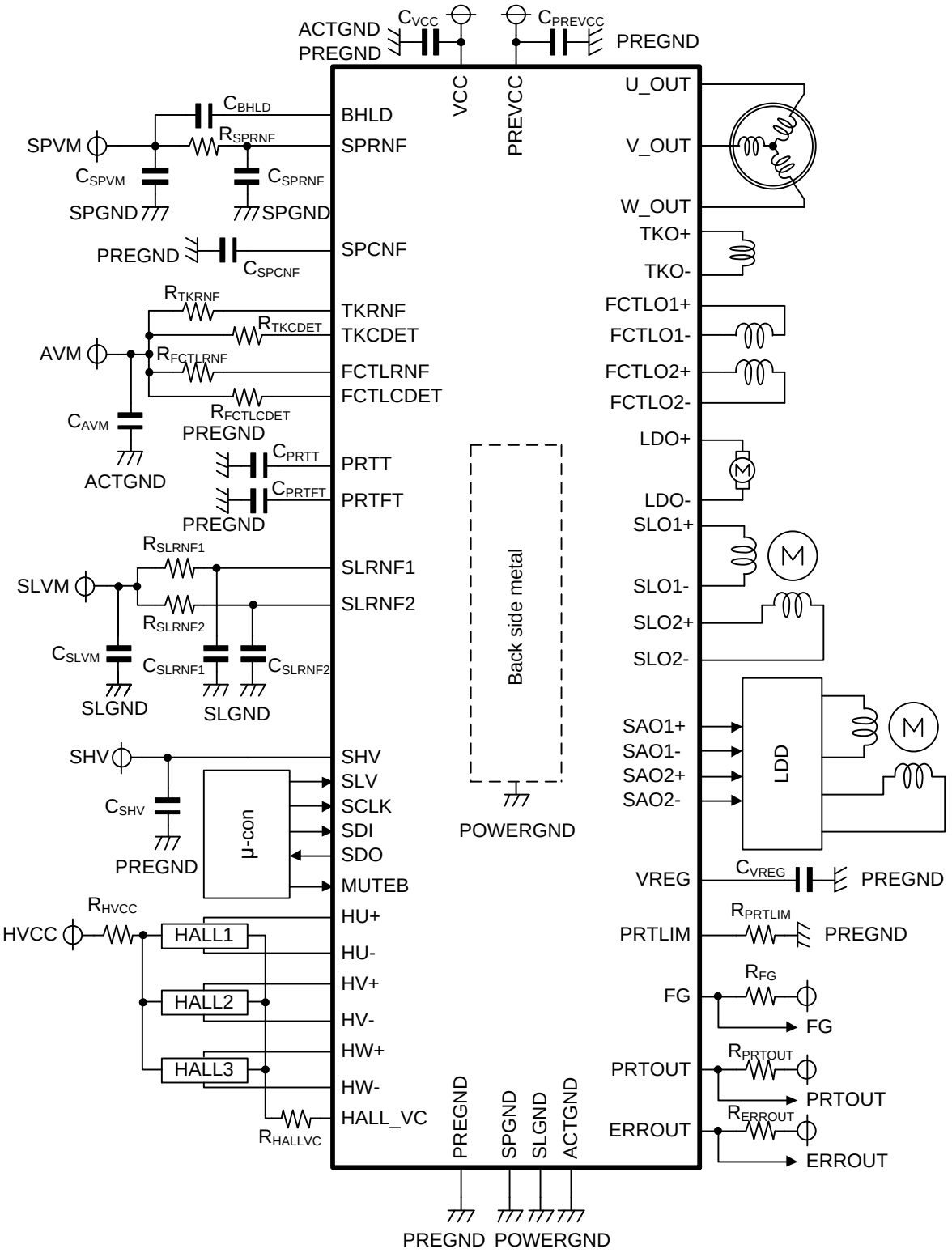


Figure 34. Application Example

▼Recommended values1 for Application Example1

Component name	Component value	Product name	Manufacturer
C_{VCC}	0.1μF	GCM188R11H Series	murata
	47μF	UCD1E470MCL	Nichicon
C_{PREVCC}	0.1μF	GCM188R11H Series	murata
C_{BHLD}	470pF	GCM188R11H Series	murata
C_{SPVM}	0.1μF	GCM188R11H Series	murata
	47μF	UCD1E470MCL	Nichicon
R_{SPRNF}	0.33Ω	MCR100 Series	Rohm
C_{SPRNF}	0.1μF	GCM188R11H Series	murata
C_{SPCNF}	0.01μF	GCM188R11H Series	murata
C_{AVM}	0.1μF	GCM188R11H Series	murata
	47μF	UCD1E470MCL	Nichicon
R_{TKRNF}	0.5Ω	MCR100 Series	Rohm
R_{TKCDET}	10kΩ	MCR03 Series	Rohm
$R_{FCTLRNF}$	0.5Ω	MCR100 Series	Rohm
$R_{FCTLCDET}$	10kΩ	MCR03 Series	Rohm
C_{PRTT}	0.1μF	GCM188R11H Series	murata
C_{PRTFT}	0.1μF	GCM188R11H Series	murata
C_{SLVM}	0.1μF	GCM188R11H Series	murata
	47μF	UCD1E470MCL	Nichicon
R_{SLRNF1}	0.56Ω	MCR100 Series	Rohm
R_{SLRNF2}	0.56Ω	MCR100 Series	Rohm
C_{SLRNF1}	0.1μF	GCM188R11H Series	murata
C_{SLRNF2}	0.1μF	GCM188R11H Series	murata
C_{SHV}	0.1μF	GCM188R11H Series	murata
R_{HVCC}	100Ω	MCR03 Series	Rohm
R_{HALLVC}	100Ω	MCR03 Series	Rohm
C_{VREG}	0.01μF	GCM188R11H Series	murata
R_{PRTLIM}	47kΩ	MCR03 Series	Rohm
R_{FG}	3.3kΩ	MCR03 Series	Rohm
R_{PRTOUT}	33kΩ	MCR03 Series	Rohm
R_{ERROUT}	33kΩ	MCR03 Series	Rohm

Application Example2

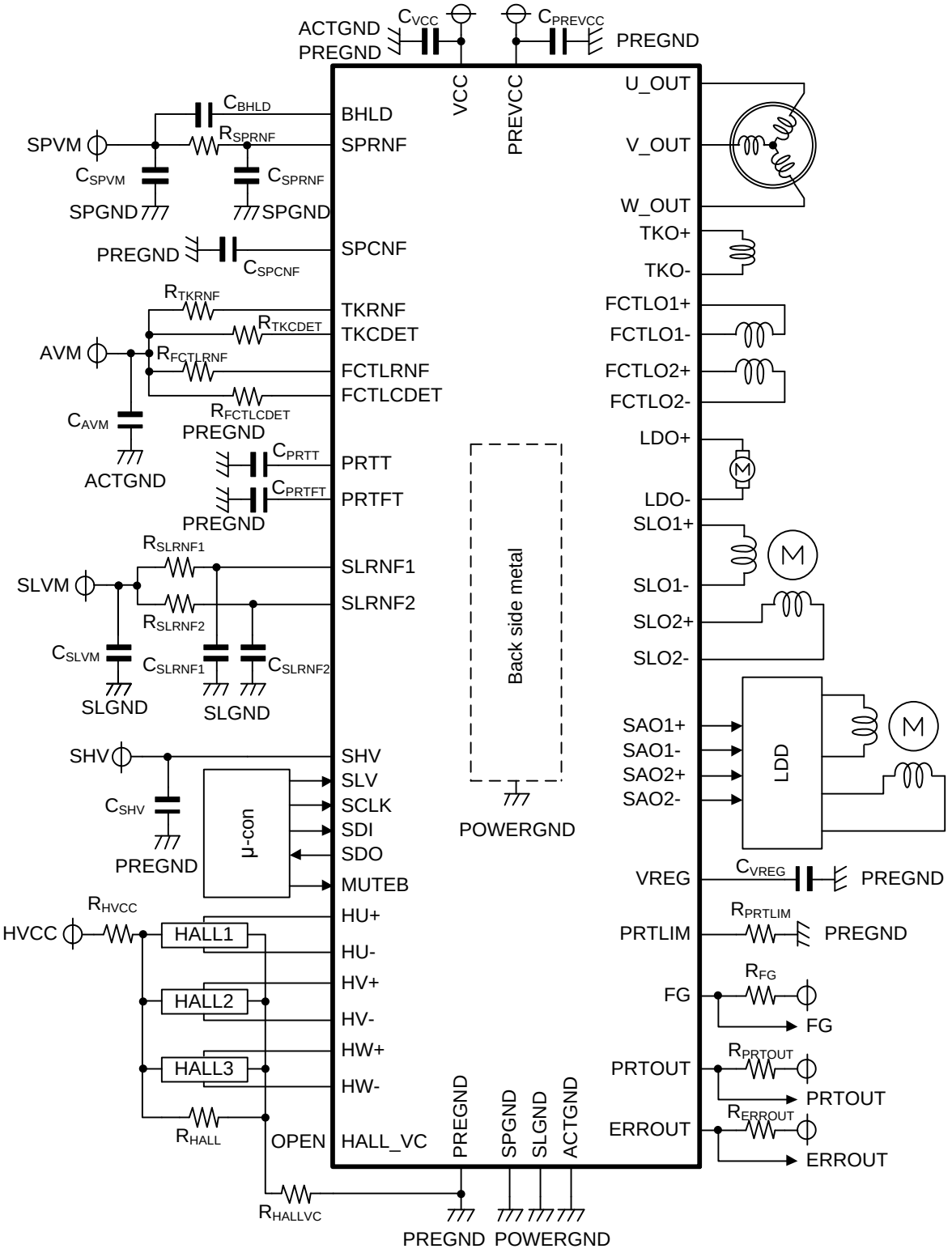


Figure 34. Application Example

▼Recommended values2 for Application Example2

Component name	Component value	Product name	Manufacturer
C_{VCC}	0.1μF	GCM188R11H Series	murata
	47μF	UCD1E470MCL	Nichicon
C_{PREVCC}	0.1μF	GCM188R11H Series	murata
C_{BHLD}	470pF	GCM188R11H Series	murata
C_{SPVM}	0.1μF	GCM188R11H Series	murata
	47μF	UCD1E470MCL	Nichicon
R_{SPRNF}	0.33Ω	MCR100 Series	Rohm
C_{SPRNF}	0.1μF	GCM188R11H Series	murata
C_{SPCNF}	0.01μF	GCM188R11H Series	murata
C_{AVM}	0.1μF	GCM188R11H Series	murata
	47μF	UCD1E470MCL	Nichicon
R_{TKRNF}	0.5Ω	MCR100 Series	Rohm
R_{TKCDET}	10kΩ	MCR03 Series	Rohm
$R_{FCTLRNF}$	0.5Ω	MCR100 Series	Rohm
$R_{FCTLCDET}$	10kΩ	MCR03 Series	Rohm
C_{PRTT}	0.1μF	GCM188R11H Series	murata
C_{PRTFT}	0.1μF	GCM188R11H Series	murata
C_{SLVM}	0.1μF	GCM188R11H Series	murata
	47μF	UCD1E470MCL	Nichicon
R_{SLRNF1}	0.56Ω	MCR100 Series	Rohm
R_{SLRNF2}	0.56Ω	MCR100 Series	Rohm
C_{SLRNF1}	0.1μF	GCM188R11H Series	murata
C_{SLRNF2}	0.1μF	GCM188R11H Series	murata
C_{SHV}	0.1μF	GCM188R11H Series	murata
R_{HVCC}	10Ω(1)	MCR03 Series	Rohm
R_{HALL}	100Ω(1)	MCR03 Series	Rohm
R_{HALLVC}	100Ω(1)	MCR03 Series	Rohm
C_{VREG}	0.01μF	GCM188R11H Series	murata
R_{PRTLIM}	47kΩ	MCR03 Series	Rohm
R_{FG}	3.3kΩ	MCR03 Series	Rohm
R_{PRTOUT}	33kΩ	MCR03 Series	Rohm
R_{ERROUT}	33kΩ	MCR03 Series	Rohm

(1)at HVCC = 3.3V, Hall elements 25°C resistance = 250Ω~450Ω

Power Dissipation

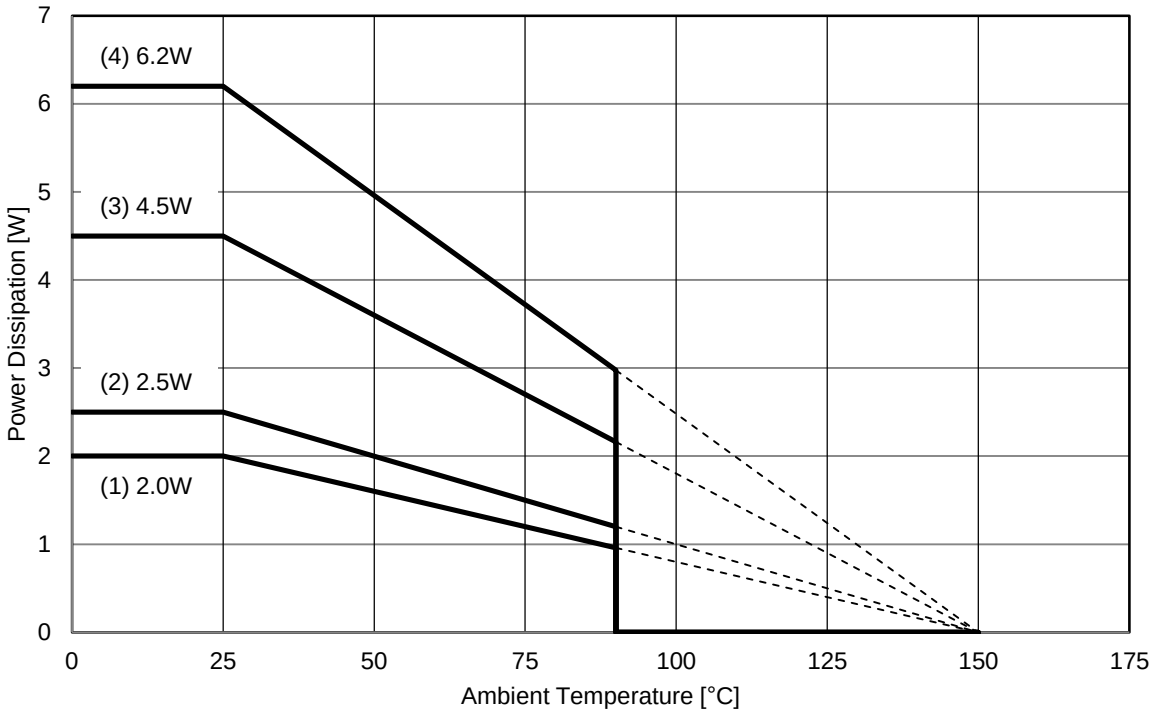


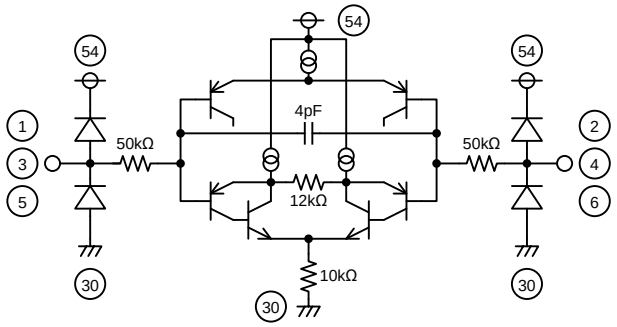
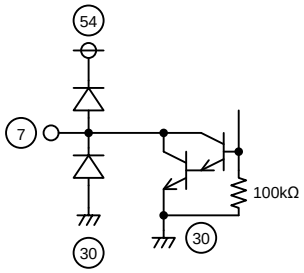
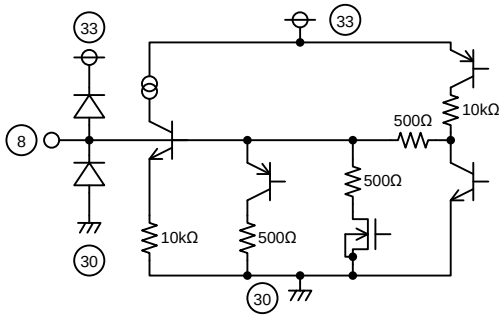
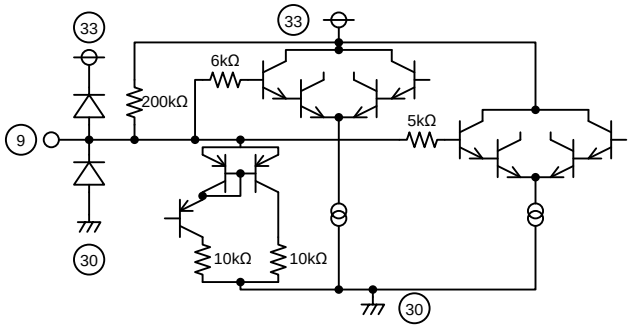
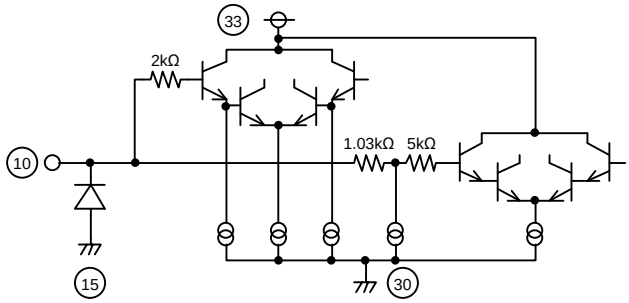
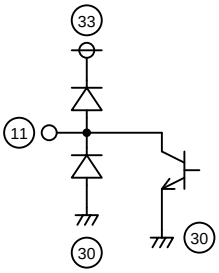
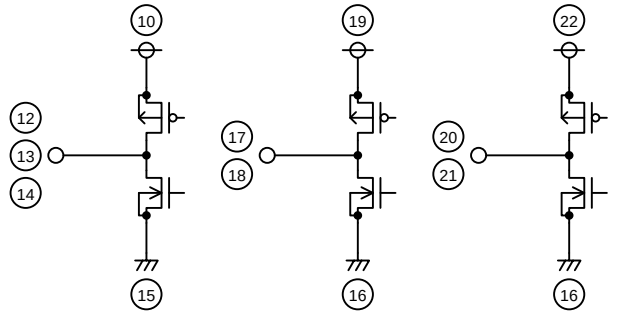
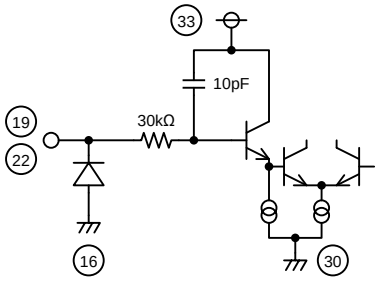
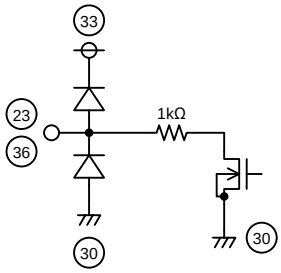
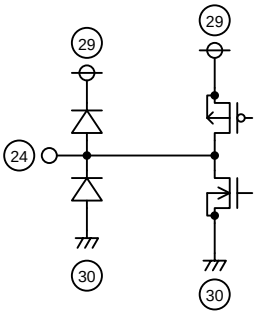
Figure 35. Power dissipation

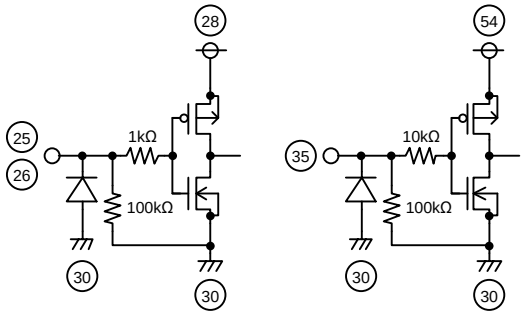
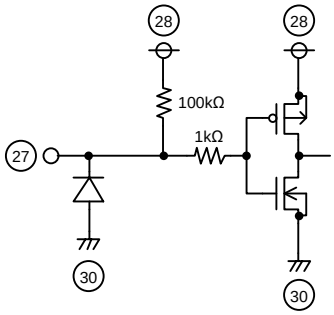
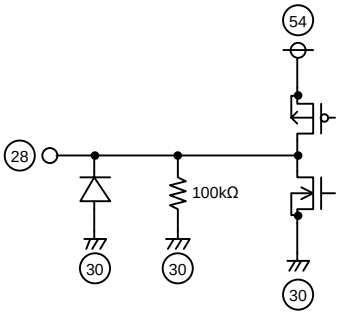
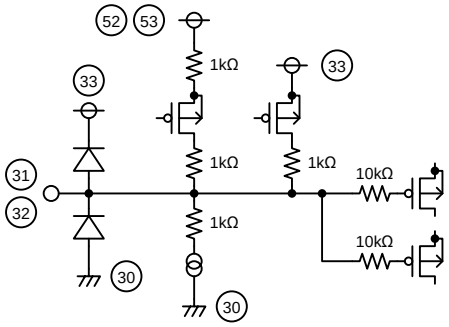
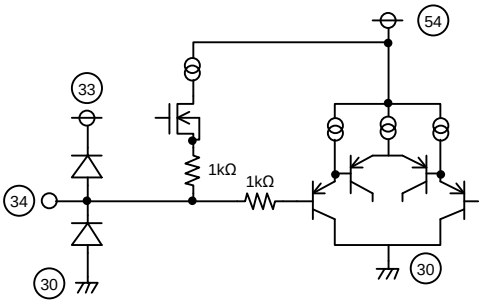
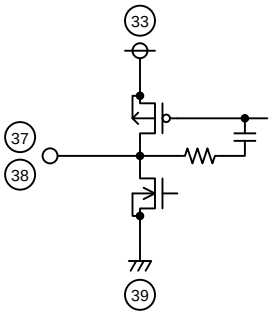
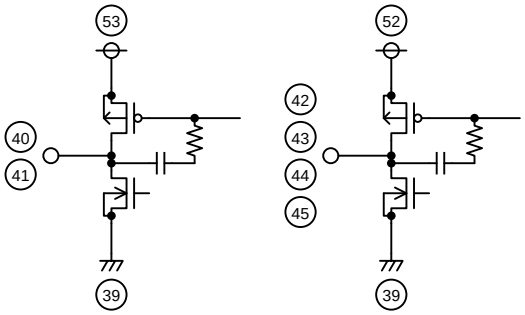
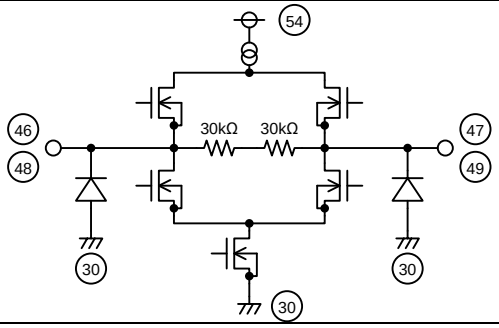
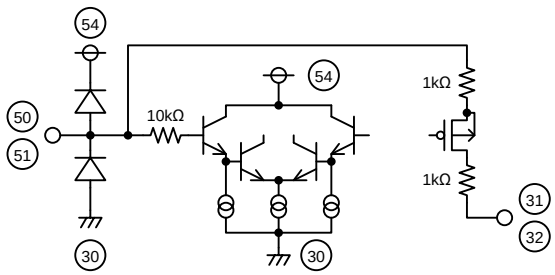
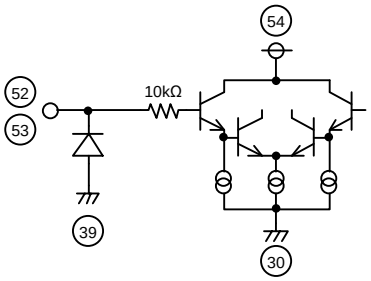
Note 1: Power dissipation calculated when mounted on 70mm X 70mm X 1.6mm glass epoxy substrate 1-layer platform.
Note 2: Power dissipation changes with the copper foil density of the board. This value represents only observed values, not guaranteed values.

The board and the back exposure heat radiation board are connected through solder.
Board(1) : 1-layer board (backside copper thickness 0mm × 0mm)
Board(2) : 2-layer board (backside copper thickness 20mm × 11mm)
Board(3) : 2-layer board (backside copper thickness 70mm × 70mm)
Board(4) : 4-layer board (backside copper thickness 70mm × 70mm)

Board(1) : θja = 62.5 °C/W
Board(2) : θja = 50.0 °C/W
Board(3) : θja = 27.8 °C/W
Board(4) : θja = 20.2 °C/W

Input-Output Equivalent Circuit (Number is pin number, the value of resistor and capacitor is typical value)

1.HU+, 2.HU-, 3.HV+, 4.HV-, 5.HW+, 6.HW-	7.HALL_VC
	
8.SPCNF	**9.BHLD**
	
10.SPRNF	**11.FG**
	
12.W_OUT, 13.V_OUT, 14.U_OUT, 17.SLO1+, 18.SLO1-, 20.SLO2+, 21.SLO2-	**19.SLRNF1, 22.SLRNF2**
	
23.ERROUT, 36.PRTOUT	**24.SDO**
	

25.SDI, 26.SCLK, 35.MUTEB	27.SLV
	
28.VREG	31.PRTT, 32.PRTFT
	
34.PRTLIM	37.LDO-, 38.LDO+
	
40.TKO+, 41.TKO-, 42.FCTLO1+, 43.FCTLO1-, 44.FCTLO2+, 45.FCTLO2-	46.SAO1+, 47.SAO1-, 48.SAO2+, 49.SAO2-
	
50.TKCDET, 51.FCTLCDET	52.FCTLRNF, 53.TKRNF
	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

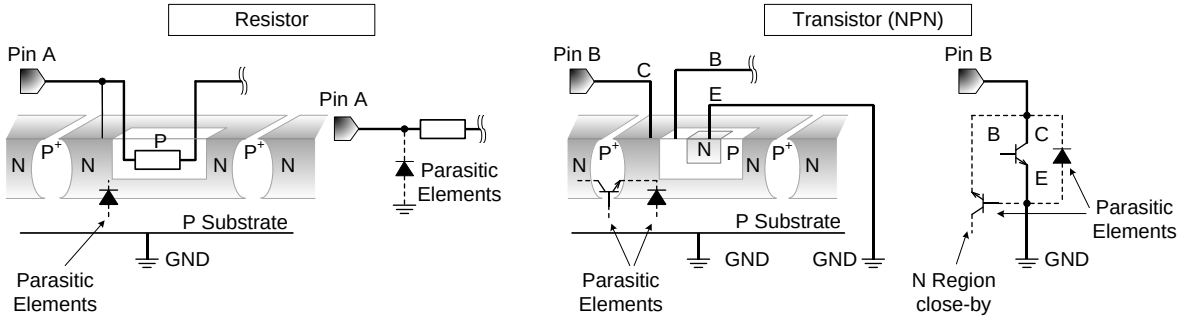


Figure 36. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

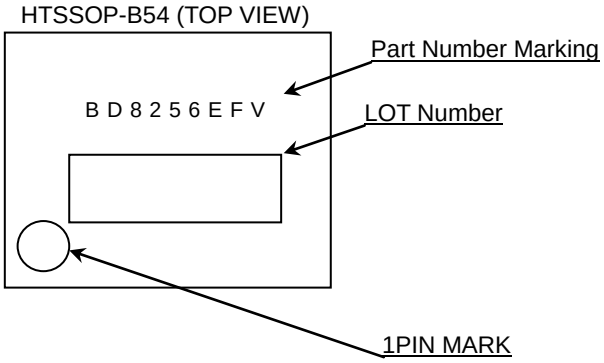
15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

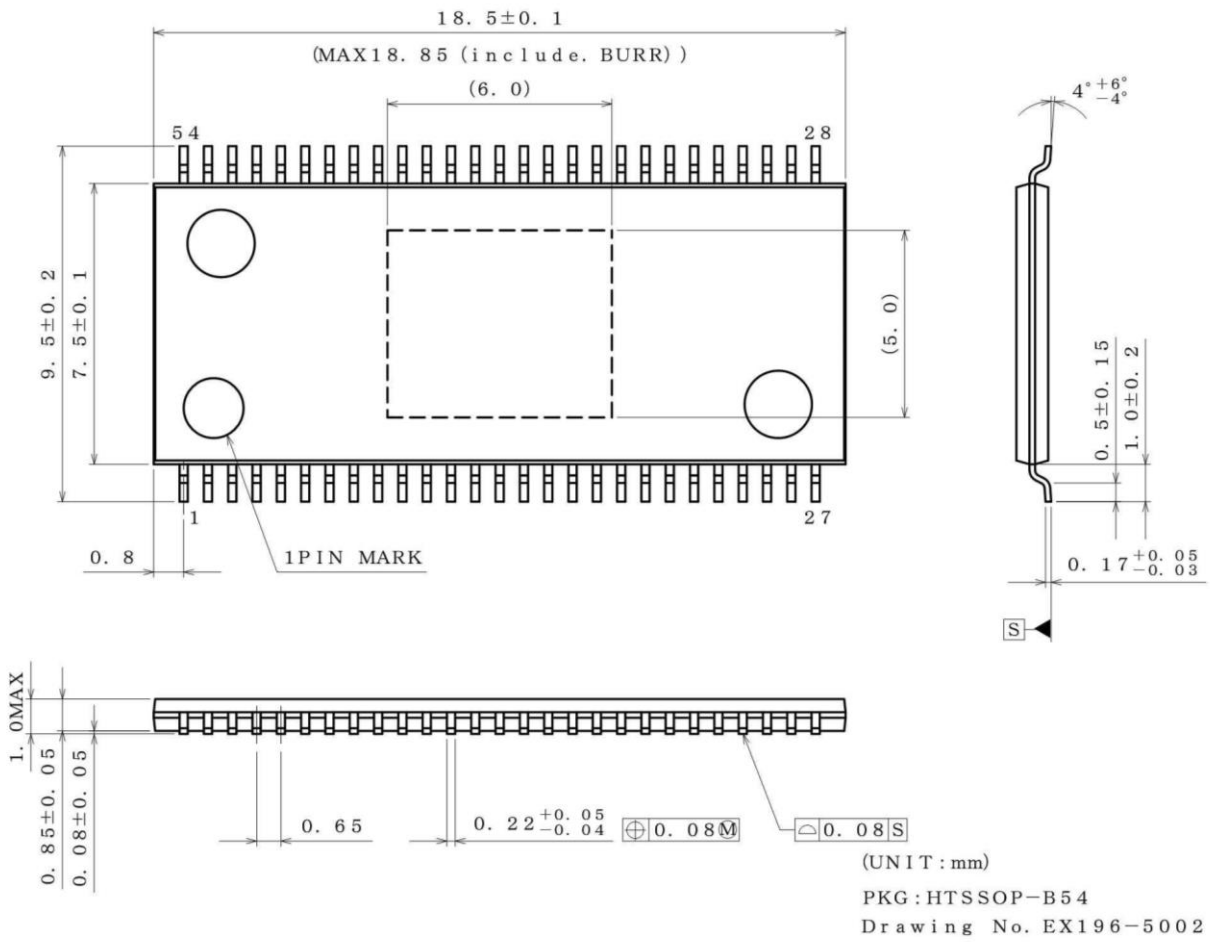
B D 8 2 5 6 E F V	-	M E 2
Part Number	Package EFV : HTSSOP-B54	Packaging and forming specification M: High relaiability E2: Embossed tape and reel (HTSSOP-B54)

Marking Diagram



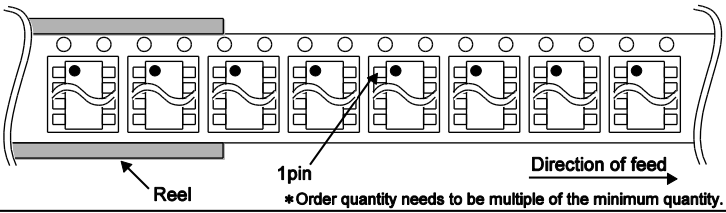
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B54



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
1.Aug.2013	002	New release
25.Apr.2014	003	P.1 Add the sentence of AEC-Q100 Qualified at the features
4.Apr.2016	004	P.2 Change : Pin3 HV+ V negative⇒V positive Pin4 HV- V positive⇒V negative P.3 Change : (2)FCCDET⇒FCTLCDET, (3)LDO⇒LDO-, (4)SAO2⇒SAO2- P.4, 5 Add R_L=8Ω at the conditions P.9 Change : **P9⇒P.15 P.18 Change : DACFCTL2 = DFCTL2 - DFCTL2⇒DACFCTL2 = DFCTL2 - DFCTL1 P.20 Add *Condition:R_{SLRNF}=0.56Ω P.21 Add *Condition:R_{SPRNF}=0.33Ω P.26 Change : Figure 22. C_{SPRNF}⇒C_{SPCNF} P.27 5.Update : Hall input voltage range from 1.0 ~ 3.8V to 1.5 ~ 3.8V Add : Explanation about Hall bias P.33 Change : VPRTDET:3.0V(Typ)⇒2.95V(Typ), Vd=VPRTLIM-VPRREF⇒Vd=VPRTDET-VPRTREF P.37 Change : FCTLO+, SA1O+, SA2O- ⇒FCTLO1+, SAO1+, SAO2- P.38 Change : title : from Application Example to Application Example1, Change : FCRNF, FCCDET, R_{FCRNF}, R_{FCCDET}⇒FCTLRNF, FCTLCDET, $R_{FCTLRNF}$, $R_{FCTLCDET}$ P.39 Change title : from Recommended values to Recommended values1 for Application Example1 Change : R_{FCRNF}, R_{FCCDET}⇒$R_{FCTLRNF}$, $R_{FCTLCDET}$ P.40 New addition : Application Example2 P.41 New addition : Recommended values2 for Application Example2 P.43, P.44 Change : 12.U_OUT, 14.W_OUT⇒12.W_OUT, 14.U_OUT, Update : Figure about Pin10, 25, 26, 35, 27, 28, 34, 52, 53

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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