For Automotive 45 V 150 mA Fixed/Adjustable Output Nano Cap™ LDO Regulators

Nano Cap

BD9xxN1-C Series

General Description

The BD9xxN1-C series are linear regulators using the Nano Cap™ topology *(Note 1)* designed as low current consumption products for power supplies in various automotive applications requiring a direct connection to the battery.

These products are designed for up to 45 V as an absolute maximum voltage and to operate until 150 mA for the output current with low current consumption 28 µA (Typ). These can regulate the output with a very high accuracy ±2.0 %.

The output capacitor 100 nF (Typ) or more can be used for this product series, and it can realize a brilliant transient characteristic even with small capacitance.

The output voltage line-up are 3.3 V, 5.0 V and Adjustable type by an external resistive divider. The output voltage can be adjusted between 1.0 V and 18 V by an external resistive divider connected to the ADJ pin.

Enable feature is integrated in the devices. A logical “HIGH” at the EN pin turns on the device, and the devices are controlled to disable by a logical “LOW” input to the EN pin *(Note 2)*.

The devices feature the integrated Over Current Protection to protect the device from a damage caused by a short-circuiting or an overload. These products also integrate Thermal Shutdown Protection to avoid the damage by overheating and Under Voltage Lock Out to avoid false operation at low input voltage.

Furthermore, low ESR ceramic capacitors are sufficiently applicable for the phase compensation.

(Note 1) Nano Cap™ is a combination of technologies which allow stable operation even if output capacitance is connected with the range of nF unit.
(Note 2) Applicable for product with Enable Function

Key Specifications

- Wide Temperature Range (Tj): -40 °C to +150 °C
- Wide Operating Input Range: 3 V to 42 V
- Output Voltage: 3.3 V / 5.0 V / Adjustable
- Low Current Consumption *(Note 3)*: 28 µA (Typ)
- Output Current Capability: 150 mA
- High Output Voltage Accuracy *(Note 4)*: ±2.0 %

(Note 3) It does not contain the current of external feedback resistance.
(Note 4) The effect of external feedback resistor is not included.

Features

- Nano Cap™ Topology *(Note 1)*
- QuiCur™ Topology *(Note 5)*
- AEC-Q100 *(Note 6)*
- Automotive grade
- Over Current Protection (OCP)
- Thermal Shutdown Protection (TSD)
- Under Voltage Lock Out (UVLO)

(Note 5) QuiCur™ is a combination of technologies that provides high-speed load response.
(Note 6) Grade 1

Applications

- Automotive (Power Train, Body ECU)
- Car Infotainment system, etc.

Packages

	W (Typ) x D (Typ) x H (Max)
■SSOP5	2.90 mm x 2.80 mm x 1.25 mm
■HTSOP-J8	4.9 mm x 6.0 mm x 1.0 mm

SSOP5

HTSOP-J8

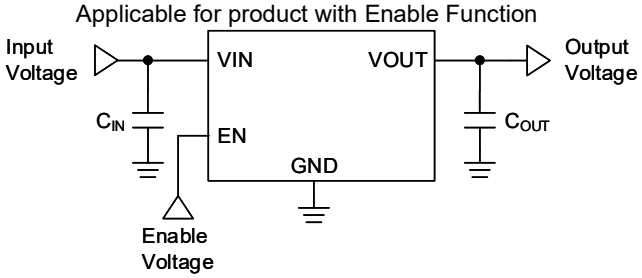
Typical Application Circuits1 (Output voltage fixed type)

Components Externally Connected

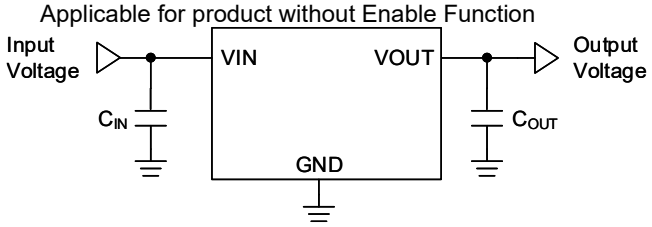
Capacitor: 0.047 μF ≤ C_{IN} (Min), 0.05 μF ≤ C_{OUT} (Min) *(Note 1)*

(Note 1) Electrolytic capacitor, tantalum capacitor and ceramic capacitors can be used.
In case of using electrolytic capacitor or ceramic capacitor with large ESR (> 500 mΩ), note that ceramic capacitor with 0.05 μF and more must be connected near VOUT pin in parallel.

Applicable for product with Enable Function



Applicable for product without Enable Function



Typical Application Circuits2 (Output voltage adjustable type)

Components Externally Connected

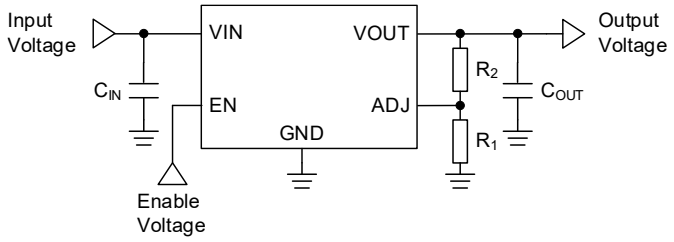
Capacitor: 0.047 μF ≤ C_{IN} (Min), 0.05 μF ≤ C_{OUT} (Min) *(Note 2)*
Resistor: 5 kΩ ≤ R_1 ≤ 200 kΩ *(Note 3)*
V_{ADJ} (Typ): 0.65 V

$$R_2 = R_1\left(\frac{V_{OUT}}{V_{ADJ}} - 1\right)$$

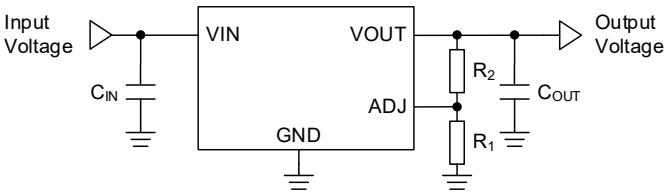
(Note 2) Electrolytic capacitor, tantalum capacitor and ceramic capacitors can be used.
In case of using electrolytic capacitor or ceramic capacitor with large ESR (> 500 mΩ), note that ceramic capacitor with 0.05 μF and more must be connected near VOUT pin in parallel.

(Note 3) The value of a feedback resistor R_1 must be within this range.
R_2 value is defined by following the formula using the limitation of R_1.
Error occurs due to the resistance value used and the ADJ terminal input current.

Applicable for product with Enable Function



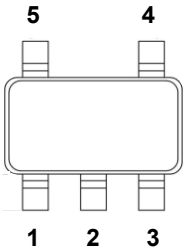
Applicable for product without Enable Function



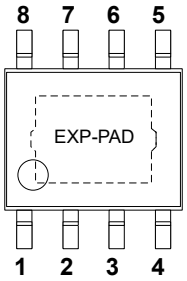
Contents

Pin Configurations

SSOP5
(TOP VIEW)



HTSOP-J8
(TOP VIEW)



Pin Descriptions

(SSOP5) BD9xxN1G-C, BD9xxN1WG-C (xx = 33, 50, 00)

Pin No.	Pin Name	Function	Descriptions
1	(ADJ)	(Adjustment Pin For Output Voltage)	Connect an external resistor between VOUT pin and ADJ pin and between ADJ pin and GND pin to adjust output voltage. Output voltage fixed type, this pin is not connected (N.C.) to the chip. *(Note 1)*
2	GND	Ground Pin	Ground.
3	(EN)	(Control Output ON / OFF Pin)	A logical “HIGH” (V_{EN} ≥ 2.0 V) at the EN pin enables the device and “LOW” (V_{EN} ≤ 0.8 V) at the EN pin disables the device. Although the output is turned off when the EN pin is open, it is recommended to connect it to GND with low impedance to prevent incorrect operation. Without enable function, this pin is not connected (N.C.) to the chip. *(Note 1)*
4	VIN	Input Supply Voltage Pin	Set a capacitor with a capacitance of 0.047 µF (Min) or higher between the VIN pin and GND. The selecting method is described in **Selection of External Components.** If the inductance of power supply line is high, please adjust input capacitor value.
5	VOUT	Output Voltage Pin	Set a capacitor with a capacitance of 0.05 µF (Min) or higher between the VOUT pin and GND. The selecting method is described in **Selection of External Components**.

(Note 1) N.C. pin can be either left floated or for connect to GND.

Pin Descriptions – continued

(HTSOP-J8) BD9xxN1EFJ-C, BD9xxN1WEFJ-C (xx = 33, 50, 00)

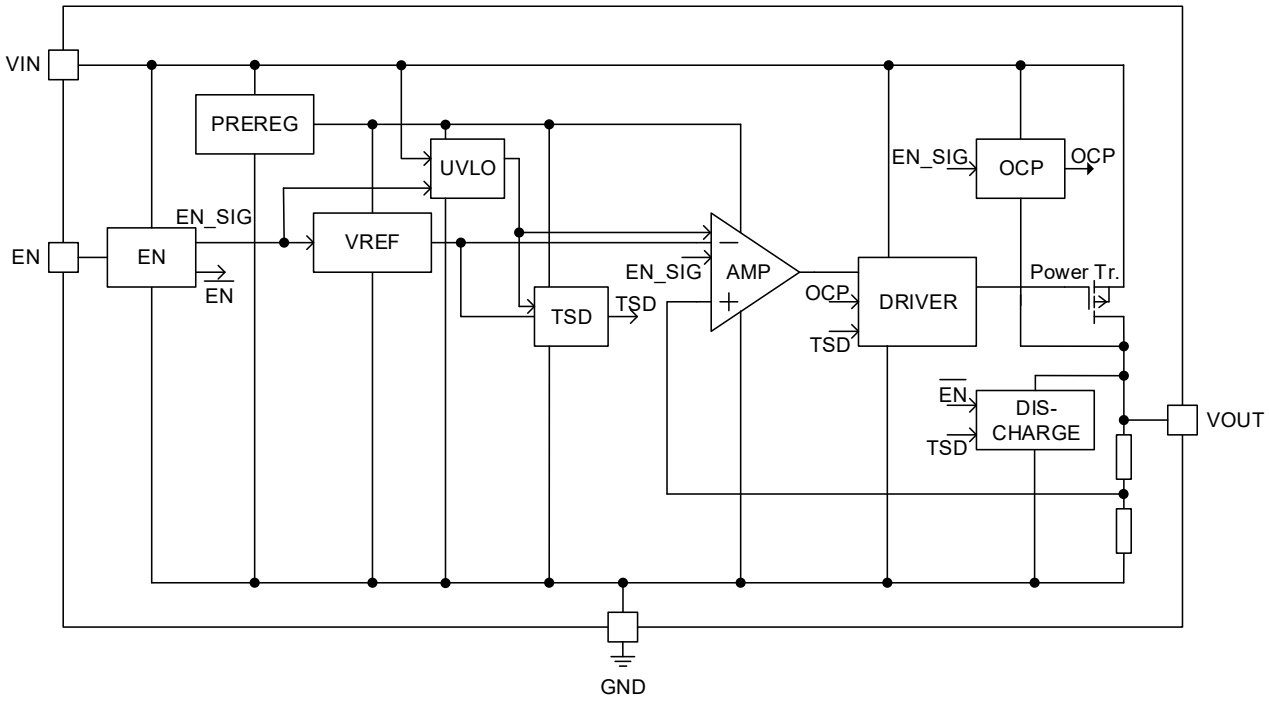
Pin No.	Pin Name	Function	Descriptions
1	VOUT	Output Voltage Pin	Set a capacitor with a capacitance of 0.05 µF (Min) or higher between the VOUT pin and GND. The selecting method is described in **Selection of External Components**.
2	(ADJ)	(Adjustment Pin For Output Voltage)	Connect an external resistor between VOUT pin and ADJ pin and between ADJ pin and GND pin to adjust output voltage. Output voltage fixed type, this pin is not connected (N.C.) to the chip. *(Note 1)*
3	N.C.	-	This pin is not connected (N.C.) to the chip. *(Note 1)*
4	N.C.	-	This pin is not connected (N.C.) to the chip. *(Note 1)*
5	GND	Ground Pin	Ground.
6	N.C.	-	This pin is not connected (N.C.) to the chip. *(Note 1)*
7	(EN)	(Control Output ON / OFF Pin)	A logical “HIGH” (V_{EN} ≥ 2.0 V) at the EN pin enables the device and “LOW” (V_{EN} ≤ 0.8 V) at the EN pin disables the device. Although the output is turned off when the EN pin is open, it is recommended to connect it to GND with low impedance to prevent incorrect operation. Without enable function, this pin is not connected (N.C.) to the chip. *(Note 1)*
8	VIN	Input Supply Voltage Pin	Set a capacitor with a capacitance of 0.047 µF (Min) or higher between the VIN pin and GND. The selecting method is described in **Selection of External Components.** If the inductance of power supply line is high, please adjust input capacitor value.
-	EXP-PAD	Heat Dissipation	It is recommended to connect EXP-PAD on the back side to external Ground pattern in order to make heat dissipation better.

(Note 1) N.C. pin can be either left floated or for connect to GND.

Block Diagram

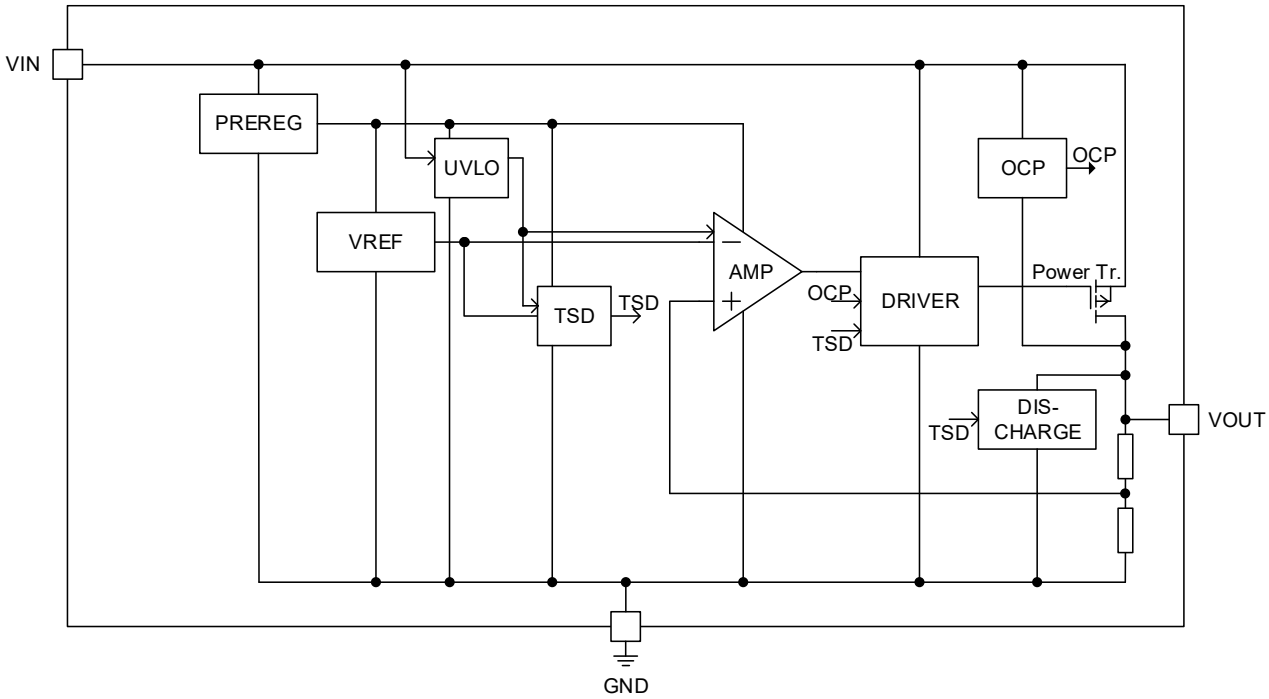
Applicable for product output voltage fixed type with Enable Function

・BD9xxN1WG-C, BD9xxN1WEFJ-C (xx = 33, 50)



Applicable for product output voltage fixed type without Enable Function

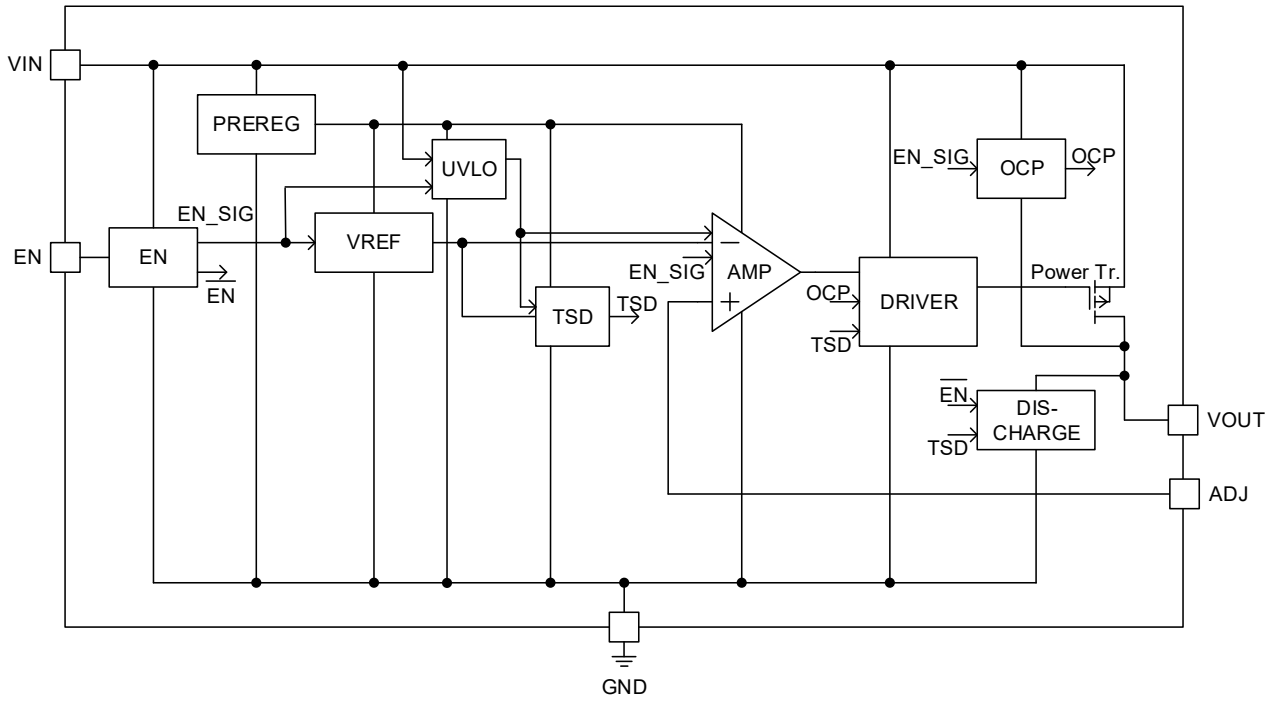
・BD9xxN1G-C, BD9xxN1EFJ-C (xx = 33, 50)



Block Diagram – continued

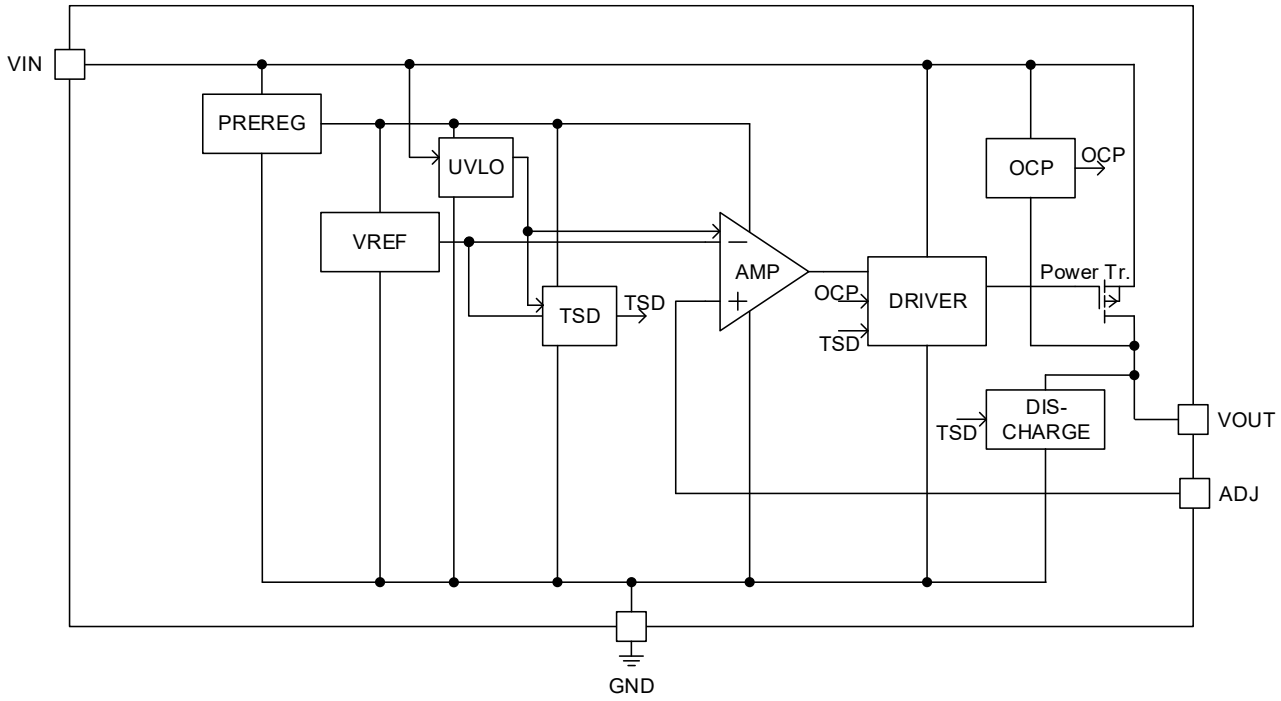
Applicable for product output voltage adjustable type with Enable Function

・BD900N1WG-C, BD900N1WEFJ-C



Applicable for product output voltage adjustable type without Enable Function

・BD900N1G-C, BD900N1EFJ-C



Description of Blocks

BD9xxN1WG-C, BD9xxN1WEFJ-C (xx = 33, 50, 00)

Block Name	Function	Description of Blocks
EN	Enable Input	A logical “HIGH” (V_{EN} ≥ 2.0 V) at the EN pin enables the device and “LOW” (V_{EN} ≤ 0.8 V) at the EN pin disables the device.
PREREG	Internal Power Supply	Power supply for internal circuit.
TSD	Thermal Shutdown Protection	In case maximum power dissipation exceeds or when the junction temperature rises and the chip temperature (Tj) exceeds the heating protection set temperature. The TSD protection circuit detects this and forces the gate of output MOSFET to turn off in order to protect the device from overheating. (Typ: 175 °C) When the junction temperature decreases to low, the thermal Shutdown protection is released and the output turns on automatically.
VREF	Reference Voltage	Generate the reference voltage.
AMP	Error Amplifier	The fixed output voltage product compares the voltage obtained by dividing the output voltage with the reference voltage, and the variable output voltage product compares the ADJ voltage with the reference voltage, and controls the output power transistor via the DRIVER.
DRIVER	Output MOSFET Driver	Drive the output MOSFET.
OCP	Over Current Protection	If the output current increases higher than the maximum output current, it is limited by Over Current Protection in order to protect the device from a damage caused by an over current. (Typ: 280 mA) While this block is operating, the output voltage may decrease because the output current is limited. If an abnormal state is removed and the output current value returns to normal, the output voltage also returns to normal state.
DISCHARGE	Output Discharge Function	Output pin is discharged by the internal resistance when EN = LOW input or TSD is detected.
UVLO	Under Voltage Lock Out	The Under Voltage Lock Out protection detects when V_{IN} voltage becomes less than 2.4 V (Typ), it forces AMP to turn off in order to avoid any false operation at low input voltage.

BD9xxN1G-C, BD9xxN1EFJ-C (xx = 33, 50, 00)

Block Name	Function	Description of Blocks
PREREG	Internal Power Supply	Power supply for internal circuit.
TSD	Thermal Shutdown Protection	In case maximum power dissipation exceeds or when the junction temperature rises and the chip temperature (Tj) exceeds the heating protection set temperature. The TSD protection circuit detects this and forces the gate of output MOSFET to turn off in order to protect the device from overheating. (Typ: 175 °C) When the junction temperature decreases to low, the thermal Shutdown protection is released and the output turns on automatically.
VREF	Reference Voltage	Generate the reference voltage.
AMP	Error Amplifier	The fixed output voltage product compares the voltage obtained by dividing the output voltage with the reference voltage, and the variable output voltage product compares the ADJ voltage with the reference voltage, and controls the output power transistor via the DRIVER.
DRIVER	Output MOSFET Driver	Drive the output MOSFET.
OCP	Over Current Protection	If the output current increases higher than the maximum output current, it is limited by Over Current Protection in order to protect the device from a damage caused by an over current. (Typ: 280 mA) While this block is operating, the output voltage may decrease because the output current is limited. If an abnormal state is removed and the output current value returns to normal, the output voltage also returns to normal state.
DISCHARGE	Output Discharge Function	Output pin is discharged by the internal resistance when TSD is detected.
UVLO	Under Voltage Lock Out	The Under Voltage Lock Out protection detects when V_{IN} voltage becomes less than 2.4 V (Typ), it forces AMP to turn off in order to avoid any false operation at low input voltage.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage *(Note 1)*	V_{IN}	-0.3 to +45	V
EN Pin Voltage *(Note 2)*	V_{EN}	-0.3 to +45	V
VOUT Pin Voltage	V_{OUT}	-0.3 to +20 (≤ V_{IN} + 0.3)	V
ADJ Pin Voltage *(Note 3)*	V_{ADJ}	-0.3 to +7	V
Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C
ESD Withstand Voltage (HBM) *(Note 4)*	V_{ESD_HBM}	±2000	V
ESD Withstand Voltage (CDM) *(Note 5)*	V_{ESD_CDM}	±750	V

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance and power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Do not exceed Tjmax.

(Note 2) Applicable for product with BD9xxN1WG-C, BD9xxN1WEFJ-C (xx = 33, 50, 00)
The start-up orders of power supply (V_{IN}) and the V_{EN} do not influence if the voltage is within the operation power supply voltage range.

(Note 3) Applicable for product with BD900N1G-C, BD900N1WG-C, BD900N1EFJ-C, BD900N1WEFJ-C.

(Note 4) ESD susceptibility Human Body Model “HBM”; base on ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).

(Note 5) ESD susceptibility Charged Device Model “CDM”; base on AEC-Q100-011.

Thermal Resistances

Parameter	Symbol	Thermal Resistance (Typ)(Note 1)		Unit
		1s (Note 3)	2s2p (Note 4)	
SSOP5				
Junction to Ambient	θ_{JA}	271.3	146.7	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	46	37	°C/W
HTSOP-J8				
Junction to Ambient	θ_{JA}	157.2	36.2	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	32	11	°C/W

(Note 1) Based on JESD51-2A (Still-Air), using a BD950N1G-C, BD950N1EFJ-C Chip.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of 1,2,4 layers. Placement follows the land pattern.

Operating Conditions(-40 °C ≤ Tj ≤ +150 °C)

Parameter	Symbol	Min	Max	Unit
Input Voltage *(Note 1) (Note 2)*	V_{IN}	4.5	42.0	V
		V_{OUT} (Max) + ΔV_D (Max)	42.0	V
Start-Up Voltage	$V_{IN\ Start\text{-}Up}$	3.0	-	V
Output Voltage *(Note 3)*	V_{OUT}	1.0	18.0	V
Feedback Resistor ADJ vs GND *(Note 3)*	R_1	5	200	kΩ
Enable Input Voltage *(Note 4)*	V_{EN}	0	42	V
Output Current	I_{OUT}	0	150	mA
Input Capacitor *(Note 5) (Note 6)*	C_{IN}	0.047	-	µF
Output Capacitor *(Note 6)*	C_{OUT}	0.05	470	µF
Output Capacitor Equivalent Series Resistance *(Note 7)*	ESR (C_{OUT})	-	500	mΩ
Operating Temperature Ratings	Ta	-40	+125	°C

(Note 1) Please consider that the output voltage would be dropped (Dropout voltage ΔVd) by the output current.
(Note 2) Apply 4.5V or VOUT (Max) + ΔVd (Max), whichever is higher.
(Note 3) Applicable for product with BD900N1G-C, BD900N1WG-C, BD900N1EFJ-C, BD900N1WEFJ-C.
(Note 4) Applicable for product with BD9xxN1WG-C, BD9xxN1WEFJ-C (xx = 33, 50, 00)
(Note 5) If the inductance of power supply line is high, please adjust input capacitor value in order to lower the input impedance.
A lower input impedance can bring out the ideal characteristic of IC as much as possible.
It also has the effect of preventing the voltage-drop at the input line.
(Note 6) Set capacitor value which do not fall below the minimum value. This value needs to consider the temperature characteristics and DC device characteristics. For applications where the output voltage is 1.5 V or less, it is recommended to use an output capacitor of 0.22 µF or more because the output capacitor holds less charge, increasing the amount of voltage fluctuation during transient response.
(Note 7) It is recommended to use ceramic capacitors that have low ESR characteristics for output phase compensation.
In case of using electrolytic capacitor or ceramic capacitor with large ESR (>500 mΩ), note that ceramic capacitor with 0.05µF and more must be connected near VOUT pin in parallel.

Electrical Characteristics

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 0.1 µF
V_{OUT} setting = 5 V, R_1 = 10 kΩ, R_2 = 67 kΩ
Typical values are defined at Tj = 25 °C, V_{IN} = 13.5 V

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Current Consumption *(Note 1)*	I_{CC}	-	28	48	µA	I_{OUT} = 0 mA, Tj ≤ 125 °C
		-	28	60	µA	I_{OUT} = 0 mA, Tj ≤ 150 °C
Output Voltage *(Note 2)*	V_{OUT}	4.900	5.000	5.100	V	6.0 V ≤ V_{IN} ≤ 42 V, Tj = -40 °C to +150 °C 0 mA ≤ I_{OUT} ≤ 100 mA, or 6.5 V ≤ V_{IN} ≤ 42 V, Tj = -40 °C to +150 °C 0 mA ≤ I_{OUT} ≤ 150 mA
Output Voltage *(Note 3)*	V_{OUT}	3.234	3.300	3.366	V	4.5 V ≤ V_{IN} ≤ 42 V, Tj = -40 °C to +150 °C 0 mA ≤ I_{OUT} ≤ 100 mA, or 4.9 V ≤ V_{IN} ≤ 42 V, Tj = -40 °C to +150 °C 0 mA ≤ I_{OUT} ≤ 150 mA
Reference Voltage *(Note 4)*	V_{ADJ}	0.637	0.650	0.663	V	4.5 V ≤ V_{IN} ≤ 42 V, Tj = -40 °C to +150 °C, 0 mA ≤ I_{OUT} ≤ 150 mA
Dropout Voltage	ΔV_{D1}	-	420	1000	mV	V_{IN} = 4.75 V (V_{OUT} ≥ 5 V) I_{OUT} = 100 mA
	ΔV_{D2}	-	500	1200	mV	V_{IN} = 3.135 V (V_{OUT} ≥ 3.3 V) I_{OUT} = 100 mA
	ΔV_{D3}	-	650	1500	mV	V_{IN} = 4.75 V (V_{OUT} ≥ 5 V) I_{OUT} = 150 mA
	ΔV_{D4}	-	780	1800	mV	V_{IN} = 3.135 V (V_{OUT} ≥ 3.3 V) I_{OUT} = 150 mA
Ripple Rejection *(Note 5)*	R.R.	-	70	-	dB	f = 1kHz, V_{Ripple} = 1 Vrms I_{OUT} = 10 mA
Line Regulation	Reg.I1	-	0.05	0.20	%	V_{OUT} + 1.5V ≤ V_{IN} ≤ 42 V (V_{OUT} ≥ 3.0 V)
	Reg.I2	-	2	6	mV	4.5 V ≤ V_{IN} ≤ 42 V (V_{OUT} < 3.0 V)
Load Regulation	Reg.L1	-	0.1	0.3	%	0 mA ≤ I_{OUT} ≤ 150 mA (V_{OUT} ≥ 3.0 V)
	Reg.L2	-	3	9	mV	0 mA ≤ I_{OUT} ≤ 150 mA (V_{OUT} < 3.0 V)
ADJ Input Current *(Note 4)(Note 5)*	I_{ADJ}	-	0	15	nA	V_{ADJ} = 1 V

(Note 1) Adjustable output voltage type does not contain the current of R_1 and R_2.
(Note 2) BD950N1G-C, BD950N1WG-C, BD950N1EFJ-C, BD950N1WEFJ-C.
(Note 3) BD933N1G-C, BD933N1WG-C, BD933N1EFJ-C, BD933N1WEFJ-C.
(Note 4) BD900N1G-C, BD900N1WG-C, BD900N1EFJ-C, BD900N1WEFJ-C.
(Note 5) Not all devices are measured for shipment.

Electrical Characteristics – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 0.1 µF
V_{OUT} setting = 5 V, R_1 = 10 kΩ, R_2 = 67 kΩ
Typical values are defined at Tj = 25 °C, V_{IN} = 13.5 V

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
UVLO fall threshold	V_{UVLOF}	1.8	2.4	2.8	V	V_{IN} falling
UVLO rise threshold	V_{UVLOR}	2.0	2.6	3.0	V	V_{IN} rising
UVLO hysteresis	$V_{UVLOHYS}$	-	0.2	-	V	
Over Current Protection	I_{OCP}	151	280	400	mA	V_{OUT} = 0 V
Thermal Shutdown Temperature	T_{TSD}	151	175	-	°C	-
Thermal Shutdown Hysteresis	T_{TSDHYS}	-	15	-	°C	-

Electrical Characteristics (Applicable for product with Enable Function) ***(Note6)***

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 0.1 µF, V_{EN} = 5 V
V_{OUT} setting = 5 V, R_1 = 10 kΩ, R_2 = 67 kΩ
Typical values are defined at Tj = 25 °C, V_{IN} = 13.5 V

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Shutdown Current	I_{SHUT}	-	1.0	4.8	µA	V_{EN} = 0 V Tj ≤ 125 °C
Enable ON threshold Voltage	V_{ENTH}	1.05	1.45	2.00	V	V_{EN} rising
Enable OFF threshold Voltage	V_{ENTL}	0.80	1.27	1.70	V	V_{EN} falling
Enable Hysteresis Voltage	V_{ENHYS}	-	0.18	-	V	-
Enable Bias Current	I_{EN}	-	4	8	µA	V_{EN} = 5 V
VOUT Discharge Resistance	R_{DSC}	2.6	6.5	11.0	kΩ	V_{EN} = 0 V

(Note 6) BD9xxN1WG-C, BD9xxN1WEFJ-C (xx = 33, 50, 00).

Typical Performance Curves 5 V Output

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

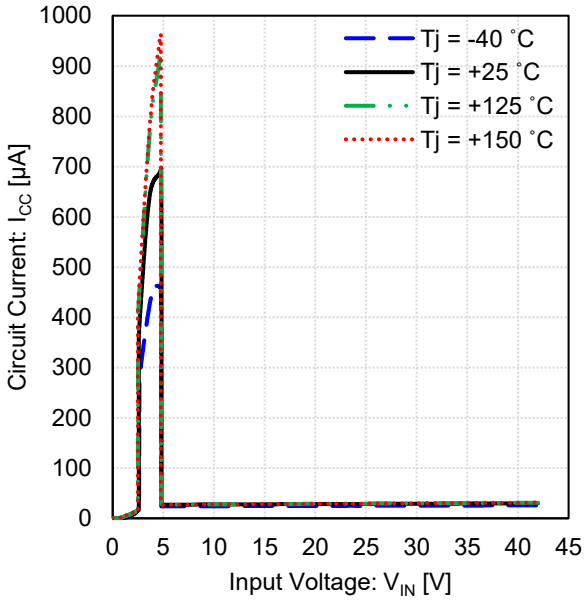


Figure 1. Circuit Current vs Input Voltage
(5 V output)

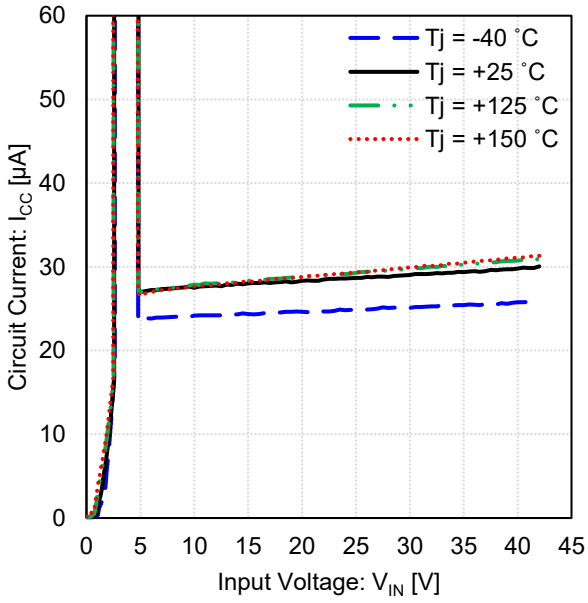


Figure 2. Circuit Current vs Input Voltage
*magnification of Figure 1 at narrow range circuit current
(5 V output)

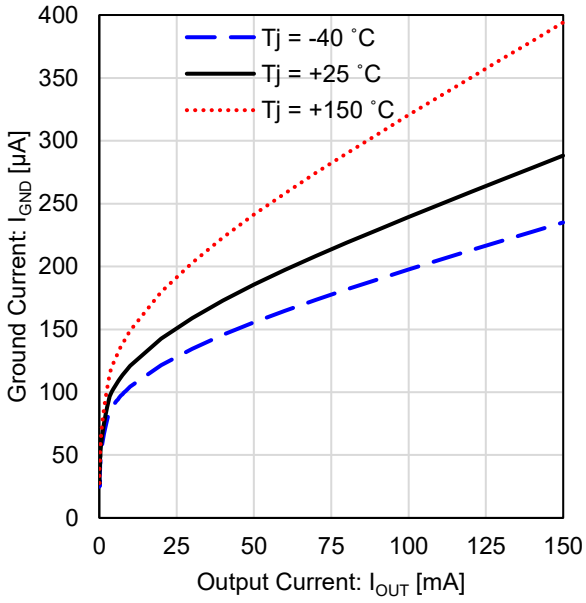


Figure 3. Ground Current vs Output Current
(5 V output)

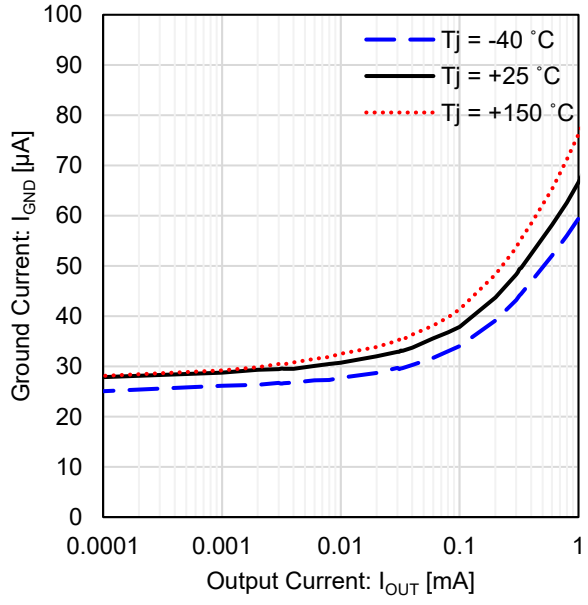


Figure 4. Ground Current vs Output Current
*magnification of Figure 3 at low output current
(5 V output)

Typical Performance Curves 5 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

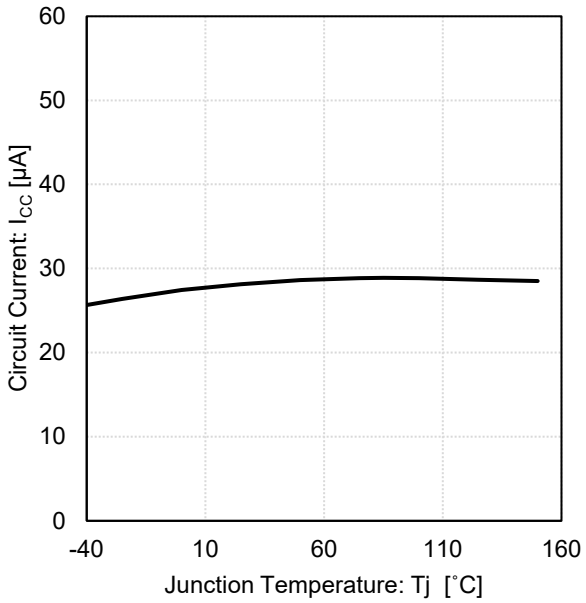


Figure 5. Circuit Current vs Junction Temperature
(5 V output)

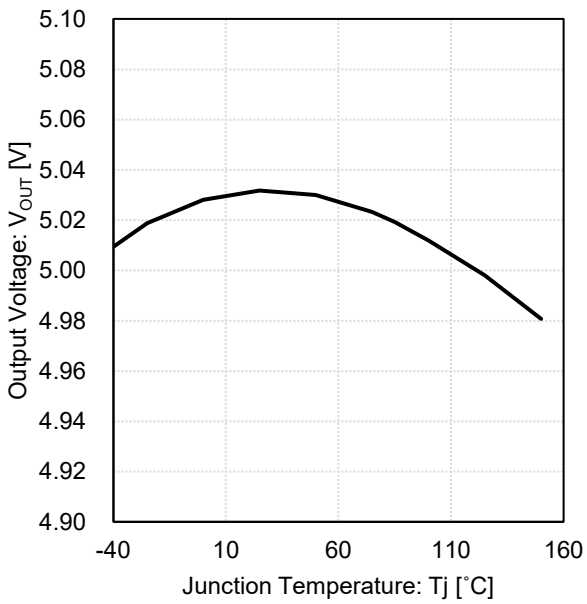


Figure 6. Output Voltage vs Junction Temperature
(5 V output)

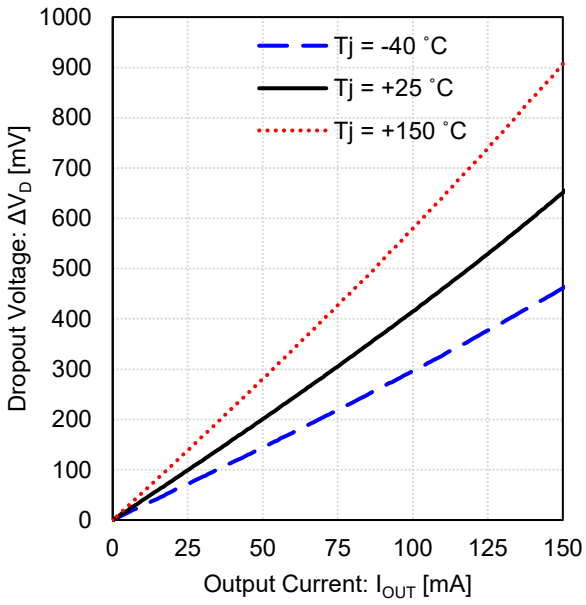


Figure 7. Dropout Voltage vs Output Current
(5 V output, V_{IN} = 4.75 V)

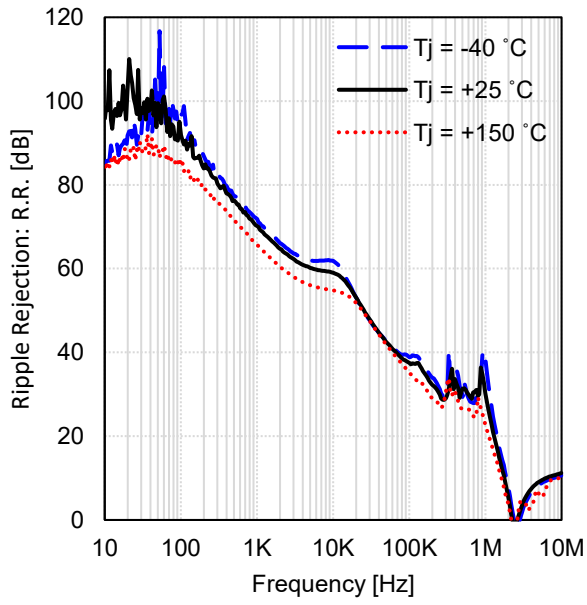


Figure 8. Ripple Rejection vs Frequency
(5 V output, V_{Ripple} = 1 Vrms, I_{OUT} = 10 mA)

Typical Performance Curves 5 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

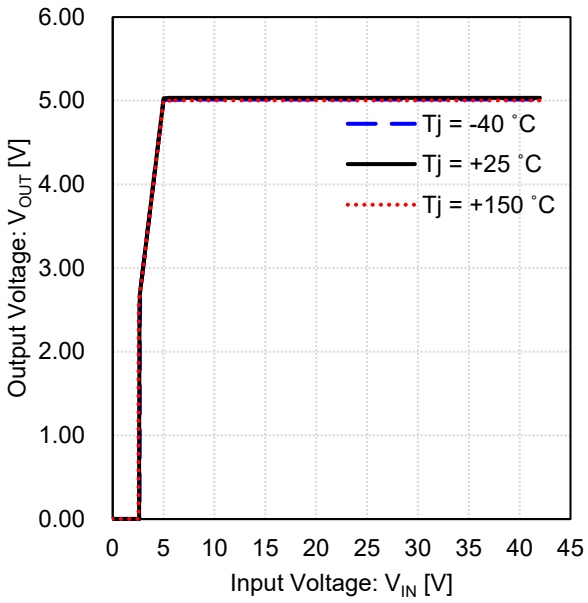


Figure 9. Output Voltage vs Input Voltage
(5 V output)

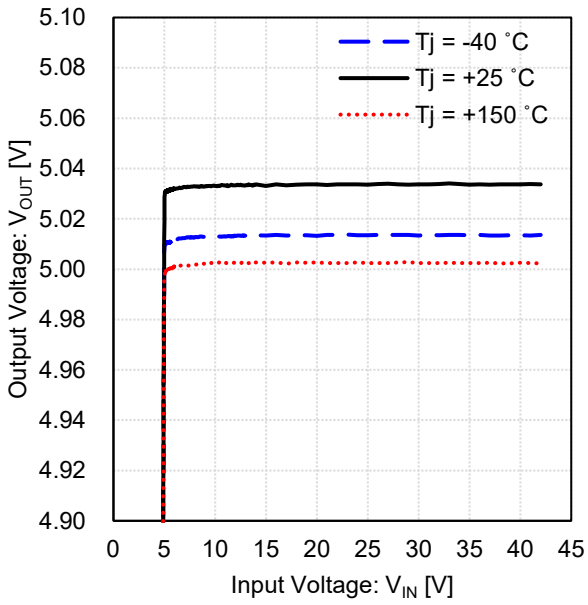


Figure 10. Output Voltage vs Input Voltage
*magnification of Figure 9 at narrow range output voltage
(5 V output)

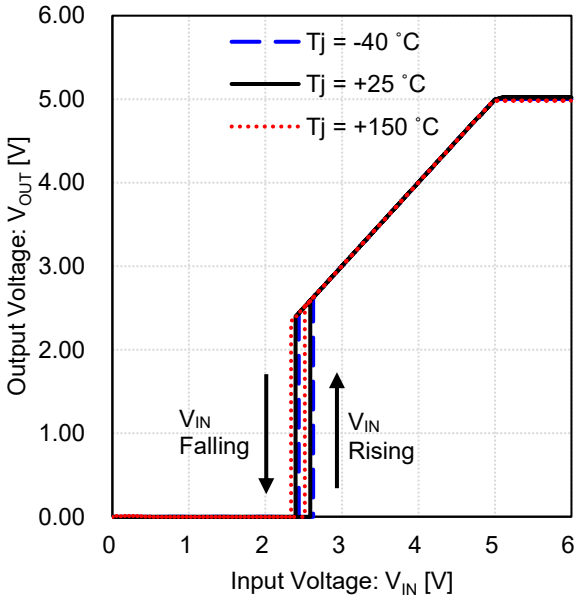


Figure 11. Output Voltage vs Input Voltage
*magnification of Figure 9 at low input voltage
(5 V output)

Typical Performance Curves 5 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

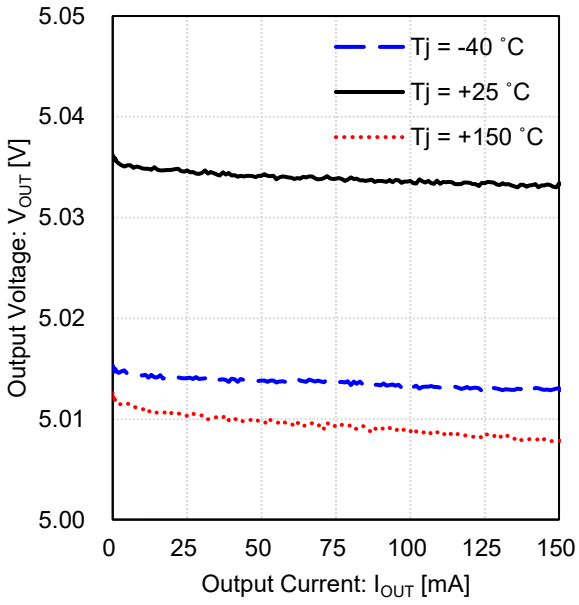


Figure 12. Output Voltage vs Output Current
(5 V output, Load Regulation)

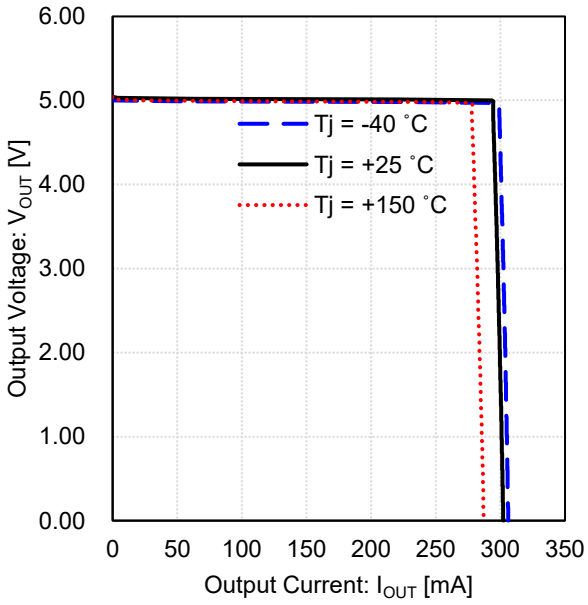


Figure 13. Output Voltage vs Output Current
(5 V output, Over Current Protection)

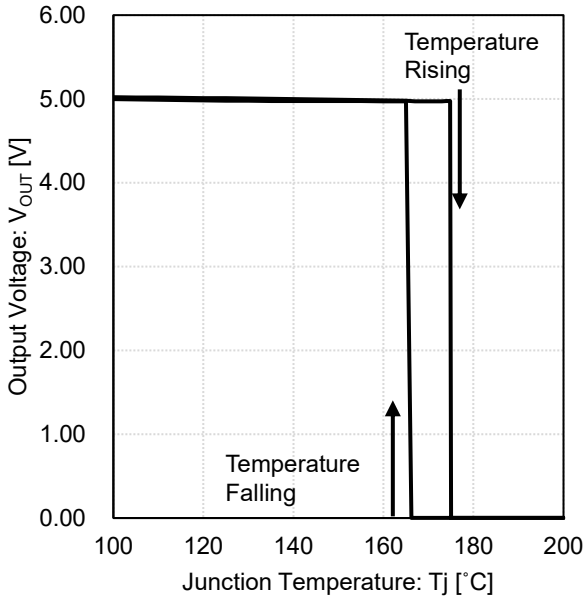


Figure 14. Output Voltage vs Junction Temperature
(5 V output)

Typical Performance Curves 5 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

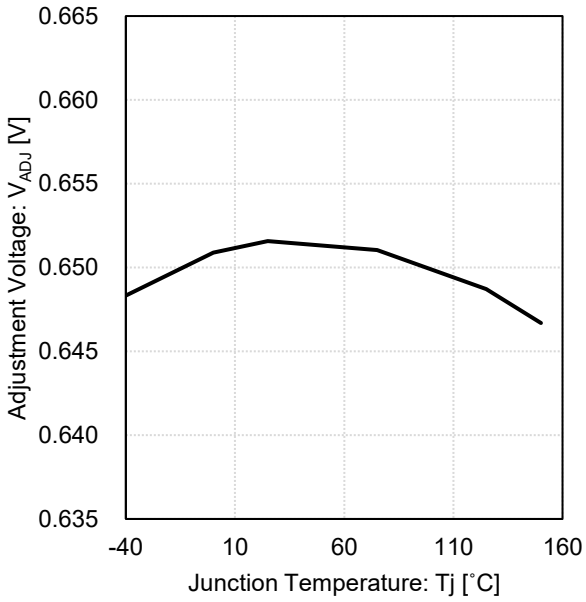


Figure 15. Adjustment Voltage vs Junction Temperature

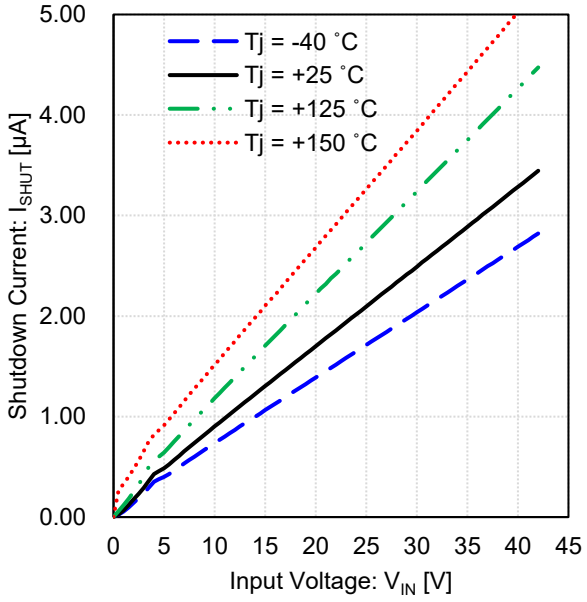


Figure 16. Shutdown Current vs Input Voltage (V_{EN} = 0 V)

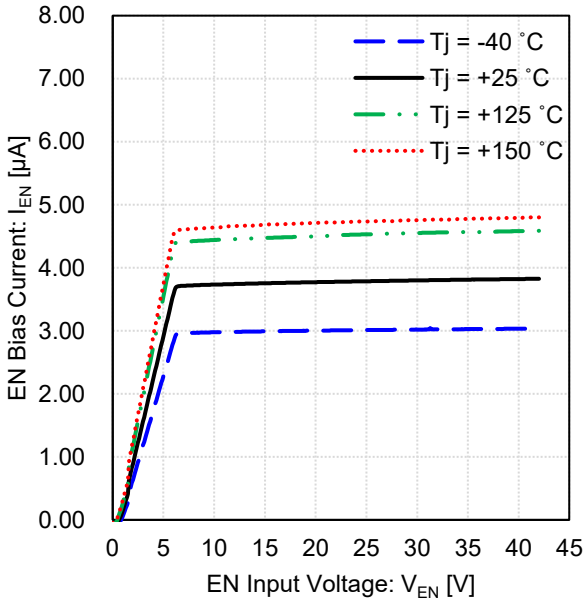


Figure 17. EN Bias Current vs EN Input Voltage

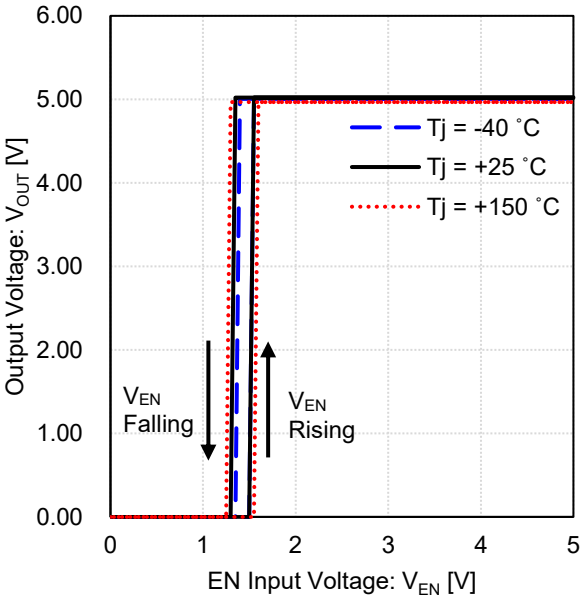


Figure 18. Output Voltage vs EN Input Voltage (5 V output)

Typical Performance Curves 5 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

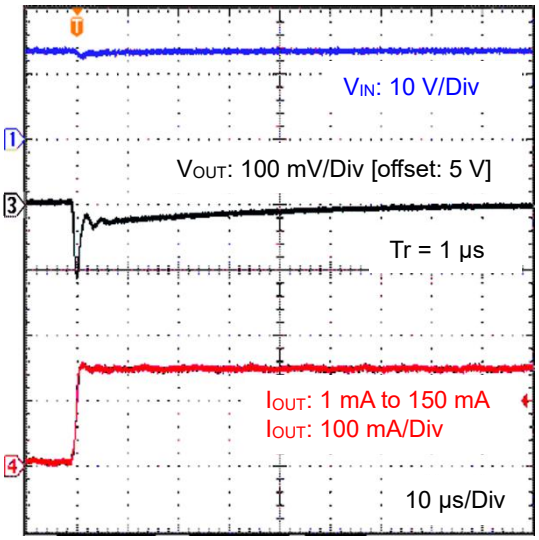


Figure 19. Load Transient 1 mA to 150 mA (5 V output, Tr = 1 µs)

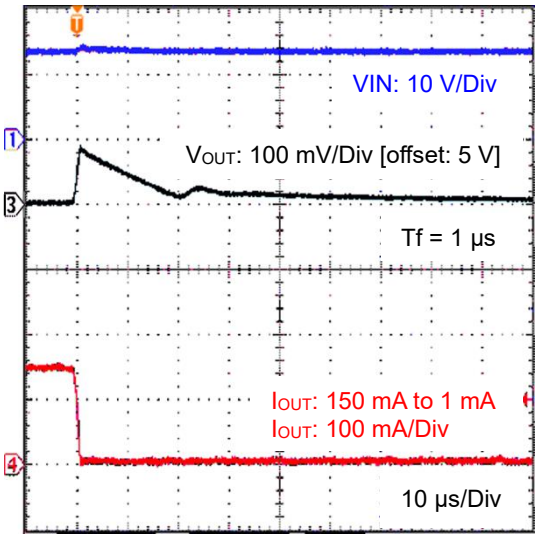


Figure 20. Load Transient 150 mA to 1 mA (5 V output, Tf = 1 µs)

Typical Performance Curves 5 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

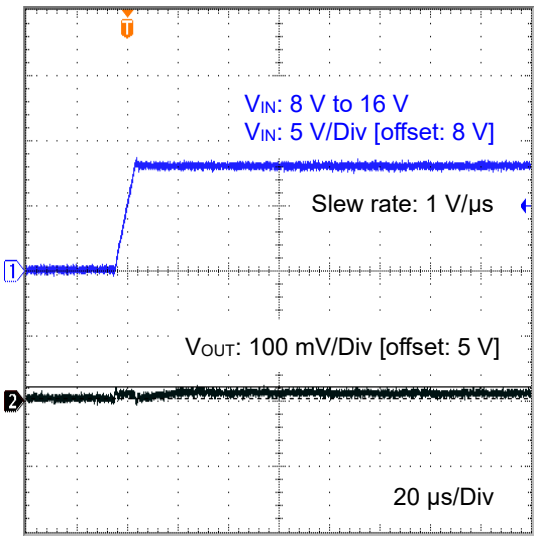


Figure 21. Line Transient 8 V to 16 V
(5 V output, I_{OUT} = 0 mA)

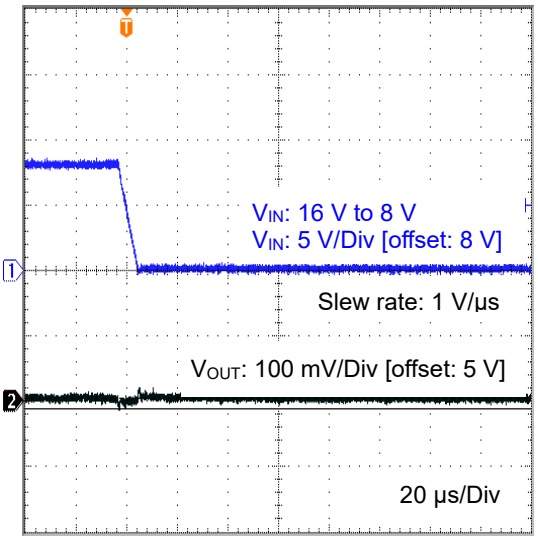


Figure 22. Line Transient 16 V to 8 V
(5 V output, I_{OUT} = 0 mA)

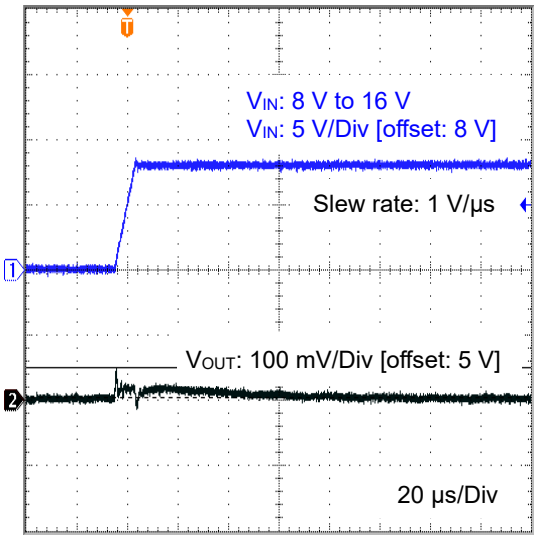


Figure 23. Line Transient 8 V to 16 V
(5 V output, I_{OUT} = 150 mA)

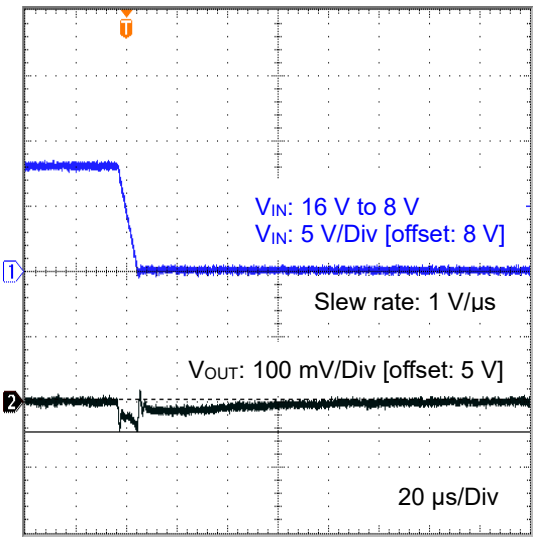


Figure 24. Line Transient 16 V to 8 V
(5 V output, I_{OUT} = 150 mA)

Typical Performance Curves 5 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

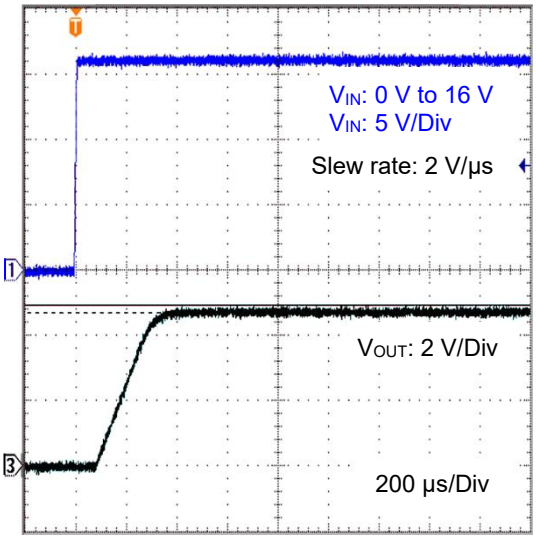


Figure 25. VIN Startup Waveform
VIN: 0 V to 16 V
(5 V output, I_{OUT} = 0 mA)

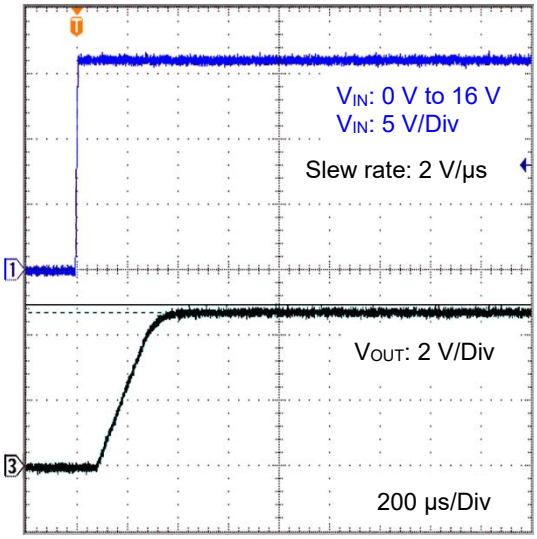


Figure 26. VIN Startup Waveform
VIN: 0 V to 16 V
(5 V output, I_{OUT} = 150 mA)

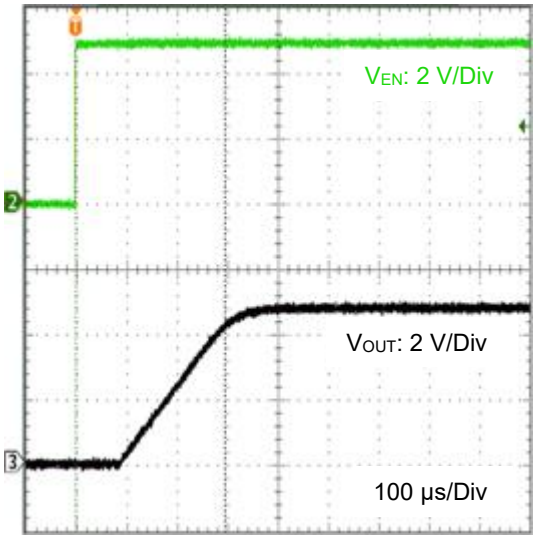


Figure 27. EN Startup Waveform
(5 V output, I_{OUT} = 1 mA)

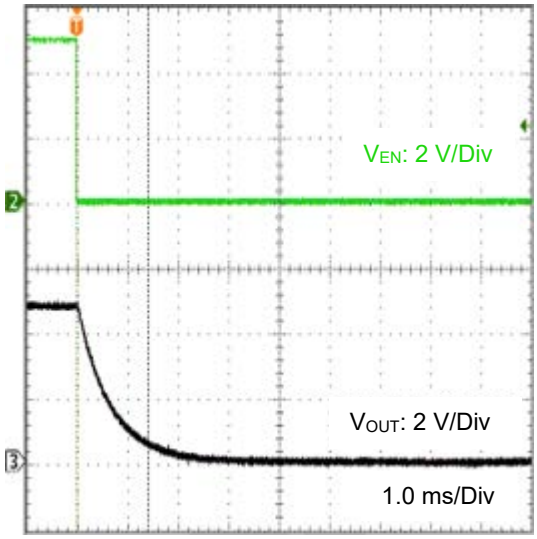


Figure 28. EN Shutdown Waveform
(5 V output, I_{OUT} = 1 mA)

Typical Performance Curves 3.3 V Output

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

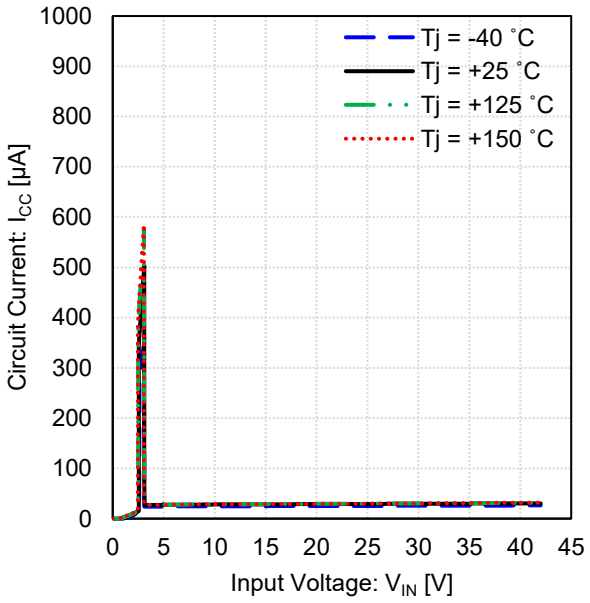


Figure 29. Circuit Current vs Input Voltage
(3.3 V output)

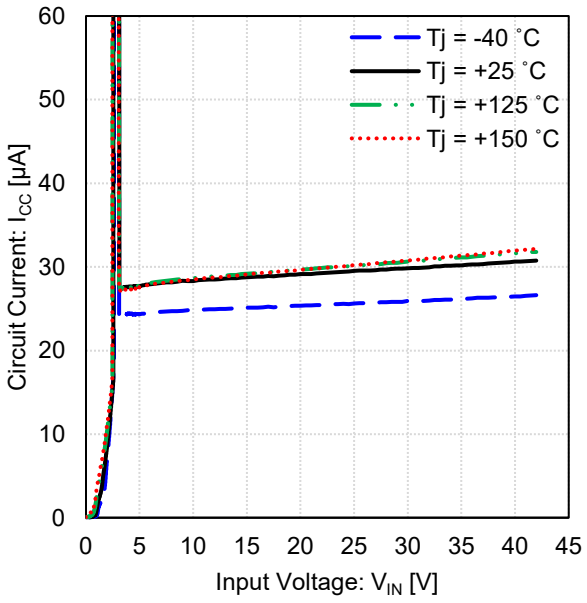


Figure 30. Circuit Current vs Input Voltage
*magnification of Figure 29 at narrow range circuit current
(3.3 V output)

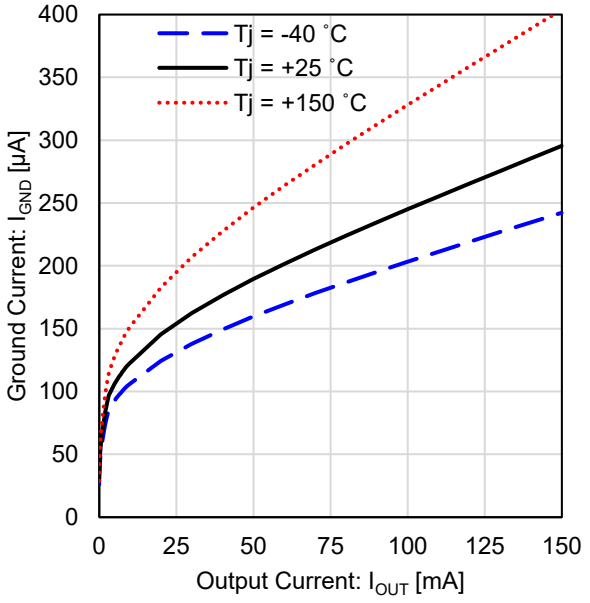


Figure 31. Ground Current vs Output Current
(3.3 V output)

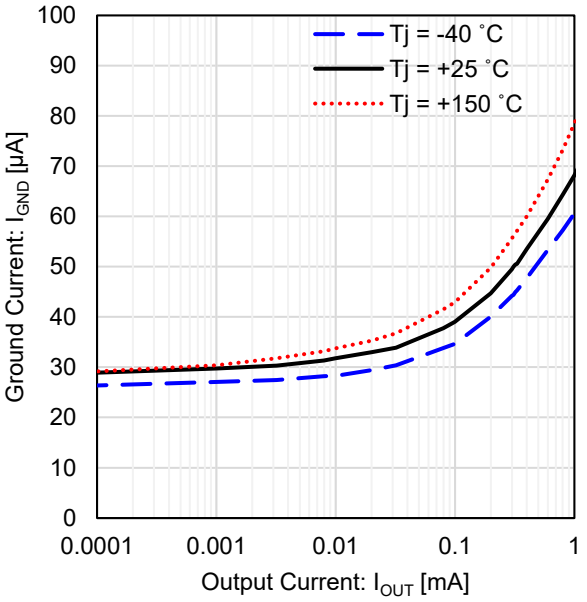


Figure 32. Ground Current vs Output Current
*magnification of Figure 31 at low output current
(3.3 V output)

Typical Performance Curves 3.3 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

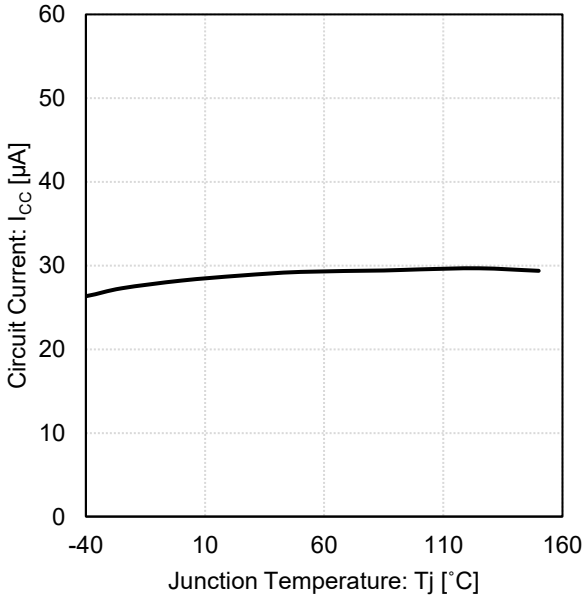


Figure 33. Circuit Current vs Junction Temperature (3.3 V output)

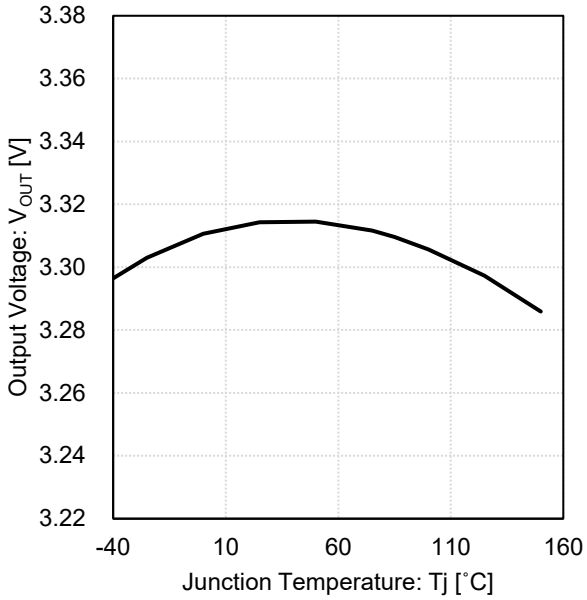


Figure 34. Output Voltage vs Junction Temperature (3.3 V output)

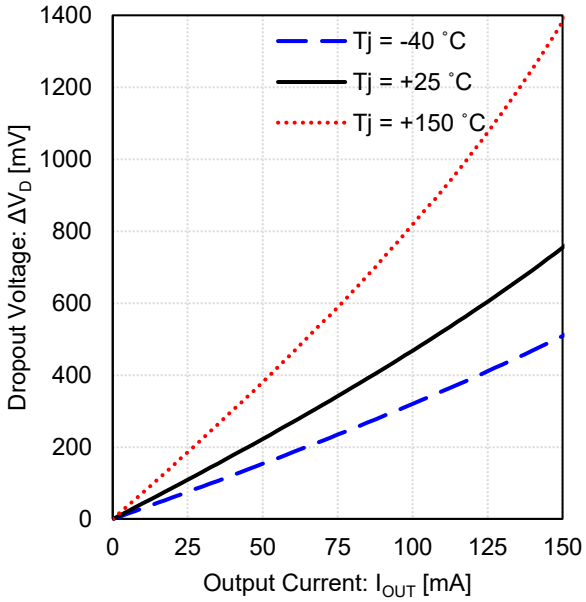


Figure 35. Dropout Voltage vs Output Current (3.3 V output, V_{IN} = 3.135 V)

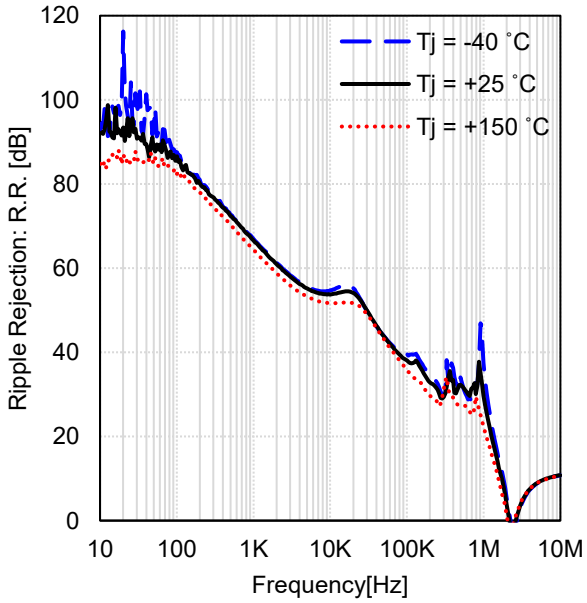


Figure 36. Ripple Rejection vs Frequency (3.3 V output, V_{Ripple} = 1 Vrms, I_{OUT} = 10 mA)

Typical Performance Curves 3.3 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

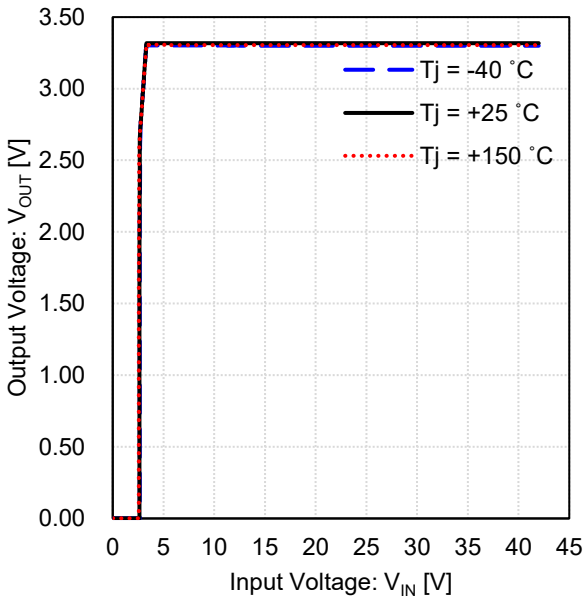


Figure 37. Output Voltage vs Input Voltage
(3.3 V output)

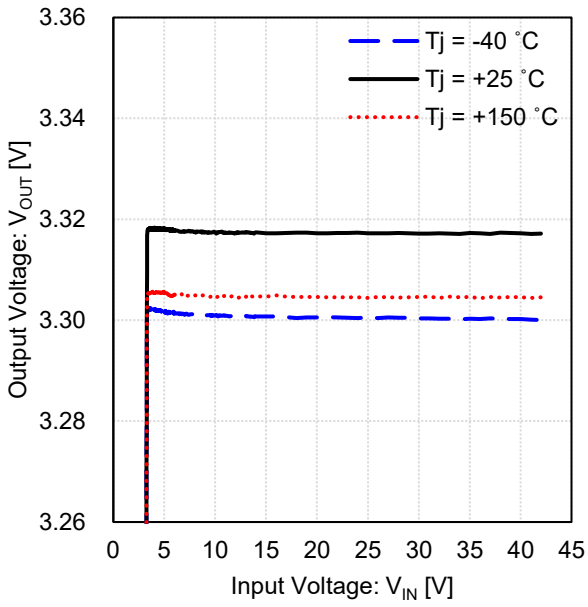


Figure 38. Output Voltage vs Input Voltage
*magnification of Figure 37 at narrow range output voltage
(3.3 V output)

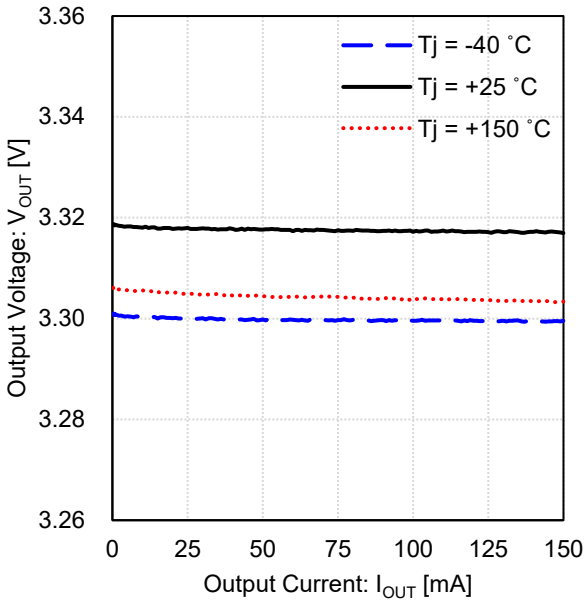


Figure 39. Output Current vs Output Voltage
(3.3 V output, Load Regulation)

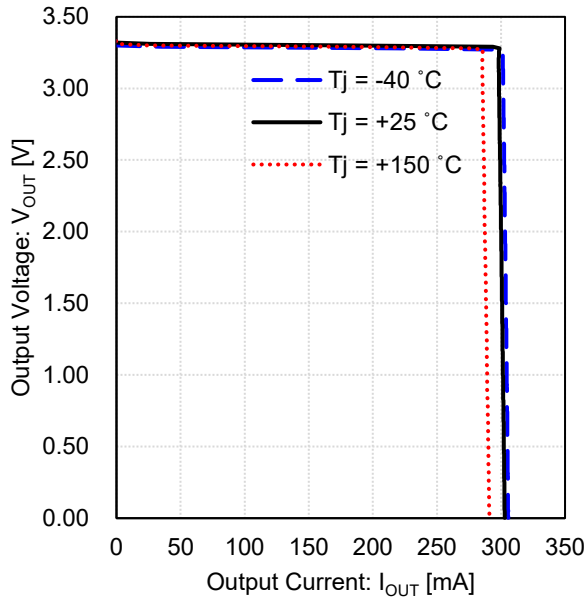


Figure 40. Output Current vs Output Voltage
(3.3 V output, Over Current Protection)

Typical Performance Curves 3.3 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

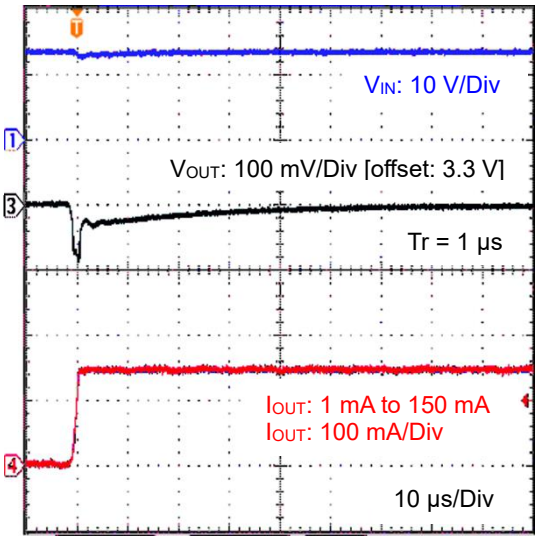


Figure 41. Load Transient 1 mA to 150 mA (3.3 V output, Tr = 1 µs)

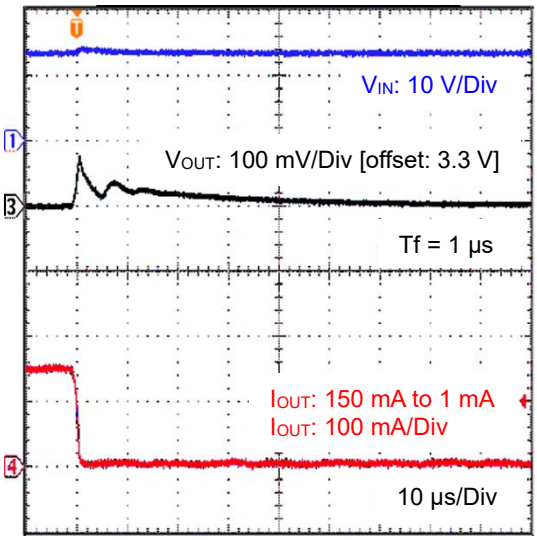


Figure 42. Load Transient 150 mA to 1 mA (3.3 V output, Tf = 1 µs)

Typical Performance Curves 3.3 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

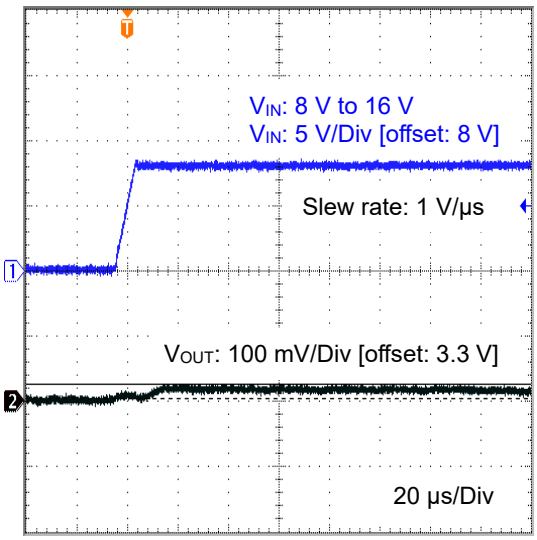


Figure 43. Line Transient 8 V to 16 V
(3.3 V output, I_{OUT} = 0 mA)

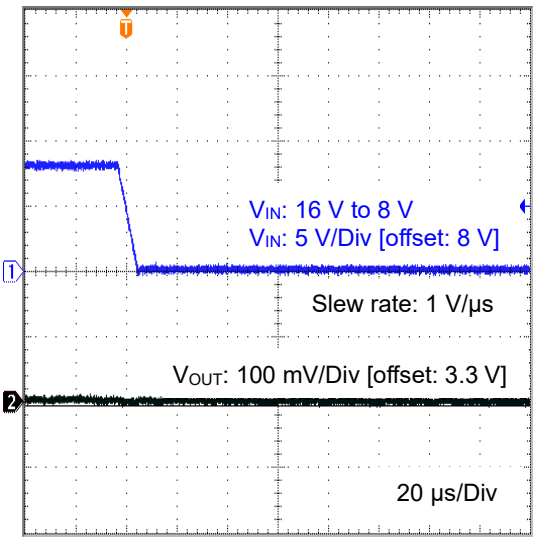


Figure 44. Line Transient 16 V to 8 V
(3.3 V output, I_{OUT} = 0 mA)

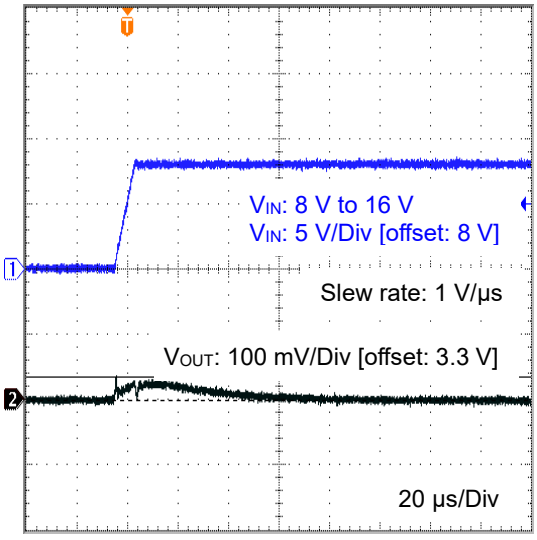


Figure 45. Line Transient 8 V to 16 V
(3.3 V output, I_{OUT} = 150 mA)

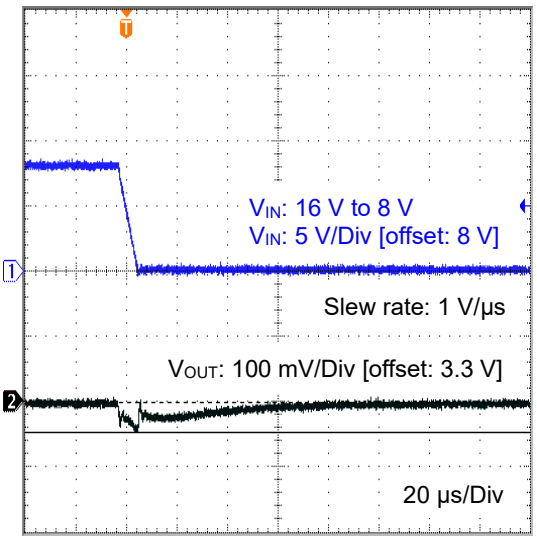


Figure 46. Line Transient 16 V to 8 V
(3.3 V output, I_{OUT} = 150 mA)

Typical Performance Curves 3.3 V Output - continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, V_{EN} = 5 V, C_{OUT} = 0.1 µF

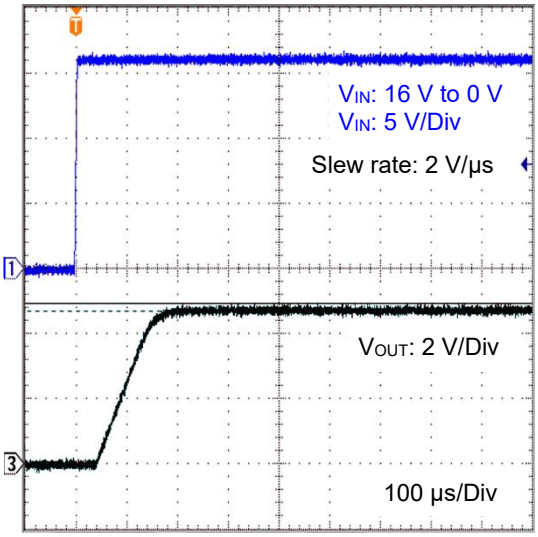


Figure 47. VIN Startup Waveform
VIN: 0 V to 16 V
(3.3 V output, I_{OUT} = 0 mA)

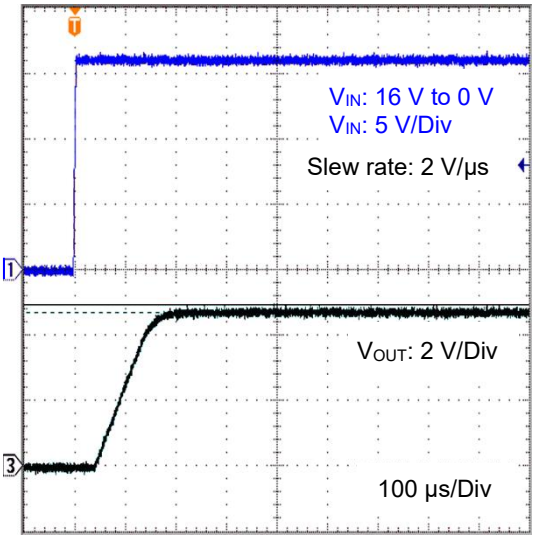


Figure 48. VIN Startup Waveform
VIN: 0 V to 16 V
(3.3 V output, I_{OUT} = 150 mA)

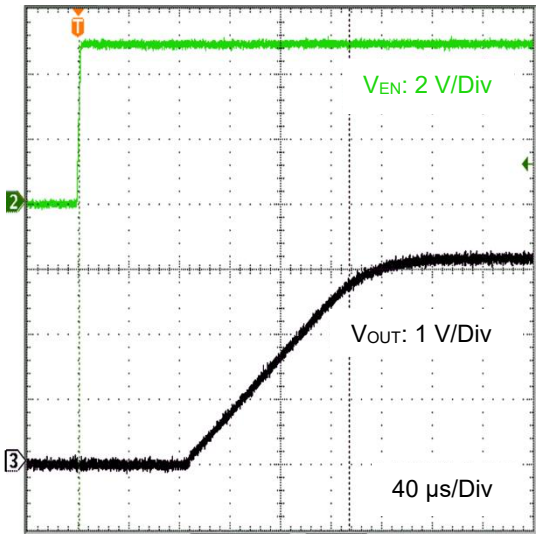


Figure 49. EN Startup Waveform
(3.3 V output, I_{OUT} = 1 mA)

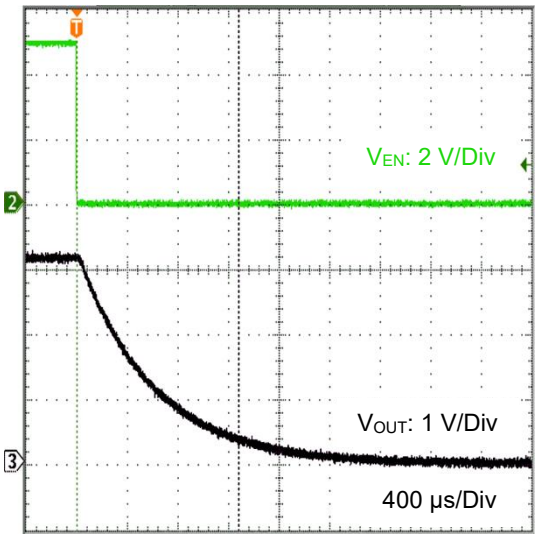
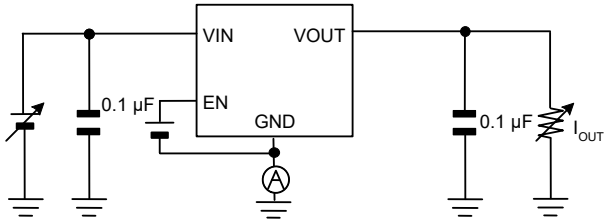
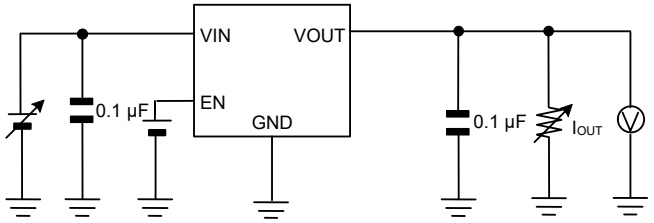


Figure 50. EN Shutdown Waveform
(3.3 V output, I_{OUT} = 1 mA)

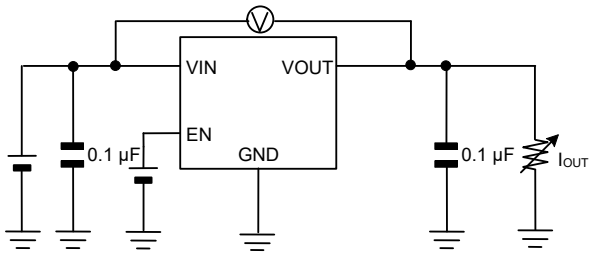
Measurement Circuit for Typical Performance Curves



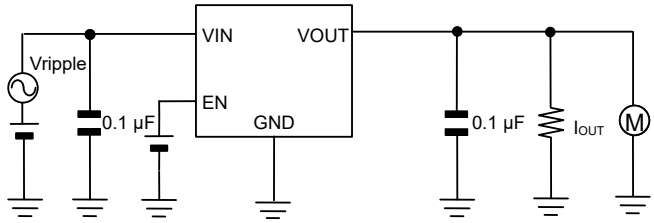
Measurement Setup for
Figure 1 to 5, 16, 29 to 33



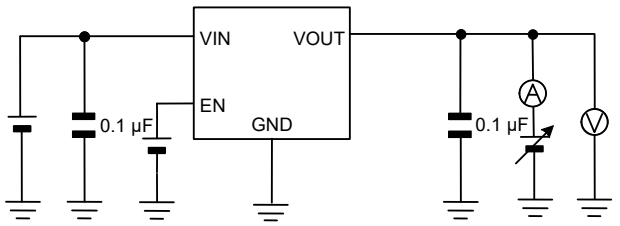
Measurement Setup for
Figure 6, 9 to 12, 14, 34, 37 to 39



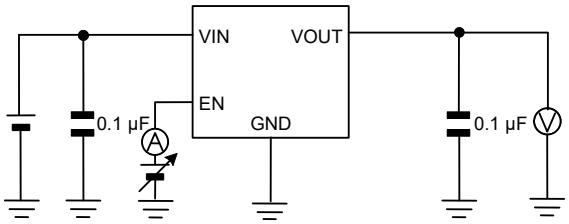
Measurement Setup for
Figure 7, 35



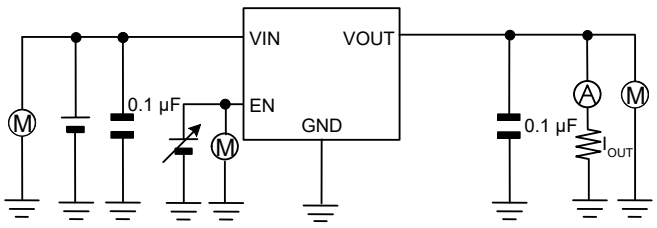
Measurement Setup for
Figure 8, 36



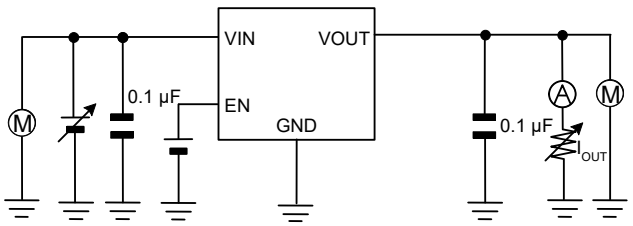
Measurement Setup for
Figure 13, 40



Measurement Setup for
Figure 17 to 18

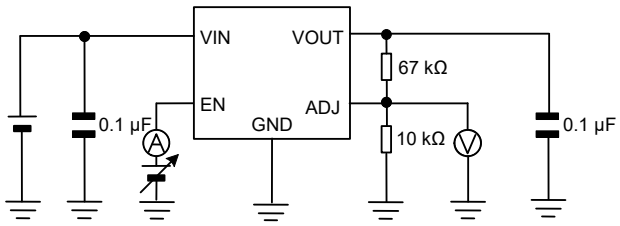


Measurement Setup for
Figure 27 to 28, 49 to 50



Measurement Setup for
Figure 19 to 26, 41 to 48

Measurement Circuit for Typical Performance Curves - continued



Measurement Setup for
Figure 15

Application and Implementation

Notice: The following information is given as a reference or hint for the application and the implementation. Therefore, it does not guarantee its operation on the specific function, accuracy or external components in the application. In the application, it shall be designed with sufficient margin by enough understanding about characteristics of the external components, e.g. capacitor, and also by appropriate verification in the actual operating conditions.

Selection of External Components

Input Pin Capacitor

In order to fully demonstrate the performance of this IC, it is recommended that the input capacitor be placed as close as possible to the input pin and the GND pin without being affected by mounting impedance, etc., and that it be laid out on the same mounting surface. In this case, a capacitor with a capacitance value of 0.047 µF (Min) or higher is recommended.
Depending on the layout of the peripheral components, including this IC, from the input power supply, if the distance from the battery is too far or the impedance of the input side is too high, for example, the current supply due to the load response of the IC cannot be withstood, and the output voltage may become unstable due to fluctuations in the input voltage. In such a case, it is necessary to use a large capacitor to prevent the line voltage from dropping. Select the capacitance of the input terminal capacitor according to the line impedance between the power smoothing circuit and the input terminal, and the load response required by the application.

In addition, the consideration should be taken as the output pin capacitor, to prevent an influence to the regulator's characteristic from the deviation or the variation of the external capacitor's characteristic. All output capacitors mentioned above are recommended to have a good DC bias characteristic and a temperature characteristic (approximately ±15 %, e.g. X7R, X8R) with being satisfied high absolute maximum voltage rating based on EIA standard. These capacitors should be placed close to the input pin and mounted on the same board side of the regulator not to be influenced by implement impedance.

Output Pin Capacitor

The output capacitor is mandatory for the regulator in order to realize stable operation. The output capacitor with capacitance value of 0.05 µF (Min) or higher and ESR up to 500 mΩ (Max) must be required between the output pin and the GND pin. For applications where the output voltage is 1.5 V or less, it is recommended to use an output capacitor with capacitance value of 0.22 µF or higher because the output capacitor holds less charge, increasing the amount of voltage fluctuation during transient response.

A proper selection of appropriate both the capacitance value and ESR for the output capacitor can improve the transient behavior of the regulator and can also keep the stability with better regulation loop. The correlation of the output capacitance value and ESR is shown in the graph on the next page as the output capacitor's capacitance value and the stability region for ESR. As described in this graph, this regulator is designed to be stable with ceramic capacitors as of MLCC, with the capacitance value from 0.05 µF to 470 µF and with ESR value within almost 0 Ω to 500 mΩ. The frequency range of ESR can be generally considered as within about 10 kHz to 100 kHz.

Note that the provided the stable area of the capacitance value and ESR in the graph is obtained under a specific set of conditions which is based on the measurement result in single IC on our board with a resistive load. In the actual environment, the stability is affected by wire impedance on the board, input power supply impedance and also loads impedance. Therefore, please note that a careful evaluation of the actual application, the actual usage environment and the actual conditions should be done to confirm the actual stability of the system.

Generally, in the transient event which is caused by the input voltage fluctuation or the load fluctuation beyond the gain bandwidth of the regulation loop, the transient response ability of the regulator depends on the capacitance value of the output capacitor. Basically the capacitance value of 0.05 µF (Min) or higher for the output capacitor is recommended as shown in the table on Output Capacitance C_{OUT}, ESR Available Area. Using bigger capacitance value can be expected to improve better the transient response ability in a high frequency. Various types of capacitors can be used for the output capacitor with high capacity which includes electrolytic capacitor, electro-conductive polymer capacitor and tantalum capacitor. Noted that, depending on the type of capacitors, its characteristics such as ESR (≤ 500 mΩ) absolute value range, a temperature dependency of capacitance value and increased ESR at cold temperature needs to be taken into consideration. When using capacitor with large ESR (≤500mΩ) , note that ceramic capacitor with 0.05 uF or higher must be connected in parallel to keep stability. In this case, the total capacitance should be less than 470 µF.

In addition, the same consideration should be taken as the input pin capacitor, to prevent an influence to the regulator's characteristic from the deviation or the variation of the external capacitor's characteristic. All output capacitors mentioned above are recommended to have a good DC bias characteristic and a temperature characteristic (approximately ±15 %, e.g. X7R, X8R) with being satisfied high absolute maximum voltage rating based on EIA standard. These capacitors should be placed close to the output pin and mounted on the same board side of the regulator not to be influenced by implement impedance.

Application and Implementation - continued

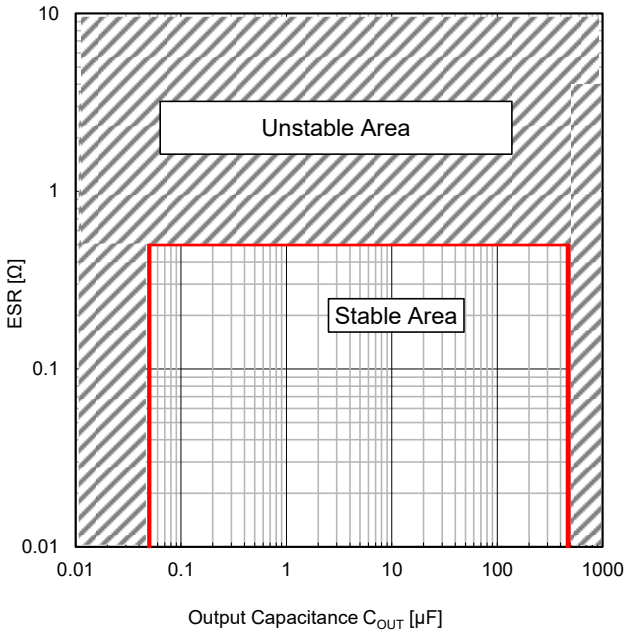


Figure 51. Output Capacitance C_{OUT}, ESR Available Area
(-40 °C ≤ Tj ≤ +150 °C, 4.5 V ≤ V_{IN} ≤ 42 V, V_{EN} = 5 V, IOUT = 0 mA to 150 mA)

Typical Application

Parameter	Symbol	Reference Value for Application
Output Current Range	I_{OUT}	I_{OUT} ≤ 150 mA
Output Capacitor	C_{OUT}	0.1 µF
Input Voltage	V_{IN}	13.5 V
Input Capacitor *(Note 1)*	C_{IN}	0.1 µF

(Note 1) If the inductance of power supply line is high, please adjust input capacitor value.
To avoid any malfunctions by input voltage drop of power supply line, please consider to adjust the impedance of power supply line to small as much as possible.

Application and Implementation - continued

Surge Voltage Protection for Linear Regulators

The following shows some helpful tips to protect ICs from possible inputting surge voltage which exceeds absolute maximum ratings.

Positive Surge to the Input

If there is any potential risk that positive surges higher than absolute maximum ratings, it is applied to the input, a Zener Diode should be inserted between the VIN pin and the GND to protect the device as shown in Figure 52.

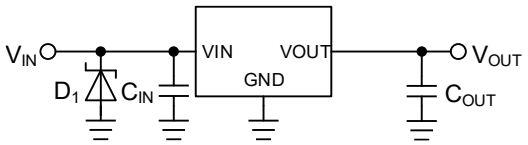


Figure 52. Surges Higher than absolute maximum ratings is Applied to the Input

Negative Surge to the Input

If there is any potential risk that negative surges below the absolute maximum ratings, (e.g.) -0.3 V, is applied to the input, a Schottky Diode should be inserted between the VIN and the GND to protect the device as shown in Figure 53.

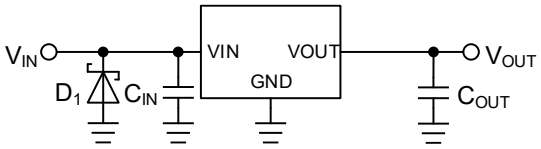


Figure 53. Surges Lower than -0.3 V is Applied to the Input

Reverse Voltage Protection for Linear Regulators

A linear regulator which is one of the integrated circuit (IC) operates normally in the condition that the input voltage is higher than the output voltage. However, it is possible to happen the abnormal situation in specific conditions which is the output voltage becomes higher than the input voltage. A reverse polarity connection between the input and the output might be occurred or a certain inductor component can also cause a polarity reverse conditions. If the countermeasure is not implemented, it may cause damage to the IC. The following shows some helpful tips to protect ICs from the reverse voltage occasion.

Protection against Reverse Input/Output Voltage

In the case that MOSFET is used for the pass transistor, a parasitic body diode between the drain-source generally exists. If the output voltage becomes higher than the input voltage and if its voltage difference exceeds V_F of the body diode, a reverse current flows from the output to the input through the body diode as shown in Figure 54. The current flows in the parasitic body diode is not limited in the protection circuit because it is the parasitic element, therefore too much reverse current may cause damage to degrade or destroy the semiconductor elements of the regulator.

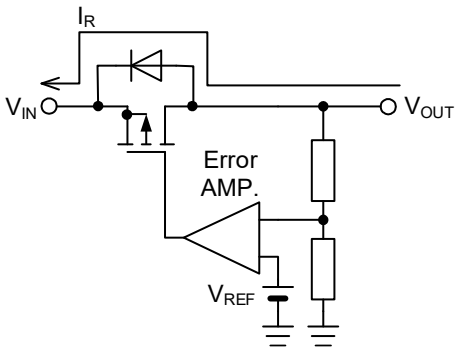


Figure 54. Reverse Current Path in a MOS Linear Regulator

Protection against Reverse Input/Output Voltage – continued

An effective solution for this problem is to implement an external bypass diode in order to prevent the reverse current flow inside the IC as shown in Figure 55. Especially in applications where the output voltage setting is high and a large output capacitor is connected, be sure to consider countermeasures for large reverse current values. Note that the bypass diode must be turned on prior to the internal body diode of the IC. This external bypass diode should be chosen as being lower forward voltage V_F than the internal body diode. It should to be selected a diode which has a rated reverse voltage greater than the IC's input maximum voltage and also which has a rated forward current greater than the anticipated reverse current in the actual application.

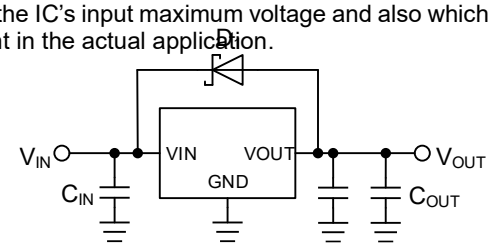


Figure 55. Bypass Diode for Reverse Current Diversion

A Schottky barrier diode which has a characteristic of low forward voltage (V_F) can meet to the requirement for the external diode to protect the IC from the reverse current. However, it also has a characteristic that the leakage (I_R) caused by the reverse voltage is bigger than other diodes. Therefore, it should be taken into the consideration to choose it because if I_R is large, it may cause increase of the current consumption, or raise of the output voltage in the light-load current condition. I_R characteristic of Schottky diode has positive temperature characteristic, which the details shall be checked with the datasheet of the products, and the careful confirmation of behavior in the actual application is mandatory.

Even in the condition when the input/output voltage is inverted, if the VIN pin is open as shown in Figure 56, or if the VIN pin becomes high-impedance condition as designed in the system, it cannot damage or degrade the parasitic element. It's because a reverse current via the pass transistor becomes extremely low. In this case, therefore, the protection external diode is not necessary.

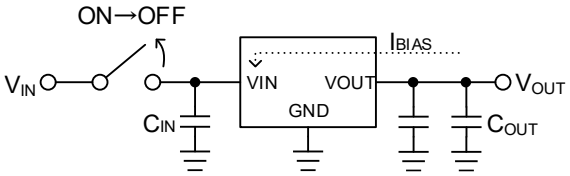


Figure 56. Open VIN

Protection against Input Reverse Voltage

When the input of the IC is connected to the power supply, accidentally if plus and minus are routed in reverse, or if there is a possibility that the input may become lower than the GND pin, it may cause to destroy the IC because a large current passes via the internal electrostatic breakdown prevention diode between the input pin and the GND pin inside the IC as shown in Figure 57.

The simplest solution to avoid this problem is to connect a Schottky barrier diode or a rectifier diode in series to the power supply line as shown in Figure 58. However, it increases a power loss calculated as V_F x I_{CC}, and it also causes the voltage drop by a forward voltage V_F at the supply voltage while normal operation.
Generally, since the Schottky barrier diode has lower V_F, so it contributes to rather smaller power loss than rectifier diodes. If IC has load currents, the required input current to the IC is also bigger. In this case, this external diode generates heat more, therefore select a diode with enough margin in power dissipation. On the other hand, a reverse current passes this diode in the reverse connection condition, however, it is negligible because its small amount.

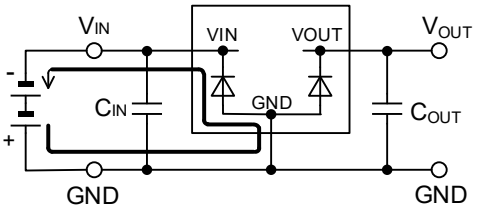


Figure 57. Current Path in Reverse Input Connection

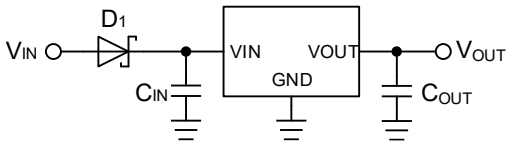


Figure 58. Protection against Reverse Polarity 1

Protection against Input Reverse Voltage - continued

Figure 59 shows a circuit in which a P-channel MOSFET is connected in series to the power. The body diode (parasitic element) is located in the drain-source junction area of the MOSFET. The drop voltage in a forward connection is calculated from the on state resistance of the MOSFET and the output current I_O. It is smaller than the drop voltage by the diode as shown in Figure 59 and results in less of a power loss. No current flows in a reverse connection where the MOSFET remains off in Figure 59.

If the gate-source voltage exceeds maximum rating of MOSFET gate-source junction with derating curve in consideration, reduce the gate-source junction voltage by connecting resistor voltage divider as shown in Figure 60.

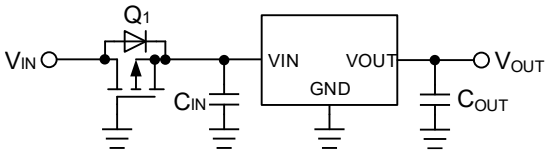


Figure 59. Protection against Reverse Polarity 2

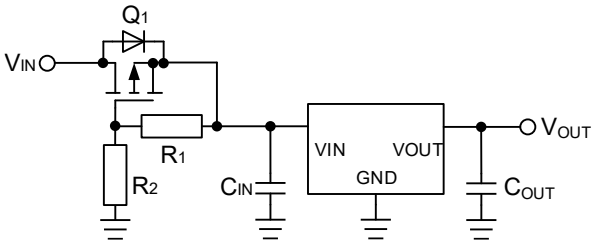


Figure 60. Protection against Reverse Polarity 3

Protection against Reverse Output Voltage when Output Connect to an Inductor

If the output load is inductive, electrical energy accumulated in the inductive load is released to the ground at the moment that the output voltage is turned off. IC integrates ESD protection diodes between the IC output and ground pins. A large current may flow in such condition finally resulting on destruction of the IC. To prevent this situation, connect a Schottky barrier diode in parallel to the integrated diodes as shown in Figure 61.

Further, if a long wire is in use for the connection between the output pin of the IC and the load, confirm that the negative voltage is not generated at the VOUT pin when the output voltage is turned off by observation of the waveform on an oscilloscope, since it is possible that the load becomes inductive. An additional diode is required for a motor load that is affected by its counter electromotive force, as it produces an electrical current in a similar way.

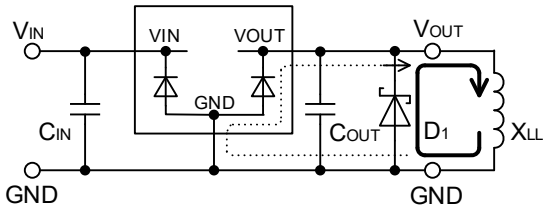


Figure 61. Current Path in Inductive Load (Output: Off)

Power Dissipation

■SSOP5

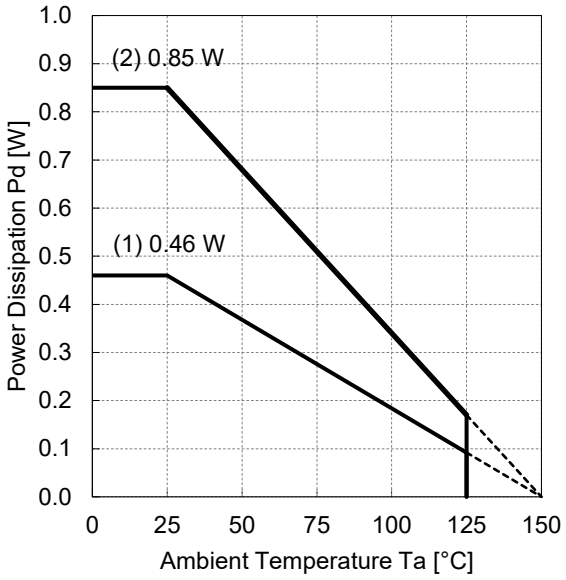


Figure 62. Power Dissipation Graph (SSOP5)

(1): 1-layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR-4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Top copper foil: ROHM recommended footprint
+ wiring to measure, 70 µm. copper.

(2): 4-layer PCB
(Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR-4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Top copper foil: ROHM recommended footprint
+ wiring to measure, 70 µm. copper.
2 inner layers copper foil area of PCB:
74.2 mm x 74.2 mm, 35 µm. copper.
Copper foil area on the reverse side of PCB:
74.2 mm x 74.2 mm, 70 µm. copper.

Condition (1) : θ_{JA} = 271.3 °C/W, Ψ_{JT} (top center) = 46 °C/W
Condition (2) : θ_{JA} = 146.7 °C/W, Ψ_{JT} (top center) = 37 °C/W

■HTSOP-J8

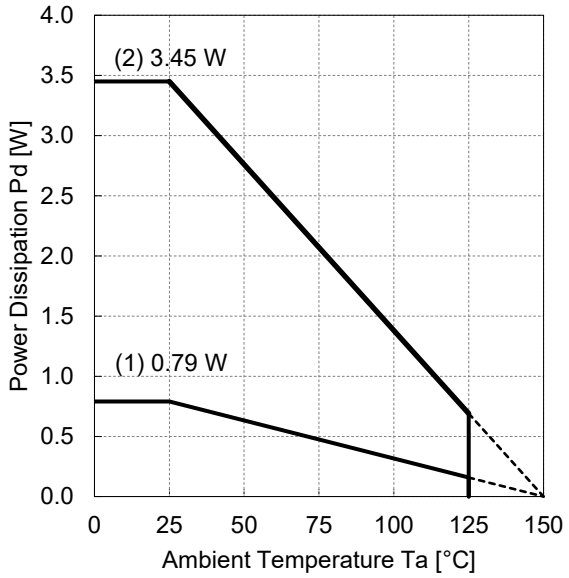


Figure 63. Power Dissipation Graph (HTSOP-J8)

(1): 1-layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR-4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Top copper foil: ROHM recommended footprint
+ wiring to measure, 70 µm. copper.

(2): 4-layer PCB
(Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR-4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Top copper foil: ROHM recommended footprint
+ wiring to measure, 70 µm. copper.
2 inner layers copper foil area of PCB:
74.2 mm x 74.2 mm, 35 µm. copper.
Copper foil area on the reverse side of PCB:
74.2 mm x 74.2 mm, 70 µm. copper.

Condition (1) : θ_{JA} = 157.2 °C/W, Ψ_{JT} (top center) = 32 °C/W
Condition (2) : θ_{JA} = 36.2 °C/W, Ψ_{JT} (top center) = 11 °C/W

Thermal Design

This product exposes a frame on the back side of the package for thermal efficiency improvement. The power consumption of the IC is decided by the dropout voltage condition, the load current and the current consumption. Refer to power dissipation curves illustrated in Figure 62 and 63 when using the IC in an environment of Ta ≥ 25 °C. Even if the ambient temperature Ta is at 25°C, chip junction temperature (Tj) can be very high depending on the input voltage and the load current. Consider the design to be Tj ≤ Tjmax = 150 °C in whole operating temperature range.
Should by any condition the maximum junction temperature Tjmax = 150 °C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Therefore, need to be careful because it might be different from the actual use condition. Verify the application and allow sufficient margins in the thermal design by the following method to calculate the junction temperature Tj. Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature Tj with ambient temperature Ta.

$$Tj = Ta + P_C \times \theta_{JA} \text{ [°C]}$$

Where:

Tj is the Junction Temperature
Ta is the Ambient Temperature
P_C is the Power Consumption
θ_{JA} is the Thermal Resistance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature Tj with top center of case's (mold) temperature T_T.

$$Tj = T_T + P_C \times \Psi_{JT} \text{ [°C]}$$

Where:

Tj is the Junction Temperature
T_T is the Top Center of Case's (mold) Temperature
P_C is the Power consumption
Ψ_{JT} is the Thermal Resistance (Junction to Top Center of Case)

3. The following method is used to calculate the power consumption Pc (W).

$$Pc = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC} \text{ [W]}$$

Where:

P_C is the Power Consumption
V_{IN} is the Input Voltage
V_{OUT} is the Output Voltage
I_{OUT} is the Load Current
I_{CC} is the Current Consumption

Calculation Example (SSOP5)
If V_{IN} = 13.5 V, V_{OUT} = 5.0 V, I_{OUT} = 40 mA, I_{CC} = 28 μA, the power consumption Pc can be calculated as follows:

$$\begin{aligned} P_C &= (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC} \\ &= (13.5\,V - 5.0\,V) \times 40\,mA + 13.5\,V \times 28\,\mu A \\ &= 0.34\,W \end{aligned}$$

At the maximum ambient temperature Tamax = 85 °C,
the thermal impedance (Junction to Ambient) θ_{JA} = 146.7 °C/W (4-layer PCB)

$$\begin{aligned} Tj &= Tamax + P_C \times \theta_{JA} \\ &= 85\,°C + 0.34\,W \times 146.7\,°C/W \\ &= 134.9\,°C \end{aligned}$$

When operating the IC, the top center of case's (mold) temperature T_T = 100 °C, Ψ_{JT} = 46 °C/W (1-layer PCB)

$$\begin{aligned} Tj &= T_T + P_C \times \Psi_{JT} \\ &= 100\,°C + 0.34\,W \times 46\,°C/W \\ &= 115.6\,°C \end{aligned}$$

If it is difficult to ensure the margin by the calculations above, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad for optimum thermal performance.

Calculation Example (HTSOP-J8)
If V_{IN} = 13.5 V, V_{OUT} = 5.0 V, I_{OUT} = 40 mA, I_{CC} = 28 μA, the power consumption Pc can be calculated as follows:

$$\begin{aligned} P_C &= (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC} \\ &= (13.5\,V - 5.0\,V) \times 40\,mA + 13.5\,V \times 28\,\mu A \\ &= 0.34\,W \end{aligned}$$

At the maximum ambient temperature Tamax = 85 °C,
the thermal impedance (Junction to Ambient) θ_{JA} = 36.2 °C/W (4-layer PCB)

$$\begin{aligned} Tj &= Tamax + P_C \times \theta_{JA} \\ &= 85\,°C + 0.34\,W \times 36.2\,°C/W \\ &= 97.3\,°C \end{aligned}$$

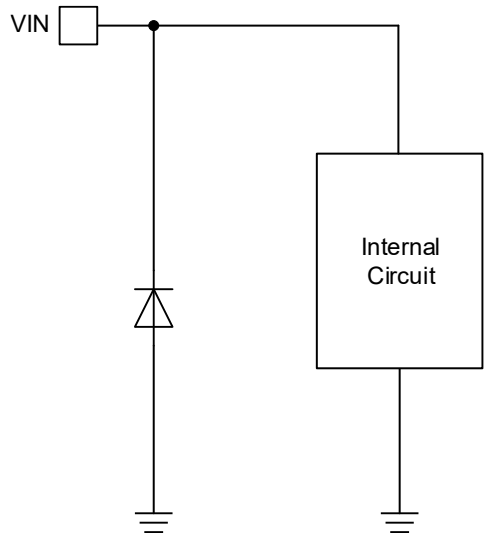
When operating the IC, the top center of case's (mold) temperature T_T = 100 °C, Ψ_{JT} = 32 °C/W (1-layer PCB)

$$\begin{aligned} Tj &= T_T + P_C \times \Psi_{JT} \\ &= 100\,°C + 0.34\,W \times 32\,°C/W \\ &= 110.9\,°C \end{aligned}$$

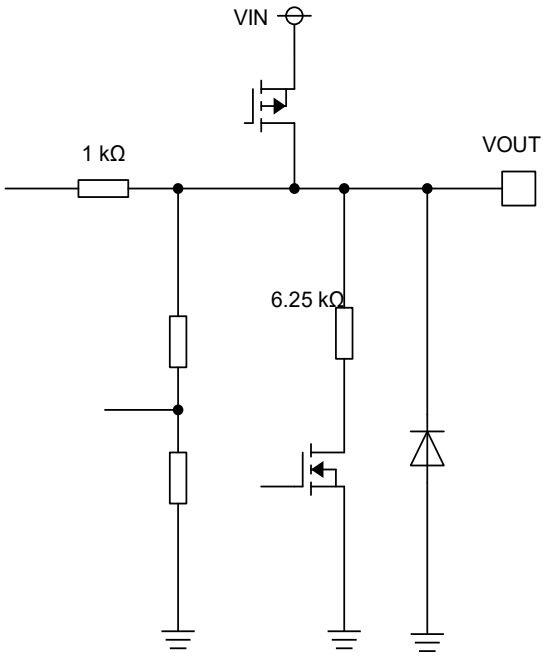
If it is difficult to ensure the margin by the calculations above, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad for optimum thermal performance.

I/O Equivalence Circuit

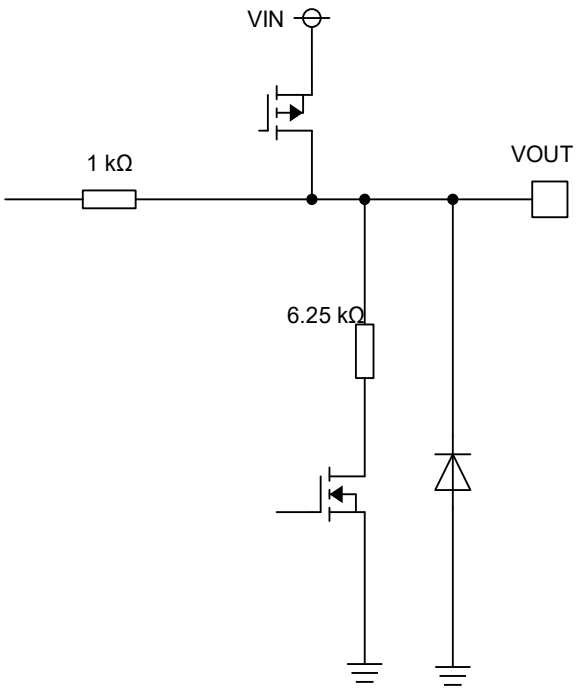
VIN Pin



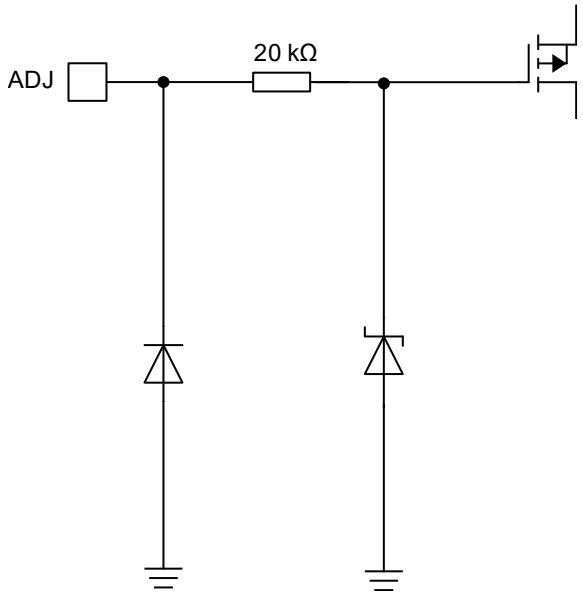
VOUT Pin *(Note 1)*



VOUT Pin *(Note 2)*

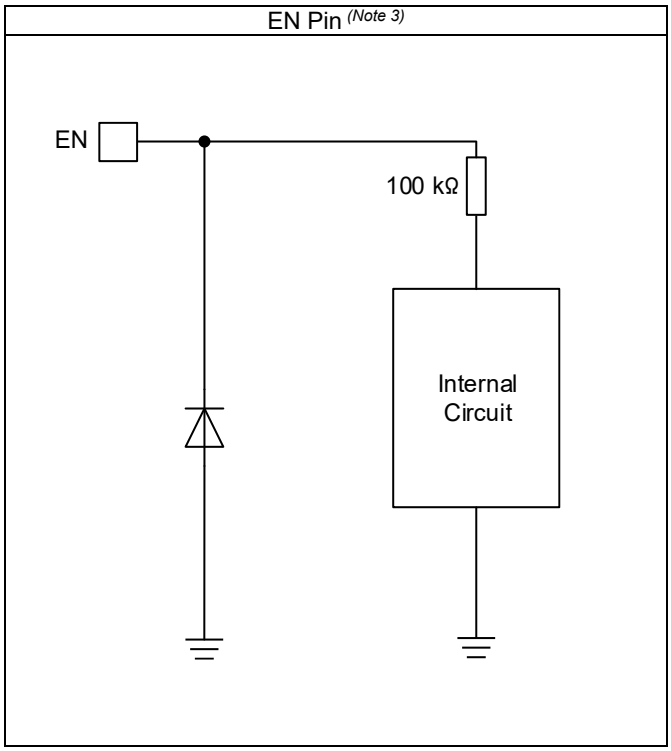


ADJ Pin *(Note 2)*



(Note 1) Applicable for product with BD9xxN1G-C, BD9xxN1WG-C, BD9xxN1EFJ-C, BD9xxN1WEFJ-C.
(Note 2) Applicable for product with BD900N1G-C, BD900N1WG-C, BD900N1EFJ-C, BD900N1WEFJ-C.

I/O Equivalence Circuit - continued



(Note 3) Applicable for product with BD9xxN1WG-C, BD9xxN1WEFJ-C (xx = 33, 50, 00).

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Thermal Consideration**
   The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. The amount of heat generation depends on the voltage difference between the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating. If Junction temperature is over Tjmax (=150 °C), IC characteristics may be worse due to rising chip temperature. Heat resistance in specification is measurement under PCB condition and environment recommended in JEDEC. Ensure that heat resistance in specification is different from actual environment.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

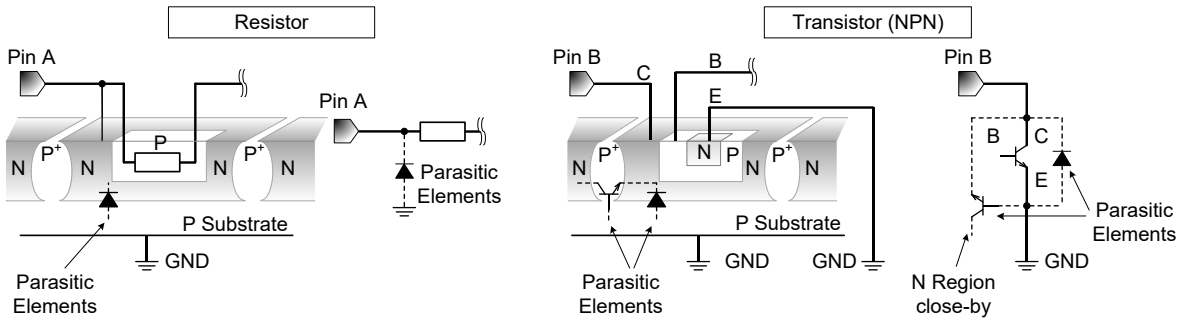
Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

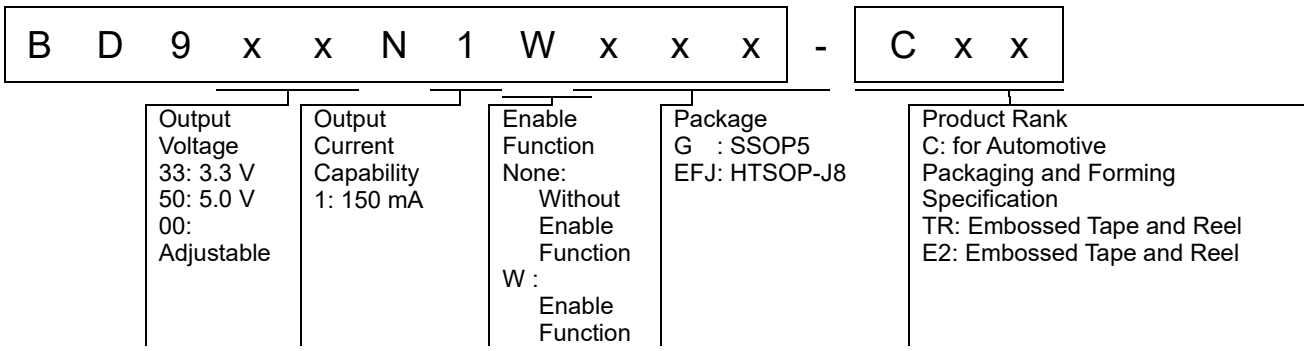
13. Thermal Shutdown Protection Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

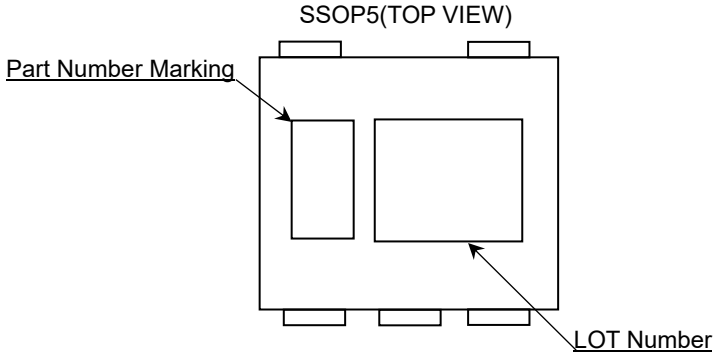
Ordering Information



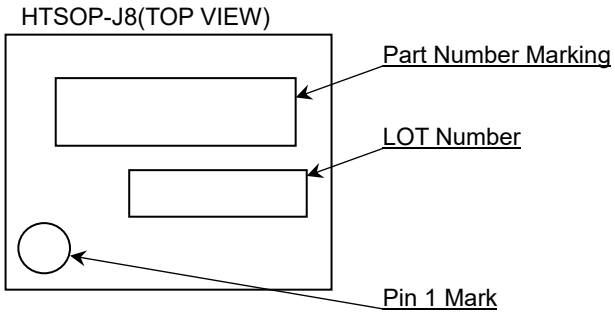
Lineup

Output Current Capability	Output Voltage	Enable Function	Package	Ordering
150 mA	3.3 V	not available	SSOP5	BD933N1G-CTR
			HTSOP-J8	BD933N1EFJ-CE2
		available	SSOP5	BD933N1WG-CTR
			HTSOP-J8	BD933N1WEFJ-CE2
	5.0 V	not available	SSOP5	BD950N1G-CTR
			HTSOP-J8	BD950N1EFJ-CE2
		available	SSOP5	BD950N1WG-CTR
			HTSOP-J8	BD950N1WEFJ-CE2
	Adjustable	not available	SSOP5	BD900N1G-CTR
			HTSOP-J8	BD900N1EFJ-CE2
		available	SSOP5	BD900N1WG-CTR
			HTSOP-J8	BD900N1WEFJ-CE2

Marking Diagrams



Part Number	Part Number Marking	Output Voltage [V]	Enable Input*(Note 1)*
BD950N1G-C	dd	5.0	not available
BD933N1G-C	de	3.3	not available
BD900N1G-C	df	Adjustable	not available
BD950N1WG-C	dk	5.0	available
BD933N1WG-C	dm	3.3	available
BD900N1WG-C	dn	Adjustable	available

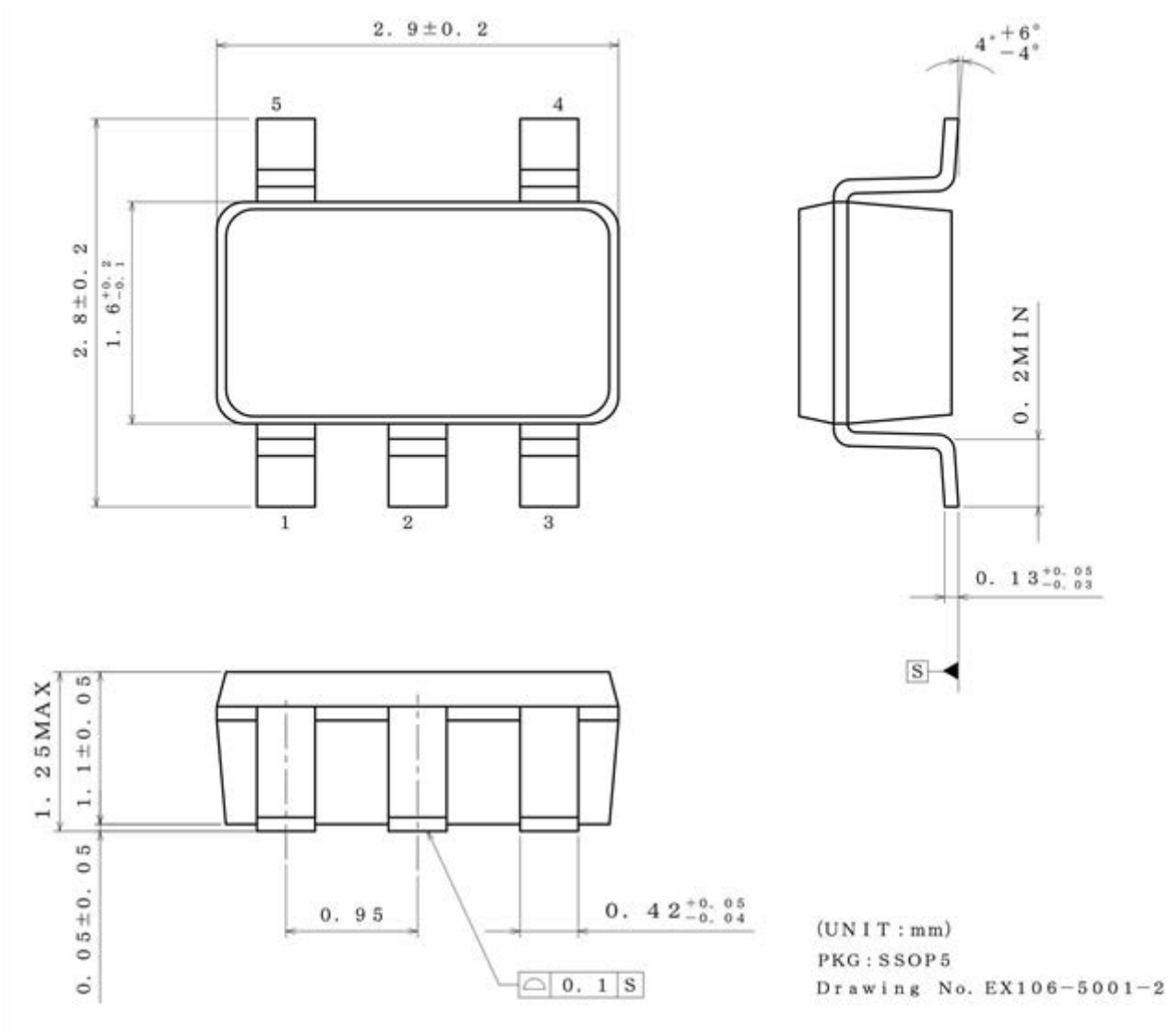


Part Number	Part Number Marking	Output Voltage [V]	Enable Input*(Note 1)*
BD950N1EFJ-C	950N1	5.0	not available
BD933N1EFJ-C	933N1	3.3	not available
BD900N1EFJ-C	900N1	Adjustable	not available
BD950N1WEFJ-C	950N1W	5.0	available
BD933N1WEFJ-C	933N1W	3.3	available
BD900N1WEFJ-C	900N1W	Adjustable	available

(Note 1) available: With Enable Input not available: Without Enable Input

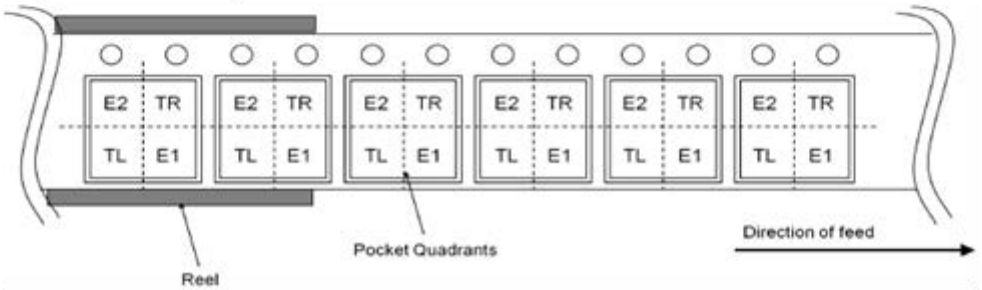
Physical Dimension and Packing Information

Package Name	SSOP5



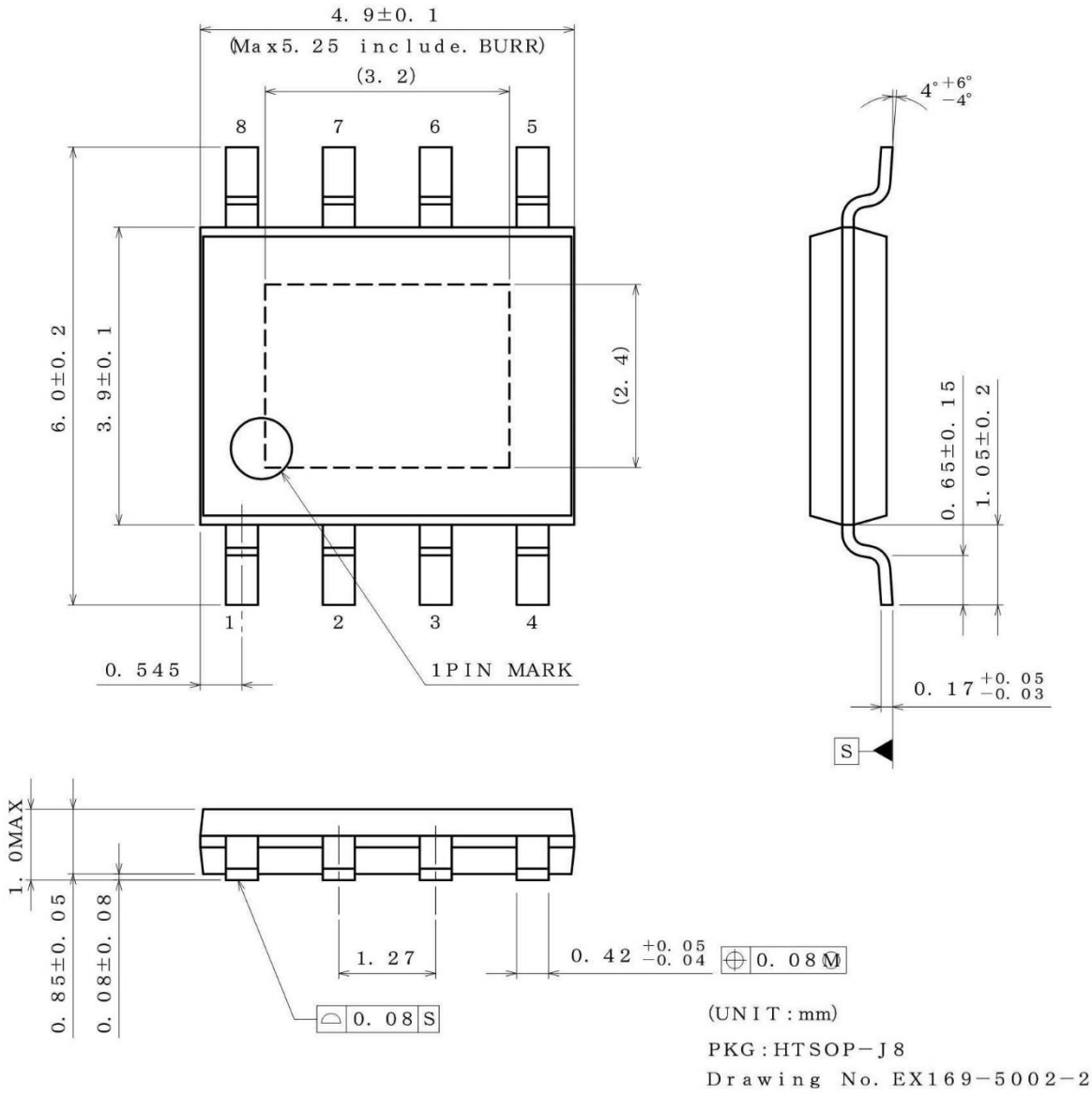
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



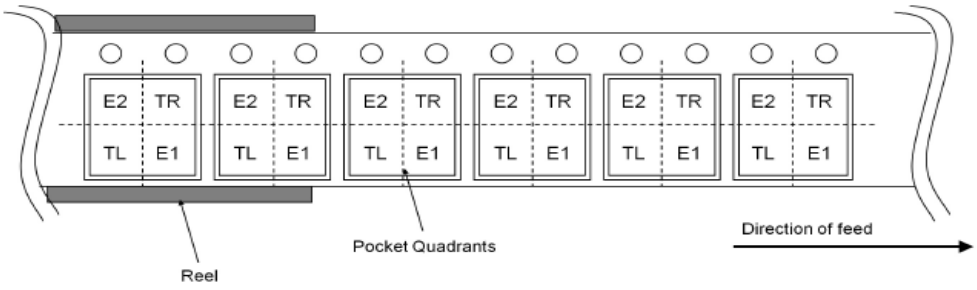
Physical Dimension and Packing Information – continued

Package Name	HTSOP-J8



<Tape and Reel information>

Tape	**Embossed carrier tape**
Quantity	**2500pcs**
Direction of feed	**E2** **(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)**



Revision History

Date	Revision	Changes
12.May.2022	001	New Release

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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