5.5 V, 2 A
Pch/Nch Power MOSFET with Drivers For Automotive

BD90302NUF-C

General Description

BD90302NUF-C are boost MOSFET with drivers for BD8Pxxx Series(Note 1) exclusive use.
BD8Pxxx Series is a buck DC/DC Converter with boost function.
When used with BD8Pxxx Series, a synchronous buck-boost DC/DC Converter is constituted.

(Note 1) About whether it supports BD90302NUF-C, refer to Datasheet of BD8Pxxx Series.

Features

- AEC-Q100 Qualified(Note 1)
- Built-in Pch/Nch Power MOSFET with Drivers
- CTLIN Pin Enables to Control Pch/Nch Power MOSFET
- Wettable Flank SON Package

(Note 1) Grade 1

Applications

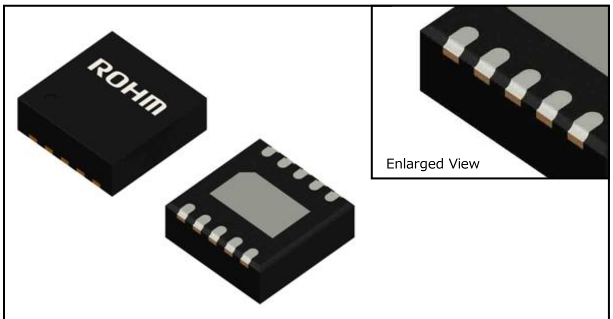
- Automotive Equipment (Cluster Panel, Infotainment Systems)
- Other Electronic Equipment

Key Specifications

- PVOUT Pin Voltage: 3.0 V to 5.5 V
- SW2 Pin Current: 2 A (Max)
- Pch Power MOSFET ON Resistance: 55 mΩ (Typ)
- Nch Power MOSFET ON Resistance: 65 mΩ (Typ)
- Shutdown Circuit Current: 0 μA (Typ)
- Operating Temperature: -40 °C to +125 °C

Package

Package	W(Typ) x D(Typ) x H(Max)
VSON10FV3030	3.00 mm x 3.00 mm x 1.00 mm



VSON10FV3030
Wettable Flank Package

Typical Application Circuit

Buck-Boost DC/DC Converter using BD8P250MUF-C.

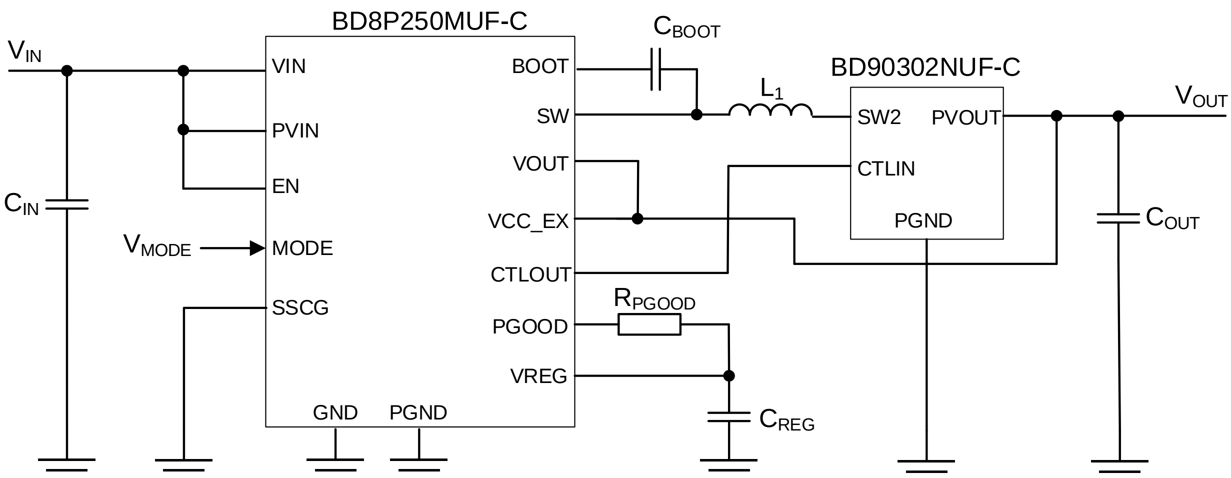
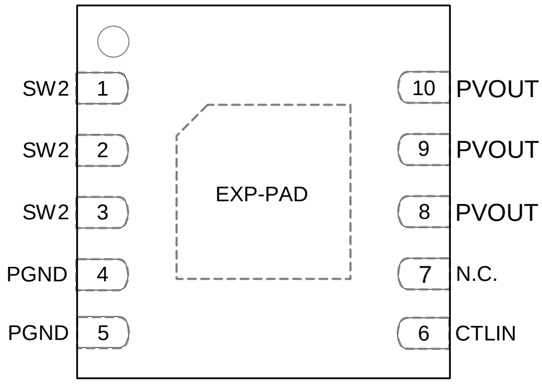


Figure 1. Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration



(TOP VIEW)

Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Function
1, 2, 3	SW2	Inductor connection pins. These pins are connected to the drain of Pch/Nch Power MOSFET.
4, 5	PGND	Ground pins. These pins are connected to the source of Nch Power MOSFET.
6	CTLIN	The pin for control of Pch/Nch Power MOSFET. Connect to the CTLOUT pin of BD8Pxxx Series.
7	N.C.	No connection pin. Leave this pin open.
8, 9, 10	PVOUT	Output and internal power supply pins. These pins are connected to the source of Pch Power MOSFET.
-	EXP-PAD	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using via provides excellent heat dissipation characteristics.

Block Diagram

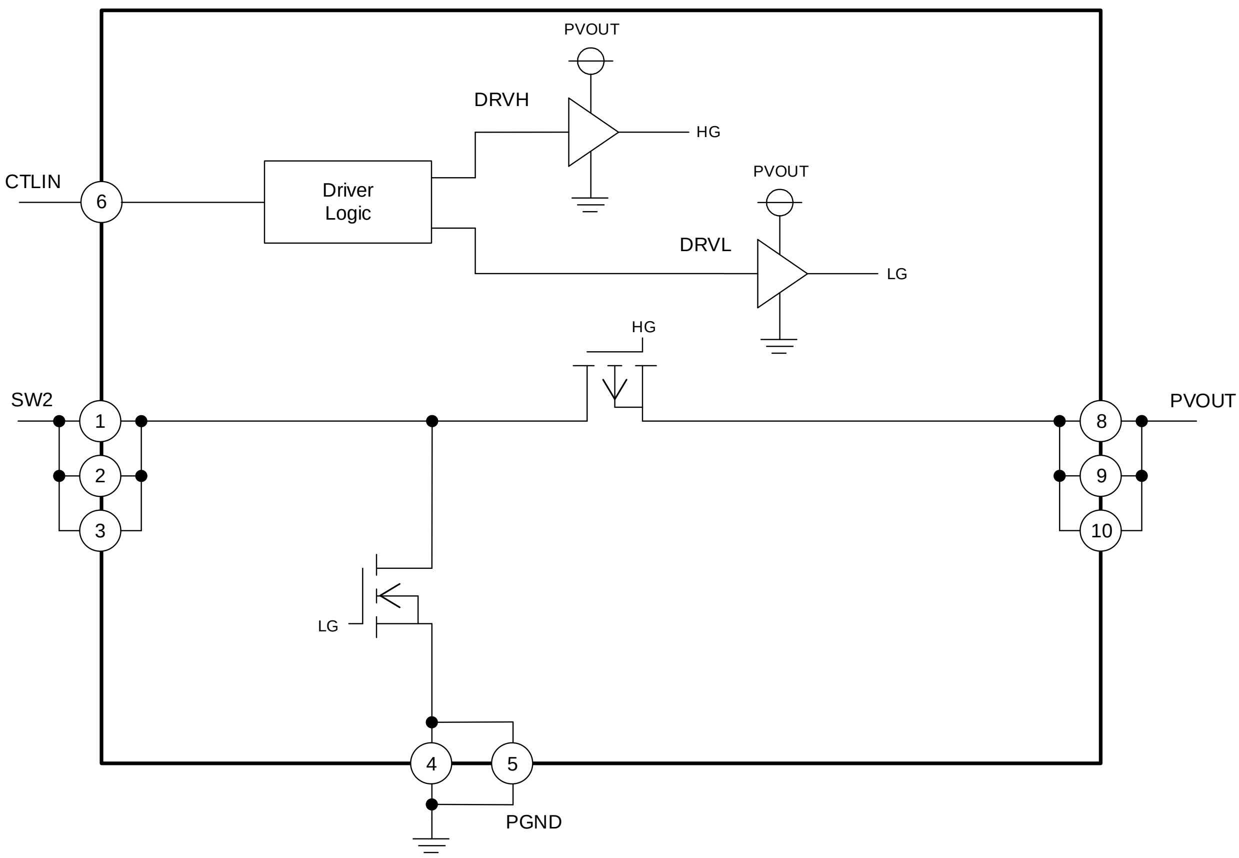


Figure 3. Block Diagram

Description of Blocks

1. Driver Logic
   This circuit receives the CTLOUT signal output from BD8Pxxx Series and controls the Pch/Nch Power MOSFET for boost.
   Pch Power MOSFET is OFF and Nch Power MOSFET is ON when the CTLIN pin is 2.0 V or more.
   Pch Power MOSFET is ON and Nch Power MOSFET is OFF when the CTLIN pin is 0.8 V or less.

2. DRVH
   This is the driver circuit to drive the gate of Pch Power MOSFET.

3. DRVL
   This is the driver circuit to drive the gate of Nch Power MOSFET.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
PVOUT Pin Voltage	V_{PVOUT}	-0.3 to +7.0	V
SW2 Pin Voltage	V_{SW2}	-0.3 to +7.0	V
CTLIN Pin Voltage	V_{CTLIN}	-0.3 to +7.0	V
SW2 Pin Current	I_{SW2}	3.5	A
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Caution 3: *This IC does not have built-in thermal shutdown circuit and over current protection circuit that prevent damage to the IC. Operation of IC should always be within the IC's absolute maximum ratings.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
VSON10FV3030				
Junction to Ambient	θ_{JA}	223.3	41.5	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	56	6	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
PVOUT Pin Voltage	V_{PVOUT}	3.0	5.0	5.5	V
Operating Temperature	Topr	-40	-	+125	°C
SW2 Pin Current	I_{SW2}	-	-	2	A
CTLIN Frequency	f_{CTLIN}	-	-	2.4	MHz

Electrical Characteristics (Unless otherwise specified Ta = -40 °C~+125 °C, V_{PVOUT} = 5.0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Shutdown Circuit Current	I_{SDN}	-	0	1	μA	V_{CTLIN} = 0 V, Ta = 25 °C
Circuit Current	I_{CC}	-	65	105	μA	V_{CTLIN} = 5 V, Ta = 25 °C
Pch Power MOSFET ON Resistance	R_{ONP}	-	55	90	mΩ	V_{CTLIN} = 0 V, I_{SW2} = -50 mA
Nch Power MOSFET ON Resistance	R_{ONN}	-	65	110	mΩ	V_{CTLIN} = 5 V, I_{SW2} = +50 mA
CTLIN Threshold Voltage High	V_{CTLINH}	2.0	-	5.5	V	
CTLIN Threshold Voltage Low	V_{CTLINL}	0	-	0.8	V	
CTLIN Input Current	I_{CTLIN}	-	0	1	μA	V_{CTLIN} = 5 V

Typical Performance Curves

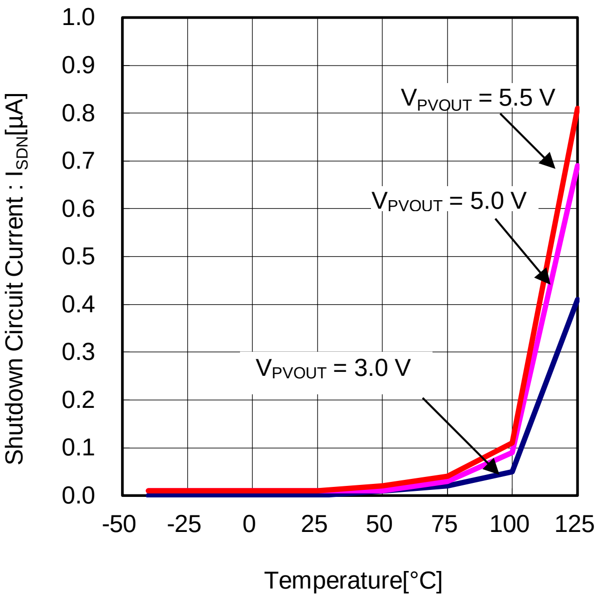


Figure 4. Shutdown Circuit Current vs Temperature

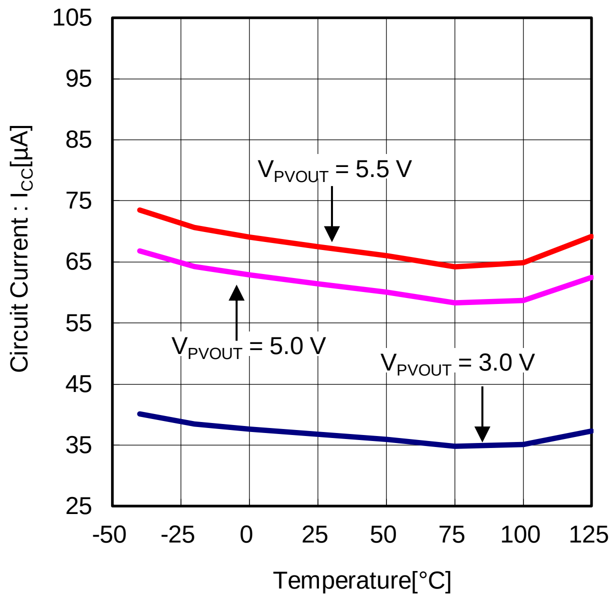


Figure 5. Circuit Current vs Temperature

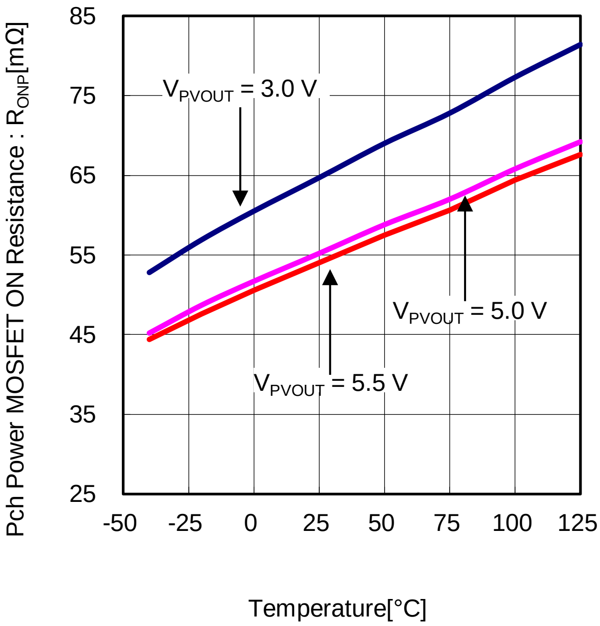


Figure 6. Pch Power MOSFET ON Resistance vs Temperature

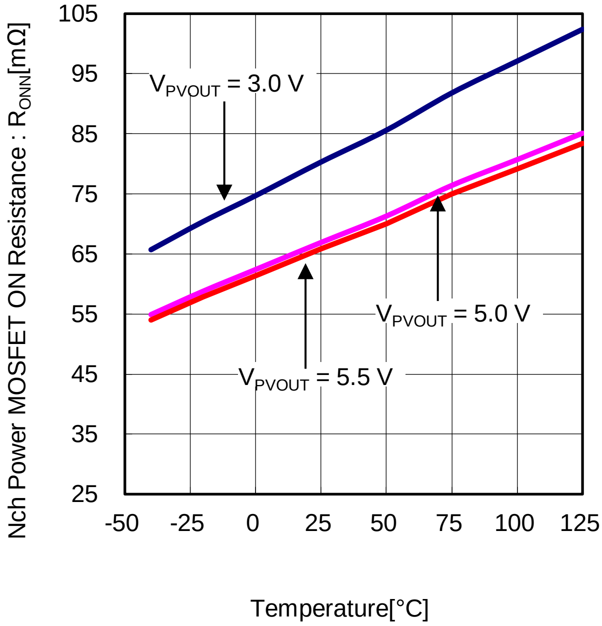


Figure 7. Nch Power MOSFET ON Resistance vs Temperature

Typical Performance Curves – continued

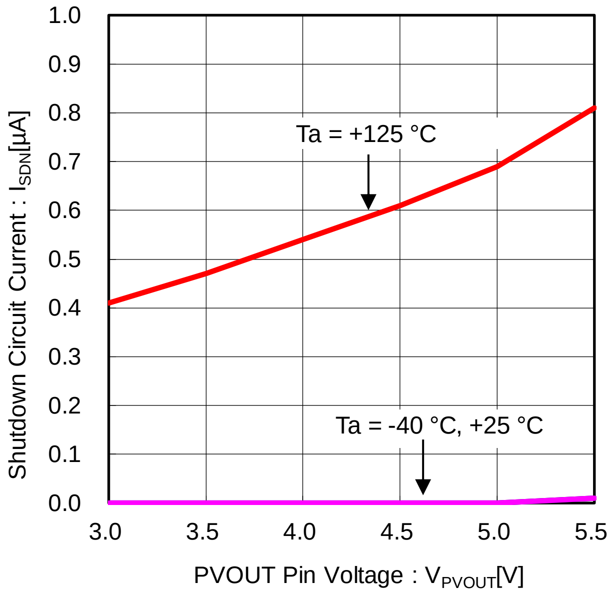


Figure 6. Shutdown Circuit Current vs PVOUT Pin Voltage

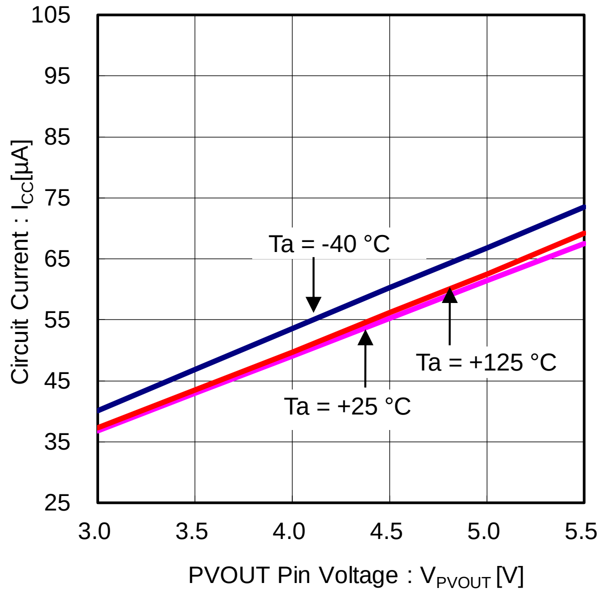


Figure 7. Circuit Current vs PVOUT Pin Voltage

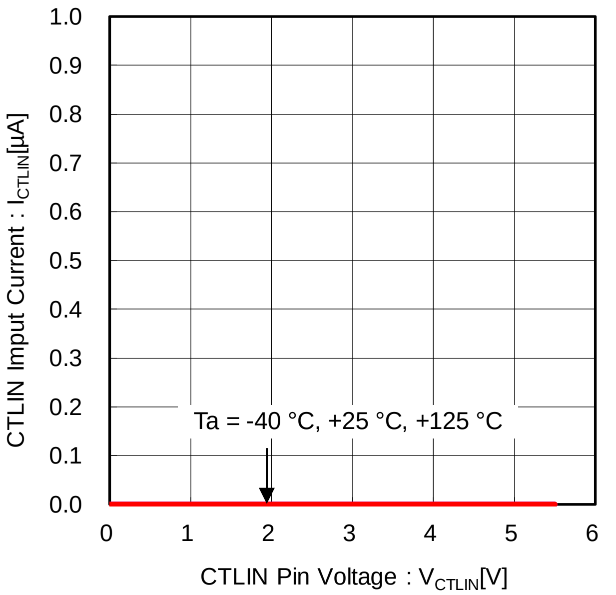


Figure 8. CTLIN Input Current vs CTLIN Pin Voltage

Function Explanations

Control Function

ON or OFF of Power MOSFET can be controlled by the voltage applied to the CTLIN pin.
Pch Power MOSFET is OFF and Nch Power MOSFET is ON when the CTLIN pin is 2.0 V or more.
Pch Power MOSFET is ON and Nch Power MOSFET is OFF when the CTLIN pin is 0.8 V or less.

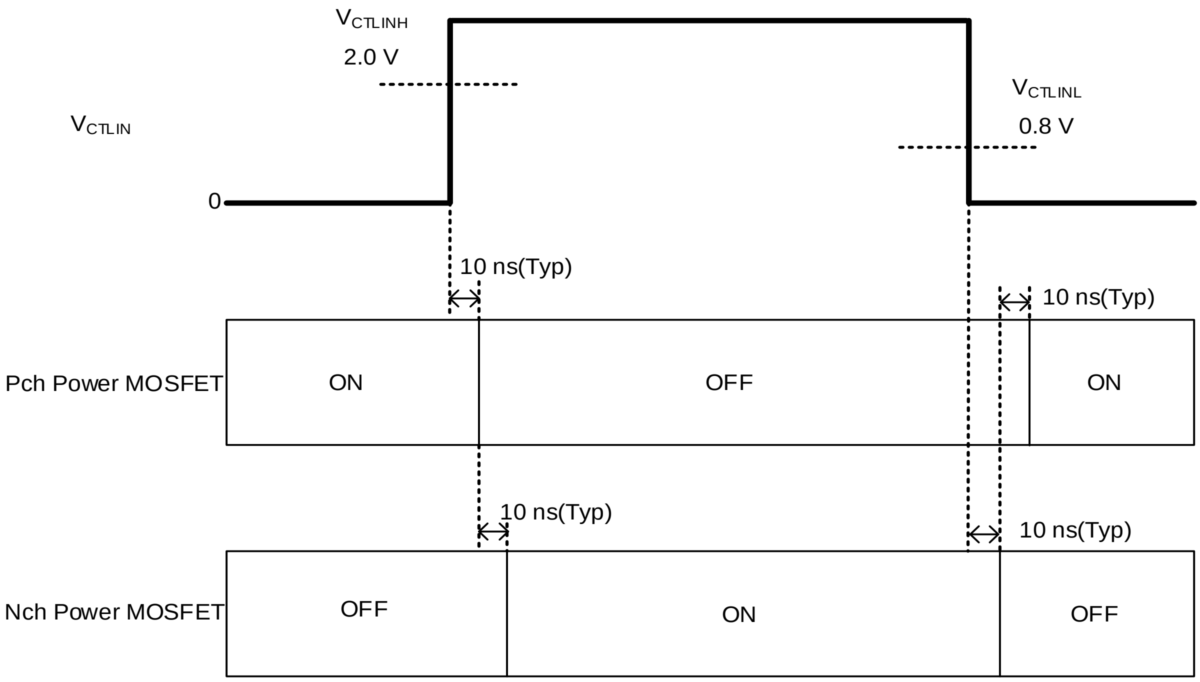


Figure 11. Control Function Timing Chart

Application Example

For Application Example, refer to Datasheet of BD8Pxxx Series.

PCB Layout Design

For the PCB Layout Design, refer to Datasheet of BD8Pxxx Series.

Power Dissipation

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. The ambient temperature Ta is to be 125 °C or less.
2. The chip junction temperature Tj is to be 150 °C or less.

The chip junction temperature Tj can be obtained in the following two equations:

1. To obtain Tj from the package surface center temperature Tt in actual use

$$Tj = Tt + \psi_{JT} \times W \ \text{[°C]}$$

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta_{JA} \times W \ \text{[°C]}$$

Where:

ψ_{JT} is junction to top characterization parameter [°C/W] (Refer to page 4)
θ_{JA} is junction to ambient [°C/W] (Refer to page 4)

The heat loss W of the IC in the Shutdown can be obtained by the formula shown below:

$$W = R_{ONP} \times {I_{OUT}}^2 + V_{OUT} \times I_{SDN} \ \text{[W]}$$

Where:

R_{ONP} is the Pch Power MOSFET ON Resistance [Ω] (Refer to page 5)
I_{OUT} is the Output Current [A]
V_{OUT} is the Output Voltage [V]
I_{SDN} is the Shutdown Circuit Current [A] (Refer to page 5)

I/O Equivalence Circuits

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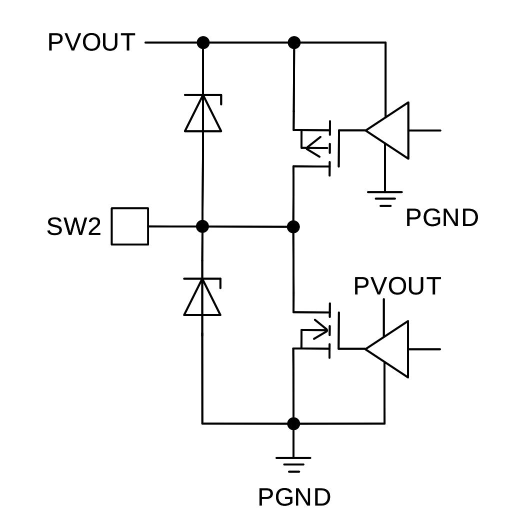
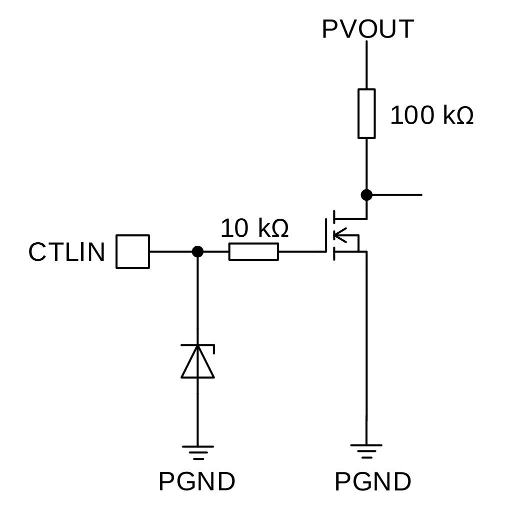
<tr><th>1.2.3. SW2</th><th>6. CTLIN</th></tr>
<tr><td>
</td><td>
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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

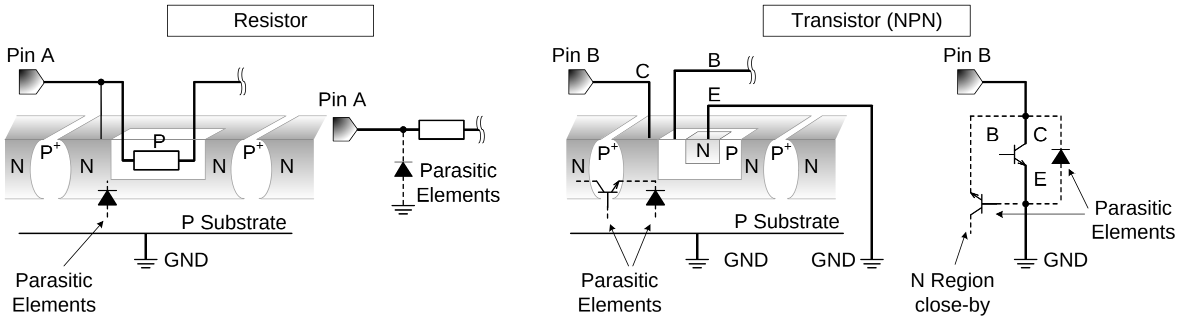


Figure 12. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

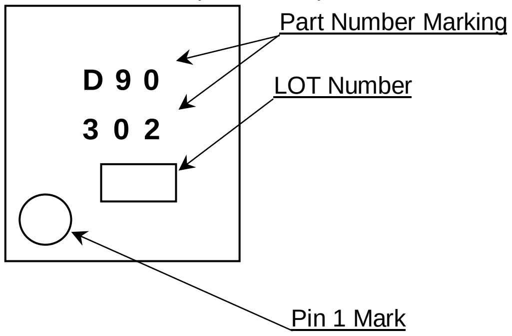
Ordering Information

B D 9 0 3 0 2 N U F - C E 2

- Part Number
- Package: VSON10FV3030
- Product class: C for Automotive applications
- Packaging and forming specification: E2: Embossed tape and reel

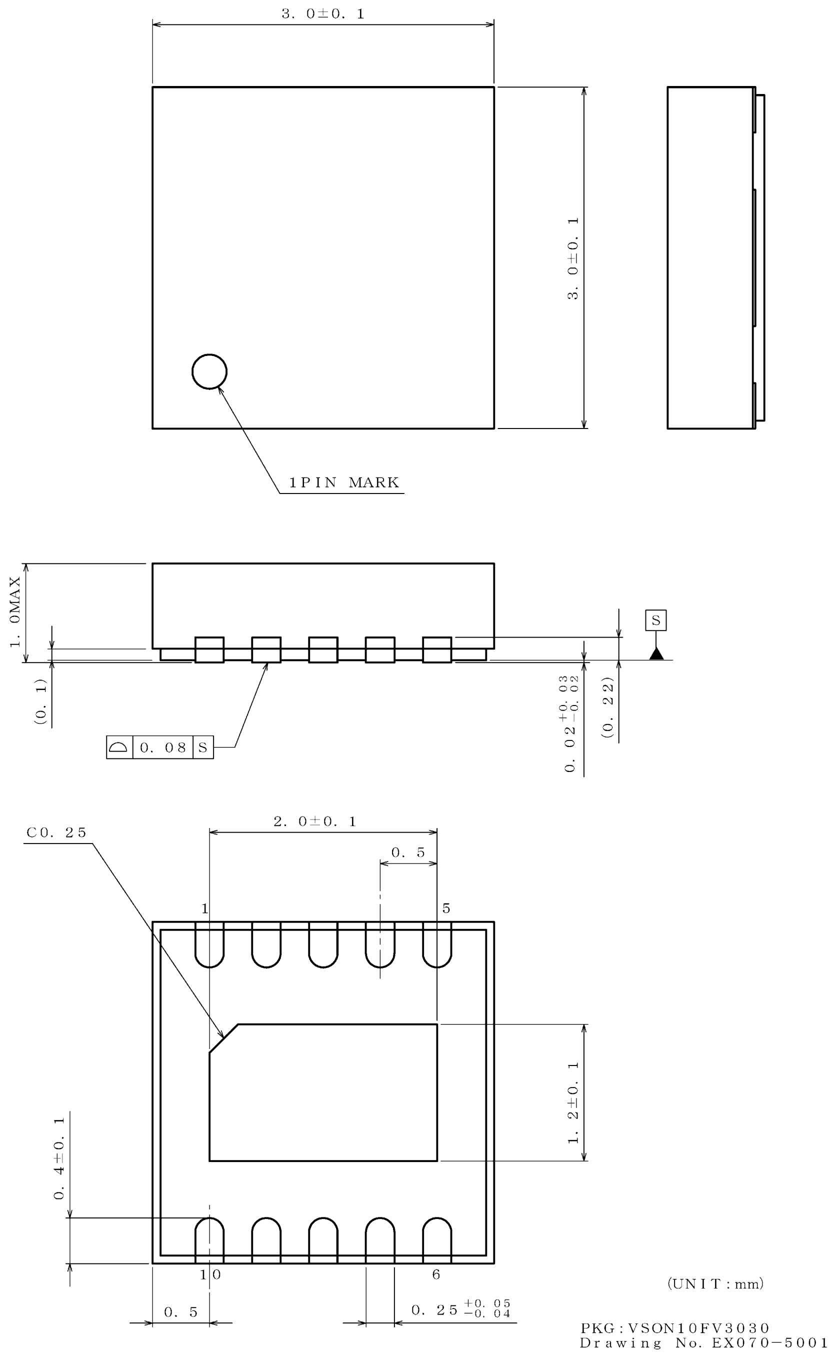
Marking Diagram

VSON10FV3030 (TOP VIEW)



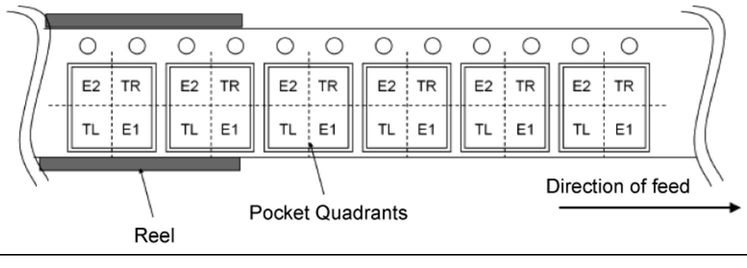
Physical Dimension and Packing Information

Package Name	VSON10FV3030



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
12.Sep.2018	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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