Controller type switching regulator with high frequency, high accuracy external FET

Automatically Controlled Buck-Boost Switching Regulator

BD9035AEFV-C

General Description

The BD9035AEFV-C is a buck-boost switching controller with a high withstand voltage and a wide input range (VIN=3.8~30V) capable of generating buck-boost output with one inductor. The IC has a ±7% high accuracy switching frequency for the entire operating temperature range (Ta=-40°C~+125°C). Because of the automatically controlled buck-boost system the BD9035AEFV-C also has a higher efficiency compared to regular switching regulators employing Sepic or H-Bridge systems.

Features

- Power supply voltage: 40V (maximum rating)
- Automatically controlled buck-boost system.
- ±7% High accuracy switching frequency (Ta=-40°C~+125°C).
- PLL circuit for external synchronization: 100kHz~600kHz
- Two-stage overcurrent protection through one external resistor
- Various protection functions
- Undervoltage, overvoltage output detection circuit & constant output monitor pin (PGOOD)
- AEC-Q100 Qualified

Applications

- Automotive micro controller, car audio and navigation system, LCD TV, PDP TV, DVD, PC, etc.

Key Specifications

- Input voltage range: 3.8V to 30V (Initial startup is over 4.5V)
- Oscillation frequency: 100kHz to 600kHz
- Reference voltage accuracy: 0.8V±1.5%
- Circuit current at shutdown: 0μA (Typ.)
- Operating temperature range: -40℃ to +125℃

Package

	W(Typ.) x D(Typ.) x H(Max.)
HTSSOP-B24	7.80mm x 7.60mm x 1.00mm

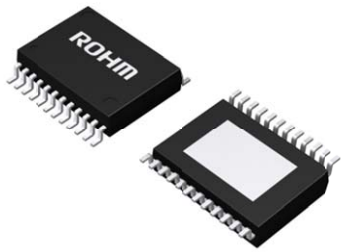


Figure 1. HTSSOP-B24

Typical Application Circuit

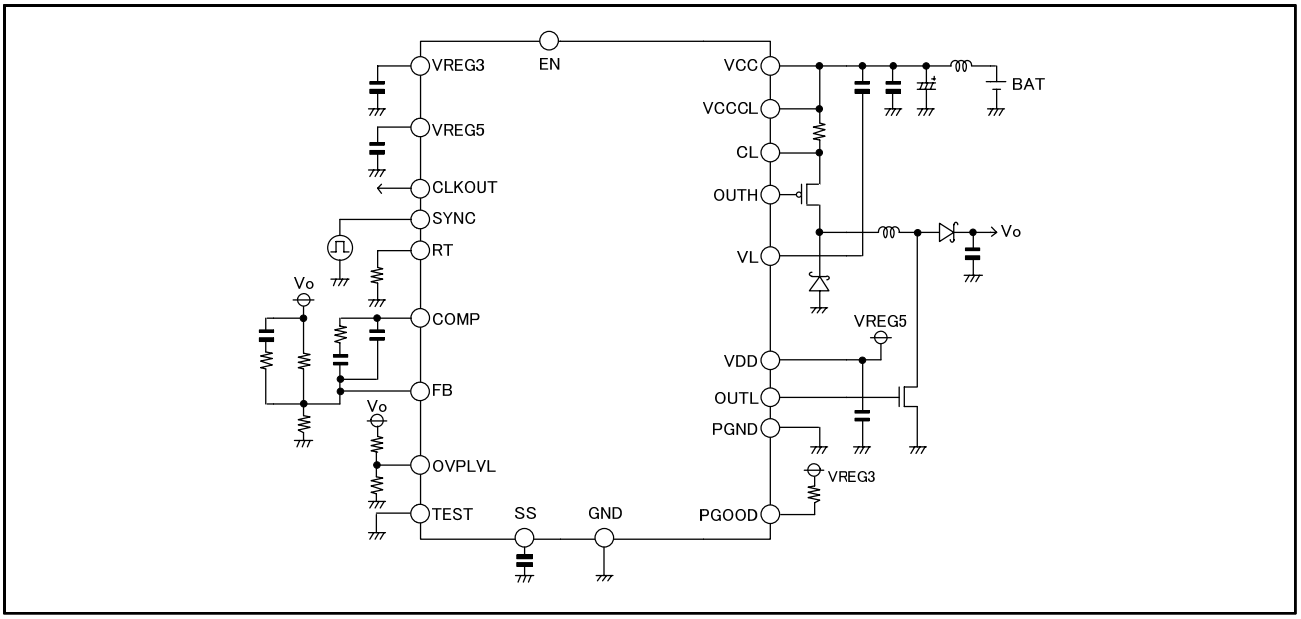


Figure 2. Typical application circuit diagram

Pin Configuration

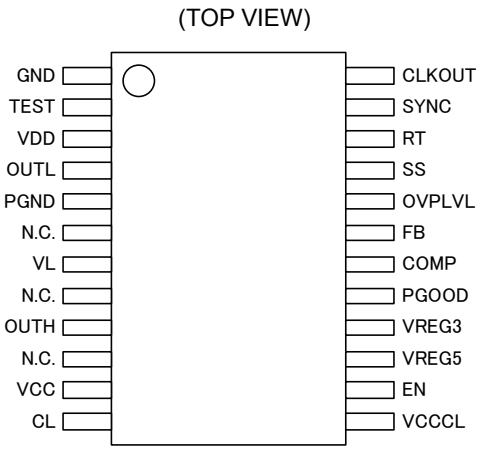


Figure 3. Pin configuration

Pin Description

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground pin	13	VCCCL	Overcurrent detection setting pin 1
2	TEST	Test pin	14	EN	Output ON/OFF pin
3	VDD	NchFET drive supply pin	15	VREG5	5V internal power supply pin
4	OUTL	NchFET drive pin	16	VREG3	3.5V internal power supply pin
5	PGND	Power GND pin	17	PGOOD	Power good output pin
6	N.C.	Not connected	18	COMP	Error-amp output pin
7	VL	PchFET gate clamp pin	19	FB	Feedback pin
8	N.C.	Not connected	20	OVPLVL	Overvoltage detection setting pin
9	OUTH	PchFET drive pin	21	SS	Soft start time setting pin
10	N.C.	Not connected	22	RT	Frequency setting pin
11	VCC	Power supply pin	23	SYNC	External synchronization pulse input pin
12	CL	Overcurrent detection setting pin 2	24	CLKOUT	Clock pulse output pin

Block Diagram

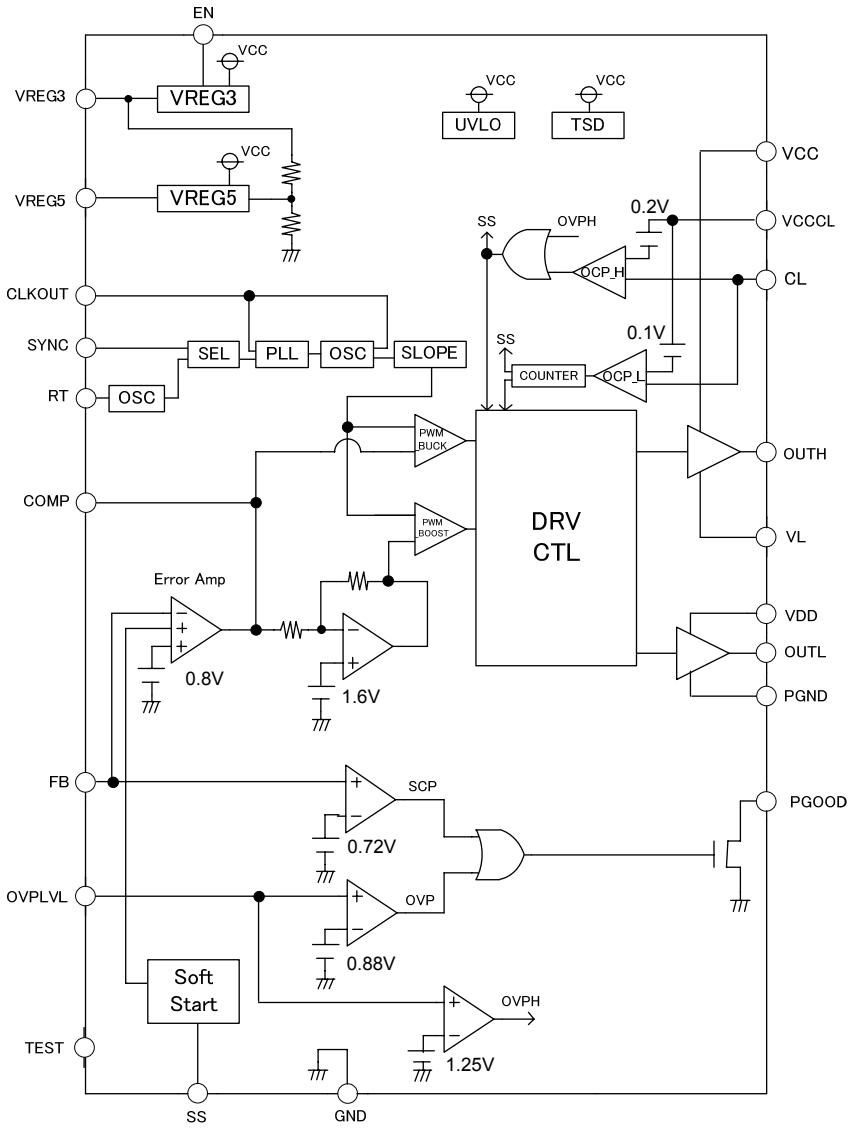


Figure 4. Block diagram

Description of Blocks

■Error amplifier (Error Amp)

The error amplifier compares the output feedback voltage to the 0.8V reference voltage and provides the comparison result as COMP voltage, which is used to determine the switching duty. Because at startup, the soft start is triggered based on the soft start voltage, the COMP voltage is limited by the soft start voltage.

■Oscillator (OSC)

The oscillation frequency is determined by the RT resistance and the current generated by the pin voltage. The oscillation frequency can be set in the range of 100 kHz to 600 kHz.

■SLOPE

The slope block uses the clock produced by the oscillator to generate a sawtooth wave and sends this wave to the PWM comparator.

■PWM_BUCK

The PWM_BUCK comparator determines the switching duty by comparing the output COMP voltage of the error amp, with the triangular wave of the SLOPE block.

■PWM_BOOST

The PWM_BOOST comparator determines the switching duty by comparing the output voltage of the inverting amplifier, with the triangular wave of the SLOPE block.

■PGOOD pin

1) Output overvoltage detection (OVP)
   The PGOOD pin monitors the OVPLVL voltage and outputs “H” if the voltage is less than 0.88V (Typ.) and outputs “L” if the voltage exceeds 0.88V (Typ.).
2) Output undervoltage detection (SCP)
   The PGOOD pin monitors the output voltage (FB) and outputs “H” if the output voltage exceeds 90% (Typ.) and outputs “L” if the voltage is less than 90% (Typ.).
   Because the PGOOD pin is an open drain output, a pull up resistor should be connected when the pin is used.

■Overcurrent protection function (OCP_L, OCP_H)

The overcurrent protection has a two-stage system with a control method as shown below.

1) OCP low level operations
   In case the inter VCCL-CL pin voltage exceeds 100mV (Typ.) the chip goes into OCP low level operations and the OUTH and OUTL pin pulses are limited. Also, in case this pulse limitation status continues for 256clk in a situation where the FB pin voltage drops below the undervoltage detection voltage VLOW, the soft start pin capacitor is discharged and the output is turned OFF for 8192clk.
   During the 8192clk in which the output is turned OFF the logic of OUTH and OUTL pin changes as follows; OUTH=H and OUTL=H. After the 8192clk the chip returns to normal operations and the soft start pin is recharged.
2) OCP high level operations
   In case the inter VCCL-CL pin voltage exceeds 200mV (Typ.), the chip goes into OCP high level operations, the soft start pin capacitor is discharged and the output is turned OFF for 8192clk. During the 8192clk in which the output is turned OFF the logic of OUTH and OUTL pin changes as follows; OUTH=H and OUTL=H. After the 8192clk the chip returns to normal operations and the soft start pin is recharged.

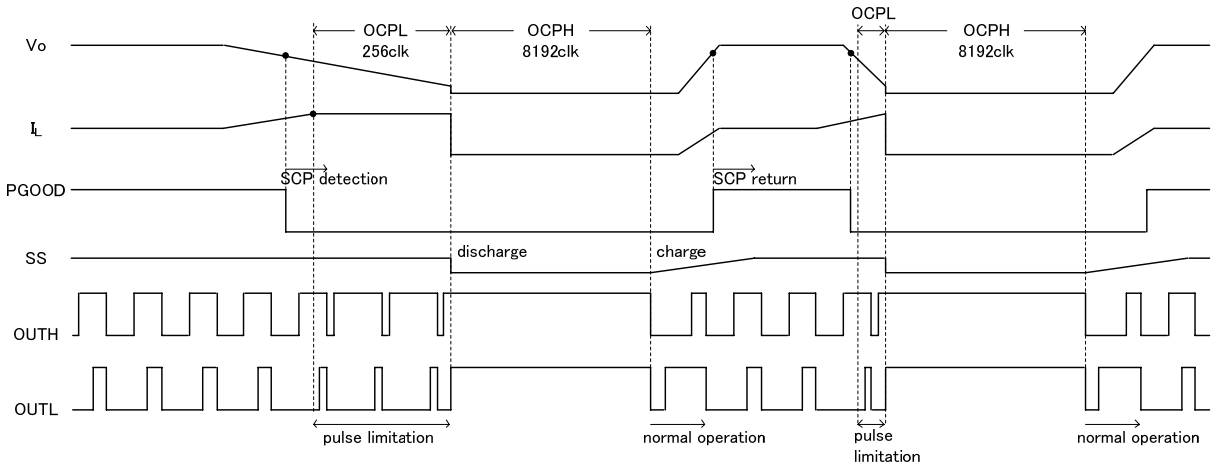


Figure 5. Timing chart of two-stage overcurrent protection operations

■Overvoltage protection function (OVPH)

In case the OVPLVL pin voltage exceeds 1.25V (Typ.), the soft start pin capacitor is discharged and the output is turned OFF for 8192clk. During the 8192clk in which the output is turned OFF the logic of OUTH and OUTL pin changes as follows; OUTH=H and OUTL=H. After the 8192clk the chip returns to normal operations and the soft start pin is recharged.

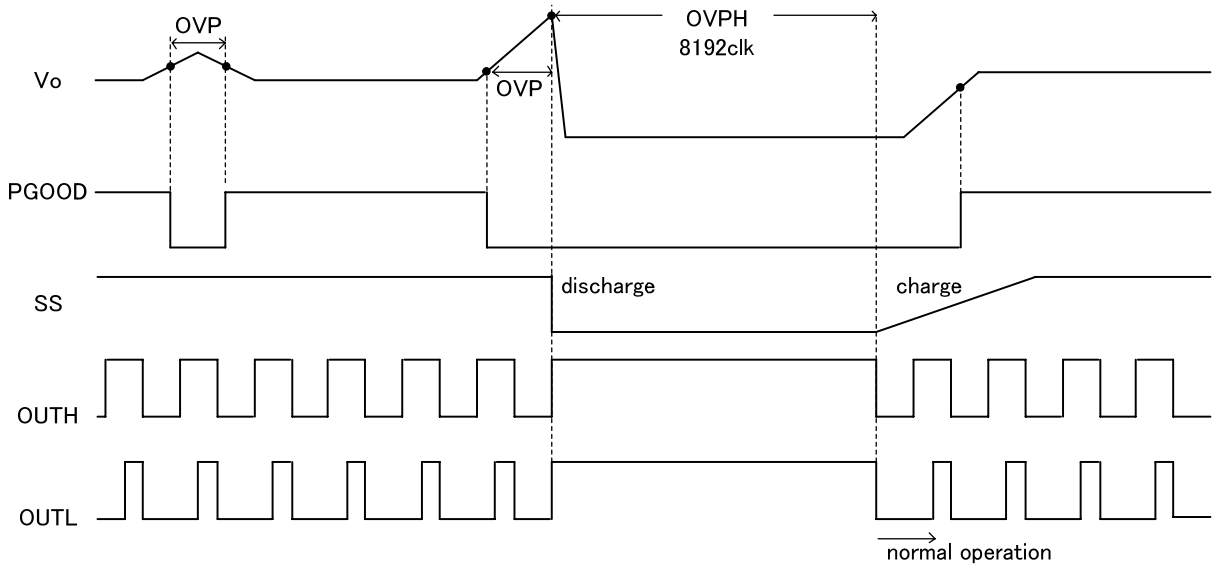


Figure 6. Overvoltage protection timing chart

■Soft Start

The soft start block provides a function to prevent the overshoot of the output voltage Vo through gradually increasing the normal rotation input of the error amplifier when power supply turns ON to gradually increase the switching duty. The soft start time is set by the charge capacity of the soft start pin capacitor. (Refer to P. 17)

■Low voltage lockout circuit (UVLO)

This is a Low Voltage Error Prevention Circuit.
This prevents internal circuit error during increase of Power supply Voltage and during decline of Power supply Voltage.
If the VCC drops below 3.4V (typ.), the UVLO is activated and the circuit is shut down.

■Thermal protection circuit (TSD)

In order to prevent thermal destruction/thermal runaway of this IC, the TSD block will turn OFF the output when the chip temperature reaches approximately 150℃ or more. When the chip temperature falls to a specified level from thermal shutdown detection, the output will reset. However, since the TSD is designed to protect the IC, the margin for thermal design must be provided to guarantee that the chip junction temperature should be less than 150°C, which is the thermal shutdown detection temperature.

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
VCC voltage	VCC	40 *1	V
EN voltage	EN	VCC	V
VCCCL voltage	VCCCL	VCC	V
CL voltage	VCL	VCCCL	V
Inter VCC-VL voltage	VCC-VL	13	V
VDD voltage	VDD	VCC or 7 (whichever is lower)	V
VREG3 voltage	VREG3	VCC or 7 (whichever is lower)	V
VREG5 voltage	VREG5	VCC or 7 (whichever is lower)	V
SS voltage	SS	VREG3	V
FB voltage	FB	VREG3	V
OVPLVL voltage	OVPLVL	VREG3	V
COMP voltage	COMP	VREG3	V
SYNC voltage	SYNC	VREG3	V
PGOOD voltage	PGOOD	VREG3	V
Power dissipation *2	Pd	4.00	W
Operating temperature range	Topr	-40～+125	ºC
Storage temperature range	Tstg	-55～+150	ºC
Junction temperature	Tjmax	150	ºC

*1 Pd and ASO should not be exceeded.
*2 If mounted on a standard ROHM 4 layer PCB (copper foil area: 70x70mm) (Standard ROHM PCB size: 70x70x1.6mm)
Reduce by 32mW for every 1℃ increase. (Above 25℃)

Recommended Operating Rating(Ta=-40℃～125℃)

Parameter	Symbol	Maximum ratings		Unit
		Min.	Max.	
Voltage power supply	VCC	3.8 *3	30	V
Oscillation frequency	FOSC	100	600	kHz
External synchronization frequency	FSYNC	100	600	kHz

*3 Initial startup is over 4.5V

Electrical Characteristic (unless otherwise specified: Ta=-40~125°C, VCC=12V, EN=5V)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
【Circuit Current】						
Circuit current	IVCC	-	7	15	mA	
Circuit current at shutdown	IST	-	0	10	μA	EN=0V
【EN】						
EN pin ON threshold voltage	VENON	2.5	-	-	V	
EN pin OFF threshold voltage	VENOFF	-	-	0.5	V	
EN pull down resistance	REN	188	375	750	kΩ	
【VREG3】						
VREG3 output voltage	VVREG3	3.3	3.5	3.7	V	
【VREG5】						
VREG5 output voltage	VVREG5	4.5	5.0	5.4	V	
【UVLO】						
UVLO_VCC detection voltage	VUVLO	3.1	3.4	3.7	V	
UVLO hysteresis voltage	VUVLOHYS	0.4	0.6	0.8	V	
【Error amp】						
FB input bias current	IFB	-	0	-	μA	FB=VFB2
Reference voltage 1	VFB1	0.792	0.800	0.808	V	Ta=25 ºC
Reference voltage 2	VFB2	0.788	0.800	0.812	V	Ta=-40 ºC～+105 ºC
【Soft start】						
Soft start charge current	ISS	5	10	15	μA	SS=0.1V
【Oscillator】						
Oscillation frequency	FOSC	326	350	375	kHz	RT=33kΩ
External synchronization frequency	FSYNC	-	350	-	kHz	SYNC=350kHz
SYNC threshold voltage	VSYNC	0.5	1.8	2.5	V	
SYNC pull down resistance	RSYNC	125	250	500	kΩ	SYNC=3V
SYNC input maximum ON duty	DONMAX	80	-	-	%	
SYNC input minimum ON duty	DONMIN	-	-	20	%	

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
【Driver】						
OUTH pin upper ON resistance	RONHH	-	1.7	-	Ω	
OUTH pin lower ON resistance	RONHL	-	3	-	Ω	
OUTL pin upper ON resistance	RONLH	-	24	-	Ω	
OUTL pin lower ON resistance	RONLL	-	22	-	Ω	
Boost max duty 1	DBSTMAX1	-	92	-	%	f=600kHz
Boost max duty 2	DBSTMAX2	60	-	-	%	VCC=3.8V
【OCP】						
Overcurrent detection CL pin voltage 1	VCL1	86	100	114	mV	Inter VCC-VL voltage
Overcurrent detection CL pin voltage 2	VCL2	172	200	228	mV	Inter VCC-VL voltage
【PGOOD】						
PGOOD pin ON resistance	RPG	-	0.1	0.4	kΩ	PGOOD=0.15V,FB=0V
PGOOD pin leak current	IPG	-	0	1	μA	PGOOD=3.3V,FB=0.8V, Ta=-40~+105 ºC
Output overvoltage detection voltage	VOVER	0.85	0.88	0.91	V	OVPLVL voltage
Output undervoltage detection voltage	VLOW	0.70	0.72	0.74	V	FB voltage

Typical Performance Curves (unless otherwise specified: Ta=25°C)

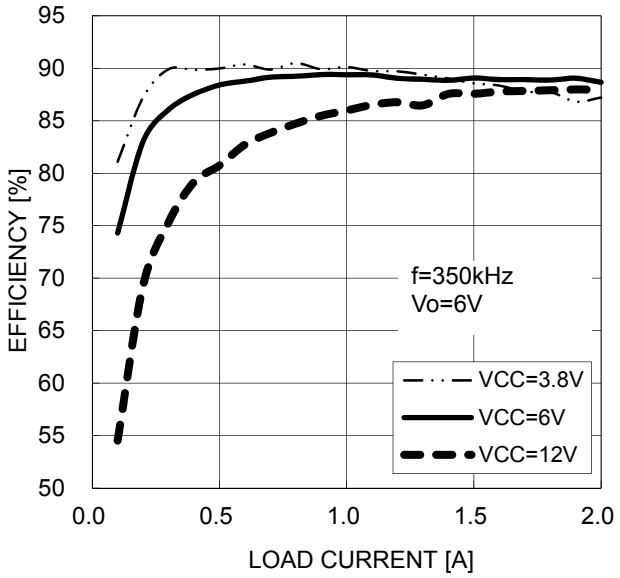


Figure 7. Efficiency
(Vo=6V, fosc=350 kHz)

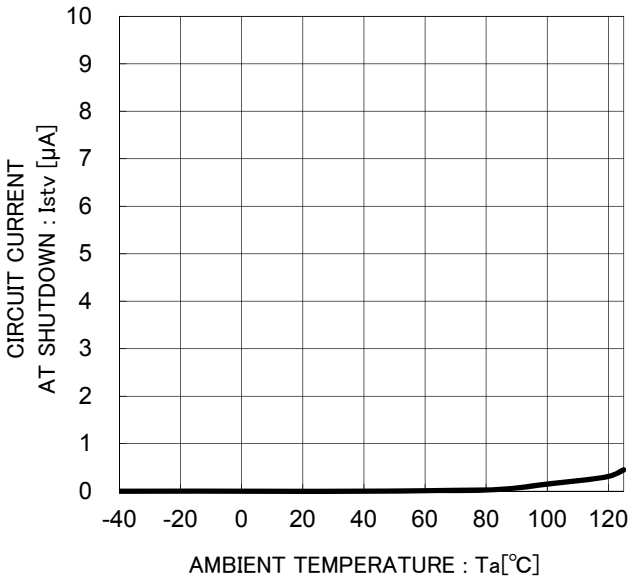


Figure 8. Circuit current at shutdown vs. temperature characteristics

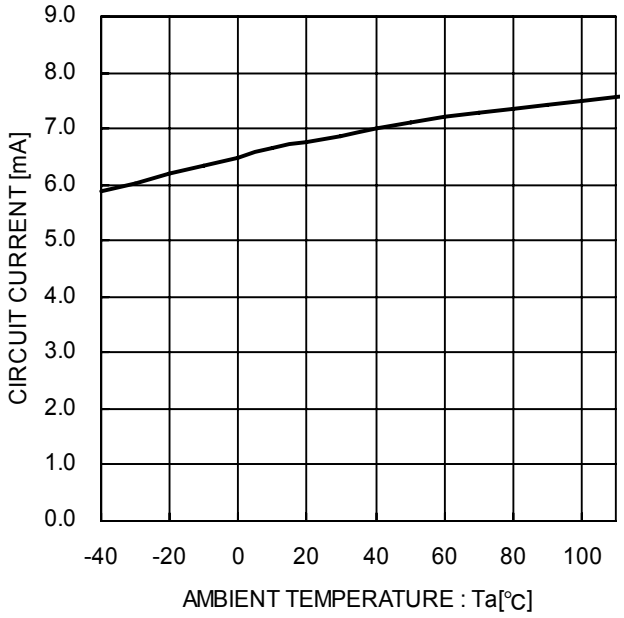


Figure 9. Circuit current vs. temperature characteristics

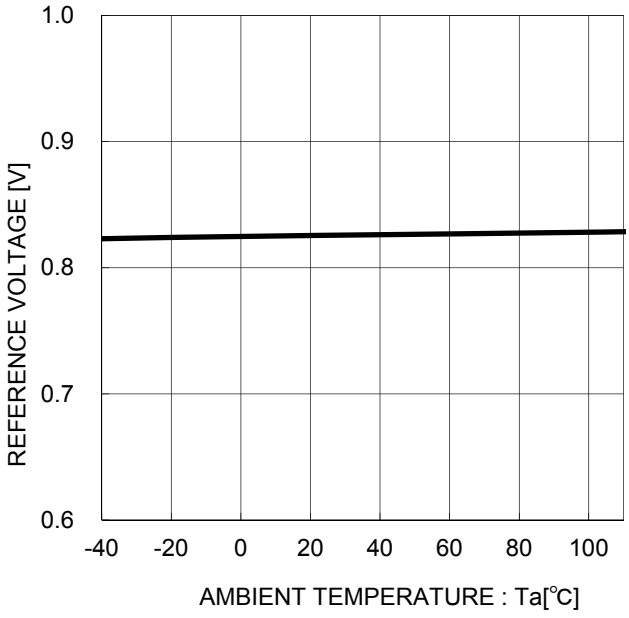


Figure 10. Reference voltage vs. temperature characteristics

Typical Performance Curves (unless otherwise specified: Ta=25°C)

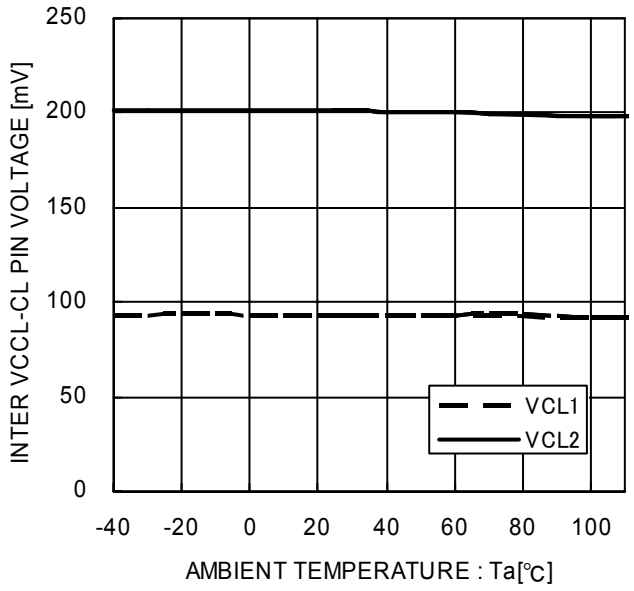


Figure 11. Overcurrent detection CL pin voltage vs. temperature characteristics

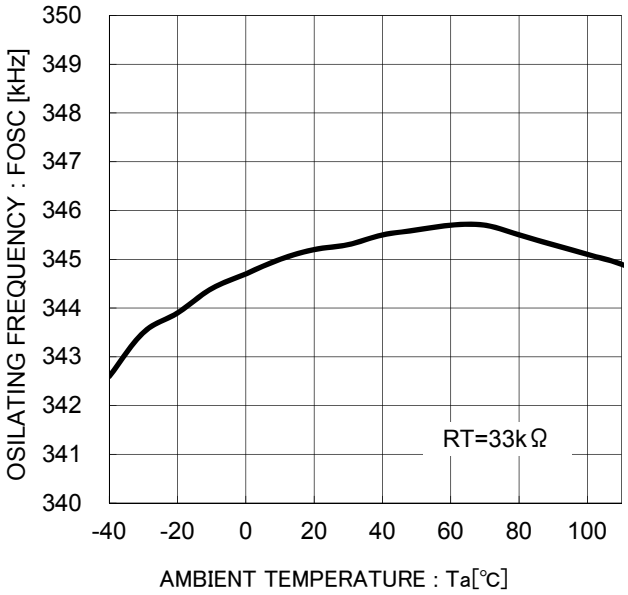


Figure 12. Oscillating frequency vs. temperature characteristics

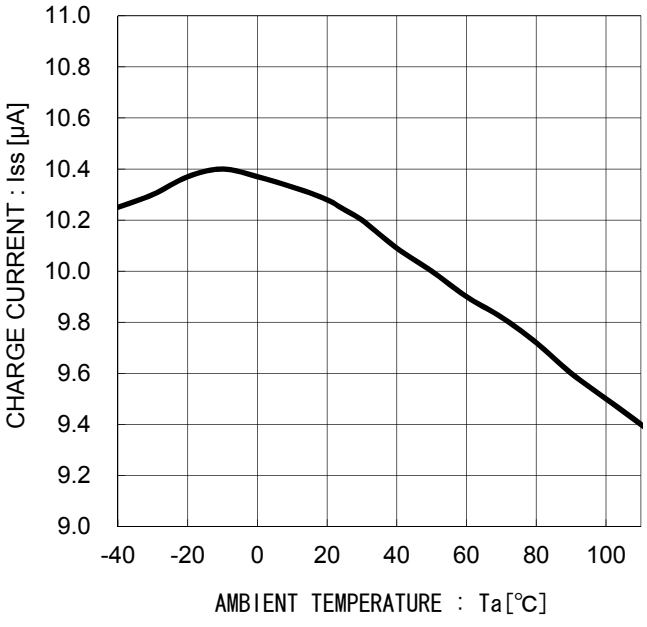


Figure 13. Soft start charge current vs. temperature characteristics

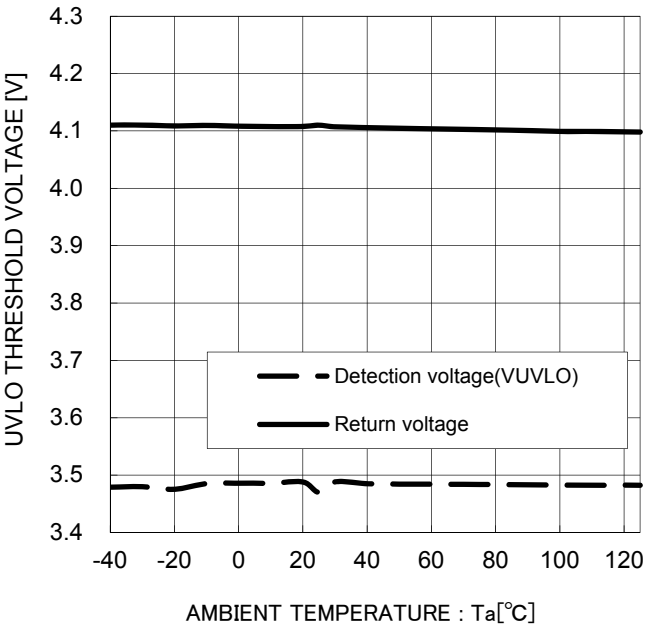


Figure 14. UVLO detection/return voltage vs. temperature characteristics

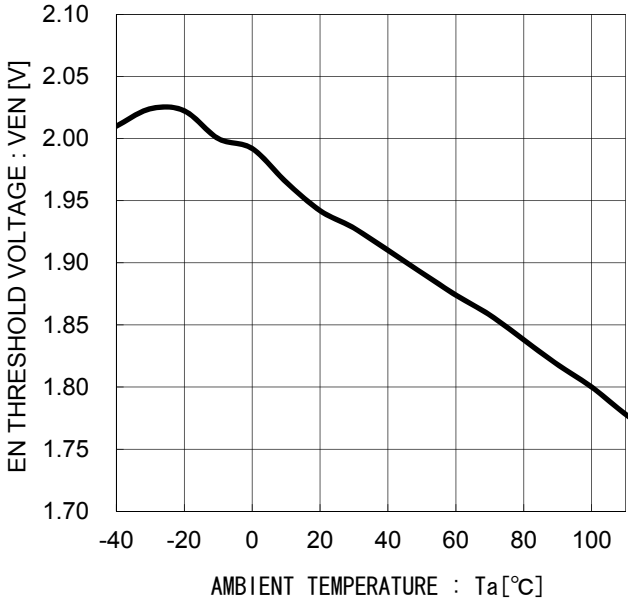


Figure 15. EN threshold voltage vs. temperature characteristics

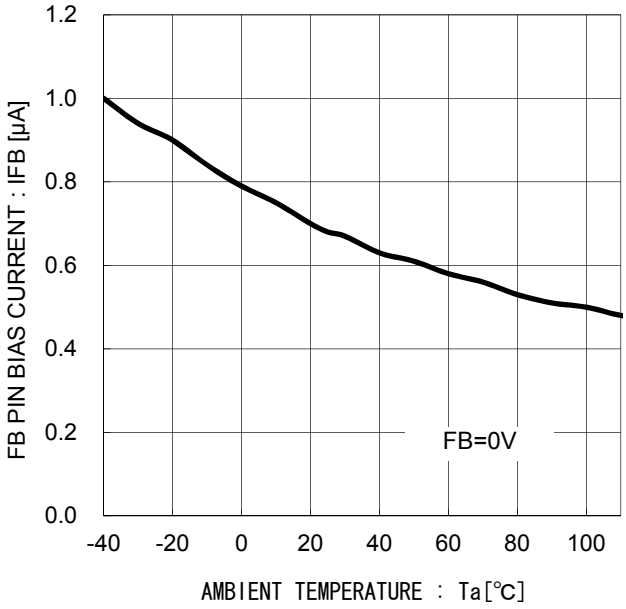


Figure 16. FB pin bias current vs. temperature characteristics

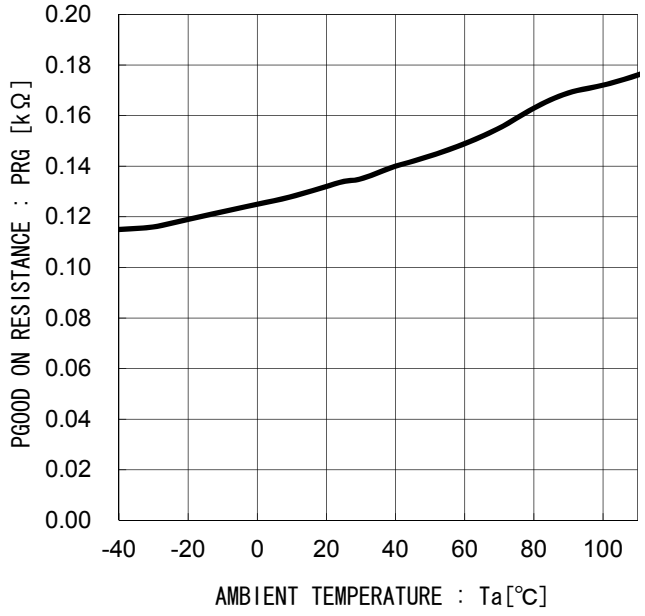


Figure 17. PGOOD pin ON resistance vs. temperature characteristics

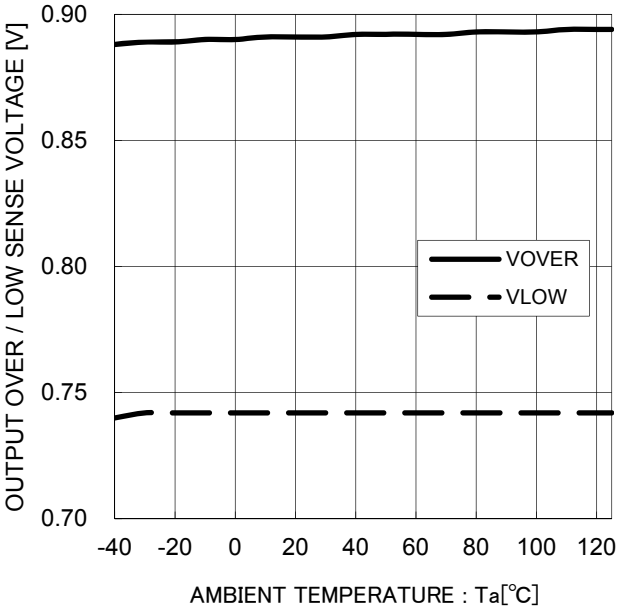


Figure 18. Output overvoltage / undervoltage detection voltage vs. temperature characteristics

Application Example

N.B. There are many factors (PCB, output current, etc.) that can affect the DCDC characteristics.
Please verify and confirm using practical applications.

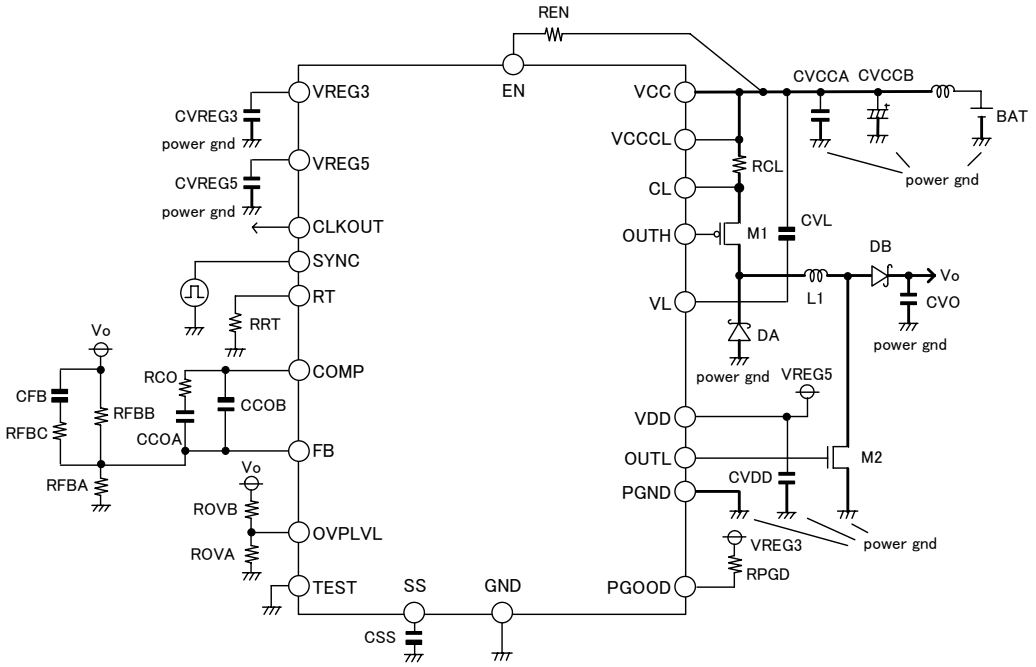
N.B. No connection (N.C) pin should not be connected to any other lines.

N.B. Be sure to connect the TEST pin to ground.

N.B. In case the external synchronization function is not used, be sure to connect SYNC pin to ground.

N.B. This IC is not designed to operate as BOOST or BUCK application with single MOSFET. Be sure to use both M1 & M2.

N.B. If EN pin is connected to VCC pin, please insert REN 150kΩ between the pins.



An example of parts values:
In case of VCC=3.8～30V, Vo=5V, Io=0～3A, 350kHz

Parts No.	Value	Parts No.	Value
DA	RB225NS-40	L1	10μ (TDK SLF series)
DB	RB225NS-40	CVO	100μ(16V)
M1	RSJ250P10	RCO	2.2k
M2	RSJ450N04	RFBA	15.6k
RCL	13.33m	RFBB	82k
REN	150k	RFBC	330
RRT	33k	ROVA	15.6k
RPGD	47k	ROVB	82k
CVDD	1μ (10V)	CCOA	0.015μ (10V)
CVL	0.1μ (50V)	CCOB	100p (10V)
CVCCA	2.2μ (50V)	CFB	680p (10V)
CVCCB	220μ (50V)		
CVREG3	0.47μ (10V)		
CVREG5	0.47μ (10V)		
CSS	0.047μ (10V)		

Directions for pattern layout of PCB

1) Design the wirings shown by heavy lines as short as possible.
2) Place the input ceramic capacitor CVCCA, CVCCB as close to the M1 as possible.
3) Place the RRT as close to the GND pin as possible.
4) Place the RFBA and RFBB as close to the FB pin as possible and provide the shortest wiring from the FB pin.
5) Place the ROVA and ROVB as close to the OVPLVL pin as possible and provide the shortest wiring from the OVPLVL pin.
6) Place the RFBA, RFBB, ROVA, and ROVB as far away from the L as possible.
7) Separate power GND and signal GND so that SW noise doesn't affect the signal GND.

The control of automatic buck-boost system

The following shows the switching state of three control modes.

(1) Buck mode (VCC>>Vo)

In case the input voltage is high compared to the output voltage, the chip will go into buck mode, resulting OUTH to repeatedly switch between H and L and that the OUTL will go to L (=OFF). This operation is the same as that of standard step-down switching regulators.
Below, the OUTH and OUTL waveforms are shown.

$$VCC \times Dpon = Vo \qquad \text{(eq.1)}$$

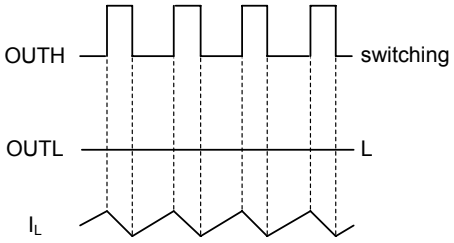


Figure 19.

(2) Buck-Boost mode (VCC≒Vo)

In case the input voltage is close to the output voltage, the chip will go into buck-boost mode, resulting both the OUTH and OUTL to repeatedly switch between H and L. Concerning the OUTH, OUTL timing, the chip internally controls where the following sequence is upheld; when OUTH: H → L, OUTL: H → L.
Shown below are the OUTH and OUTL waveforms.

① VCC > Vo

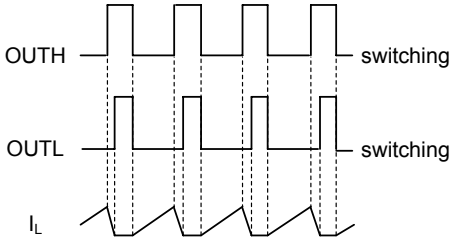


Figure 20.

② VCC < Vo

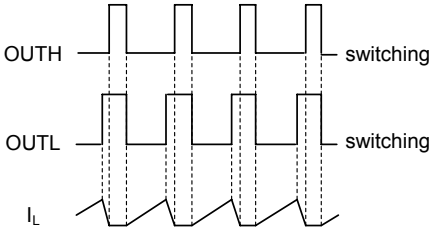


Figure 21.

※The timing excludes the SW delay

The relationship between ON duty of PMOS (Dpon), ON duty of NMOS (Dnon), VCC and Vo is shown in the following equation.

$$VCC \times Dpon / (1-Dnon) = Vo \qquad \text{(eq.2)}$$

The formula for calculation of Dpon and Dnon are shown in P.15.

(3) Boost mode (VCC<<Vo)

In case the input voltage is low compared to the output voltage, the chip will go into boost mode, resulting OUTH to go to L (=ON) and OUTL will repeatedly switch between H and L. This operation is the same as that of standard step-up switching regulators.
Below, the OUTH and OUTL waveforms are shown

$$Vo \times (1-Dnon) = VCC \qquad \text{(eq.3)}$$

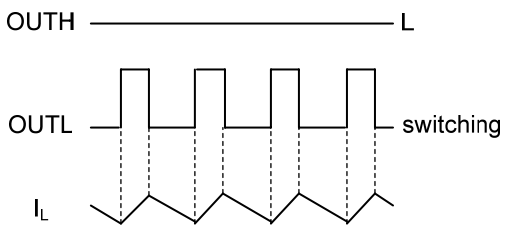


Figure 22.

(4) Mode transfer voltage and duty control

Vo, the gain of the inverting amplifier and the cross duty determines the transfer voltage at buck to buck-boost mode and buck-boost to boost mode. The general description is shown below.

The duty of OUTH is controlled by output of error amp (COMP) and SLOPE voltage.
Also, OUTL duty is controlled by the output voltage of the inverting amplifier in chip (BOOSTCOMP) and SLOPE voltage.
In case VCC = Vo, because COMP voltage becomes equal to BOOSTCOMP voltage, OUTH and OUTL switch simultaneously.

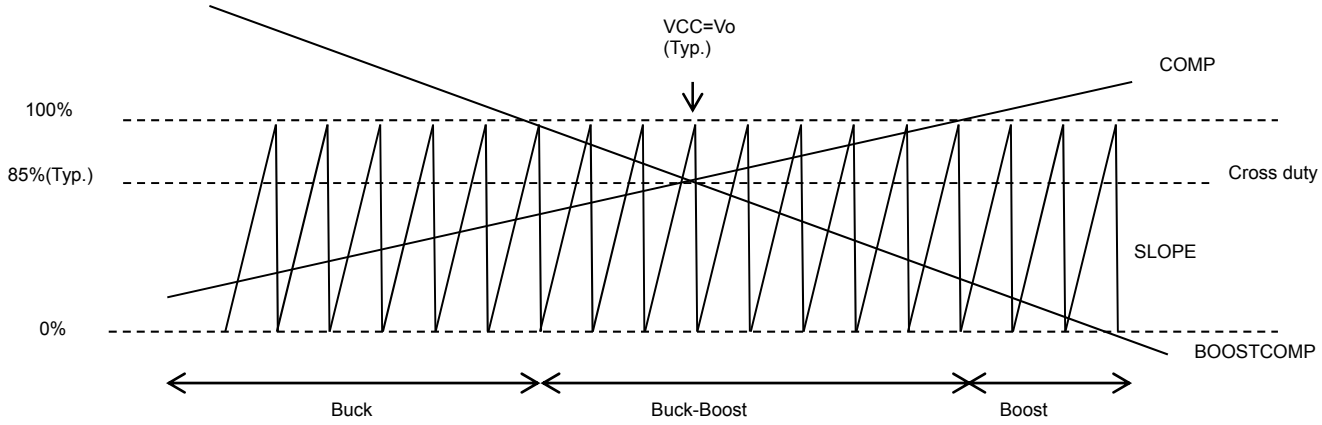


Figure 23. Buck-Boost operation controlled by COMP, BOOSTCOMP and SLOPE voltage

ON duty of PMOS in this condition is called the cross duty (Dx = 0.85, Typ.). Dpon and Dnon can be calculated by the following equation, assuming the gain of the inverting amplifier as A (1.5, Typ.).

$$Dnon = 1 - Dx + A(Dpon - Dx) \quad \text{(eq.4)}$$
$$= 1.5Dpon - 1.125 \quad (※)$$

From eq.3, eq.4 and Dpon=1, the input voltage at transition between buck-boost and boost mode is calculated by following;

$$VCC = \{Dx - A(1 - Dx)\} Vo$$
$$= 0.625 \times Vo \quad (※)$$

Also, from eq.1, eq.4 and Dnon=1, the input voltage at transition between buck-boost and buck mode is calculated by following;

$$VCC = Vo \times A / \{(1 + A)Dx - 1\}$$
$$= 1.333 \times Vo \quad (※)$$

※in case of A=1.5(Typ.) and Dx=0.85(Typ.)

Be sure to confirm Dx and A values under the actual application because these parameters vary depending on conditions of use and parts.
Dx varies with oscillating frequency shown in Fig.24.
In addition, 'A' value can be calculated by $\Delta dnon / \Delta dpon$.

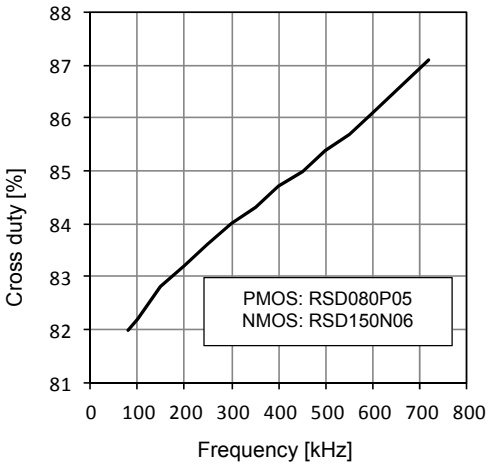


Figure 24. Cross duty vs. frequency characteristics

Selection of Components Externally Connected

(1)Setting the output L value

The coil value significantly influences the output ripple current. Thus, as seen in bellow, the larger the coil, and the higher the switching frequency, the lower the drop in ripple current. The optimal output ripple current setting is 30% of maximum current.

Buck mode	Buck-Boost mode		Boost mode
	VCC > Vo	VCC < Vo	
$\triangle I_L = \frac{(VCC-Vo) \times Vo}{L \times VCC \times f}$	$\triangle I_L = \frac{(VCC-Vo) \times Dpon}{L \times f}$	$\triangle I_L = \frac{(Vo-VCC) \times Dnoff}{L \times f}$	$\triangle I_L = \frac{(Vo-VCC) \times VCC}{L \times VOUT \times f}$
$\overline{I_L} = Io$	$\overline{I_L} = \frac{Io}{Dnoff}$		

#

ΔI_L : ripple current, $\overline{I_L}$: average coil current, f : oscillating frequency

Dpon : PMOS ON duty = Vo × Dx (1+A) / (VCC+A × Vo)

=2.13 × Vo / (Vcc+1.5 × Vo) (Typ.)

Dnoff : NMOS ON duty = (1+A) × Dx – A × Dpon

=2.13 – 1.5 × Dpon (Typ.)

An output current in excess of the coil current rating will cause magnetic saturation to the coil and decrease efficiency.

The following equation shows the peak current I_{LMAX} assuming the efficiency as η.

It is recommended to provide a sufficient margin to ensure that the peak current does not exceed the coil current rating.

$$I_{LMAX} = \frac{1}{\eta}\left(\overline{I_L} + \frac{\Delta I_L}{2}\right)$$

Use low resistance (DCR, ACR) coils to minimize coil loss and increase efficiency.

(2)Setting the output Co value

Select output capacitor with consideration to the ripple voltage ($\triangle$Vp-p) tolerance. The following equation is used to determine the output ripple voltage.

Buck mode	Boost mode
$\triangle V_{P-P} = \triangle I_L \times R_{ESR} + \frac{\triangle I_L}{8Co} \times \frac{1}{f}$	$\triangle V_{P-P} = \triangle I_L \times R_{ESR} + \frac{Io}{Co} \times \frac{Vo-VCC}{Vo} \times \frac{1}{f}$

The output Co setting needs to be kept within the allowable ripple voltage range.

Allow for a sufficient voltage output margin in establishing the capacitor rating. Low ESR capacitors provide a lower output ripple voltage. Because the output startup time needs to be set within the soft start time, please take the conditions described in the flowing equation also in consideration when selecting the value of the output capacitor.

$$Co \leqq \frac{TSS \times (Ilimit - Io)}{Vo}$$

TSS : Soft start time

Ilimit : Over current detection value

N.B. Non-optimal capacitance values may cause startup problems. Especially in cases of extremely large capacitance values, the possibility exists that the inrush current at startup will activate the overcurrent protection, thus not starting the output. Therefore, verification and conformation with the actual application is recommended.

(3)Setting the input capacitor (Cin)

The input capacitor serves to lower the output impedance of the power source connected to the input pin (VCC, VCCCL).
Increased power supply output impedance can cause input voltage (VCC) instability and may negatively impact oscillation and ripple rejection characteristics. Therefore, it is necessary to place the input capacitor in close proximity to the MOSFET and PGND pin.
Select a low-ESR capacitor with little change in capacitance due to temperature change and with a sufficiently large ripple current.
The ripple current IRMS is determined by the following equation:

$$IRMS = Io \times \frac{\sqrt{Vo\ (VCC - Vo)}}{VCC} \quad [A]$$

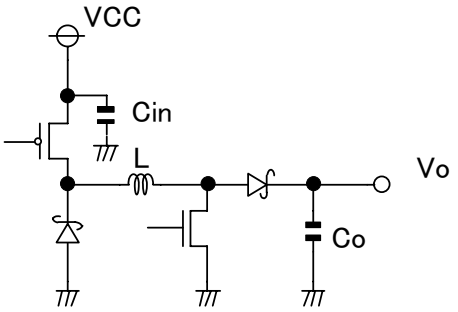


Figure 25.

Also, be certain to ascertain the operating temperature, load range and MOSFET conditions for the application in which the capacitor will be used, since capacitor performance is heavily dependent on the application's input power characteristics, substrate wiring and MOSFET gate drain capacity.

(4)Setting the output voltage

The output voltage is determined by the equation below. Select a combination of R1 and R2 to obtain the required voltage. Note that a small resistance value leads to a drop in power efficiency and that a large resistance value leads, due to the error amp output drain current to an increase of the offset voltage.

$$Vo = 0.8 \times \frac{RFBA + RFBB}{RFBA}$$

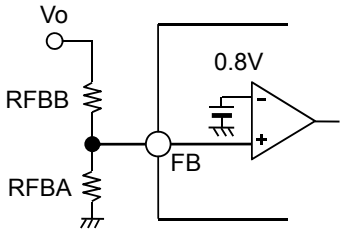


Figure 26.

(5)Setting the oscillation frequency

The internal oscillation frequency setting is possible with the corresponding value of resistor connected to RT pin.
The setting range is 100kHz to 600kHz. The correlation between the resistance value and the oscillation frequency is shown in the table below.
Settings outside of this range can lead to a switching stop and consequentially operations cannot be guaranteed.

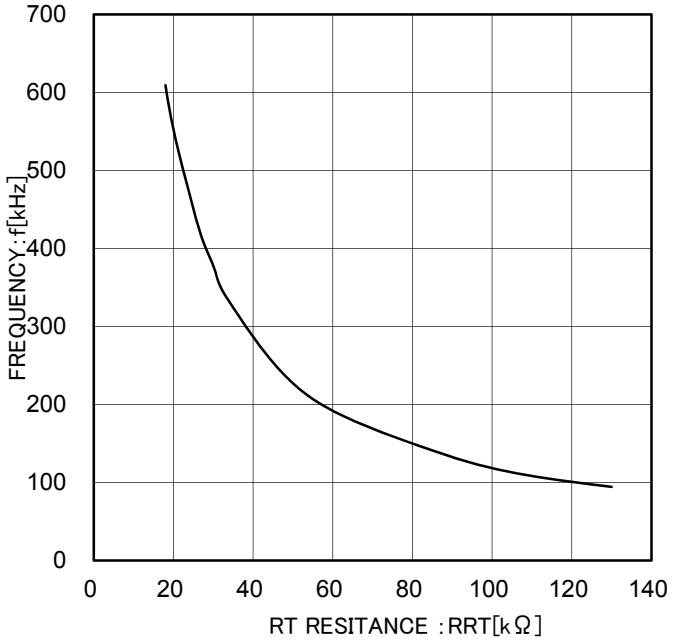


Figure 27. RT resistance vs. oscillation frequency

RT resistance	Oscillation frequency
18.7kΩ	600kHz
20kΩ	550kHz
22.5 kΩ	500kHz
24kΩ	470kHz
27kΩ	424kHz
28.5kΩ	400kHz
30kΩ	384kHz
33kΩ	350kHz
47kΩ	250kHz
62kΩ	192kHz
91kΩ	133kHz
120kΩ	100kHz

(6)Setting the soft start time

The soft start function is necessary to prevent inrush of coil current and output voltage overshoot at startup. The figure below shows the relation between soft start delay time and capacitance, which can be calculated by using the equation to the right of the figure.

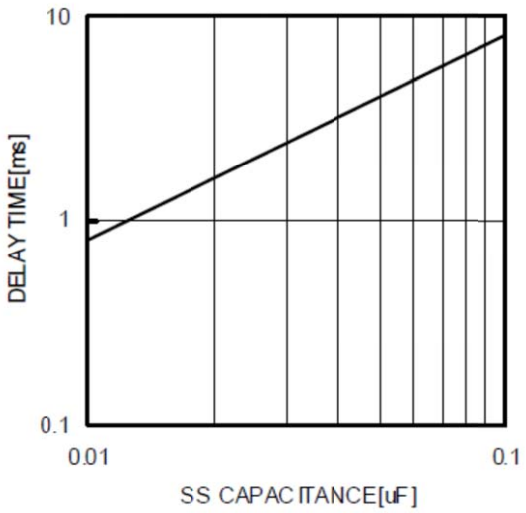


Figure 28. Soft Start capacitance vs. delay time

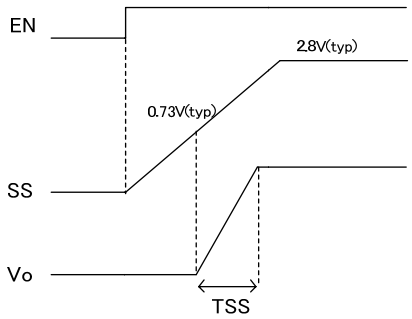


Figure 29. Soft start time TSS

$$TSS = \frac{0.8\ [V]\ (Typ.) \times CSS\ [\mu F]}{ISS\ [\mu A]\ (Typ.:10\mu A)}\ [sec]$$

Capacitance values between 0.01µF and 0.1µF are recommended. There is a possibility that an overshoot is generated in the output due to the phase constant, output capacitance, etc. Therefore, verification and confirmation with the actual application is recommended. Use high accuracy components (e.g. x5R) when implementing sequential startups involving other power sources.

(7)MOSFET selection

- PchMOS used for step-down FET
  - o V_{DS} maximum rating > V_{CC}
  - o V_{GS} maximum rating > Lower value of 13V or VCC

    N.B. The voltage between VCC-VL is kept at 10.3V(Typ.), 13V(Max.).
  - o Allowable current > Coil peak current I_{LMAX}

    N.B. A value above the overcurrent protection setting is recommended.

    N.B Selecting a low ON resistance is conducive to achieving a high efficiency.

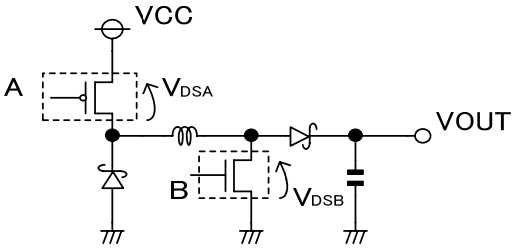


Figure 30

- NchMOS used for step-up FET
  - o V_{DS} maximum rating > V_O
  - o V_{GS} maximum rating > V_{DD}
  - o Allowable current > Coil peak current I_{LMAX}

    N.B. A value above the overcurrent protection setting is recommended.

    N.B Selecting a low ON resistance is conducive to achieving a high efficiency.

(8)Schottky barrier diode selection

- Reverse voltage V_R > VCC
- Allowable current > Coil peak current I_{LMAX}

  N.B. A value above the overcurrent protection setting is recommended.

  N.B. Selecting a diode with a low forward voltage and fast recovery is conducive to achieving a high efficiency.

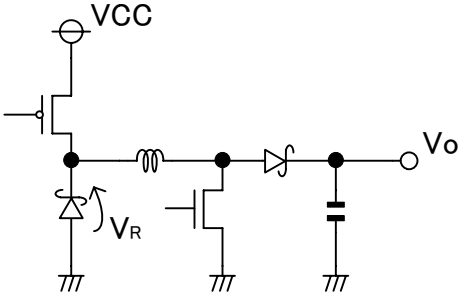


Figure 31

(9) Setting the phase compensation

The phase compensation is set by the capacitors and resistors connected in parallel to COMP and FB pin, and RFBB. At first, it is easier to achieve stability at any power supply and load condition by adjusting values at the lowest voltage power supply and maximum load. Non-optimum values can cause unstable output, like oscillation.

Assuming RFBB>>RFBC and CCOA>>CCOB, each phase compensation elements make phase delay fp1and fp2, phase lead fz1 and fz2, which can be determined by the formulas below.

$$fp1 = \frac{1}{2\pi \times CFB \times RFBC} \qquad fp2 = \frac{1}{2\pi \times CCOB \times RCO}$$

$$fz1 = \frac{1}{2\pi \times CFB \times RFBB} \qquad fz2 = \frac{1}{2\pi \times CCOA \times RCO}$$

This setting is obtained by using a simplified calculation; therefore, adjustment on the actual application may be required. Also as these characteristics are influenced by the substrate layout, load conditions, etc., verification and confirmation with the actual application at time of mass production design is recommended.

(10)Switching pulse jitter and split

Depending on the type of external FET and diode there may be jitter and split in the switching pulse. In case this jitter and split becomes a problem please use the following countermeasures.

- Add a resistor to the OUTH gate of the step-down FET.
- Add a resistor to the OUTL gate of the step-up FET.

However, as these characteristics are influenced by the substrate pattern, used FET, etc., verification and confirmation with the actual application is recommended.

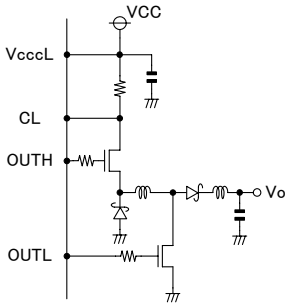


Figure 32.

(11)Measurement of the open loop of the DC/DC converter

To measure the open loop of the DC/DC converter, use the gain phase analyzer or FRA to measure the frequency characteristics.

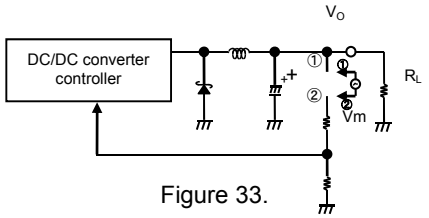


Figure 33.

<Procedure>

1. Check to ensure output causes no oscillation at the maximum load in closed loop.
2. Isolate ① and ② and insert Vm (with amplitude of approximately. 100mVpp).
3. Measure (probe) the oscillation of ① to that of ②.

Thermal derating characteristics

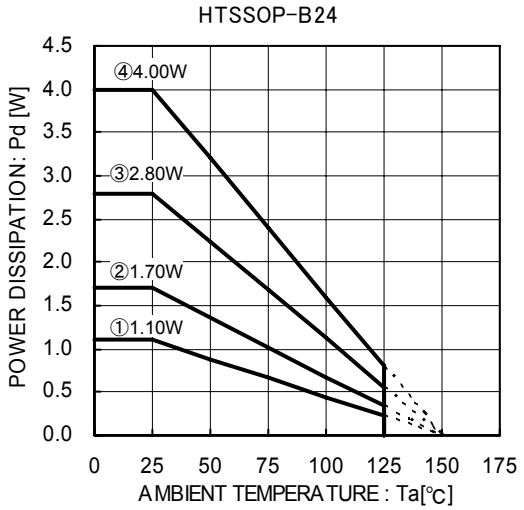


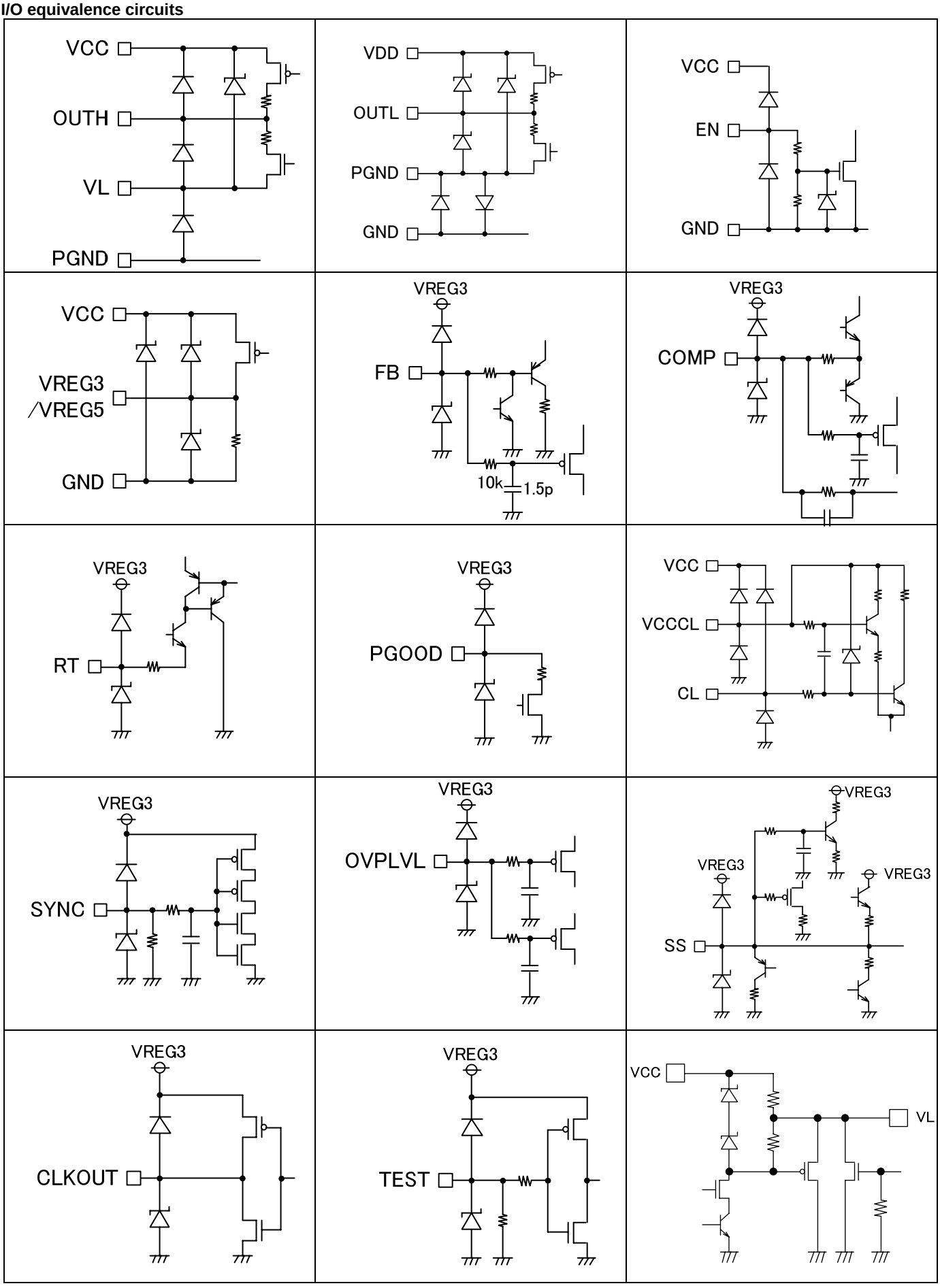
Figure 34. Thermal derating characteristics

70mm×70mm×1.6mm, occupied copper foil is less than 3%, glass epoxy substrate, the board and the back exposure heat radiation board part of package are connected with solder.

①1 layer board (copper foil 0mm × 0mm)
θja＝113.6℃/W
②2 layer board (copper foil 15mm × 15mm)
θja＝73.5℃/W
③2 layer board (copper foil 70mm × 70mm)
θja＝44.6℃/W
④4 layer board (copper foil 70mm × 70mm)
θja＝31.3℃/W

CAUTION: Pd depends on number of the PCB layer and area.
This value is measurement value, but not guaranteed value.

I/O equivalence circuits



Operational Notes

1) Absolute maximum ratings
Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters can result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

2) GND electric potential
Keep the GND terminal potential at the lowest (minimum) potential under any operating condition.

3) Thermal design
Use a thermal design that allows for a sufficient margin with regard to the power dissipation of the actual operating situation.

4) Inter-pin shorting and mounting errors
Ensure that when mounting the IC on the PCB the direction and position are correct. Incorrect mounting may result in damaging the IC. Also, shorts caused by dust entering between the output, input and GND pin may result in damaging the IC.

5) Operation in strong electromagnetic fields
Use caution when operating in the presence of strong electromagnetic fields, as this may cause the IC to malfunction.

6) Common impedance
With regard to the wiring of the power supply and of the ground, take sufficient care to decrease the common impedance and to make the ripple as small as possible (by making the wiring as wide and short as possible, reducing ripple by L, C, etc.).

7) Thermal shutdown (TSD)
Temperature Protect Circuit (TSD Circuit) is built-in in this IC. As for the Temperature Protect Circuit (TSD Circuit), because it a circuit that aims to block the IC from insistent careless runs, it is not aimed for protection and guarantee of IC. Therefore, please do not assume the continuing use after operation of this circuit and the Temperature Protect Circuit operation.

8) Rush current at power ON
With CMOS Ics and Ics featuring multiple power supplies the possibility exists of an instantaneous current rush when the power is turned ON. Therefore, attention should be given to the power coupling capacitance and power and ground wiring width and route.

9) Power input at shutdown
If VCC starts up rapidly at shutdown (EN=OFF), VREG3 voltage may be output and this may cause the IC to malfunction. Therefore, set the rise time of VCC to under 40V/ms.

10) About IC Pin Input
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. Relations between each potential may form as shown in the example below, where a resistor and transistor are connected to a pin:
- With the resistor, when GND> Pin A, and with the transistor (NPN), when GND>Pin B:
  The P-N junction operates as a parasitic diode.
- With the transistor (NPN), when GND> Pin B:
  The P-N junction operates as a parasitic transistor by interacting with the N layers of elements in proximity to the parasitic diode described above.

Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits and can cause malfunctions and, in turn, physical damage to or destruction of the chip. Therefore do not employ any method in which parasitic diodes can operate such as applying a voltage to an input pin that is lower than the (P substrate) GND

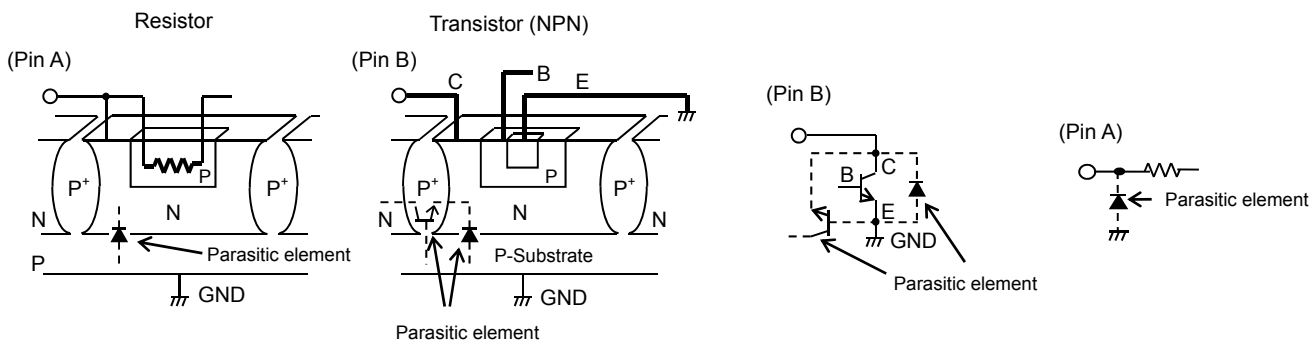
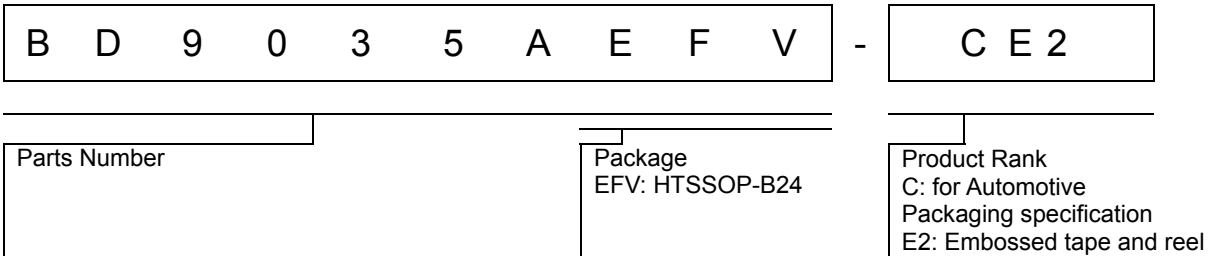


Figure 35.

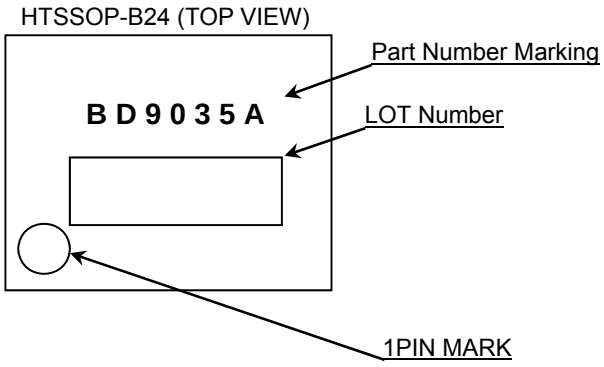
11) About TEST pin
Note that the TEST pin will go into test mode that masks protection functions when supplied with voltage. Be sure to connect TEST pin to ground.

12) About VREG3, VREG5 pin
VREG3 and VREG5 output pins are designed to supply power only into this IC. Thus, it is not recommended to use them for other purposes.

Ordering Information

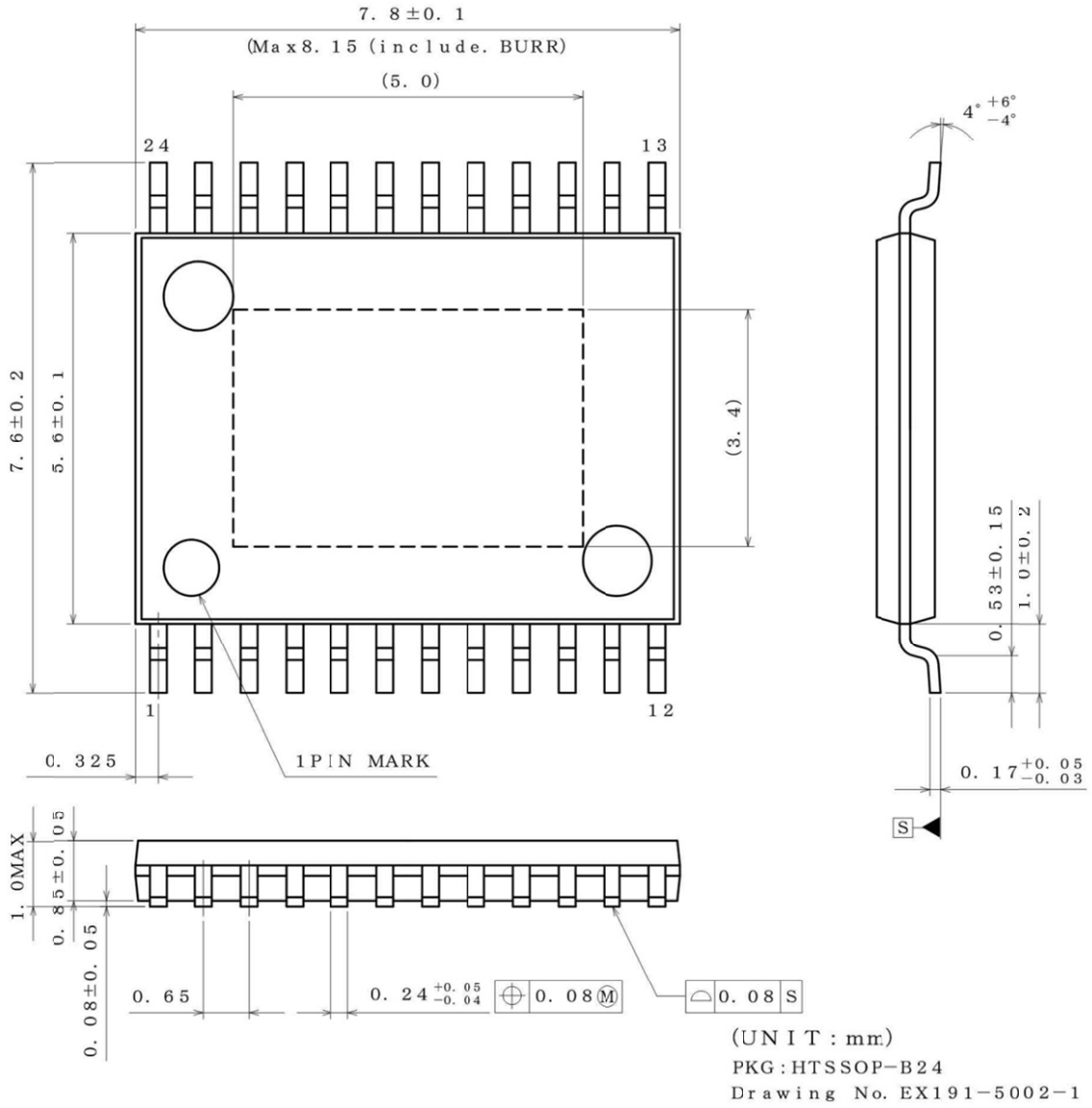


Marking Diagram



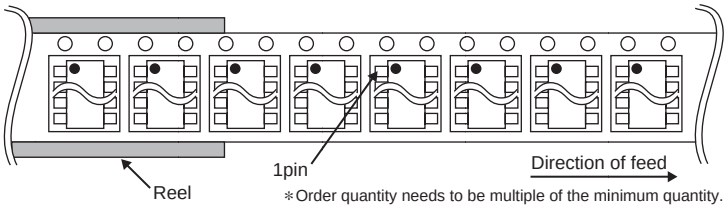
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Change log
2013.7.30	001	New version created.
2014.2.19	002	Added the term about AEC-Q100. (P.1) Replaced “Physical Dimension, Tape and Reel Information” with new format. (P.22)

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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