Secondary power supply series for automotive

2.6V to 5.5V, 2A, 0.3MHz to 2.4MHz Synchronous Step-Down Converter

BD90521MUV-C / BD90521EFV-C

General Description

The BD90521MUV/EFV -C is a synchronous step-down converter which operates in current mode. It can operate with maximum frequency of 2.4 MHz, and can downsize external parts such as inductor. It can supply a maximum output current of 2A with built-in Pch and Nch output MOSFET. Output voltage and oscillation frequency can be adjusted by external resistors and can also be synchronized with an external clock.

Features

- AEC-Q100 Qualified (Note 1)
- Up to 2.4MHz movement
- Excellent Load Response by Current Mode Control
- Built-in Pch/Nch Output MOSFET.
- Frequency Synchronization with External Clock.
- Output Error Monitor Terminal (PGOOD Terminal)
- Adjustable Output Voltage and Oscillation Frequency by External Resistors.
- Built-in Self-Reset Type Overcurrent Protection.
- Built-in Output Overvoltage/Short Circuit Detection.
- Built-in Temperature Protection (TSD) and UVLO.

(Note 1: Grade 1)

Applications

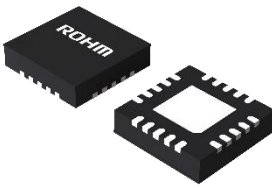
- Automotive Battery-Powered Supplies (Cluster Panels, Car Multimedia)
- Industrial / Consumer Supplies
- Other electronic equipment

Key Specifications

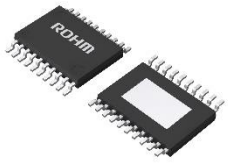
- Operating Temperature Range(Ta): -40°C to +125°C
- Input Voltage Range: 2.6V to 5.5V
- Output Current: 2.0A(Max)
- Reference Voltage Accuracy: ±1.5 %
- Output Voltage Range: 0.6V to 5.0V
- Switching Frequency: 0.3MHz to 2.4MHz

Package

	W(Typ) x D(Typ) x H(Max)
VQFN20SV4040	4.00mm x 4.00mm x 1.00mm
HTSSOP-B20	6.50mm x 6.40mm x 1.00mm

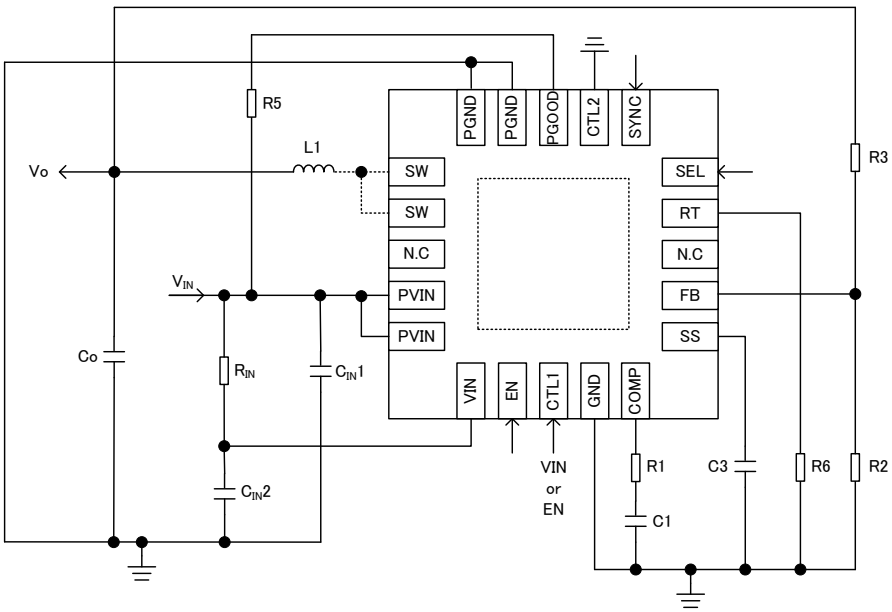


VQFN20SV4040



HTSSOP-B20

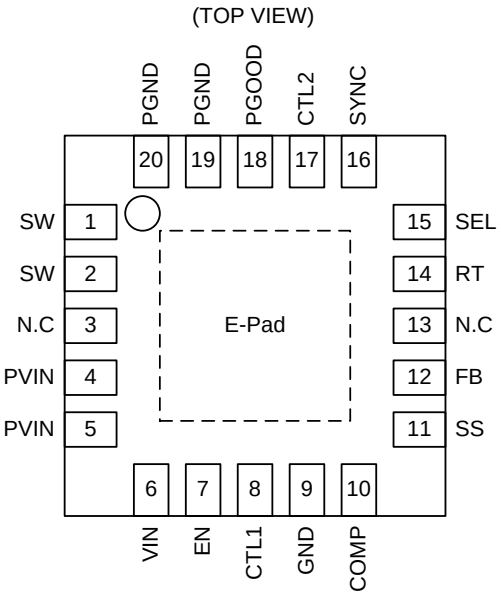
Typical Application Circuit



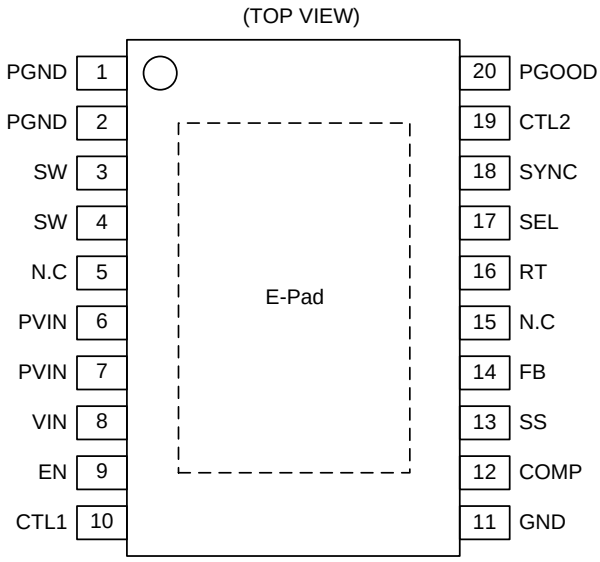
○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configurations



VQFN20SV4040



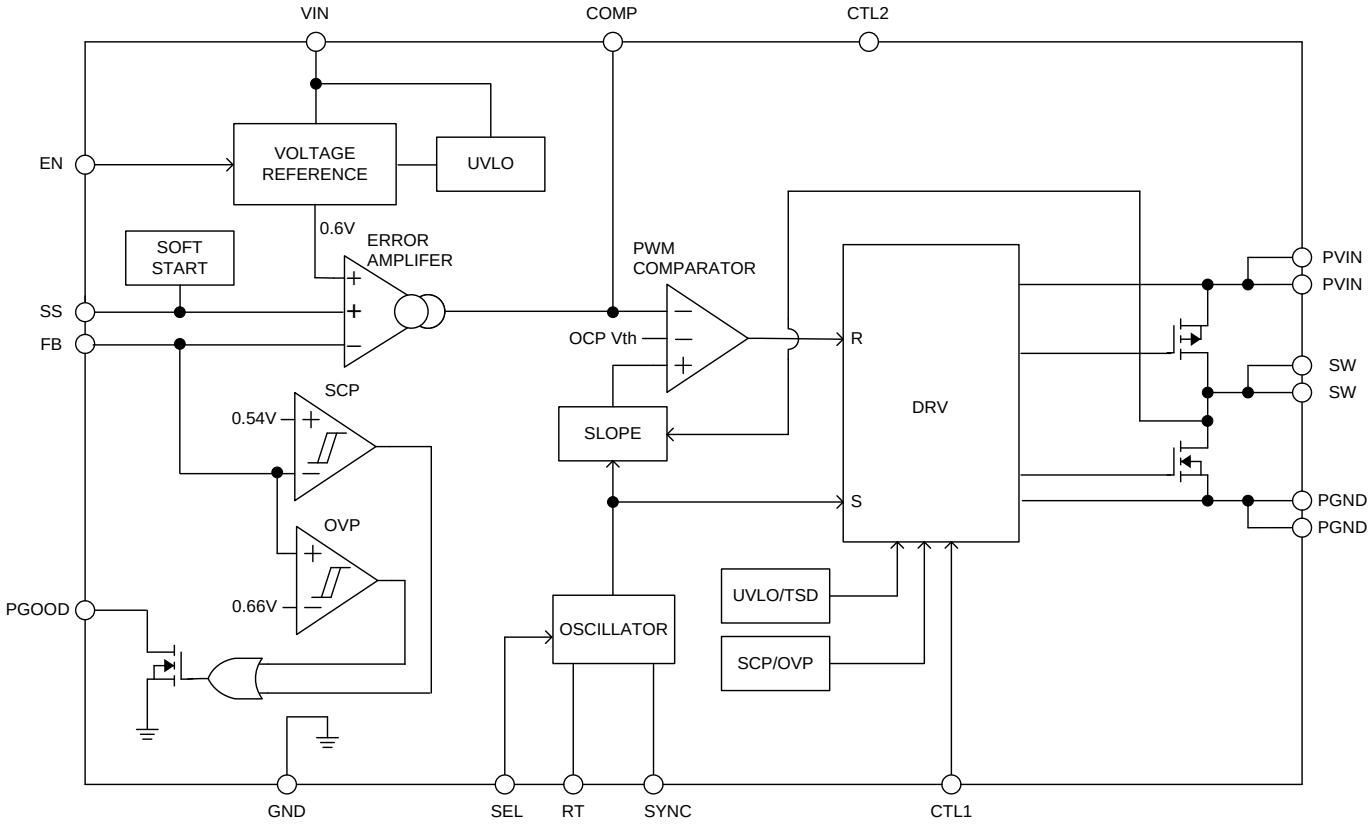
HTSSOP-B20

Pin Descriptions

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1 (3)	SW	SW pin	11 (13)	SS	Soft start time setting pin
2 (4)	SW	SW pin	12 (14)	FB	Output feedback pin
3 (5)	N.C	-	13 (15)	N.C	-
4 (6)	PVIN	Power supply pin for output FET	14 (16)	RT	Operating frequency setting pin
5 (7)	PVIN	Power supply pin for output FET	15 (17)	SEL	RT setting frequency/ Synchronization select pin
6 (8)	VIN	Power supply pin	16 (18)	SYNC	External clock input pin
7 (9)	EN	Enable pin	17 (19)	CTL2	Test pin
8 (10)	CTL1	Test pin	18 (20)	PGOOD	Power good output pin
9 (11)	GND	GND pin	19 (1)	PGND	GND pin for output FET
10 (12)	COMP	Error amp output pin	20 (2)	PGND	GND pin for output FET

E-Pad is a back radiation pad. Excellent radiation property is obtainable by connection to internal PCB ground-plane using multiple via.
Use CTL1 terminal by applying 2.1 V or higher when enable is on.
Use CTL2 terminal by short-circuiting to GND.
If N.C pin is shorted to GND, heat radiation performance becomes higher.

Block Diagram



Description of Blocks

- ERROR AMPLIFER
  This is an error amplifier using reference voltage of 0.6V (Typ) and “FB” terminal voltage as input. (Refer to p. 21 to p. 22 for phase compensation setting method). Duty width of switching pulse is controlled with “COMP” of error amplifier output. Output voltage is set using “FB” terminal. Phase compensation can be adjusted by connecting capacitor and resistor to “COMP” terminal.

- SOFT START
  This is a function for preventing overshoot of output voltage by gradually raising non-inverting input voltage of ERROR AMPLIFIER to gradually increase duty of switching pulse at power on. Soft start can be set by connecting a capacitor between “GND” terminals with “SS terminal”. (Refer to p. 22.)

- OSCILLATOR
  Oscillation frequency of 0.3 MHz to 2.4 MHz can be set by connecting a resistor between “RT” terminal and “GND” terminal in the circuit which generates pulse waveform to be input to SLOPE. (Refer to Figure 18 on p. 21)OSCILLATOR output sends clock signal to DRV. OSCILLATOR output is also used as the clock of SCP counter.

- SLOPE
  This is the block for generating saw-tooth wave from the clock formed by OSCILLATOR. Generated saw-tooth wave is combined with feedback current of coil current and sent to PWM COMPARATOR.

- PWM COMPARATOR
  This is a comparator that compares SLOPE output and ERROR AMPLIFIER output.

- DRV
  This is a latch circuit having OSCILLATOR output (set) and PWM COMPARATOR output (reset) as input. It generates PWM control signal and outputs gate signal for FET drive.

・TSD (Thermal Shut Down)
This is an overheat protection circuit. In order to prevent IC thermal destruction/runaway, output is turned off when chip temperature rises to about 150°C or higher. It is recovered when temperature returns to constant temperature. However, since overheat protection circuit is essentially built-in for the purpose of protection of IC itself, carry out thermal design to keep chip temperature below about 150°C as TSD detection temperature.

・OCP V_{TH}(Over Current Protection)
This is an overcurrent protection circuit. When output Pch POWER MOS FET is turned on and voltage between drain and source exceeds internal reference voltage value, overcurrent protection activates. This overcurrent protection is self-reset type. When overcurrent protection activates, duty becomes small and output voltage is reduced. However, since these protection circuits are effective in protection from destruction due to sudden accidents, avoid using them when continuous protection circuit is in action.

・SCP (Short Current Protection)
This is a load short-circuit protection circuit. When the state of output of 60% or lower is detected in oscillation cycle × 256 (s), POWER MOS FET is turned off. If output voltage is recovered to 60% or higher before completion of 256 cycles, POWER MOS FET is not turned off. This load short-circuit protection is cancelled after retention of oscillation cycle × 2048 (s), and it is restarted with soft start. Elongation of off time results in decrease of mean output current. During startup of power source, this function is masked until output reaches set voltage to prevent startup failure.

・UVLO (Under Voltage Lock-Out)
This is a low voltage wrong operation prevention circuit. It prevents wrong operation of internal circuits during power source voltage startup and when power source voltage is reduced. Power source voltage is monitored and when it is reduced to 2.25 V (Typ) or lower, output POWER MOS FET is turned off. When UVLO is cancelled, it is restarted with soft start. This threshold has hysteresis of 100 mV (Typ).

・VOLTAGE REFERENCE
It supplies reference voltage to internal circuits.

・OVP
When output voltage is detected to have exceeded set value + 10%, Pch FET and Nch FET of output is turned off. After detection, when output is reduced and the overvoltage state is cancelled, switching action is restarted. There is hysteresis of 2% in overvoltage detection voltage and cancel voltage.

・PGOOD
When output voltage is below 90% or above 110% of set value, output error state is assumed, and PGOOD terminal is turned “Low”. There is hysteresis of 2% in detection voltage and cancel voltage. At the time of EN OFF and when UVLO and TSD are in action, PGOOD terminal output is also turned “Low”. If VIN input voltage exceeds 2 V, PGOOD output becomes effective. Since output is open drain type, connect pull up to VIN or an external power source with resistance of 10kΩ - 100 kΩ.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}, PV_{IN}	-0.3 to 7	V
EN Pin Voltage (Note 1)	V_{EN}	-0.3 to 5.9	V
SYNC Pin Voltage	V_{SYNC}	-0.3 to V_{IN}	V
SEL Pin Voltage	V_{SEL}	-0.3 to 7	V
FB Pin Voltage	V_{FB}	-0.3 to V_{IN}	V
COMP Pin Voltage	V_{COMP}	-0.3 to V_{IN}	V
SS Pin Voltage	V_{SS}	-0.3 to V_{IN}	V
RT Pin Voltage	V_{RT}	-0.3 to V_{IN}	V
PGOOD Pin Voltage	V_{PGOOD}	-0.3 to 7	V
Maximum Junction Temperature	Tjmax	+150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
ESD Rating (HBM)	$V_{ESD, HBM}$	±2000	V

(Note 1) State enters test mode when EN terminal exceeds 6 V.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance(Note 1)

項目	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
VQFN20SV4040				
Junction to Ambient	θ_{JA}	153.9	37.4	°C / W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	13	7	°C / W
HTSSOP-B20				
Junction to Ambient	θ_{JA}	143.0	26.8	°C / W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	8	4	°C / W

(Note 1) Based on JESD51-2A(Still-Air)

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4) Using a PCB board based on JESD51-5,7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via (Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions (Ta = -40°C to +125°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{IN}, PV_{IN}	2.6	5.5	V
EN Pin Voltage (Note 1,2)	V_{EN}	0	5.5	V
SEL Pin Voltage	V_{SEL}	0	5.5	V
SYNC Pin Voltage	V_{SYNC}	0	V_{IN}	V
Setting Frequency Range	f_{RT}	0.3	2.4	MHz
External Clock Frequency Range	f_{SYNC}	0.3 (Note 3)	2.4 (Note 3)	MHz
Output Voltage Range	V_O	0.6 (Note 4)	5.0	V
Output Current	I_O	0	2 (Note 4)	A
Input Capacitor	$C_{IN}1$	11 (Note 5)	-	µF

(Note 1) State enters test mode when EN terminal exceeds 6 V.
(Note 2) Within action power voltage range, the order of startup of power (V_{IN}, PV_{IN}), EN terminal and SEL terminal does not matter.
(Note 3) As an external signal, input frequency within ±25% of frequency set by RT resistance.
(Note 4) Output voltage is limited by SW minimum ON time depending on setting of input voltage and oscillation frequency. For the setting range, see setting of output voltage of application part selection method (p. 20).
(Note 5) Ceramic capacitor is recommended. Set the capacitance value not to become below minimum value including variation, temperature property, DC bias property and aging. Since malfunction may occur depending on substrate patterns and capacitor positions, please design the substrate referring to cautions in substrate layout (p. 28).

Electrical Characteristics

(Unless otherwise specified, -40 °C ≤ Ta ≤ +125 °C、V_{IN} = PV_{IN} = 5 V、V_{EN} = 3.3 V、V_{CTL1} = 5 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Standby Circuit Current	I_{SDN}	-	0	1	μA	V_{EN} = 0V, Ta = 25°C
Circuit Current	I_{IN}	-	700	1050	μA	V_{FB} = 0.63V, Ta = 25°C
EN ON Voltage	V_{EN_ON}	2.1	-	-	V	
EN OFF Voltage	V_{EN_OFF}	-	-	0.7	V	
EN Input Current	I_{EN}	3	7	14	μA	V_{EN} = 3.3V
UVLO ON Voltage	V_{UVLO_ON}	-	2.25	2.40	V	Sweep Down
UVLO OFF Voltage	V_{UVLO_OFF}	-	2.35	2.50	V	Sweep Up
FB Input Current	I_{FB}	-	0	0.5	μA	V_{FB} = 0.6V
Reference Voltage	V_{REF}	0.591	0.600	0.609	V	FB = COMP
COMP Source Current	I_{COMP_SOURCE}	-40	-20	-5	μA	
COMP Sink Current	I_{COMP_SINK}	5	20	40	μA	
SS Charge Current	I_{SS}	-3	-2	-1	μA	V_{SS} = 0.6V
SS Discharge Current	R_{SS}	100	200	300	Ω	V_{SS} = 0.6V
Operating Frequency	f_{OSC}	0.85	1.00	1.15	MHz	R6 = 240kΩ
SW Min ON Time 1	t_{SW_ON1}	-	100	-	ns	I_O = 0A
SW Min ON Time 2	t_{SW_ON2}	-	80	-	ns	I_O = 1A
SW Min OFF Time	t_{SW_OFF}	-	100	-	ns	
SW ON-Resistance H	$R_{ON\_SW\_H}$	-	90	180	mΩ	I_{SW} = -50mA, V_{FB} = 0.58V
SW ON-Resistance L	$R_{ON\_SW\_L}$	-	60	120	mΩ	I_{SW} = +50mA, V_{FB} = 0.62V
Over-Current Detect Current	I_{SW_OCP}	2.5	5.5	-	A	
SYNC ON Voltage	V_{SYNC_ON}	0.8 x V_{IN}	-	-	V	
SYNC OFF Voltage	V_{SYNC_OFF}	-	-	0.2 x V_{IN}	V	
SYNC Input Current	I_{SYNC}	4	10	20	μA	V_{SYNC} = 5V
PGOOD Sense FB Voltage	V_{FB_PGOOD1}	±6	±10	±14	%	Pull up to VIN with 10kΩ
PGOOD ON-Resistance	R_{PGOOD}	60	120	240	Ω	V_{PGOOD} = 5V
SEL ON Voltage	V_{SEL_ON}	2.1	-	-	V	
SEL OFF Voltage	V_{SEL_OFF}	-	-	0.7	V	
SEL Input Current	I_{SEL}	3	7	14	μA	V_{SEL} = 3.3V

Typical Performance Curves(Unless otherwise specified like the condition of each item of P8)

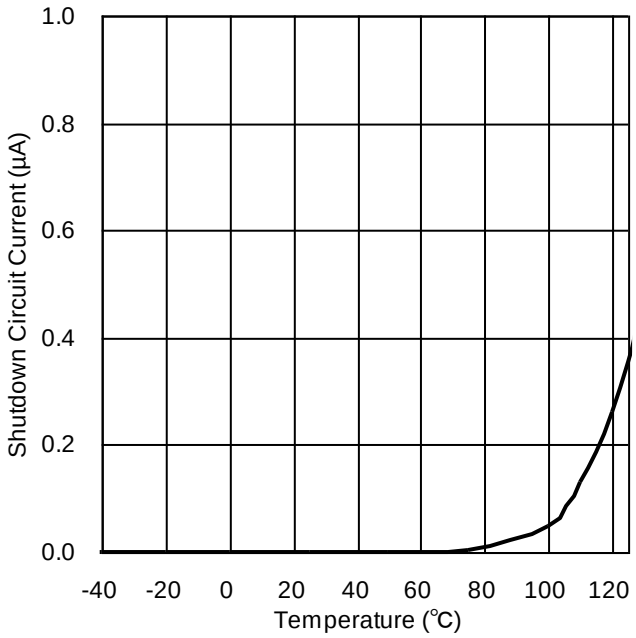


Figure 1. Standby Circuit Current vs Temperature

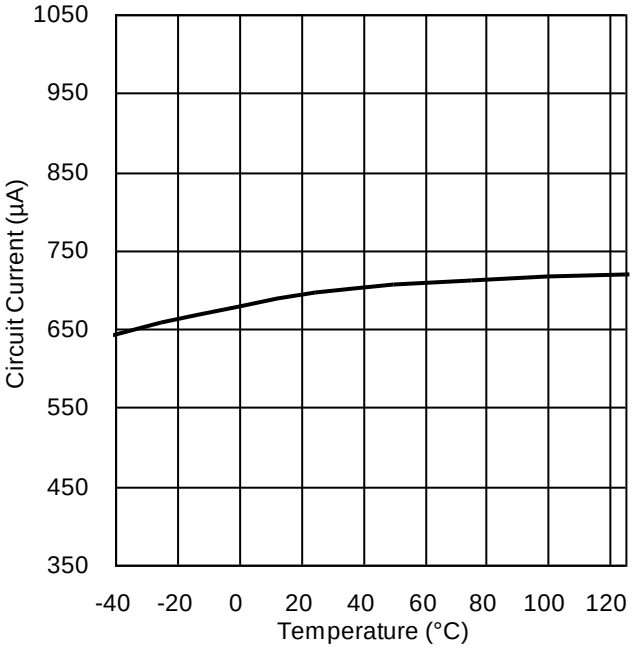


Figure 2. Circuit Current vs Temperature

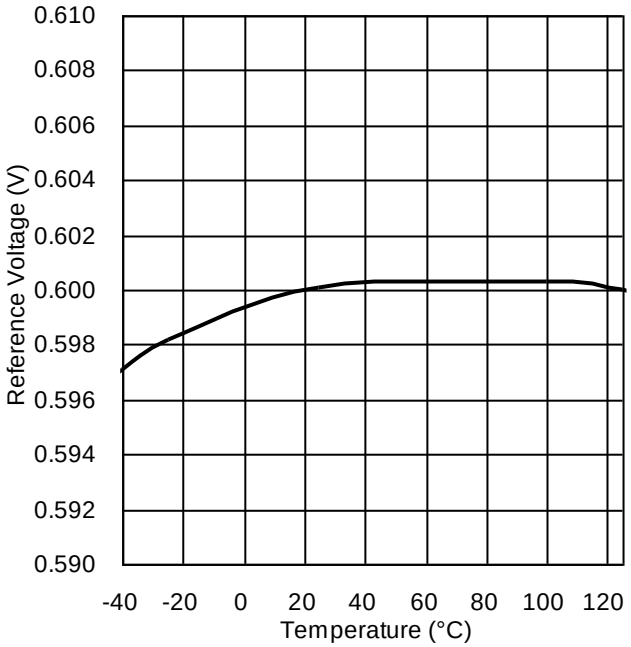


Figure 3. Reference Voltage vs Temperature

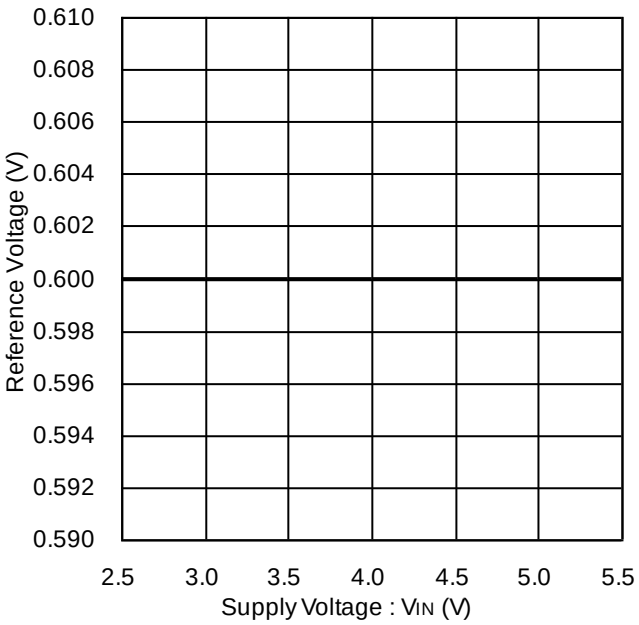


Figure 4. Reference Voltage vs Supply Voltage

Typical Performance Curves - continued

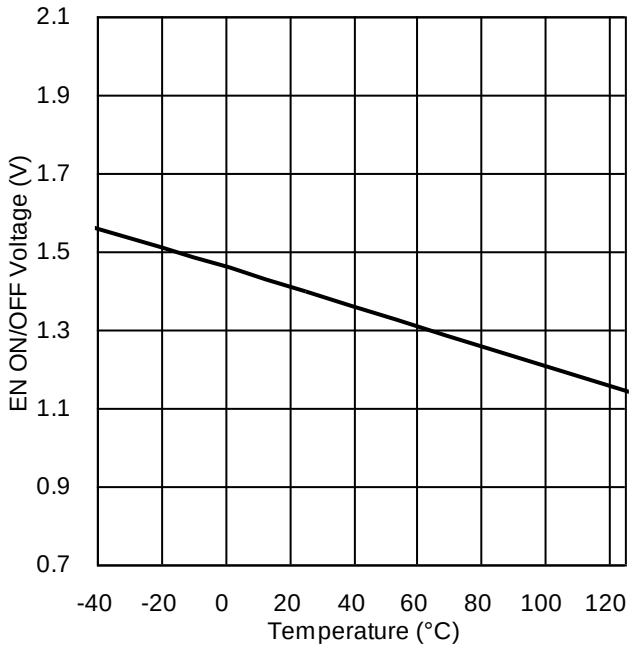


Figure 5. EN ON/OFF Voltage vs Temperature

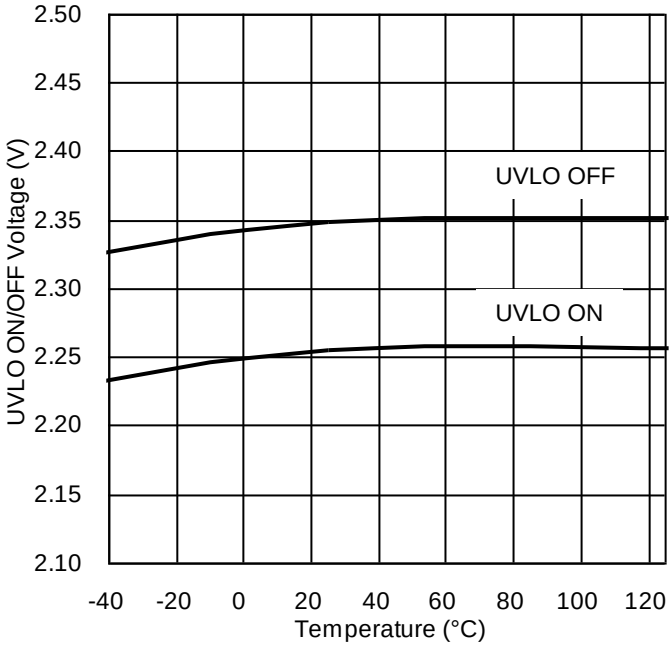


Figure 6. UVLO ON/OFF Voltage vs Temperature

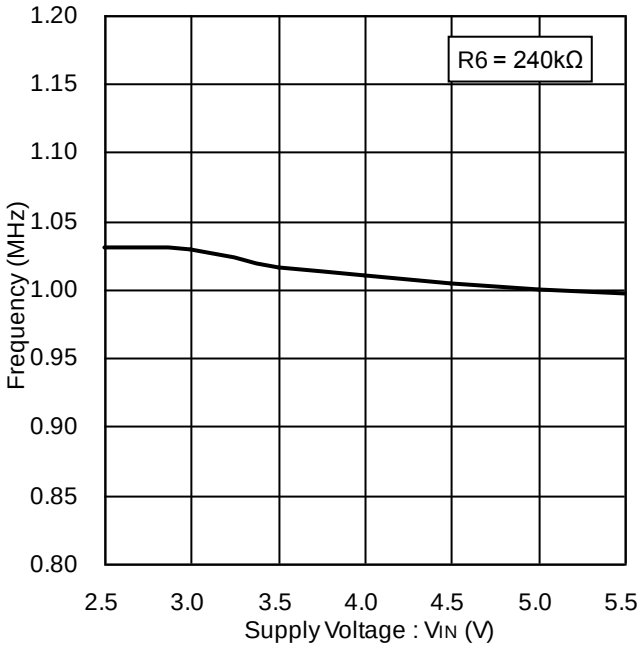


Figure 7. Frequency vs Supply Voltage

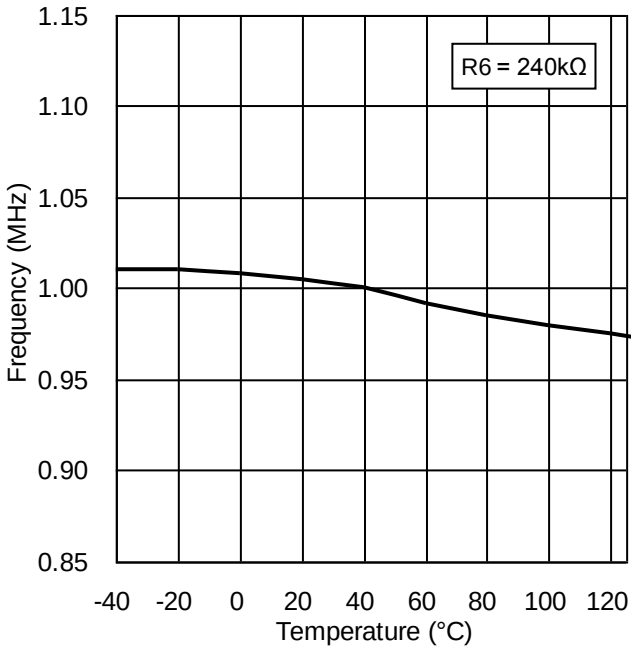


Figure 8. Frequency (1MHz) vs Temperature

Typical Performance Curves - continued

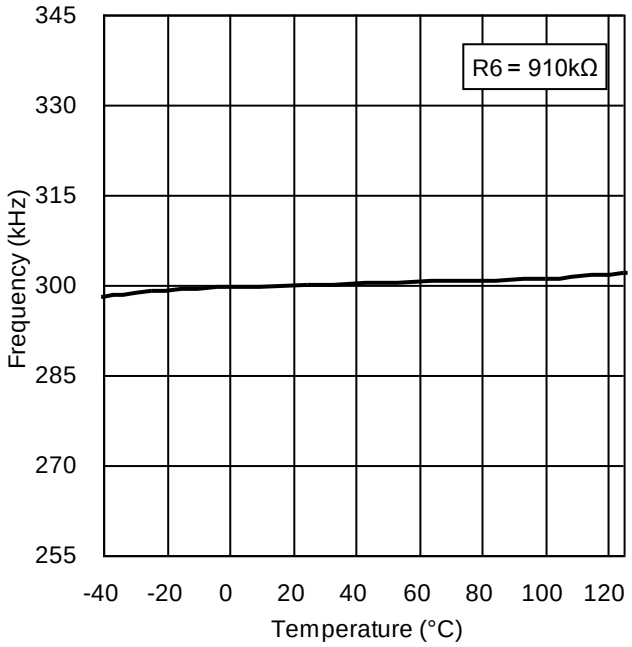


Figure 9. Frequency (300kHz) vs Temperature

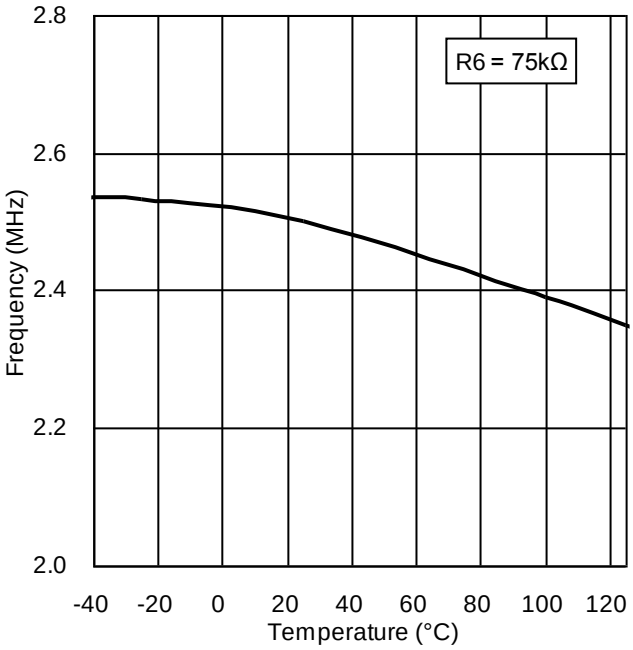


Figure 10. Frequency (2.4MHz) vs Temperature

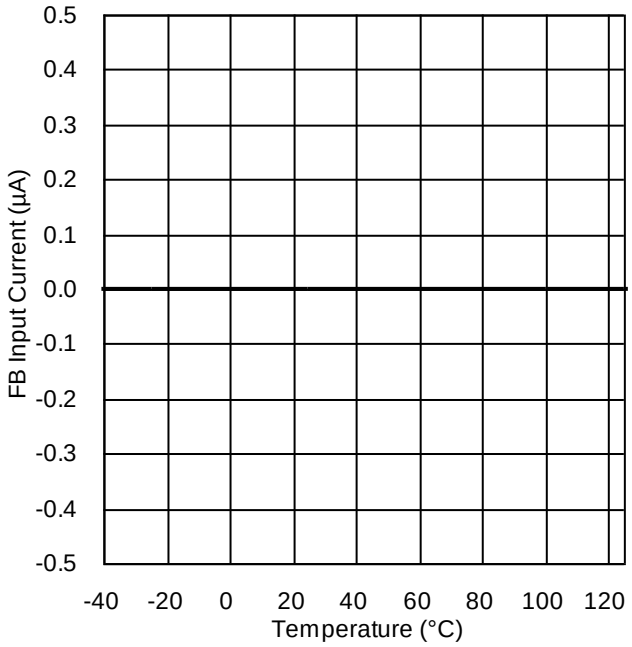


Figure 11. FB Input Current vs Temperature

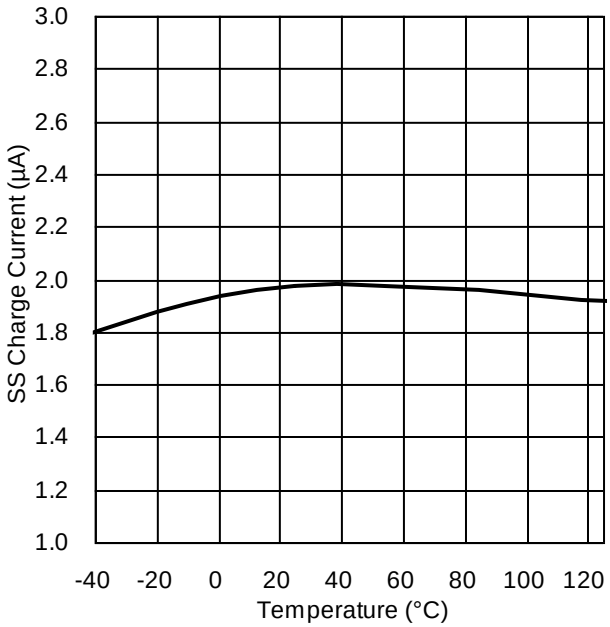


Figure 12. SS Charge Current vs Temperature

Typical Performance Curves - continued

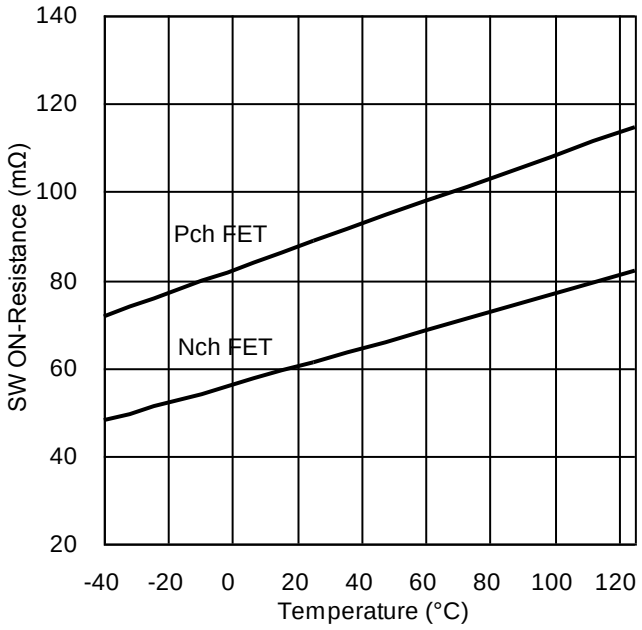


Figure 13. SW ON-Resistance vs Temperature

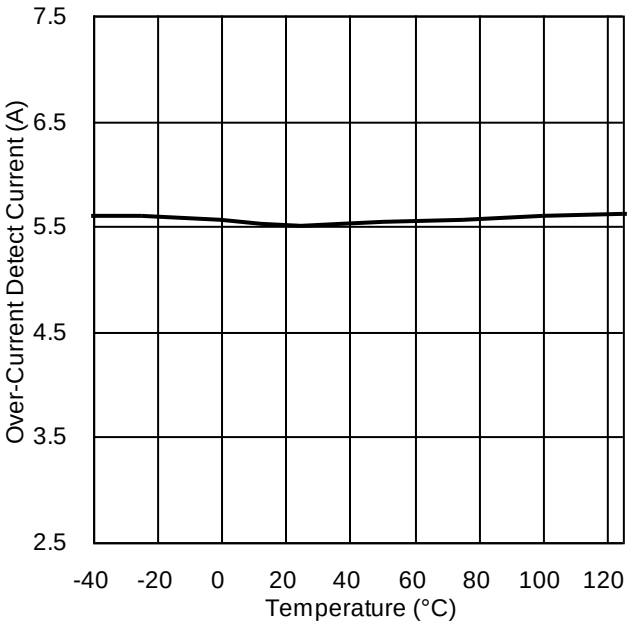


Figure 14. Over-Current Detect Current vs Temperature

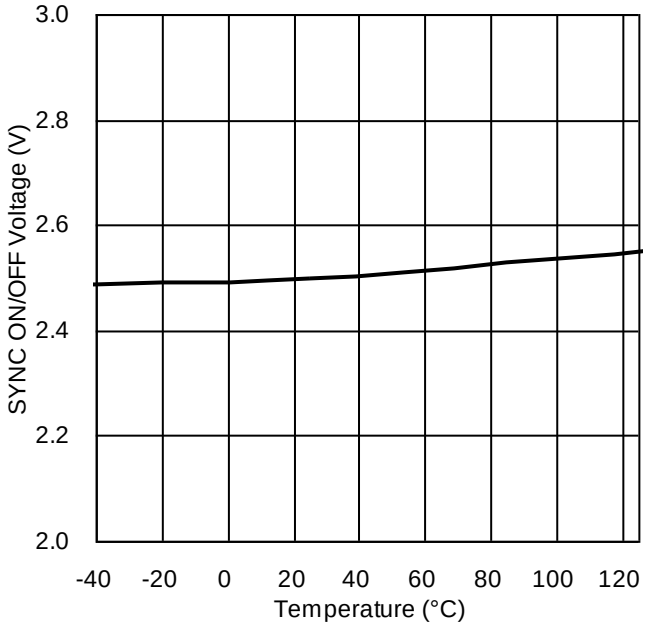


Figure 15. SYNC ON/OFF Voltage vs Temperature

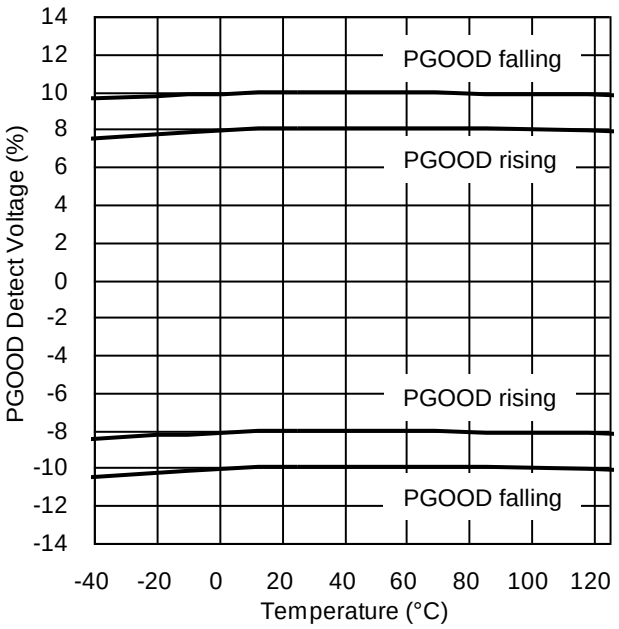


Figure 16. PGOOD DETECT Voltage vs Temperature

Typical Performance Curves - continued

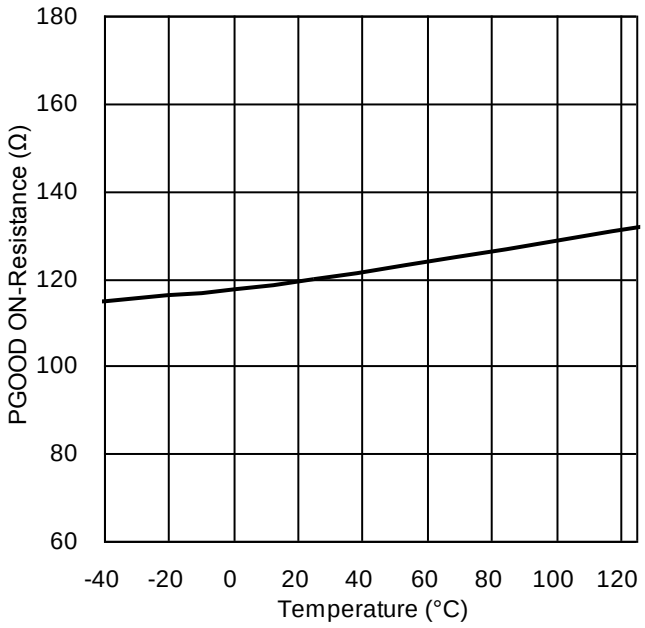
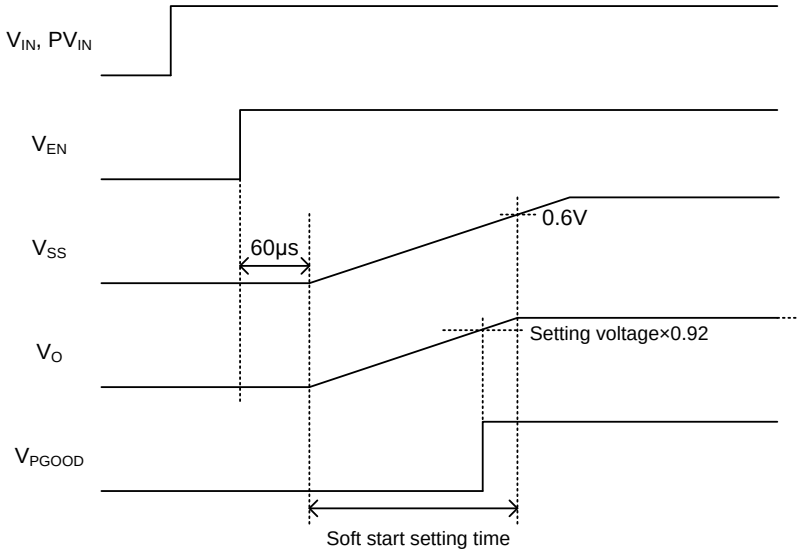


Figure 17. PGOOD ON-Resistance vs Temperature

Description of Operation and Timing Chart

■ Enable control

IC operation is controlled by voltage applied on EN terminal. When Voltage of 2.1 V or higher is applied on EN terminal, output starts in 60 µs(Typ) with soft start. Set the startup time on input voltages, VIN and PVIN, earlier than soft start time. The circuits can be shut down by opening EN terminal or reducing its voltage to below 0.7 V.

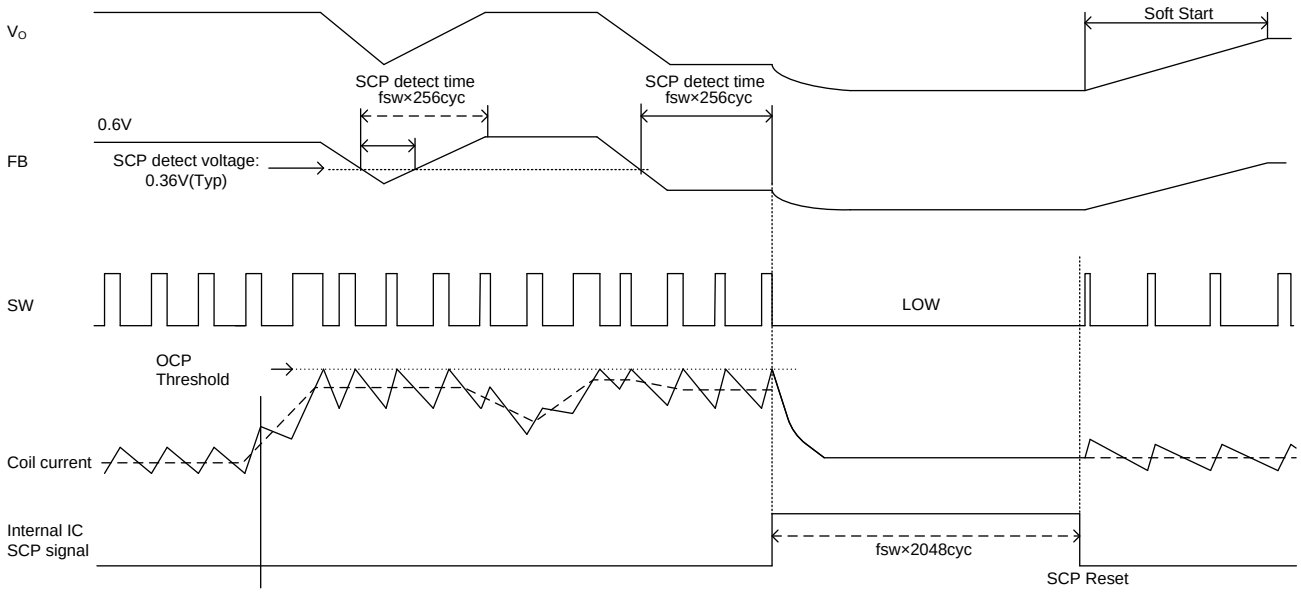


■ Protection functions

Since protection circuits are effective in protection from destruction due to sudden accidents, avoid using protection operation continuously.

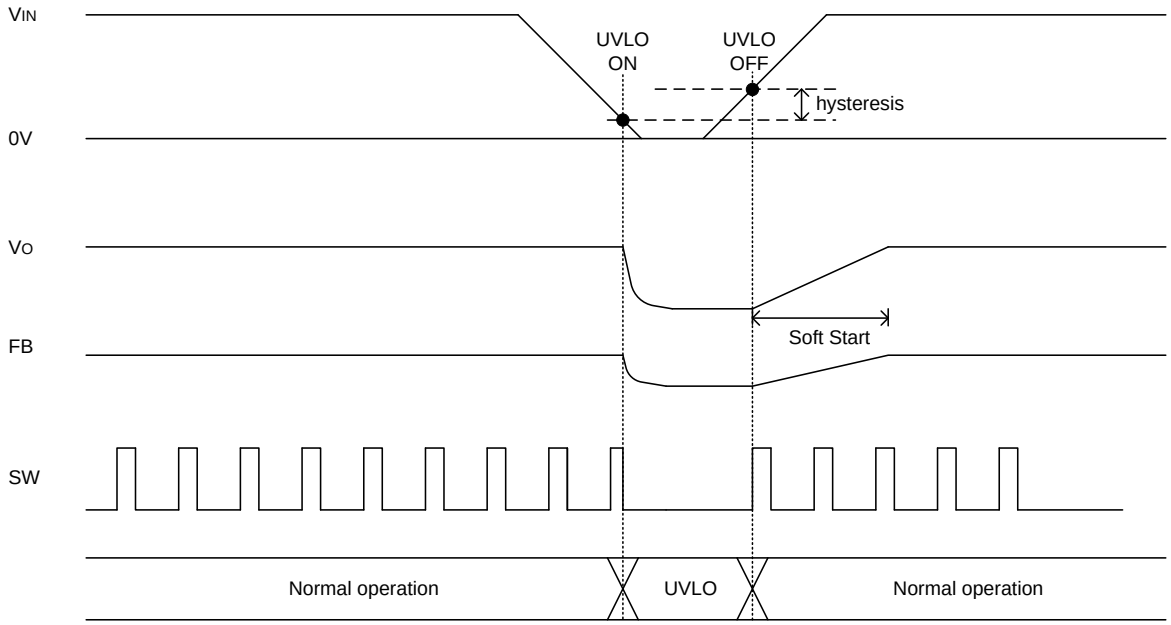
(1) Short Current Protection (SCP)

When the state of output of 60% or lower is detected in oscillation cycle × 256 (s), POWER MOS-FET is turned off. If output voltage has recovered to 60% or higher before completion of 256 cycles, POWER MOS-FET is not turned off. This load short-circuit protection is cancelled after retention for oscillation cycle × 2048 (s), and it is restarted with soft start. Elongation of off time results in decrease of mean output current. During startup of power source, this function is masked until output reaches set voltage to prevent startup failure.



(2) Under Voltage Lock-Out (UVLO)

It prevents wrong operation of internal circuits during power source voltage startup and when power source voltage is reduced. Power source voltage is monitored and when it is reduced to 2.25 V (Typ) or lower, output POWER MOS FET is turned off. When UVLO is cancelled, it is restarted with soft start. This threshold has hysteresis of 100 mV (Typ).



(3) Thermal Shut Down (TSD)

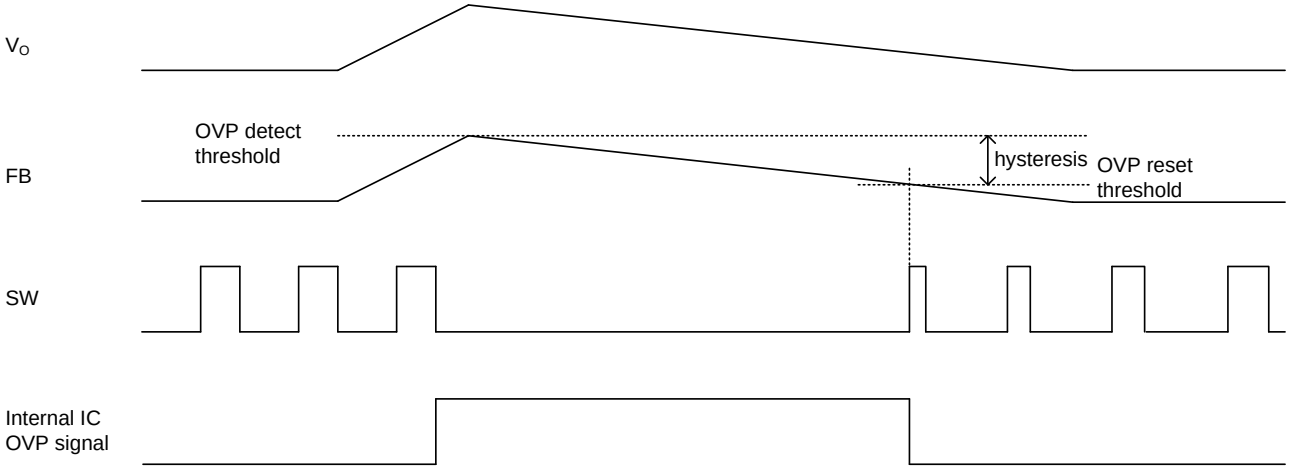
In order to prevent IC thermal destruction/runaway, output is turned off when chip temperature rises to about 150°C or higher. It is recovered when temperature returns to constant temperature. However, since overheat protection circuit is essentially built-in for the purpose of protection of IC itself, carry out thermal design to keep chip temperature below about 150°C as TSD detection temperature.

(4) Over Current Protection (OCP)

When output Pch POWER MOS FET is turned on and voltage between drain and source exceeds internal reference voltage value, overcurrent protection activates. This overcurrent protection is self-reset type. When overcurrent protection activates, duty becomes small and output voltage is reduced. However, since these protection circuits are effective in protection from destruction due to sudden accidents, avoid using them when continuous protection circuit is in action.

(5) Over Voltage Protection (OVP)

When output voltage is detected to have exceeded set value + 10%, Pch FET and Nch FET of output is turned off. After detection, when output is reduced and the overvoltage state is cancelled, switching action is restarted. There is hysteresis of 2% in overvoltage detection voltage and cancel voltage.

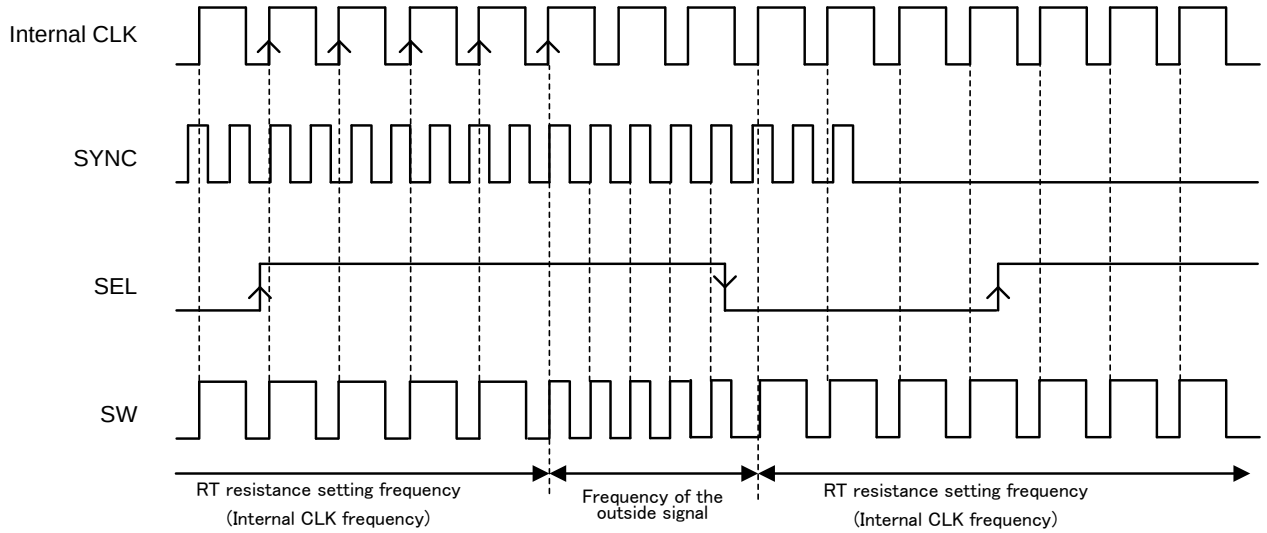


■ Synchronization to External Clock

For external synchronization operation, connect frequency setting resistor to “RT” terminal, apply voltage of 2.1 V or higher on “SEL” terminal, and input synchronous pulse signal to “SYNC” terminal. There is no restriction in the order of input in “SYNC” terminal and “SEL” terminal. When voltage is applied to both terminals, it starts external synchronization action. In case no external signal is connected to “SYNC” terminal when voltage of 2.1 V or higher is applied to “SEL” terminal (no input is assumed in the case of being fixed at low or high), external synchronization action does not occur. When voltage on “SEL” terminal is reduced to 0.7 V or lower, external synchronization operation ends. In this case, operation is carried out with frequency of internal CLK from the cycle next to internal CLK. In order to finish external synchronization operation, turn off external signal of “SYNC” terminal after “SEL” terminal input voltage becomes “Low”. Note that output voltage varies during synchronization to external signal and switching to internal CLK frequency. When using external synchronization, setting range of oscillation frequency is restricted by external resistance of “RT” terminal. The setting range becomes within ±25% of RT setting frequency.

Example) When R6 = 240 kΩ,
Since set oscillation frequency is 1.0 MHz, allowable range of external synchronization operation frequency is 0.75 MHz to 1.25 MHz.

Set LOW voltage of synchronous pulse signal to 0.2 V × V_{IN} or lower, and HIGH voltage to 0.8 V × V_{IN} or higher.
Set slew rate of rise (fall) at 30 V / µs or more, and duty within the range of 20% to 80%.
After 4 detections of rise of synchronous pulse, synchronization starts from the fifth rise.

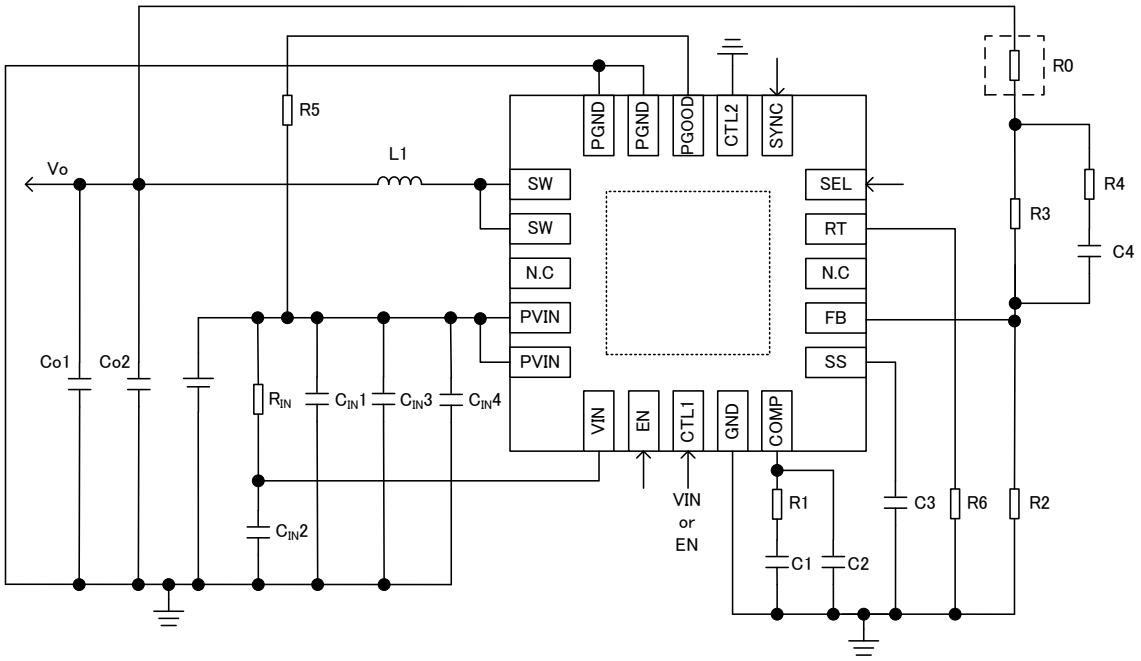


Timing chart of synchronization to external clock

Selection of Components Externally Connected

Necessary parameters in designing the power supply are as follows:

Parameter	Symbol	Specification Case
Input Voltage	V_{IN}	5 V
Output Voltage	V_O	1.2 V
Output Ripple Voltage	ΔV_{PP}	10 mV_{p-p}
Input Range	I_O	Typ 1.5 A / Max 2.0 A
Switching Frequency	f_{SW}	2.0 MHz
Operating Temperature Range	Ta	-40 °C to +105 °C



Application Sample Circuit

(1) Selection of Inductor

The switching regulator needs an LC filter for smoothing of output voltage in order to supply continuous current to load. When an inductor with large inductance value is selected, ΔI_L flowing in the inductor becomes small and output ripple voltage is reduced. Furthermore, there is a trade-off between size and cost of inductance.

The inductance value of the inductor is shown in the following equation:

$$L = \frac{(V_{IN(MAX)} - Vo) \times Vo}{V_{IN(MAX)} \times f_{SW} \times \Delta I_L} \quad [H]$$

Where:

$V_{IN\ (Max)}$ is the maximum input voltage

ΔI_L is the ripple current of inductor

Set ΔI_L to about 30% of maximum output current.

When ΔI_L becomes small, core loss (iron loss) of inductor, loss of output capacitor due to ESR and ΔV_{PP} become small.

$$\Delta V_{PP} = \Delta I_L \times ESR + \frac{\Delta I_L}{8 \times C_O \times f_{SW}} \quad [V] \qquad \cdots\cdots \text{(a)}$$

Where:

ESR is the equivalent series resistance of output capacitor
C_O is the output capacitor

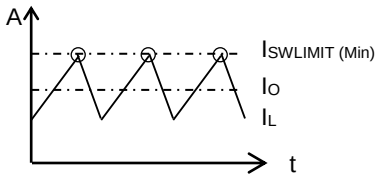
Since ceramic capacitors generally have ultra-low ESR, target ΔV_{PP} can be satisfied even if ΔI_L is large to some extent. The advantage is that inductance value of inductor can be set small. Small inductance value contributes to space-saving of sets, because large rated current enables selection of small size inductors. The disadvantages are increase of core loss of inductor and reduction of maximum output current. When using other capacitors (electrolytic capacitor, tantalum capacitor, electro-conductive polymer, etc.) as the output capacitor C_O, confirm ESR with data sheet of the manufacturer, and determine ΔI_L to fit ΔV_{PP} within allowable range.
Especially, since capacitance reduction of electrolytic capacitor is significant at low temperature, ΔV_{PP} increases. Pay attention when using it at low temperature

The maximum output electric current is limited to the overcurrent protection working current as shown in the following equation.

$$I_{O(MAX)} = I_{SW\_OCP(MIN)} - \frac{\Delta I_L}{2} \quad [A]$$

Where:

$I_{O(Max)}$ is the maximum output current
$I_{SW\_OCP(Min)}$ is the OCP operation current (Min)



I_L peak

In the case of continuous operation with duty ≥ 50%, current control mode may generate sub-harmonic oscillation. This IC has a built-in slope compensation circuit for the purpose of prevention of sub-harmonic oscillation.
Since sub-harmonic oscillation depends on increase rate of output switch current I_L, sub-harmonic oscillation may be generated when inductance value is reduced to increase slope of I_L.
On the other hand, when inductance value is increased to reduce slope of I_L, sufficient stability may not be secured.
For stable operation, restrict inductance value within the range where the following formula is applicable

$$L \geq \frac{2D-1}{2(1-D)} \times Rs \times \frac{V_{IN\ (MIN)} - V_O}{m} \quad [H]$$

$$D = \frac{V_O}{V_{IN(MIN)}}$$

$$m = 1.69 \times f_{sw} \times 10^{-6} - 0.19$$

Where:

D is the switching pulse ON Duty.
R_S is the coefficient of current sense(2.53 µA / A)
m is the slope of slope compensation current

Shield type (closed magnetic path type) inductors are recommended. There is no problem with open magnetic path type if the application is cost-emphasized and free of annoying noise. In this case, consider layout with enough allowance between parts, since there may be influence of magnetic field radiation on adjacent parts. Pay special attention to magnetic saturation for ferrite-core type inductors. Core saturation should be avoided under all use conditions. Attention is needed since rated current specification is different depending on manufacturers. Confirm rated current at maximum ambient temperature of application with the manufacturer.

(2) Selection of output Capacitor C_O

Select output capacitor based on required ESR from formula (a). ΔV_{PP} can be minimized by using capacitors with small ESR. Ceramic capacitor is the best option for satisfying the requirement. In addition to exhibiting low ESR, ceramic capacitors contribute to space saving of sets because of being small. Confirm frequency characteristics of ESR with manufacturers' data sheets, and select a capacitor with low ESR at switching frequency used.
Use ceramic capacitors carefully because DC bias property is remarkable. It is usually desirable that rated voltage of a ceramic capacitor is more than twice as high as maximum output voltage. Influence of DC bias property can be reduced by selecting a capacitor with high rated voltage. Furthermore, in order to keep good temperature characteristics, capacitors with property higher than that of X7R are recommended.

Tantalum capacitors and electro-conductive polymer hybrid aluminum electrolytic capacitors have very good temperature characteristics, for which electrolytic capacitors are disadvantageous. Further, since their ESR is smaller than that of electrolytic capacitors, relatively small ripple voltage can be obtained in wide temperature range. Similar to electrolytic capacitors, they are almost free from DC bias characteristics, and make designing easier. Usually, ones with rated voltage about twice as high as output voltage are selected for tantalum capacitors and ones with rated voltage about 1.2 times as high as output voltage are selected for electro-conductive polymer hybrid aluminum electrolytic capacitors. The disadvantage of tantalum capacitors is that failure mode is short-circuiting and withstand voltage is low. Generally, they are not selected for applications such as car-mounted applications in which reliability is required. Since failure mode is open for electro-conductive polymer hybrid aluminum electrolytic capacitors, they are effective to meet the reliability requirement, but they have a disadvantage of generally being expensive.
Pch step-down switching regulator lowers input voltage V_{IN}, and when difference between input and output voltages becomes small, switching pulse begins to disappear before 100% on-duty is reached.
As a result, when switching pulse disappears, output ripple voltage may increase.
When improvement of output ripple voltage is necessary, following measures should be considered for output capacitor C_O.

・ Use of capacitors with low ESR such as ceramic capacitors, electro-conductive polymer hybrid aluminum electrolytic capacitors, etc.
・ Increase of capacitance value

Rated ripple current is specified for these capacitors.
Pay attention to prevent RMS value $I_{CO(RMS)}$ of output ripple current, obtained by the following formula, from exceeding rated ripple current.
The RMS values of the ripple current that can be obtained in the following equation must not exceed the rated ripple current.

$$I_{CO(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \quad [A]$$

Where:

$I_{CO(RMS)}$ is the value of the ripple electric current

In addition, total value of capacitance with output line $C_{O(Max)}$, respect to C_O, choose capacitance value less than the value obtained by the following equation.

$$C_{O(MAX)} = \frac{T_{SS(MIN)} \times (I_{SW\_OCP(MIN)} - I_{SWSTART(MAX)})}{V_O} \quad [F]$$

Where:
$I_{SW\_OCP(Min)}$ is the OCP operation switch current (Min)
$T_{SS(Min)}$ is the Soft Start Time (Min)
$I_{SWSTART(Max)}$ is the maximum output current during startup

When the conditions shown above are not followed, startup failure, etc. may occur. Especially when capacitance value is extremely large, overcurrent protection may operate due to inrush current at the time of startup and output may fail to start. Confirm the capacitance value well with the set. Transient responsiveness and stable operation of loop depend on C_O. Select it after confirming setting of phase compensation circuit. When input voltage variation and load variation are big, decide capacitance value after confirming it with actual application corresponding to specifications.

(3) Selection of Input Capacitor

Ceramic capacitor is necessary for input capacitor. Ceramic capacitor is effective when placed as close as possible to PVIN terminal. One with capacitance value of 11μF or higher and with rated voltage of 1.2 or more times as high as maximum input voltage and twice or more as high as normal input voltage is recommended. Set the capacitance value not to be lower than minimum values including variation, temperature characteristics, DC bias property and aging. Since malfunction may occur depending on substrate patterns and capacitor positions, refer to precautions on substrate layout (p. 27 to 29) for designing.

In that case, please consider not to exceed the rated ripple current of the capacitor.
The ripple current I_{RMS} can be calculated using the following equation.

$$I_{CIN(RMS)} = I_{O(MAX)} \cdot \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \quad [A]$$

Where:
$I_{CIN(RMS)}$ is the RMS value of the input ripple electric current

As for capacitance values, high capacitance is required when input-side impedance is high, such as when wiring from power source to PVIN terminal is long. It is necessary to verify under actual use conditions that there is no operation problem such as output off state and overshoot of output due to reduction of V_{IN} during transient response

(4) Setting the Output Voltage

The output voltage is determined by the equation below.

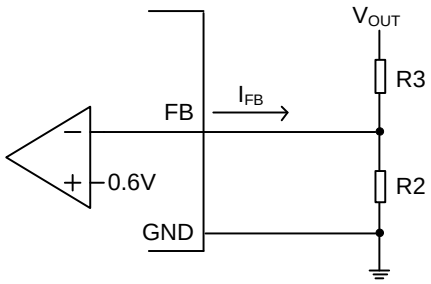
$$V_O = 0.6 \times \frac{R3+R2}{R2} \quad [V]$$

Set feedback resistance R2 at 30kΩ or lower in order to minimize error due to bias current. Set current flowing in feedback resistance sufficiently small against output current I_O, since power efficiency is reduced when R1 + R2 is small.

Whereas output voltage can be set to 0.6 V or higher, it is limited by SW minimum ON time depending on setting of input voltage and oscillation frequency. The minimum settable output voltage, V_{OUTMIN}, is determined by the following expressions.

$$V_{OUTmin} \geq \{ PVIN - I_{OUT} \times (R_{ON\_SW\_H\_min} - R_{ON\_SW\_L\_min}) \} \times f_{typ} \times T_{SW\_ON\_max} - I_{OUT} \times R_{ON\_SW\_L\_min} \quad [V]$$

Where:
$R_{ON\_SW\_H}$ is the ON-Resistance H min (60mΩ)
$R_{ON\_SW\_L}$ is the ON-Resistance L min (45mΩ)
f_{typ} is the typ.Frequency (setting RT value)
$T_{SW\_ON\_max}$ is SW Min ON time
(90ns with load,110ns without load)



The values shown above are values at 25°C. Though SW minimum ON time tends to increase when temperature rises, variation due to temperature change is cancelled because SW ON resistance tends to increase and oscillation

frequency tends to decrease at the same time. Note that the calculation formula shown above is theoretical. Actual properties may vary depending on substrate layout, properties of external parts, etc.

(5) Selection of Schottky Diode

The Schottky diode is optional. Depending on the application, efficiency may be improved by addition of Schottky diode between SW terminal and PGND terminal to create current route for the time synchronous switch (Nch FET) is off. Select Schottky diode with reverse breakdown voltage higher than input voltage and with rated current higher than maximum inductor current (sum of maximum output current and inductor ripple current).

(6) Setting the Oscillating Frequency

Internal oscillation frequency is set based on the value of resistance connected between RT terminal and GND. The setting range is between 0.3MHz and 2.4MHz. Relation between resistance value and oscillation frequency is determined as shown in the drawing below. Note that operation is not assured when the setting is out of the range, which may cause switching to stop.

R6 [kΩ]	F [kHz]
910	310
680	400
510	520
430	600
300	830
240	1000
160	1400
130	1650
110	1880
100	2000
91	2150
82	2300
75	2450

R6 vs f_{SW}

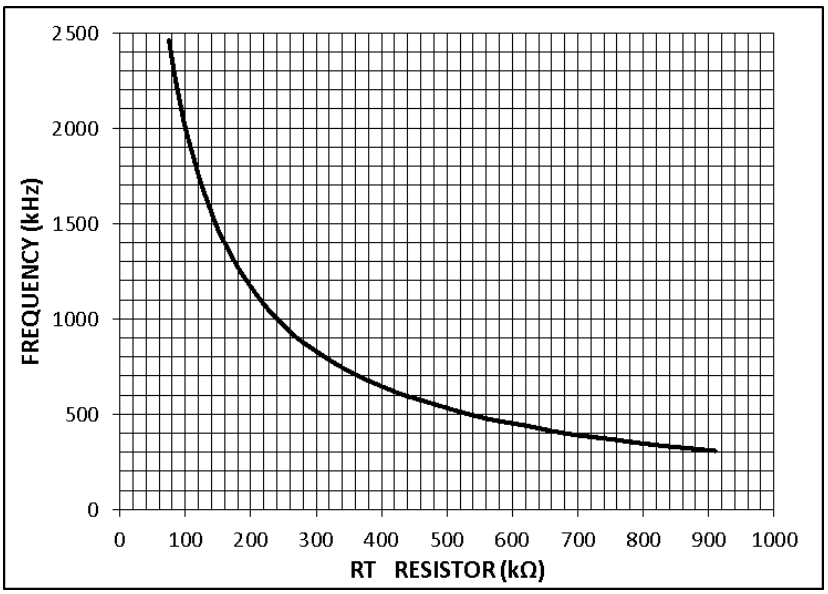


Figure 18. R6 vs f_{SW}

(7) Setting the Phase Compensation Circuit

High response function is realized by setting zero cross frequency f_C of total gain (frequency of gain 0 dB) high. However, please note that it is a trade-off with stability.

Furthermore, since switching regulator application is sampled by switching frequency, and gain in switching frequency needs to be suppressed, zero cross frequency needs to be set to 1/10 or lower of switching frequency. Characteristics aimed at by application are as follows.

Phase-lag when gain is 1 (0 dB) is within 135° (phase margin is 45° or more).

Zero cross frequency is 1/10 or lower of switching frequency.

In order to improve responsiveness, switching frequency needs to be increased.

Phase compensation is set with capacitor and resistance connected to COMP terminal. System stability is obtained by inserting phase lead fz1 against influence of two phase-lags fp1 and fp2 to cancel them. fp1, fp2 and fz1 are determined as shown in the following formula.

$$f_Z1 = \frac{1}{2\pi \times R1 \times C1} \quad [\text{Hz}]$$

$$f_P1 = \frac{1}{2\pi \times C_O \times R_O} \quad [\text{Hz}]$$

$$f_P2 = \frac{G_{EA}}{2\pi \times C1 \times A_V} \quad [\text{Hz}]$$

Frequency characteristics can be optimized by setting appropriate frequencies for the pole and zero.
The typical setting is as below.

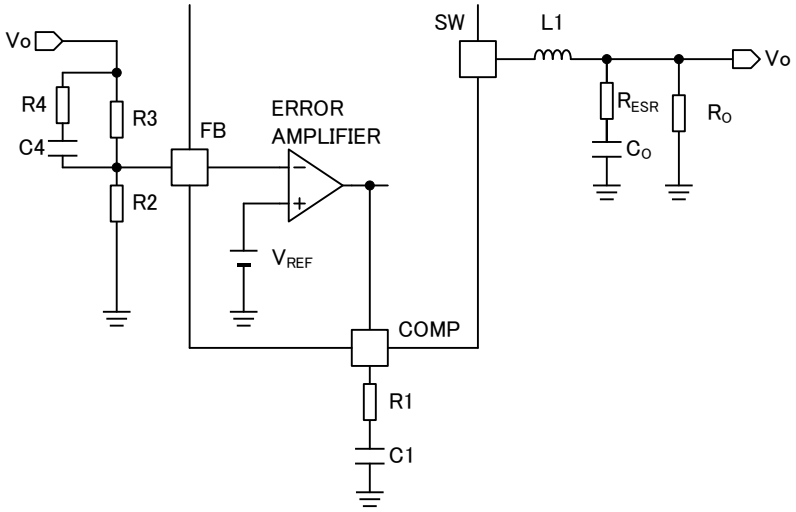
$$0.2 \times f_P1 \leqq f_Z1 \leqq 2 \times f_P1 \quad [\text{Hz}]$$

Furthermore, phase lead fz2 can be added by inserting of C4 capacitor.

$$f_Z2 = \frac{1}{2\pi \times R3 \times C4} \quad [\text{Hz}]$$

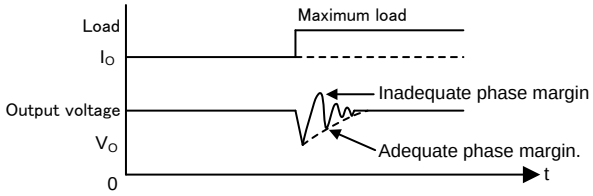
Where:

R_O is the resistance assumed actual load[Ω] = Output Voltage[V] / Output Current[A]、
G_{EA} is the Error Amp Transconductance (310 μA / V)
A_V is the Error Amp Voltage Gain (60 dB)



Setting Phase Compensation Circuit

Actually, characteristics will vary depending on PCB layout, arrangement of wiring, kinds of parts used and use conditions (temperature, etc.). Be sure to check stability and responsiveness with actual apparatus. Gain phase analyzer or FRA is used to check frequency characteristics with actual apparatus. Contact the measurement apparatus manufacturer for measurement method, etc. When these measurement apparatuses are not available, there is a method of assuming margin by load response. Variation of output when the apparatus shifts from no load state to maximum load is monitored, and it can be said that responsiveness is low if variation amount is large, and phase margin is small if ringing occurs frequently (twice or more as a guide) after variation.
However, confirmation of quantitative phase margin is not possible.



Measurement of Load Response

(8) Setting the Soft Start Time

Soft start is necessary for prevention of overshoot of output voltage at startup. Soft start time varies depending on capacitance value of capacitor connected between “SS” terminal and “GND” terminal. Set the startup time on input voltages, VIN and PVIN, earlier than soft start time. Capacitance value of 2200pF to 0.047μF is recommended.

$$\boldsymbol{T_{SS} = \frac{C3 \times 0.6}{|Iss|}} \text{ [s]}$$

(9) Setting the Input filter (R_{IN}, $C_{IN}2$)

Since V_{IN} is used as power source voltage for internal control circuit, input filter for VIN terminal is necessary in order to prevent malfunction due to transient V_{IN} variation. Connect R_{IN} of 10Ω and $C_{IN}2$ of 1μF. It is necessary to verify under actual use conditions that there is no operation problem such as output off state and overshoot of output due to reduction of V_{IN} during transient response.

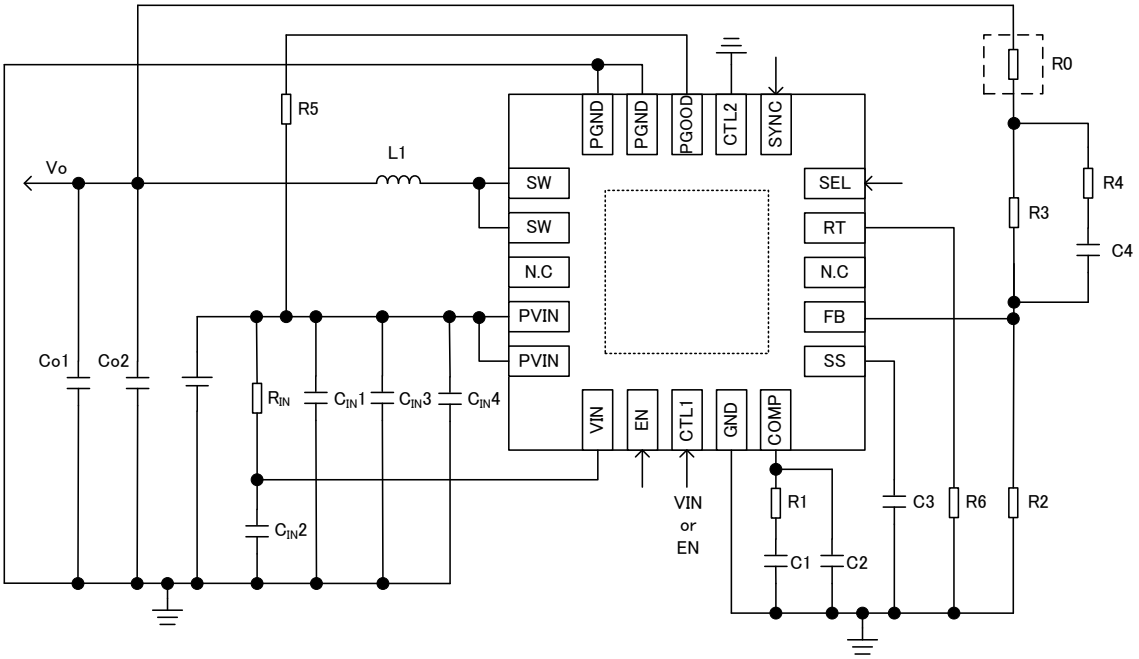
Recommended Parts Manufacturer List

Shown below is the list of the recommended parts manufacturers for reference.

Type	Manufacturer	URL
Electrolytic capacitor	NICHICON	www.nichicon.com
Ceramic capacitor	MURATA	www.murata.com
Coil	TDK	www.global.tdk.com
Coil	Coilcraft	www.coilcraft.com
Coil	Sumida	www.sumida.com
Diode/Resistor	ROHM	www.rohm.com

Application Examples 1

Parameter	Symbol	Specification case
Input Voltage	V_{IN}	5V
Output Voltage / Output Current	V_O / I_O	1.2V / 2A
Switching Frequency	f_{SW}	2.0MHz
Soft Start time	T_{SS}	1ms
Operating Temperature	Ta	-40 to +105°C



No	Package	Parameters	Part Name(series)	Type	Manufacturer
L1	W6.9 x H7.2 x L4.5 mm^3	1µH	CLF7045-D Series	Inductor	TDK
CO1	3216	22µF, X7R, 6.3V	GCM Series	Ceramic Capacitor	MURATA
CO2	3216	22µF, X7R, 6.3V	GCM Series	Ceramic Capacitor	MURATA
CIN1	3225	22µF, X7R, 10V	GCM Series	Ceramic Capacitor	MURATA
CIN2	1608	1µF, X7R, 16V	GCM Series	Ceramic Capacitor	MURATA
CIN3	-	-	-	-	-
CIN4	1608	0.01µF, X7R, 50V	GCM Series	Ceramic Capacitor	MURATA
RIN	1608	10Ω, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R0	-	SHORT	-	-	-
R1	1608	10kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R2	1608	30kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R3	1608	30kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R4	-	-	-	-	-
R5	1608	10kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R6	1608	100kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
C1	1608	2200pF, R, 50V	GCM Series	Ceramic Capacitor	MURATA
C2	-	-	-	-	-
C3	1608	3300pF, R, 50V	GCM Series	Ceramic Capacitor	MURATA
C4	-	-	-	-	-

Reference data of Application Example 1

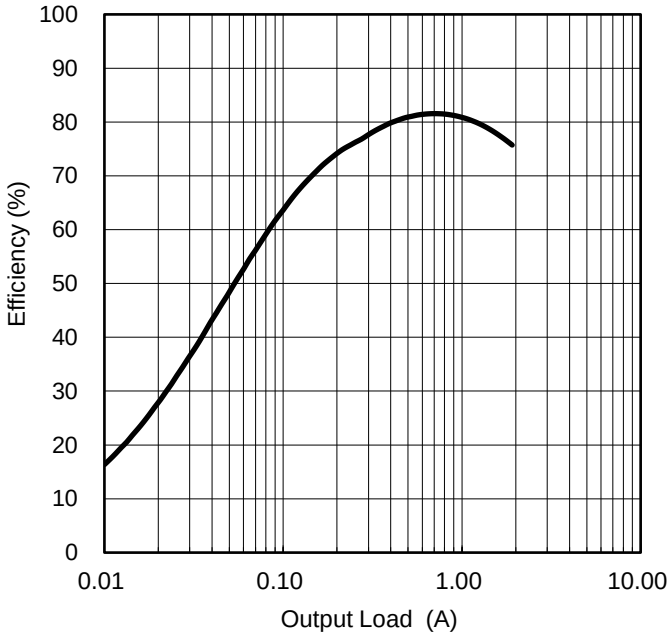


Figure 19. Efficiency vs Output Load

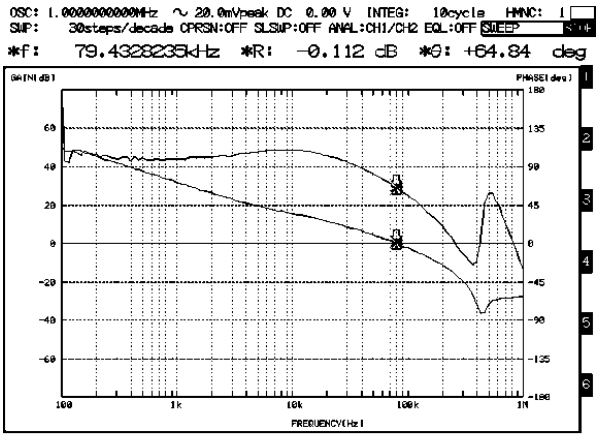


Figure 20. Loop Response, I_O = 2A

Output Load (A)

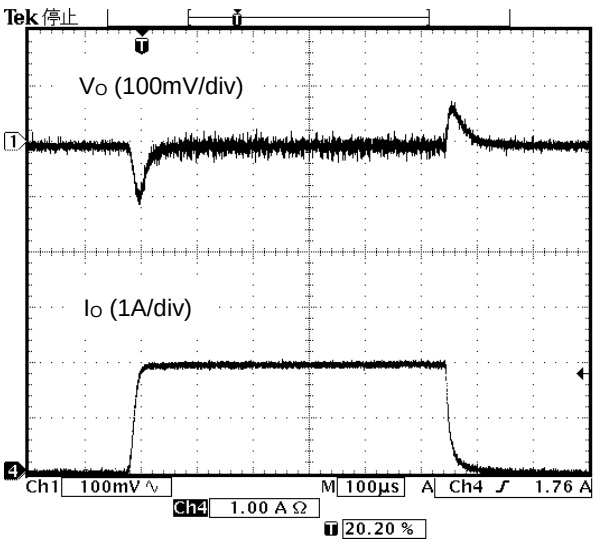


Figure 21. Load Response, I_O=0A⇔2A

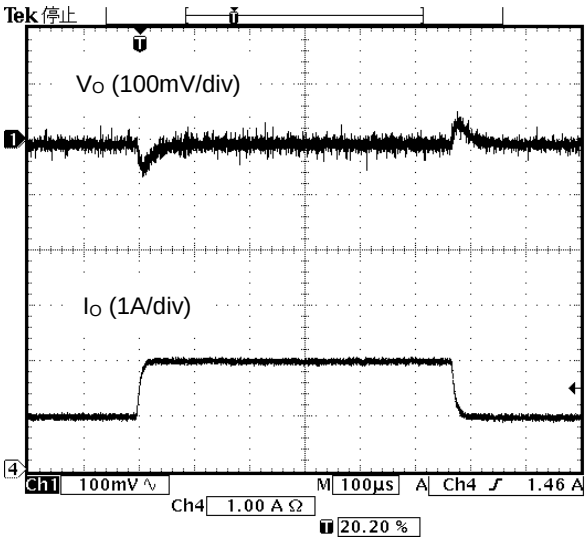
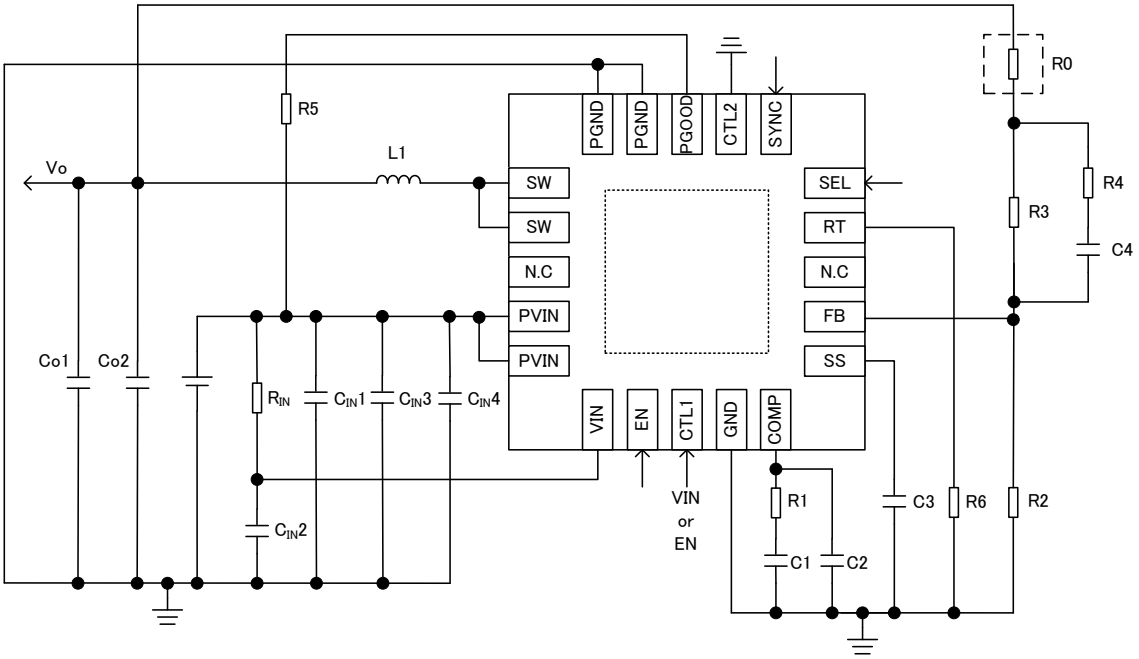


Figure 22. Load Response, I_O=1A⇔2A

Application Examples 2

Parameter	Symbol	Specification case
Input Voltage	V_{IN}	5V
Output Voltage / Output Current	V_O / I_O	3.3V / 2A
Switching Frequency	f_{SW}	2.0MHz
Soft Start time	T_{SS}	1ms
Operating Temperature	Ta	-40 to +105°C



No	Package	Parameters	Part Name(series)	Type	Manufacturer
L1	W6.9 x H7.2 x L4.5 mm^3	1µH	CLF7045-D Series	Inductor	TDK
CO1	3216	22µF, X7R, 6.3V	GCM Series	Ceramic Capacitor	MURATA
CO2	3216	22µF, X7R, 6.3V	GCM Series	Ceramic Capacitor	MURATA
CIN1	3225	22µF, X7R, 10V	GCM Series	Ceramic Capacitor	MURATA
CIN2	1608	1µF, X7R, 16V	GCM Series	Ceramic Capacitor	MURATA
CIN3	-	-	-	-	-
CIN4	1608	0.01µF, X7R, 50V	GCM Series	Ceramic Capacitor	MURATA
RIN	1608	10Ω, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R0	-	SHORT	-	-	-
R1	1608	20kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R2	1608	10kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R3 (1)	1608	30kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R3 (2)	1608	15kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R4	-	-	-	-	-
R5	1608	10kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
R6	1608	100kΩ, 1%, 1/16W	MCR03 Series	Chip resistor	ROHM
C1	1608	2200pF, R, 50V	GCM Series	Ceramic Capacitor	MURATA
C2	-	-	-	-	-
C3	1608	3300pF, R, 50V	GCM Series	Ceramic Capacitor	MURATA
C4	-	-	-	-	-

(Note) Please set to 45kΩ to combine 30 kΩ and 15 kΩ about R3.

Reference data of Application Example 2

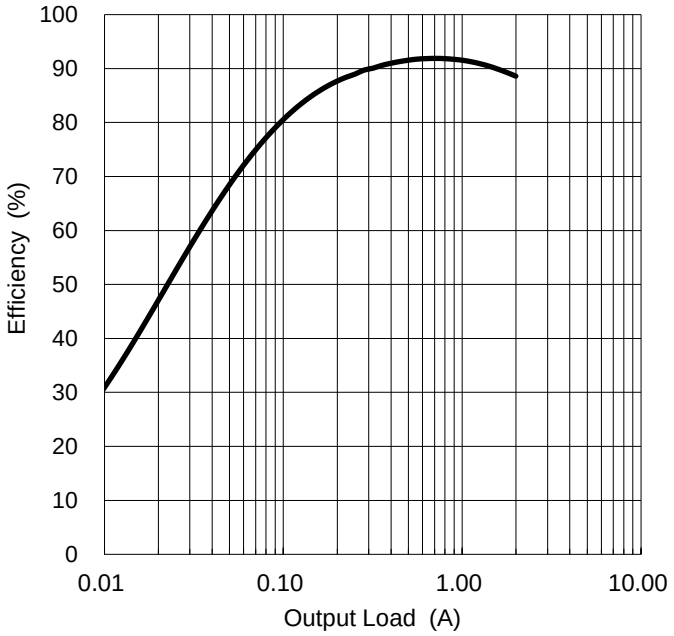


Figure 23. Efficiency vs Output Load

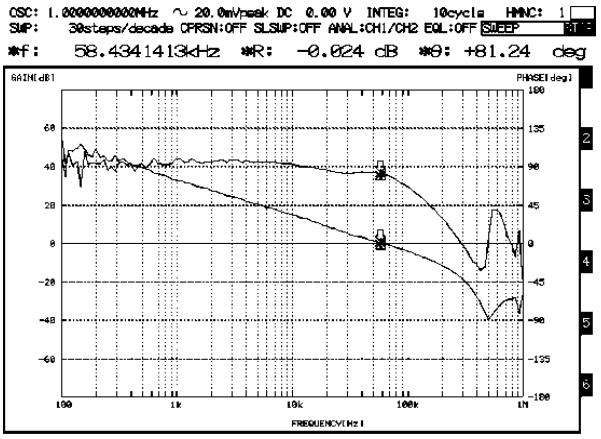


Figure 24. Loop Response, I_O = 2A

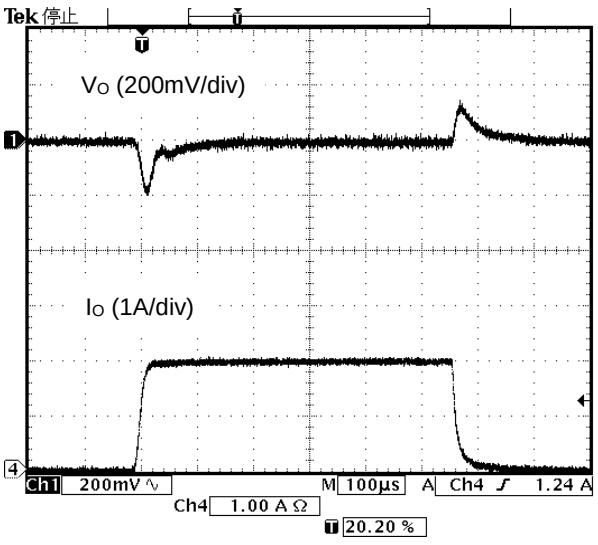


Figure 25. Load Response, I_O=0A⇔2A

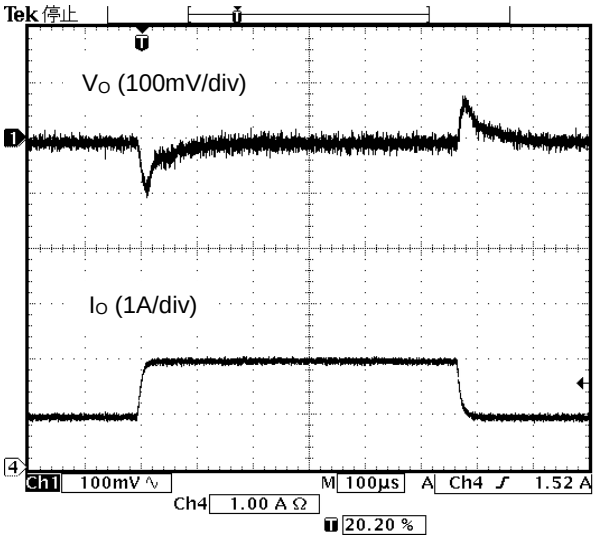
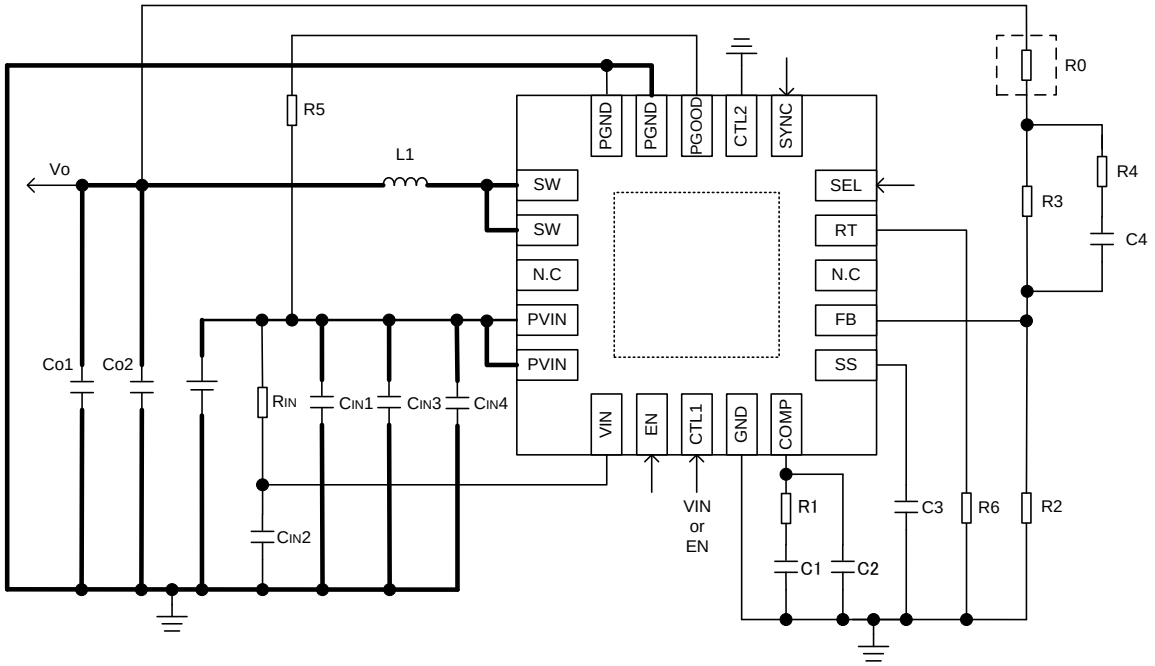


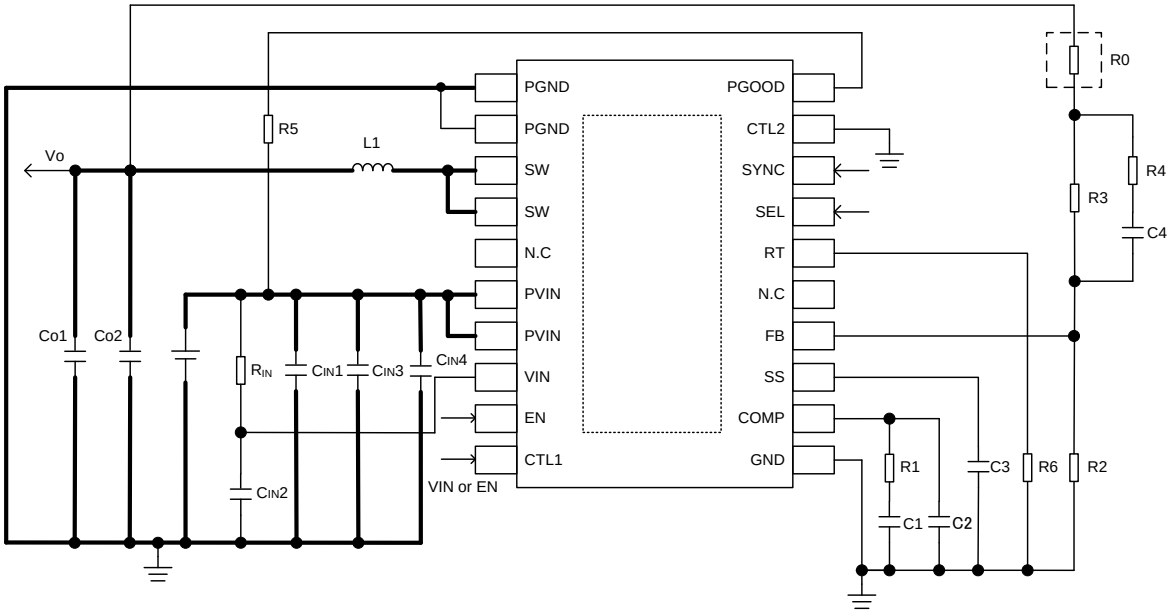
Figure 26. Load Response, I_O=1A⇔2A

Notes on the PCB Layout



Exposed die pad is needed to be connected to GND.

Application Circuit (VQFN20SV4040)



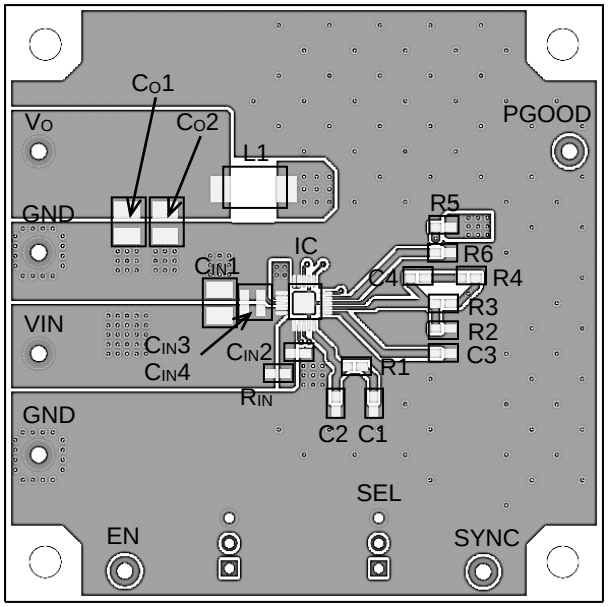
Exposed die pad is needed to be connected to GND.

Application Circuit (HTSSOP-B20)

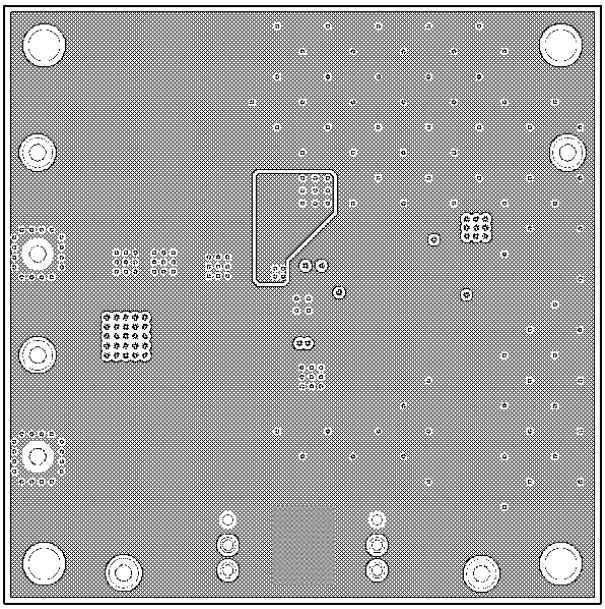
① Make bold line part as short as possible in wide pattern.
② Arrange input ceramic capacitors CIN1, CIN3 and CIN4 as close as possible to PVIN terminal and PGND terminal. Arrange CIN2 as close as possible to VIN terminal and GND terminal.
③ Arrange R6 as close as possible to RT terminal.
④ Arrange R2 and R3 as close as possible to FB terminal to shorten wirings from R2 and R3 to FB terminal.
⑤ Arrange R2 and R3 as far as possible from L1.
⑥ Influence of SW noise can be reduced by separating power system (input/output capacitor) GND from reference system (RT, COMP) GND. Connect them in common GND layers as shown in the layout in the next section.
⑦ R0 is for measurement of frequency characteristics of feedback and is optional.
Insertion of resistance in R0 enables measurement of frequency characteristics of feedback (phase margin) using FRA, etc. Under normal conditions, it is shorted.

Reference layout pattern

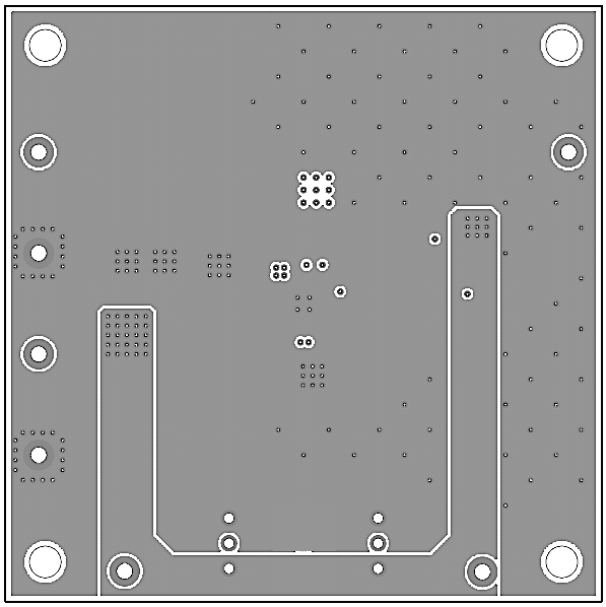
VQFN20SV4040 Reference PCB Layout (TOP VIEW)



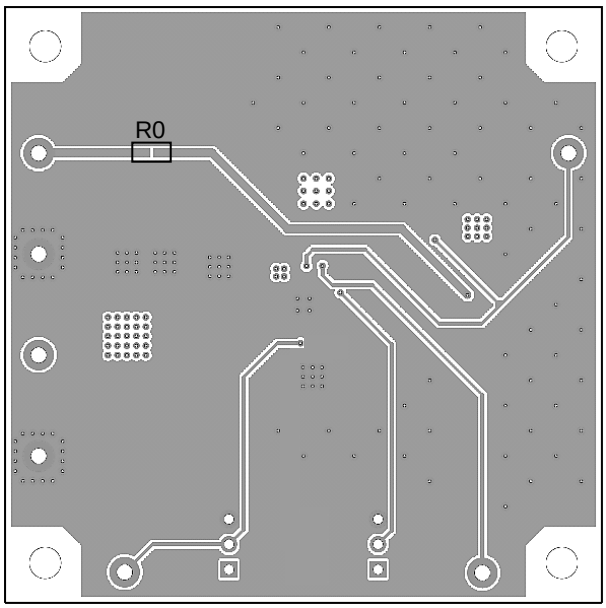
TOP Layer



Middle 1 Layer

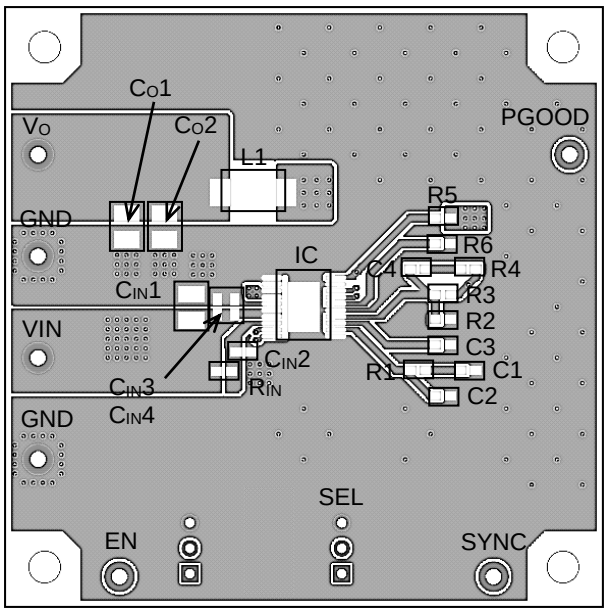


Middle 2 Layer

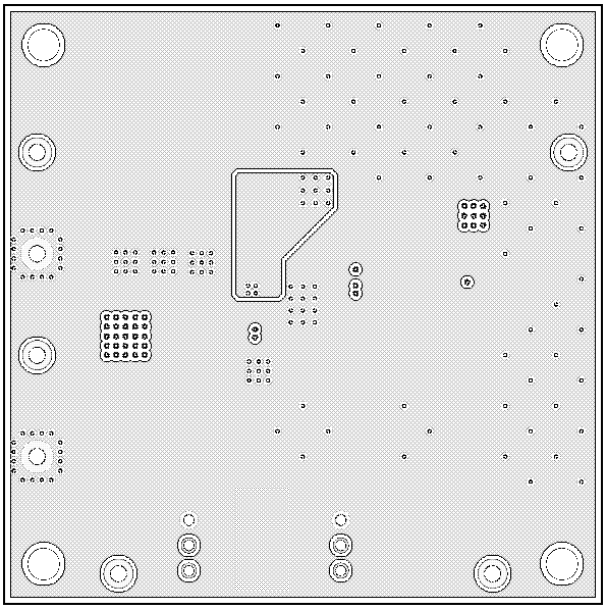


Bottom Layer

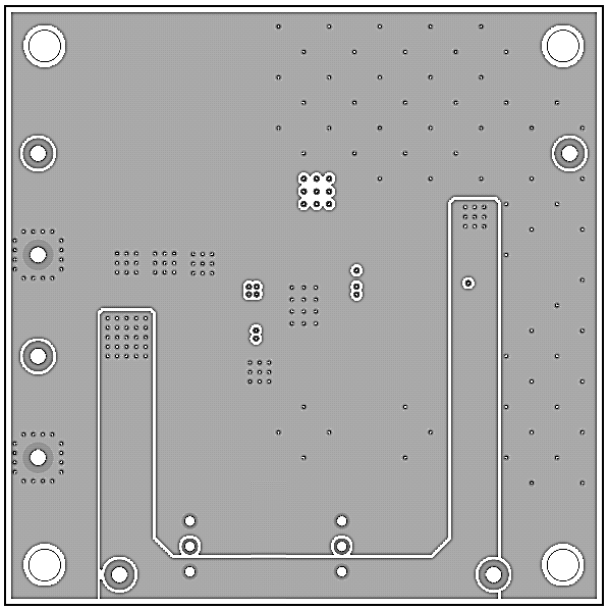
HTSSOP-B20 Reference PCB Layout (TOP VIEW)



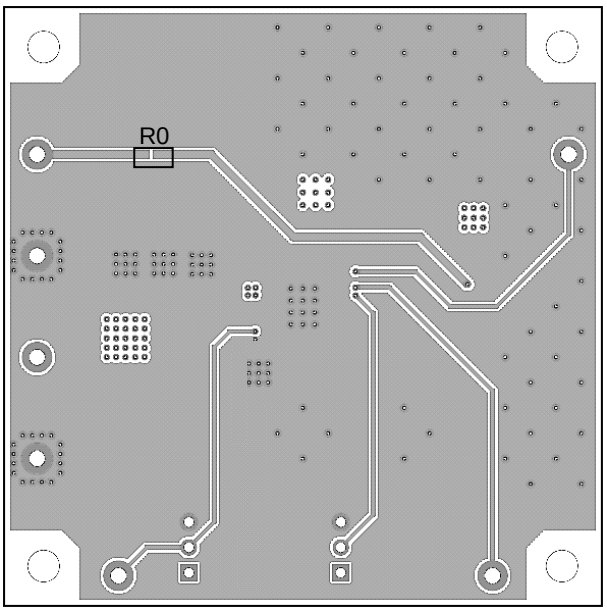
TOP Layer



Middle 1 Layer



Middle 2 Layer



Bottom Layer

Power Dissipation

In thermal design, operate under following conditions.
(Temperatures described below are guaranteed temperatures. Be sure to consider margin, etc.)

1. Ambient temperature Ta shall be 125°C or lower.
2. Chip junction temperature Tj shall be 150°C or lower.

Chip junction temperature Tj can be considered in following 2 ways.

① When obtained from temperature Tt at the center of top surface of package under actual use conditions:

$$Tj = Tt + \psi_{JT} \times P_{TOTAL}$$

② When obtained from actual ambient temperature Ta:

$$Tj = Ta + \theta ja \times P_{TOTAL}$$

＜Reference Value＞VQFN020SV4040
θjc
Top : 40 °C /W
Bottom : 15 °C /W
θjc
153.9 °C / W 1-layer PCB
37.4 °C / W 4-layer PCB
ψJT
13 °C /W 1-layer PCB
7 °C /W 4-layer PCB
PCB Size 114.3 mm x 76.2 mm x 1.6 mm

＜Reference Value＞HTSSOP-B20
θjc
Top : 25 °C /W
Bottom : 9 °C /W
θjc
143.0 °C / W 1-layer PCB
26.8 °C / W 4-layer PCB
ψJT
8 °C /W 1-layer PCB
4 °C /W 4-layer PCB
PCB Size 114.3 mm x 76.2 mm x 1.6 mm

The heat loss P_{TOTAL} of the IC can be obtained by the formula shown below:

$$P_{TOTAL} = P_{ICC} + P_{RON} + P_{SW} \quad [W]$$

$$P_{ICC} = V_{IN} \times I_{IN} \quad [W] \quad \cdots \text{Heat dissipation in control circuit}$$

$$P_{RON} = R_{ON} \times {I_O}^2 \quad [W] \quad \cdots \text{Heat dissipation in output FET}$$

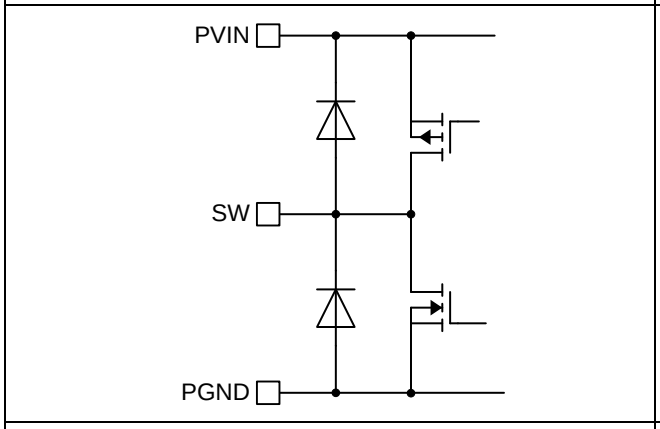
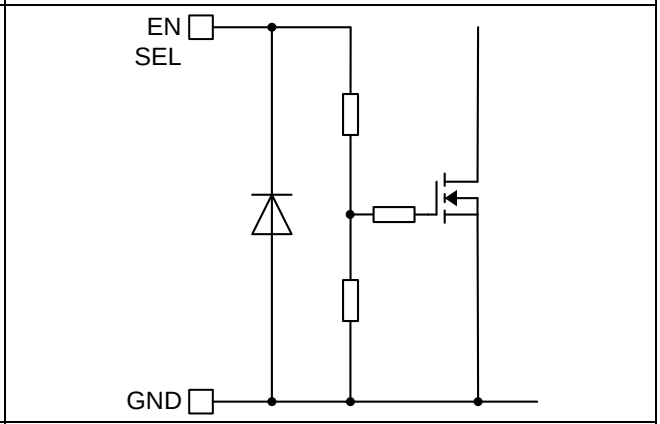
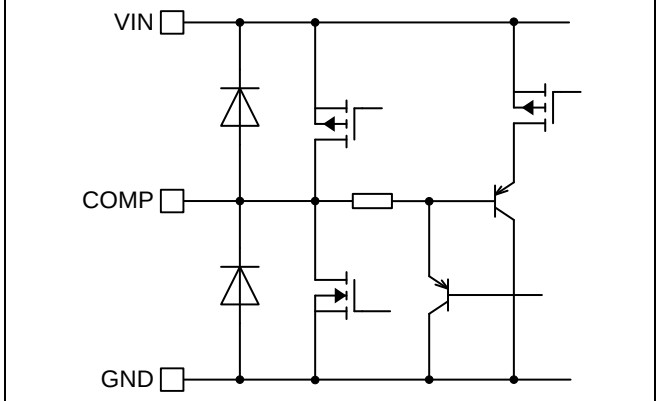
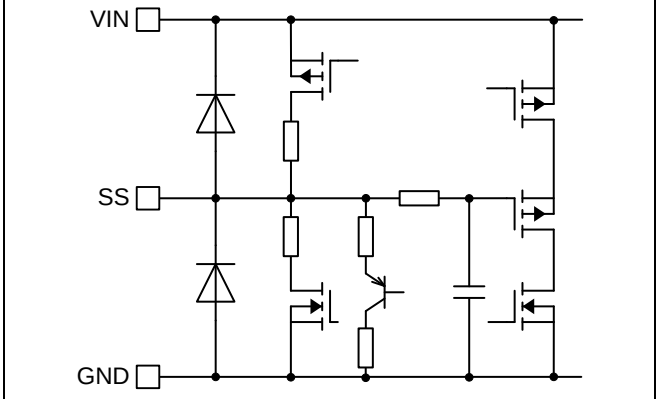
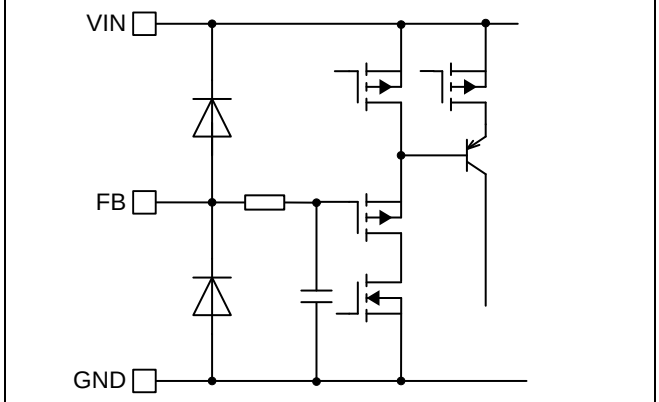
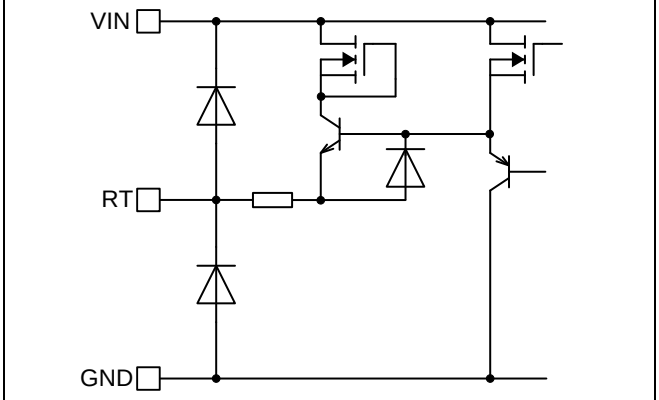
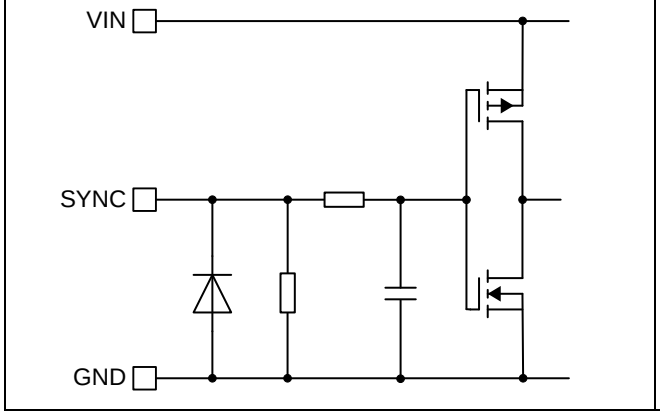
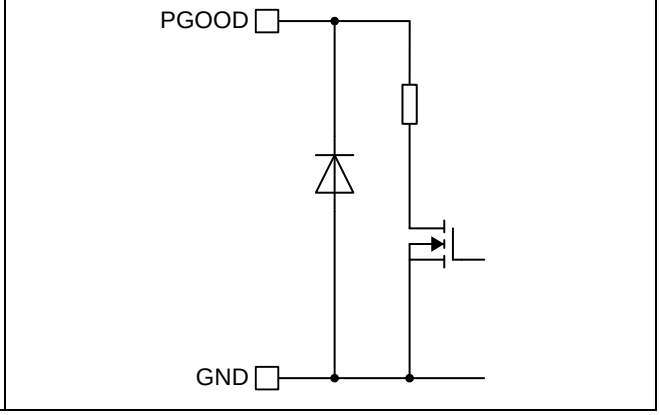
$$R_{ON} = D \times R_{ON\_SW\_H} + (1 - D) \times R_{ON\_SW\_L} \quad [\Omega] \quad \cdots \text{On Resistance in output FET}$$

$$D = \frac{V_O}{V_{IN}} \quad \cdots \quad \text{Switching pulse duty}$$

$$P_{SW} = tr \times I_O \times V_{IN} \times f_{SW} \quad [W] \quad \cdots \text{eat dissipation in switching}$$

$Where$:
V_{IN} is the input voltage [V]
I_{IN} is the circuit current [A]
I_O is the load current [A]
D is the switching pulse duty
$R_{ON\_SW\_H}$ is the H-side FET ON resistance [Ω]
$R_{ON\_SW\_L}$ is the L-side FET ON resistance [Ω]
Tr is the switching rise and fall time [S] (Typ:7ns)
f_{SW} is the oscillating frequency [Hz]

I/O Equivalent Circuits

SW	EN, SEL
	
COMP	**SS**
	
FB	**RT**
	
SYNC	**PGOOD**
	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

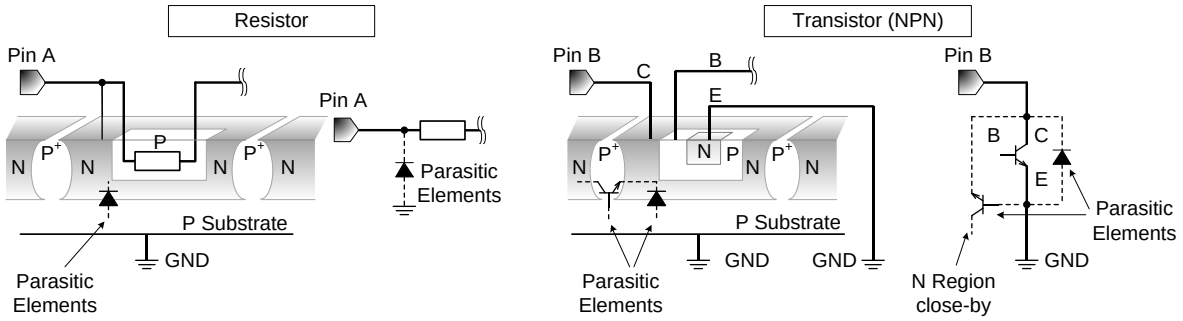


Figure 27. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

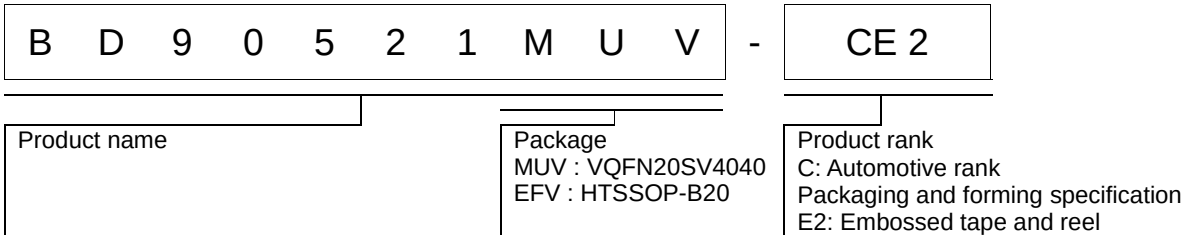
14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

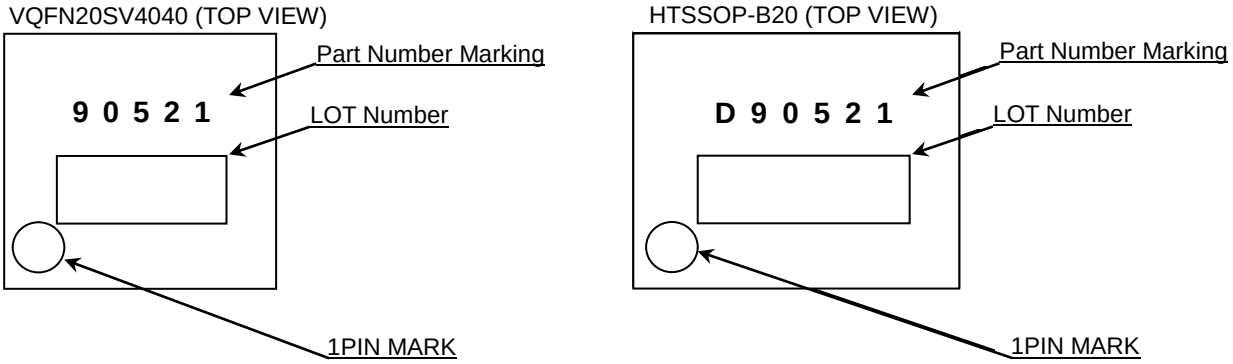
15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information



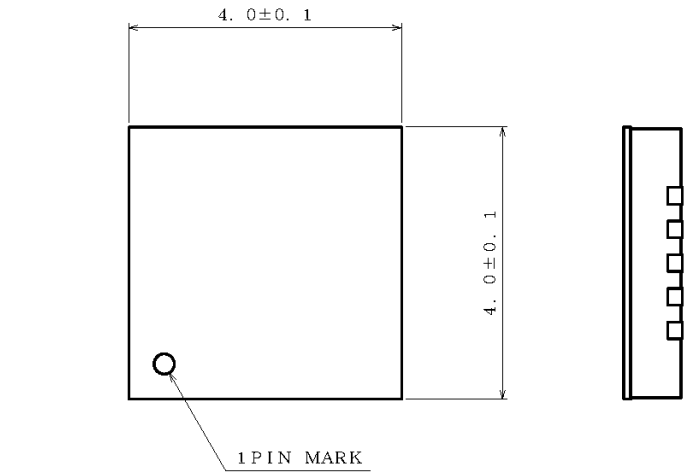
Marking Diagrams

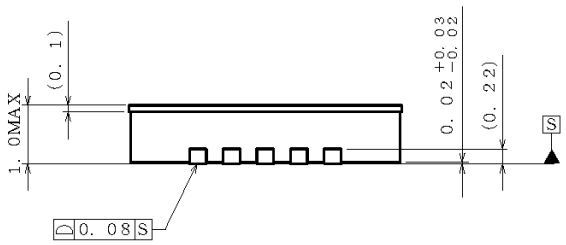


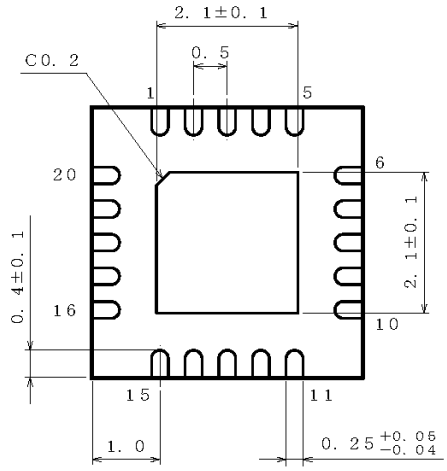
Marking	Package	Part Number Marking
90521	VQFN20SV4040	BD90521MUV-CE2
D90521	HTSSOP-B20	BD90521EFV-CE2

Physical Dimension, Tape and Reel Information

Package Name	VQFN20SV4040





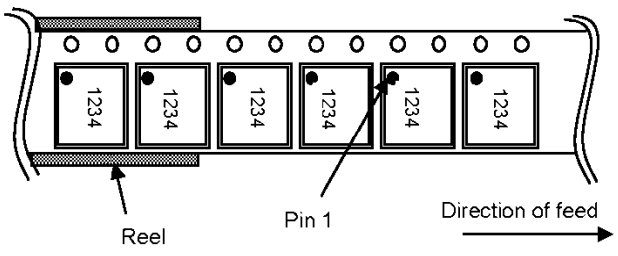


(UNIT : mm)

PKG : VQFN20SV4040
Drawing No. EX383-5001

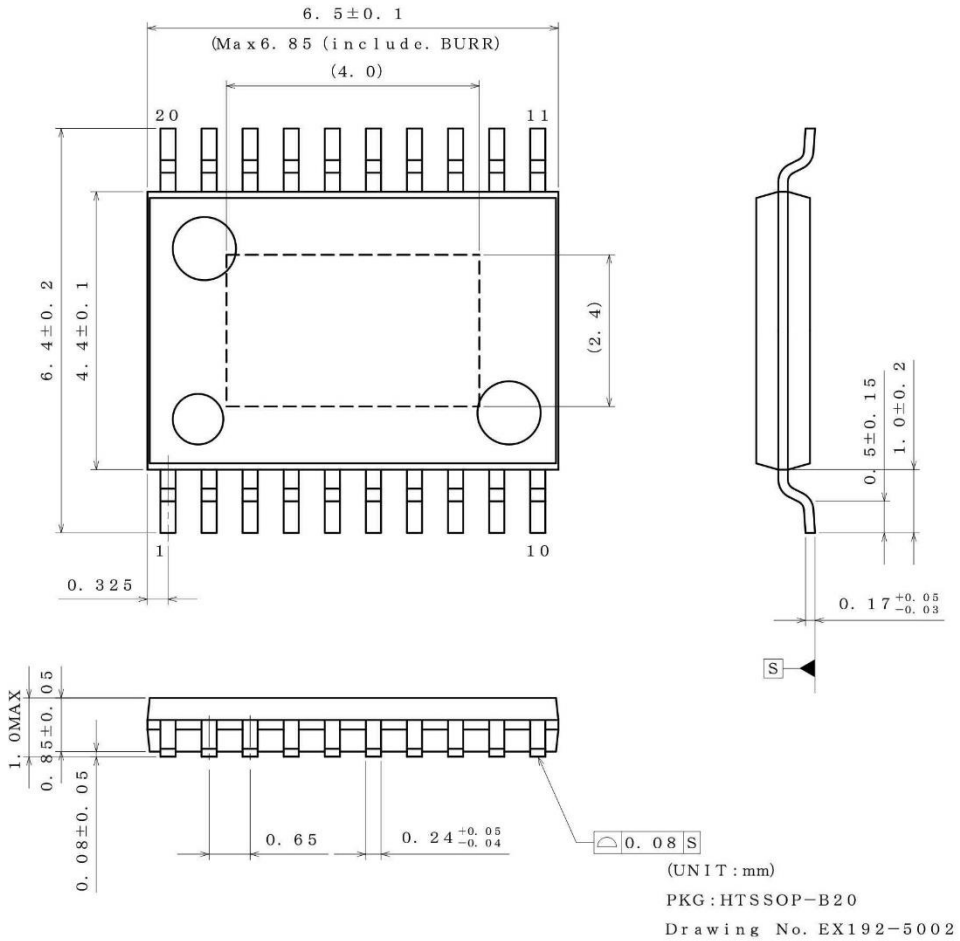
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



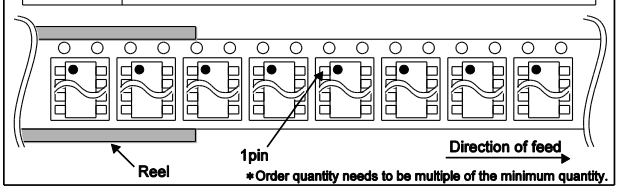
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B20



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
21.Apr.2016	001	New Release
24.Feb.2017	002	Revised Absolute Maximum Rating of EN Pin.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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