

EARTH LEAKAGE CURRENT DETECTOR EARTH LEAKAGE CURRENT DETECTOR IC



BD9582F, BD9582N

● **General Description**

BD9582F/BD9582N integrates leakage detector and amplifier. Especially, it is suitable for high sensitivity and a high-speed operation use, and since the operating temperature range is wide, it can be used for various uses.

● **Key Specifications**

- Operating supply voltage range : 12V to 22V
- Operating temperature range : -20°C to +95°C
- Supply current : 330 μA (typ.)
- Trip voltage : 4.92mV to 11.06mV
- Output current ability (Ta=-20°C) : -200 μA ~ (min.)

● **Features**

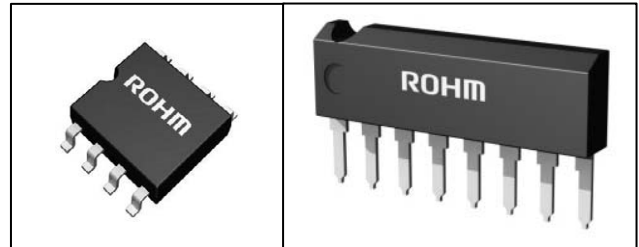
- Small temperature fluctuation and high input sensitivity
- Wide operating temperature range

● **Applications**

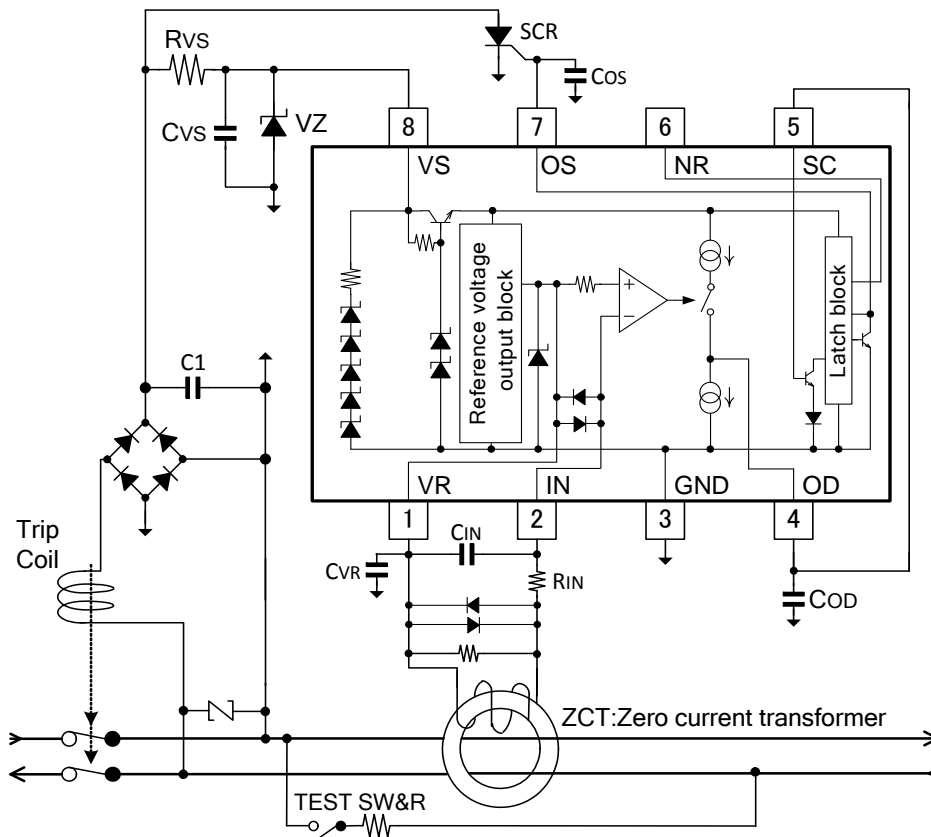
- Earth leakage circuit breaker
- Earth leakage circuit relay

● **Packages**

- | | |
|------|-----------------------------|
| SOP8 | W(Typ.) x D(Typ.) x H(Max.) |
| SIP8 | 5.00mm x 6.20mm x 1.71mm |
| | 19.30mm x 10.50mm x 3.00mm |

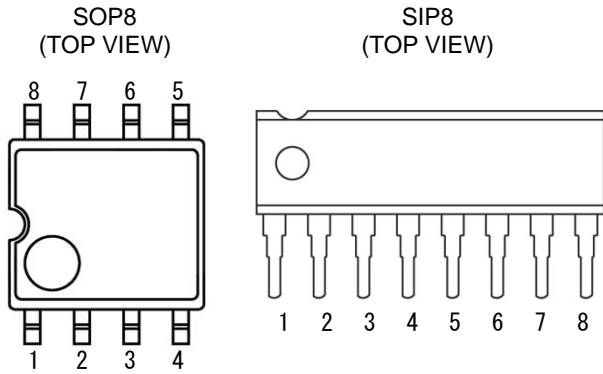


● **Typical Application Circuit Example**

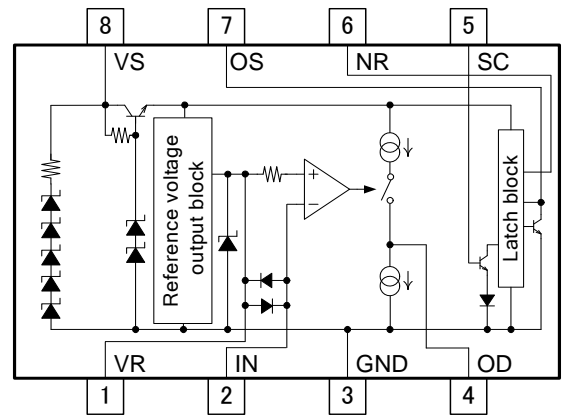


○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

●Pin Configurations



●Block Diagrams



●Pin Descriptions

Pin No.	Symbol	Function
1	VR	Reference voltage
2	IN	Input
3	GND	Ground
4	OD	Output of input comparator
5	SC	Input of latch circuit
6	NR	Noise absorption
7	OS	Output
8	VS	Power supply

●Absolute Maximum Ratings

(Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply current ^{*1}	IS	8	mA
IN-VR current	IIN-VR	±250	mA
VR pin current	IVR	30	mA
IN terminal current	IIN	30	mA
SC terminal current	ISC	5	mA
Power Supply voltage	VS	36	V
Input terminal voltage	VVR/IN	17	V
OD/SC/NR/OS terminal voltage	VOD/SC/NR/OS	8	V
Power dissipation	Pd	680(SOP8) ^{*2} 1120(SIP8) ^{*3}	mW
Storage temperature	Tstg	-55 to +150	°C

*1 The power-supply voltage is limited by the internal clamping circuit.

*2 To use at temperature above Ta=25°C reduce 5.5mW/°C. Mounted on a glass epoxy PCB (70mmx70mmx1.6mm)

*3 To use at temperature above Ta=25°C reduce 9.0mW/°C. Pd is a value in the package unit.

● Recommended Operating Ratings

Parameter	Symbol	Limits	Unit
Supply voltage	VS	12 to 22	V
Operating temperature	T _{opr}	-20 to +95	°C
External capacitor between VS and GND	C _{vs}	1 ≤	μF
External capacitor between OS and GND	C _{os}	≤ 1	μF

● Electrical Characteristics

(Unless otherwise specified, VS=12V, GND=0V, Ta=25°C)

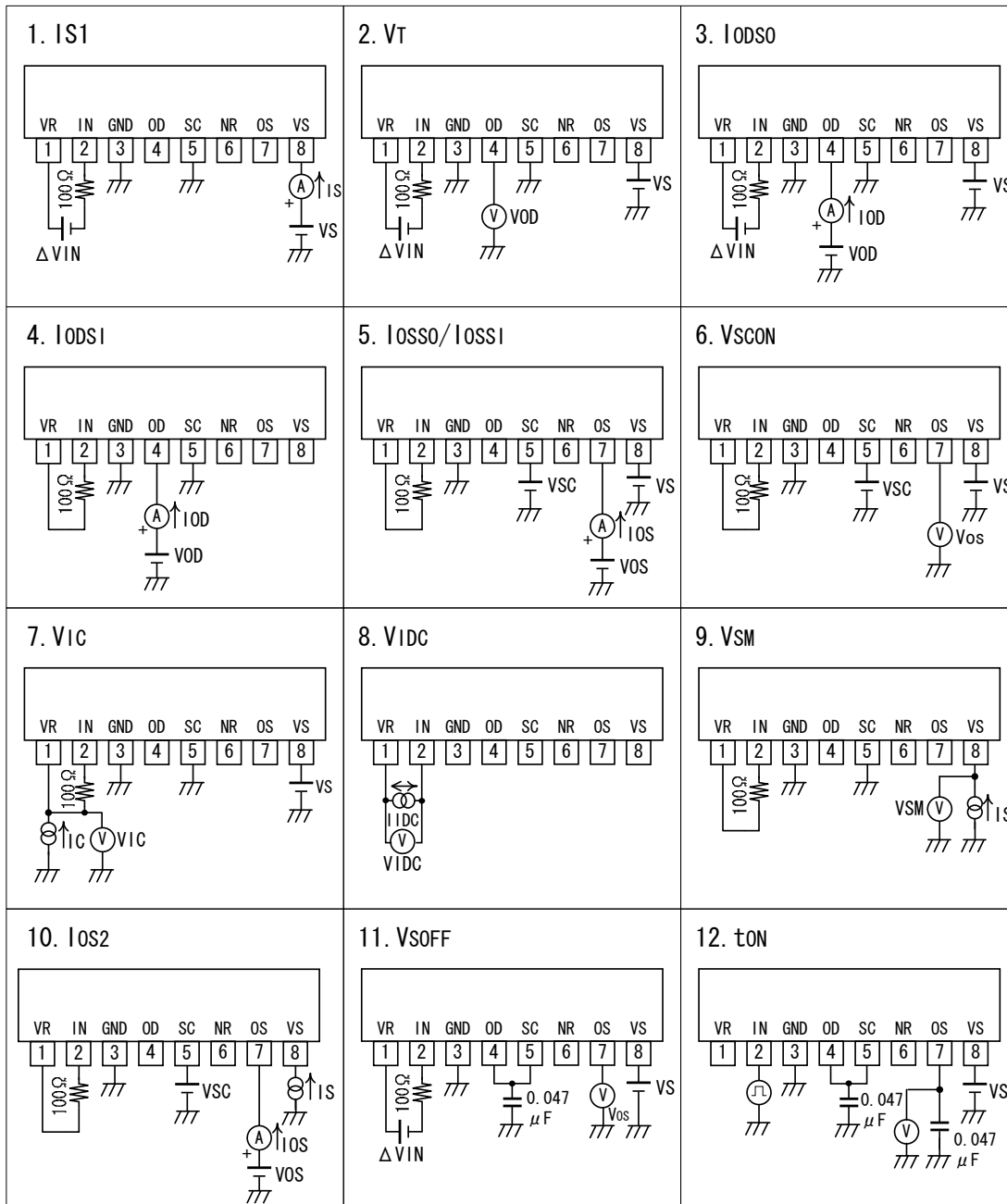
Parameter	Symbol	Temperature range	Limits			Unit	Conditions
			Min.	Typ.	Max.		
Supply current	IS1	120°C	-	-	520	μA	ΔVIN=VVR-VIN=30mV
		25°C	-	330	500		
		95°C	-	-	460		
Trip voltage	VT	-20°C to +95°C	4.92	7.50	11.06	mV	VT=ΔVIN=VVR-VIN
OD Source current	I _{ODSO}	25°C	-27.2	-20.6	-14.0	μA	ΔVIN=VVR-VIN=30mV, V _{OD} =1.2V
OD Sink current	I _{ODSI}	25°C	16.7	26.0	35.3	μA	V _{OD} =0.8V, ΔVIN=VVR-VIN=0mV
OS Source current	I _{OSSO}	-20°C	-200	-	-	μA	V _{sc} =2.0V, V _{os} =0.8V
		25°C	-100	-	-		
		95°C	-75	-	-		
OS Sink current	I _{OSSI}	-20°C to +95°C	200	-	-	μA	V _{sc} =0.2V, V _{os} =0.2V
SC ON voltage	V _{SCON}	25°C	1.00	1.24	1.48	V	
Input clamp voltage	V _{IC}	-20°C to +95°C	4.2	5.5	6.7	V	I _{IC} =20mA
Differential input clamp voltage	V _{IDC}	-20°C to +95°C	0.6	1.0	1.4	V	I _{IDC} =100mA
Maximum current voltage	V _{SM}	25°C	26	29	32	V	I _S =7mA
Supply current 2 *1	I _{OS2}	-20°C to +95°C	-100	-	-	μA	I _S =900μA, V _{sc} =2.0V, V _{os} =0.8V
Latch OFF Supply Voltage	V _{SOFF}	25°C	2.7	3.7	4.7	V	
Operating time *2	t _{ON}	25°C	1.8	2.9	4.0	ms	

*1 Supply current 2 is OS source current value when the power supply current(I_S=900μA) is given.

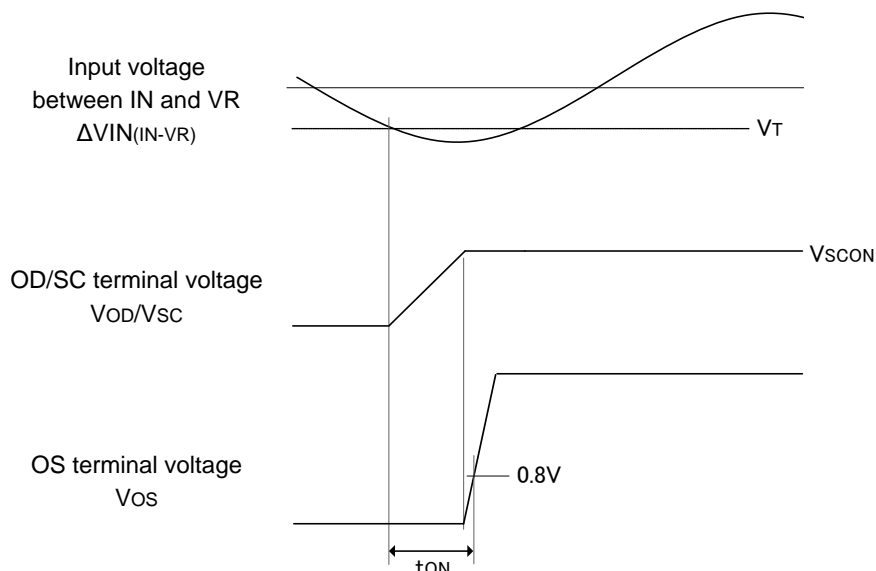
*2 Operating time is time until output voltage reaches 0.8V after detecting the leakage signal.

Conditions : Capacitor(0.047μF) is connected between OD(OS) and GND.

● Test circuits



● Timing Chart



● Typical Performance Curves(reference data)

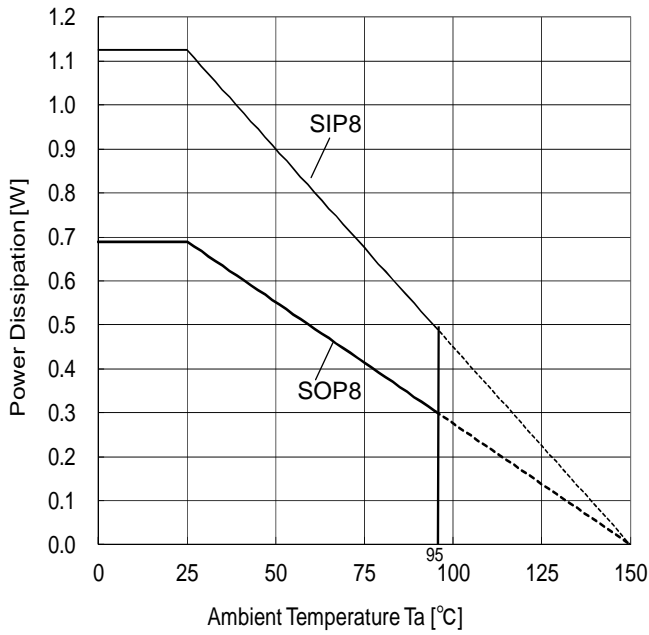


Figure 1
Derating curve

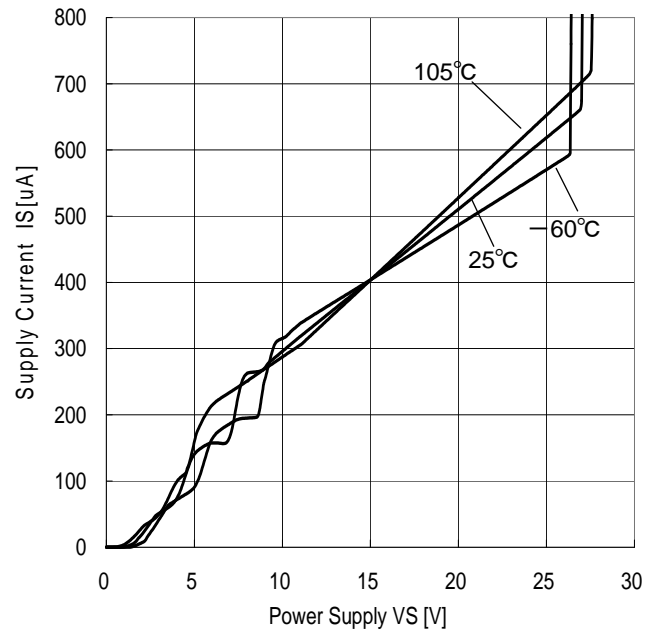


Figure 2
Circuit current - Supply voltage

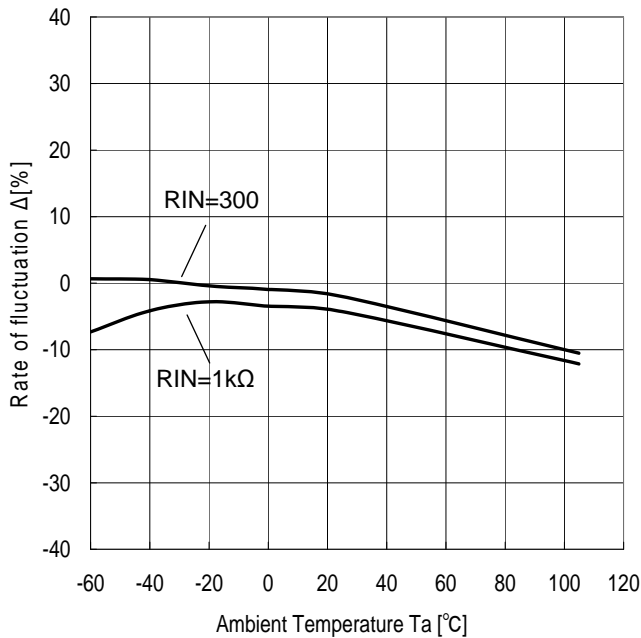


Figure 3
Trip voltage fluctuation rate
- Ambient temperature

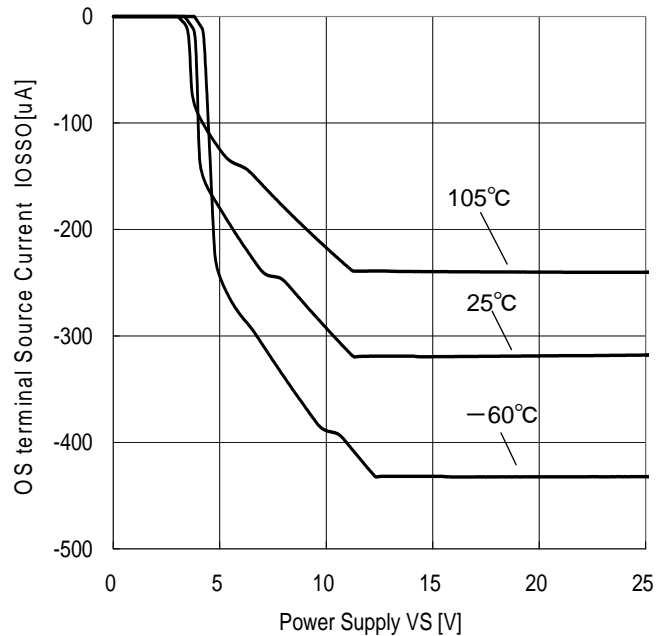


Figure 4
OS terminal source current - Supply voltage

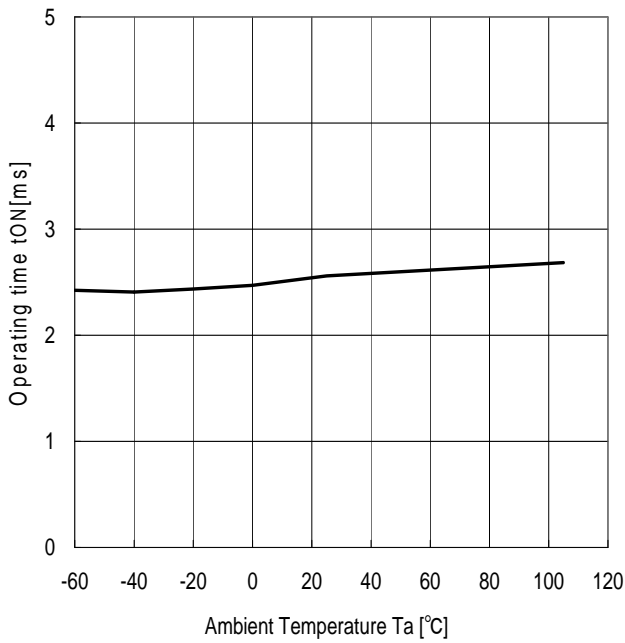


Figure 5
Operating time - Ambient temperature

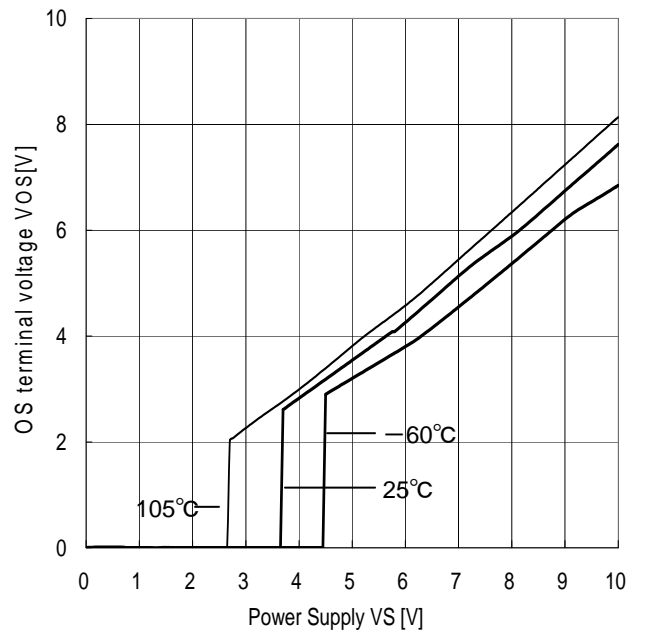


Figure 6
Latch OFF supply voltage - Ambient temperature

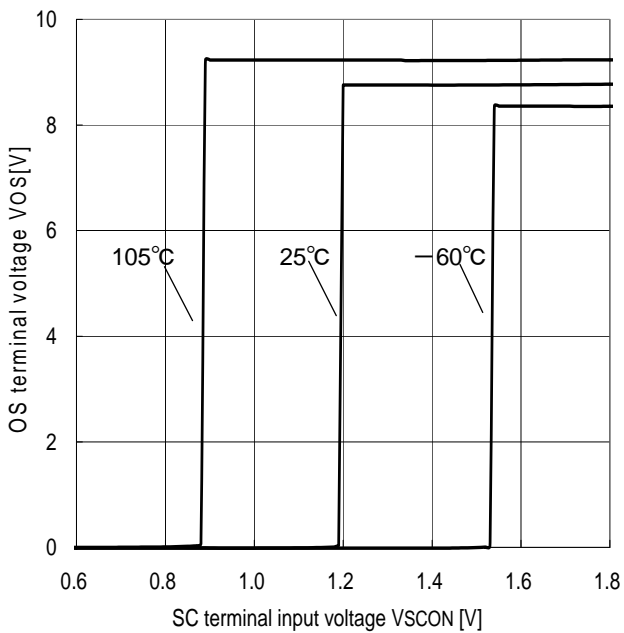


Figure 7
SC ON voltage - Ambient temperature

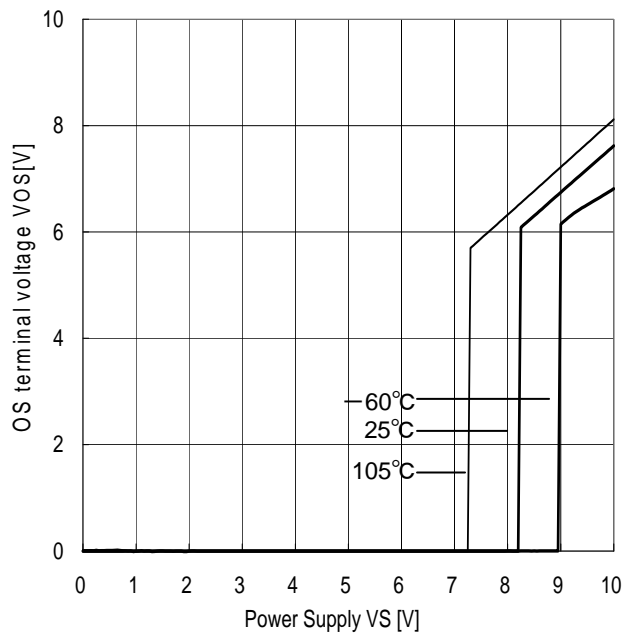


Figure 8
Latch ON supply voltage - Ambient temperature

● Power Dissipation

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25°C (normal temperature). IC is heated when it consumes power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θ_{ja} °C/W. The temperature of IC inside the package can be estimated by this thermal resistance. Fig.9(a) shows the model of thermal resistance of the package. Thermal resistance θ_{ja} , ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below

$$\theta_{ja} = (T_j - T_a) / P_d \quad \text{°C/W} \quad \dots \dots \dots (I)$$

Derating curve in Fig.9(b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{ja} . Thermal resistance θ_{ja} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig.10(a) shows a derating curve for an example of BD9582F and BD9582N.

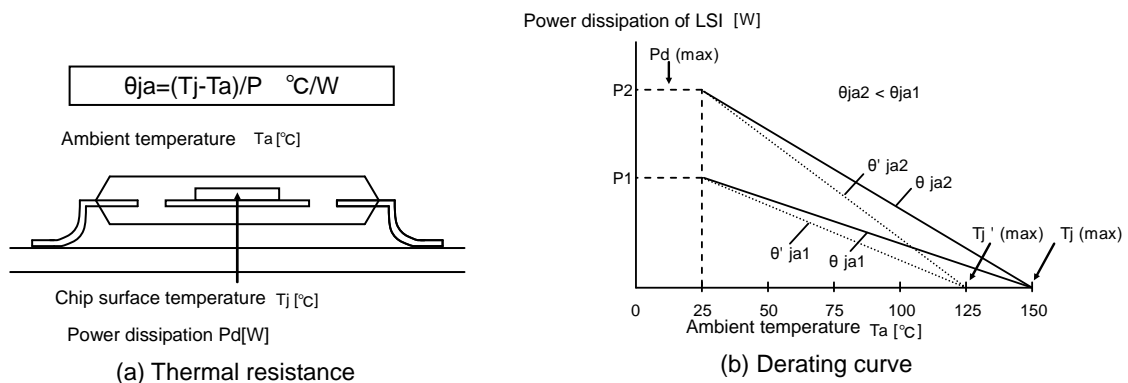
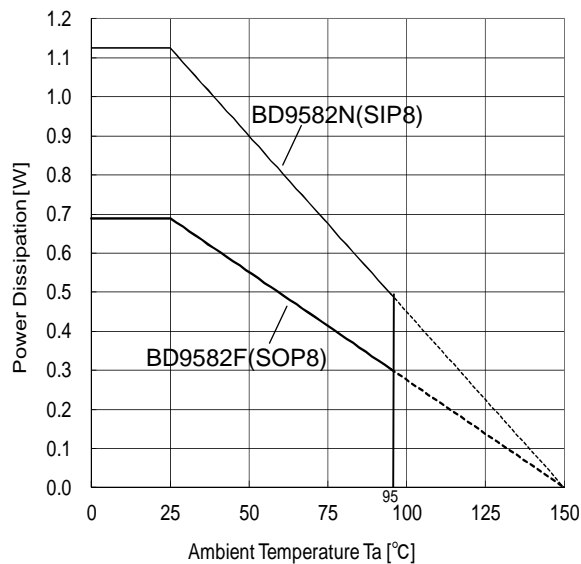


Figure 9. Thermal resistance and derating



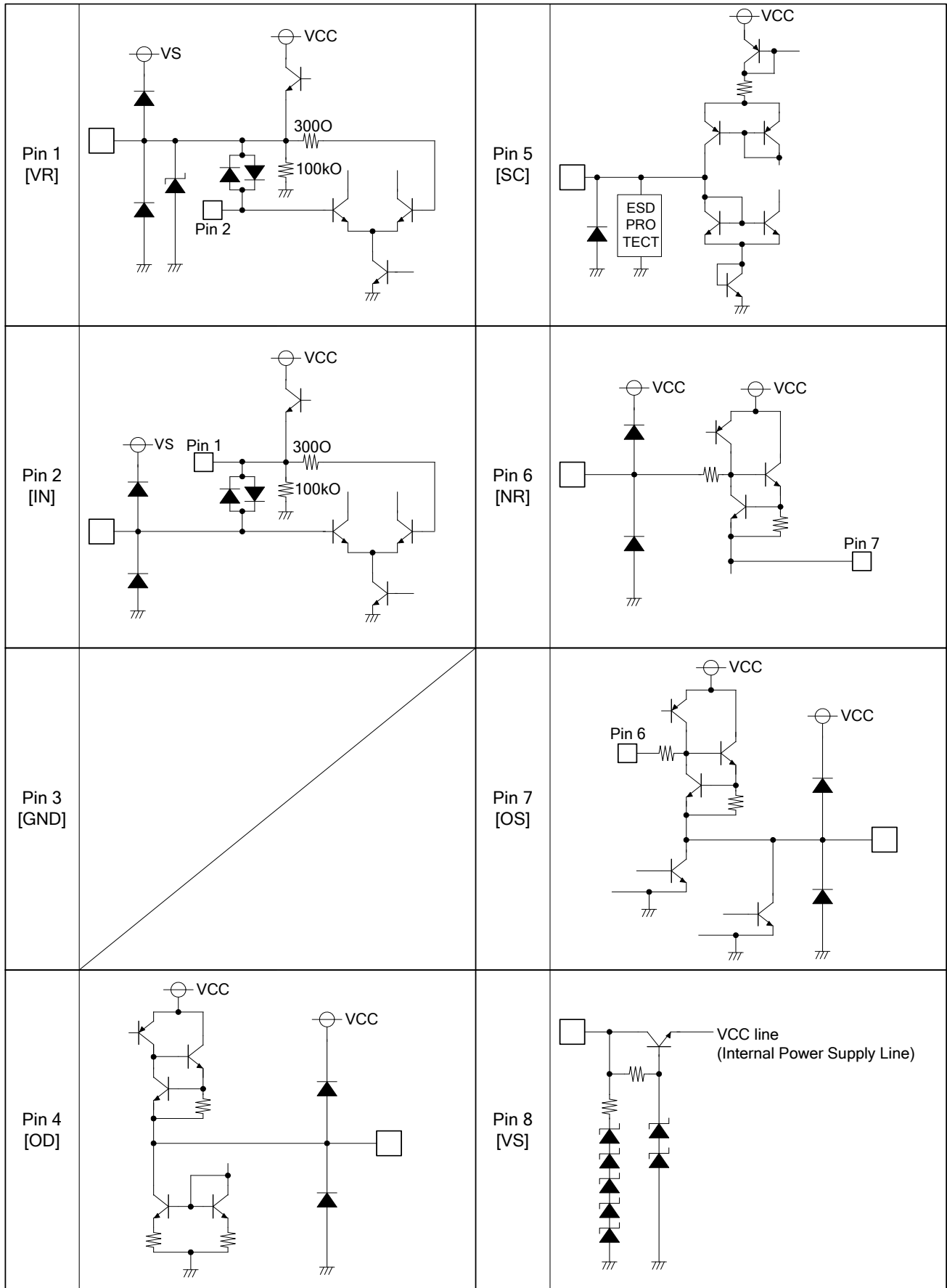
(a) BD9582F • BD9582N

	Derating curve slope	UNIT
BD9582F(SOP8)	5.5	mW/°C
BD9582N(SIP8)	9.0	

When using the unit above Ta=25°C, subtract the value above per degree°C
 BD9582F : Permissible dissipation is a value when FR4 glass epoxy board 70mmx70mmx1.6mm (copper foil area below 3%) is mounted.
 BD9582N : Permissible dissipation is a value in the package unit.

Figure 10. Derating curve

● I/O equivalence circuit



●Operational Notes

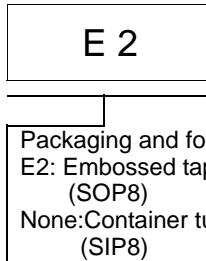
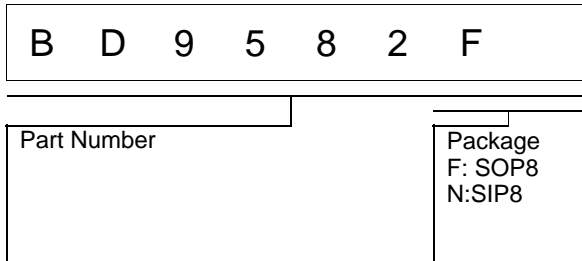
- 1) Absolute maximum ratings
Absolute maximum ratings are the values which indicate the limits, within which the given voltage range can be safely charged to the terminal. However, it does not guarantee the circuit operation.
- 2) Power dissipation Pd
Using the unit in excess of the rated power dissipation may cause deterioration in electrical characteristics due to a rise in chip temperature, including reduced current capability. Therefore, please take into consideration the power dissipation (Pd) under actual operating conditions and apply a sufficient margin in thermal design. Refer to the thermal derating curves for more information.
- 3) Terminal short-circuits
When the output and power supply terminals are shorted, excessive output current may flow, resulting in undue heat generation and, subsequently, destruction.
- 4) Ground terminal voltage
All time, Ground terminal voltage should keep lowest voltage.
In addition, please confirm whether there is not really a terminal becoming the voltage that is lower than GND including a transitional phenomenon.
- 5) Operation in a strong electromagnetic field
Operation in a strong electromagnetic field may cause malfunctions.
- 6) Short-circuit between pins and erroneous mounting
Incorrect mounting may damage the IC. In addition, the presence of foreign particles between the outputs, the output and the power supply, or the output and GND may result in IC destruction.
- 7) IC handling
Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuations in the electrical characteristics due to piezo resistance effects.
- 8) Board inspection
Connecting a capacitor to a pin with low impedance may stress the IC. Therefore, discharging the capacitor after every process is recommended. In addition, when attaching and detaching the jig during the inspection phase, ensure that the power is turned off before inspection and removal. Furthermore, please take measures against ESD in the assembly process as well as during transportation and storage.

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

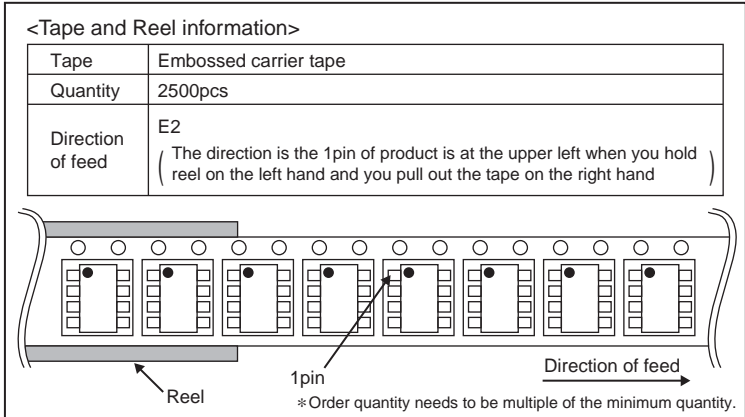
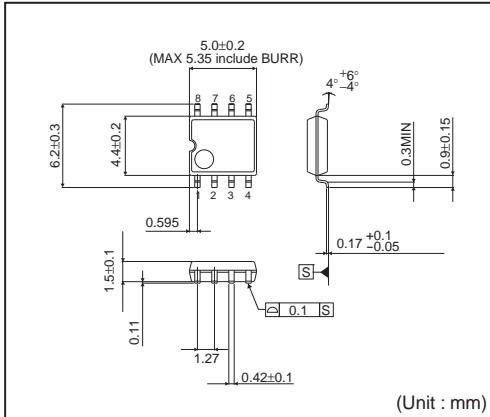
If there are any differences in translation version of this document formal version takes priority.

● Ordering Information

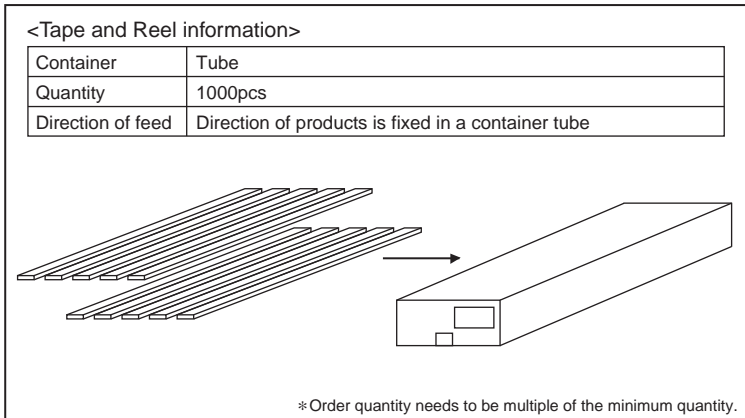
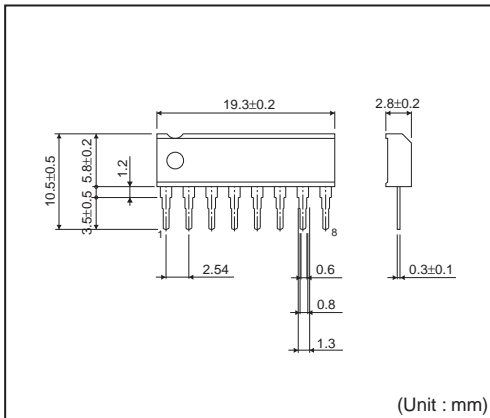


● Physical Dimension Tape and Reel Information

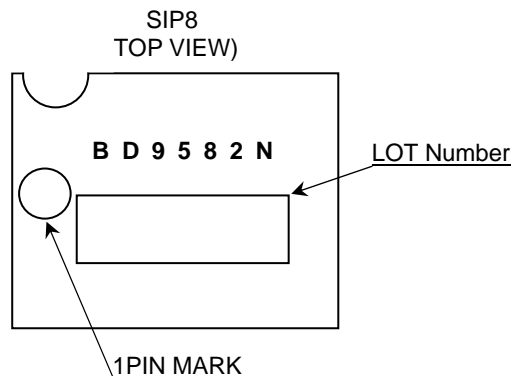
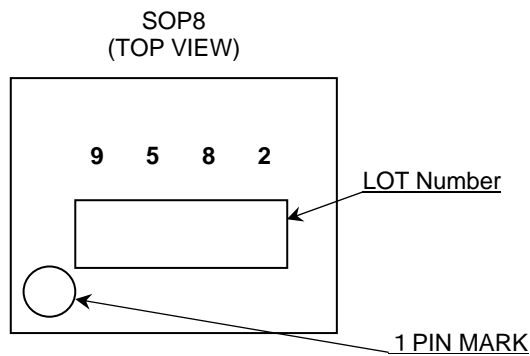
SOP8



SIP8



● Marking Diagrams



●Revision History

Date	Revision	Changes
2012.10.26	001	New Release

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 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
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- Please verify and confirm characteristics of the final or mounted products in using the Products.
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