High Performance Switching Regulator

60V Synchronous Step-down Switching Regulator (Controller Type)

BD9611MUV

● General Description

The BD9611MUV is a high-resistance, wide voltage input (10V to 56V), synchronous step-down switching regulator. BD9611MUV offers design flexibility through user-programmable functions such as soft-start, operating frequency, high-side current limit, and loop compensation. BD9611MUV uses voltage pulse width modulation, and drives 2 external N-channel FETs.

The Under-Voltage Locked Output (EXUVLO) protection connected to its CTL terminal has high accuracy reference voltage. Its threshold voltage can be adjusted by the resistance ratio between VCC and GND as seen by pin CTL.

BD9611MUV is safe for pre-biased outputs. It does not turn on the synchronous rectifier until the internal high-side FET has already started switching

● Features

- High Resistance and Wide Range Voltage Input : VCC=10V to 56V
- Regulated Voltage Output to Drive External FET gate: REG10=10V
- Internal Reference Voltage Accuracy: 0.8V±1.0%
- Safe for Pre-biased Outputs
- Adjustable Operating Frequency and Soft-start
- Master/Slave Synchronization
- Over Current Protection (OCP)
- Under Voltage Locked Output (UVLO, EXUVLO)
- Thermal Shut-down (TSD)

● Key Specifications

Input Supply Voltage	10 to 56 [V]
Output Voltage	1.0 to (Vin×0.8) [V]
Reference Voltage Accuracy	±1.0 [%]
Gate Drive Voltage (REG10)	9 to 11 [V]
Operating frequency	50 to 500 [kHz]

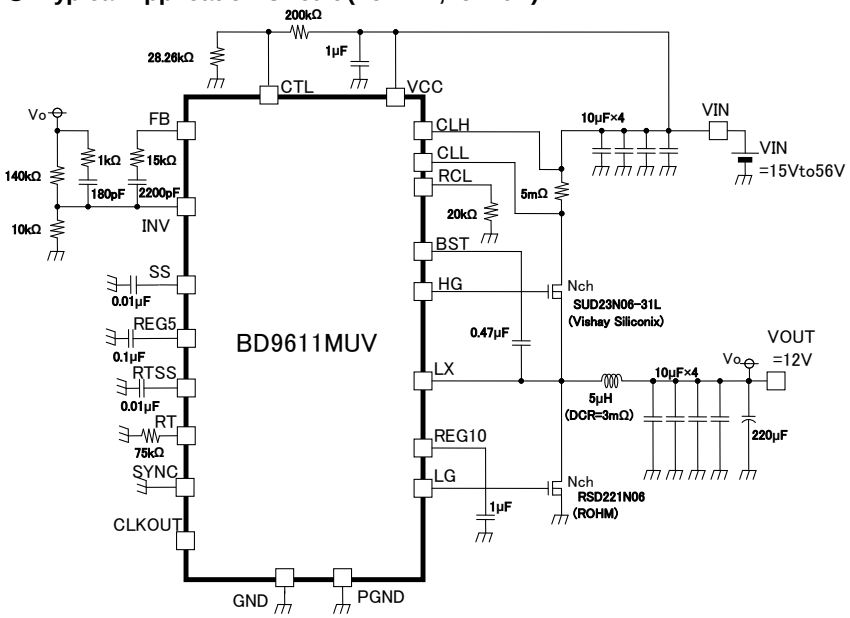
● Package

VQFN020V4040 4.00 ㎜×4.00 ㎜×1.00 ㎜

● Applications

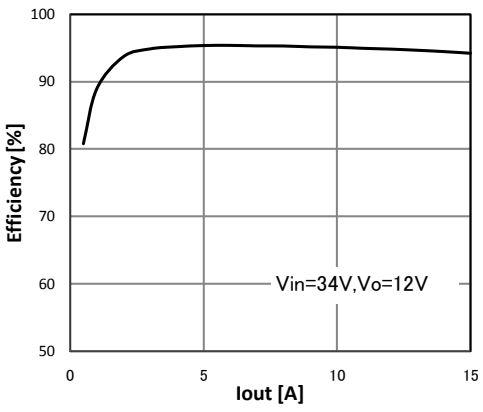
- Amusement machines
- Factory Automation Equipment
- Office Automation Equipment
- LED lighting
- General equipment that require 24V or 48V supply

● Typical Application Circuit (Vo=12V, Io=10A)



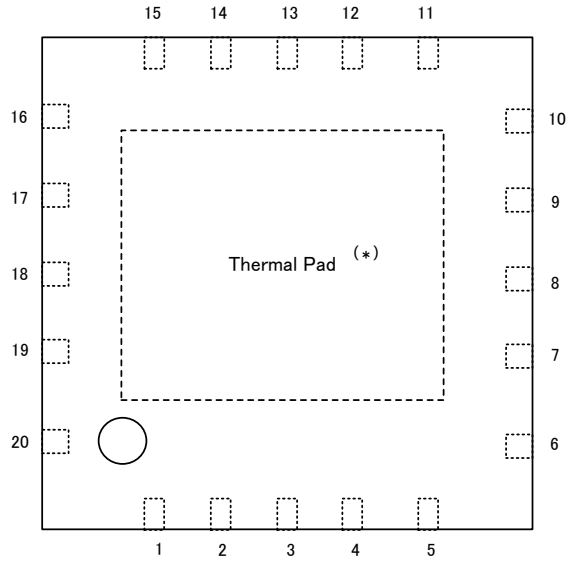
● Efficiency Curve

Efficiency: η =95%
(V_{IN}=34V, I_{OUT}=10A, f_{OSC}=250kHz)



○ **STRUCURE:** Silicon Monolithic Integrated Circuit ○ Not designed to operate under radioactive environments

● Pin Configuration (Top View)

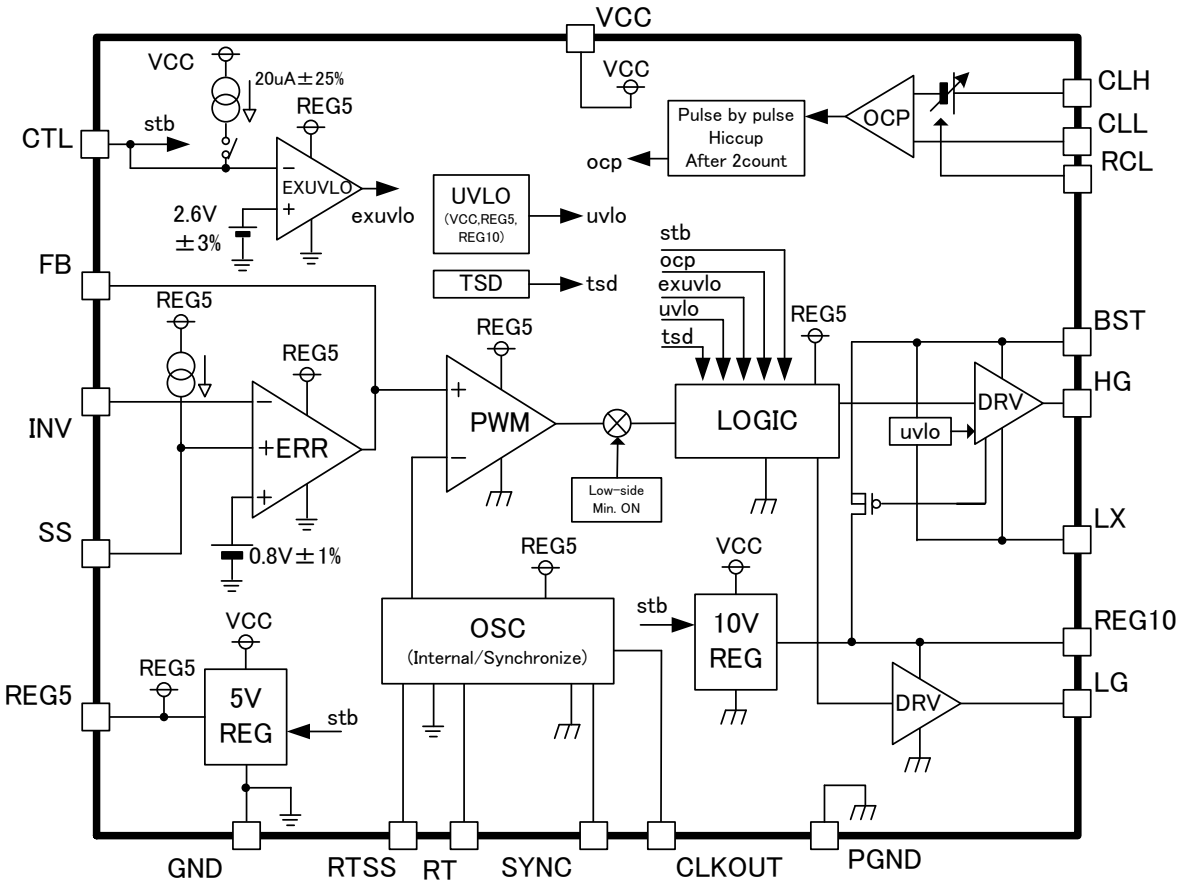


(*) Connecting the thermal pad to GND is recommended to improve thermal dispersion characteristic.

● Pin Description

Pin no.	Pin Name	Description
1	GND	Ground
2	SS	Programmable Soft-start
3	INV	Inverting input to the error amplifier
4	FB	Output of the error amplifier
5	RCL	Programmable current limit setting
6	RT	Programmable frequency setting
7	RTSS	Reference voltage pin for RT
8	CLKOUT	Internal clock pulse output
9	PGND	Ground
10	SYNC	Synchronization input for the device
11	LG	Gate driver for external Low-side, N-channel FET
12	REG10	Output of 10V internal regulator
13	LX	Connect to switching node of the converter
14	HG	Gate driver for external High-side, N-channel FET
15	BST	Gate drive voltage input for the High-side N-channel FET
16	CLL	Inverting input to current detector
17	CLH	Input to current detector
18	VCC	Power supply
19	CTL	Shutdown pin
20	REG5	Output of 5V internal regulator

● Block Diagram



● Functional Description of Blocks

1. 5VREG

Supplies regulated 5V to internal circuits (5V ± 2%).
It is available as an external supply for applications requiring a maximum current of 2mA or less.

2. ERR (Error Amp)

Error amplifier output depends on detected VOUT output and is used as PWM control signal.
Internal reference voltage is 0.8V (Accuracy: ±1%).
Connect capacitor and resistor between inverting pin (INV) and output pin (FB) as phase compensation elements.

3. Soft Start

A circuit that prevents in-rush current during startup through soft start operation of DC-DC comparator output voltage. The external capacitor of pin SS is charged with an internal source current (1uA). This produces a voltage slope input to the error amplifier and performs as the start-up reference voltage.

4. OSC

This is an oscillator that serves as reference of the PWM modulation. The frequency of the internally generated triangle wave is controlled by an external resistor RRT connected to RT pin, and can vary within 50kHz to 500kHz. RT pin outputs the RTSS voltage buffer. CLKOUT outputs the oscillator-generated square wave.
OSC can be synchronized to an external clock through the SYNC pin.

5. PWMCOMP

This is a comparator for PWM modulation which compares the output of the error amplifier and ramp wave from OSC to decide the switching duty. Switching duty is limited by HG min OFF time (350ns) because of the charging of BST-LX capacitor.

6. DRV

It drives the external FETs. High side DRV in particular has built in UVLO.

7. 10VREG

It outputs a regulated 10V that is used as supply voltage for the low-side driver. It is also used to charge the capacitor between BST and LX through an internal switch.

8. UVLO

This is a low voltage error prevention circuit. It prevents internal circuit error during changes in the power supply voltage by monitoring VCC, REG5 and REG10. Its operation turns off both external FETs and resets the soft-start function whenever a threshold is met for any of the monitored voltages.

9. EXUVLO

This is a low voltage error prevention circuit with adjustable VCC detect and release threshold voltages. The threshold voltages can be adjusted through external resistances between VCC and GND.
When the CTL input voltage is greater than the EXUVLO threshold voltage of 2.6V (±3%), a 20uA (±25%) constant current flows to the CTL terminal. Once the CTL input voltage becomes lower than this threshold, both the high-side and low-side FETs are turned off and the SS terminal capacitor is discharged.

10. TSD

This is a circuit which protects the IC from excessive heat by executing thermal shut down.
When it detects an abnormal temperature exceeding the Maximum Junction Temperature (T_J=150℃), it turns off both external FETs. TSD employs hysteresis and the IC automatically resumes normal operation once the temperature is less than the release threshold.

11. OCP

This is an Over Current Protection circuit that uses a two-tier approach.
The first tier is a pulse-by-pulse protection scheme. Current limit is implemented on the high-side FET by sensing the CLH-CLL voltage when the gate is driven high. The CLH-CLL voltage is compared to the threshold voltage configured by the RCL resistor. If the CLH-CLL voltage exceeds the threshold, the switching pulse is immediately terminated. The FET remains off until the next switching cycle is initiated.
The second tier consists of a fault counter. The fault counter is incremented whenever an over-current pulse is detected. When the counter reaches two within three successive pulses, both FETs, FB and SS are all turned off for a specified time. Afterwards, both FETs, FB and SS are released and automatically restarted with soft-start.

12. CTL

The voltage applied to pin CTL (VCTL) can control the ON / OFF state of the IC.
When VCTL > 2.4V is applied, internal regulators turn on. DRV turns on next when VCTL > 2.8V is applied.
A current value of approximately (VCTL - 5.6V) / 100kΩ sink to CTL whenever VCTL > 5.6V because of a 5.6V clamping circuit connected after a 100kΩ internal resistance and the CTL terminal.
If the CTL terminal becomes open after reaching the release voltage of EXUVLO, the IC is unable to turn off because of the internal constant current source at CTL.
The IC turns off when VCTL < 0.3V is applied. In this condition, the stand-by current is approximately 0uA.

● **Absolute Maximum Ratings**

Item	Symbol	Rating	Unit
Supply voltage	VCC	60	V
CTL pin	VCTL	VCC	V
BST pin	VBST	70	V
LX pin	VLX	VCC	V
Between BST pin – LX pin	VBSTLX	15	V
HG pin	VHG	VLX to VBST	V
LG pin	VLG	0 to VREG10	V
REG10 pin	VREG10	15	V
REG5 pin	VREG5	7	V
SYNC pin	VSYNC	7	V
INV pin	VINV	VREG5	V
CLH pin	VCLH	VLX	V
CLL pin	VCLL	VLX	V
Power Dissipation	P_D	3.56 *1	W
Operating Temperature Range	T_{OPR}	-40 to +105	℃
Storage Temperature Range	T_{STG}	-55 to +150	℃
Junction Temperature	T_{JMAX}	150	℃

*1 When mounting on a 70×70×1.6 mm 4-layer board (Copper area: 70mm×70mm).
Pd is reduced by 28.5mW for every 1℃ increase in temperature above 25℃.

● **Operating Ratings**

Item	Symbol	Range	Unit
Power supply voltage	VCC	10 to 56	V
Configurable output voltage	VOUT	1.0 to (Vin × 0.8V) *2	V
CTL input voltage	CTL	0 to VCC *3	V
Frequency	FOSC	50 to 500	kHz
RT resistor	RRT	33 to 470	kΩ
RTSS capacitor	CRTSS	0.01 to 1.0	uF
Synchronization frequency	SYNCFRQ	FOSC ± 10%	kHz
SYNC input duty	SYNCDTY	40 to 60	%
OCP program resistor	RRCL	3.3 to 20	kΩ

*2 Please refer to p.25 (13) regarding programmed output voltage (for output voltage dependent on input voltage, frequency, load current etc.)

*3 CTL remains at “H” state due to hysteresis constant current, whenever CTL terminal is opened after EXUVLO release voltage had been detected. Please refer to p.26 (14).

● **Electrical Characteristics**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

PARAMETER	SYMBOL	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
【OSCILLATOR】						
Frequency	FOSC	93	100	107	kHz	RT=200kΩ
RTSS maximum current (sink/source)	IRTSS	2.5	5	10	uA	VRTSS=0V/1.0V
RTSS pre-charge threshold	VRTSSTH	0.45	0.5	0.55	V	
RTSS pre-charge current	IRTSSP	50	100	200	uA	VRTSS=0.3V
【SOFT START】						
SS source current	ISSSO	0.7	1	1.3	uA	SS=1.0V
【UVLO】						
UVLO threshold (VCC)	VUTHVCC	8.5	9.0	9.5	V	VCC rise-up
UVLO threshold (REG10)	VUTHR10	7.9	8.7	9.5	V	REG10 rise-up
UVLO threshold (REG5)	VUTHR5	4.2	4.5	4.8	V	REG5 rise-up
UVLO hysteresis (VCC)	VUHSVCC	-	0.5	1.0	V	VCC pin
UVLO hysteresis (REG10)	VUHSR10	-	0.5	1.0	V	REG10 pin
UVLO hysteresis (REG5)	VUHSR5	-	0.2	0.4	V	REG5 pin
UVLO threshold (CTL)	VEXUTH	2.522	2.6	2.678	V	CTL rise-up
UVLO hysteresis current	IUVHYS	-25	-20	-15	uA	CTL=5V
【ERROR AMPLIFIER】						
Reference voltage	VNON	0.792	0.8	0.808	V	INV=FB
INV input bias current	IBINV	-	0.01	1.0	uA	INV=0.8V
FB max voltage	VFBH	REG5-0.5	-	REG5	V	
FB min voltage	VFBL	-	0	0.5	V	
FB sink current	IFBSI	0.5	2	-	mA	FB=1.25V, INV=1.5V
FB source current	IFBSO	60	120	-	uA	FB=1.25V, INV=0V
【PWM COMPARATOR】						
Input threshold voltage	VT0	1.4	1.5	1.6	V	0% Duty, FB pin vol.
HG min OFF pulse width	HG_{MIN}	150	350	450	ns	FB=3V
【OUTPUT DRIVER】						
Output driver PchFET Ron	RONH	-	6	10	Ω	Iout=0.1A
Output driver NchFET Ron	RONL	-	1	3	Ω	Iout=0.1A

● **Electrical Characteristics**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

PARAMETER	SYMBOL	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
【CURRENT LIMIT】						
OCP threshold voltage	VOCPTH	160	200	240	mV	Between CLH and CLL (RCL=7.5kΩ)
OCP propagation delay to output	TOCP	-	200	300	ns	
OCP counts to hiccup	NOCP	-	2	-	counts	In series or in every other cycle
OCP shut-down hold cycles	THICCUP	-	32768	-	cycles	T=1/FOSC, Hold time=T×THICCUP
【REGULATOR】						
REG10 output voltage	VREG10	9	10	11	V	
REG5 output voltage	VREG5	4.9	5.0	5.1	V	
REG5 current ability	IREG5	10	30	-	mA	V=VREG5×0.95
【SYNCHRONIZE OSCILLATOR】						
SYNC input current	ISYNC	-	8	16	uA	SYNC=5V
SYNC input voltage H	VSYNCH	2.8	-	5.0	V	
SYNC input voltage L	VSYNCL	GND	-	0.3	V	
CLKOUT output range	VCLKOUT	REG5-0.5	REG5	REG5+0.5	V	
CLKOUT sink current	ICLKSI	1.5	3	-	mA	CLKOUT=0.5V
CLKOUT source current	ICLKSO	1.5	3	-	mA	CLKOUT=4.5V
【WHOLE DEVICE】						
CTL output current	ICTL	15	20	25	uA	CTL=5V
CTL input voltage L	VCTLL	GND	-	0.3	V	
CTL input voltage1 H	VCTL1H	2.2	-	2.4	V	REG5, REG10 start up
CTL input voltage2 H	VCTL2H	2.8	-	VCC	V	DRV start up
Stand-by current	ISC	-	0	5.0	uA	CTL=0V
Quiescent current	ICC	1.0	2.0	4.0	mA	INV=5V

● **Typical Performance Curves 1**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

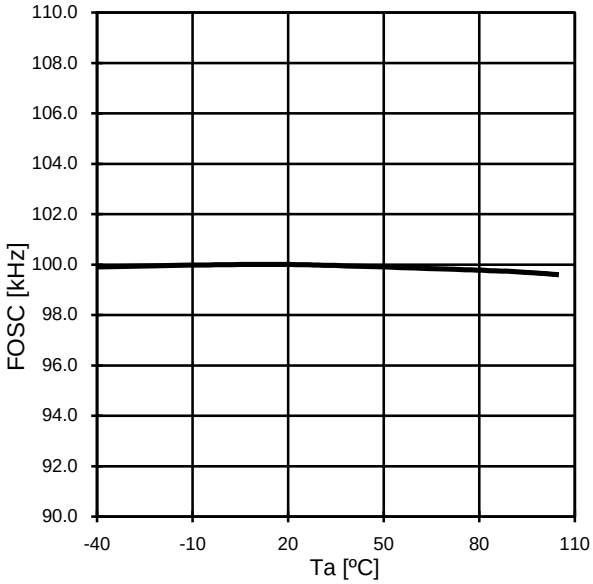


Fig.1 FOSC-Ta

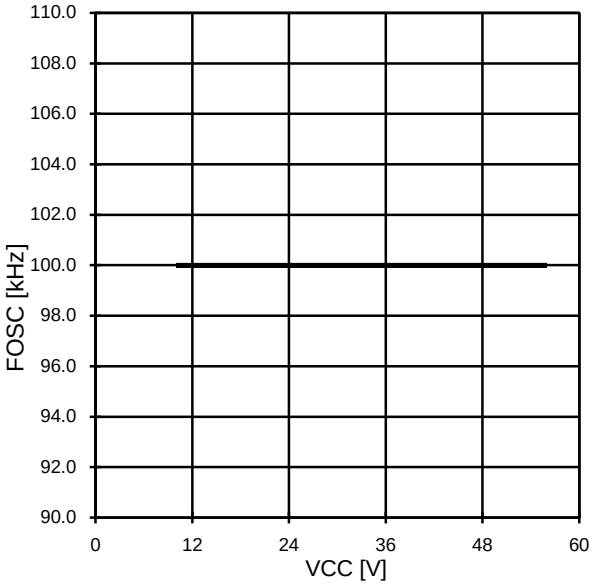


Fig.2 FOSC-VCC

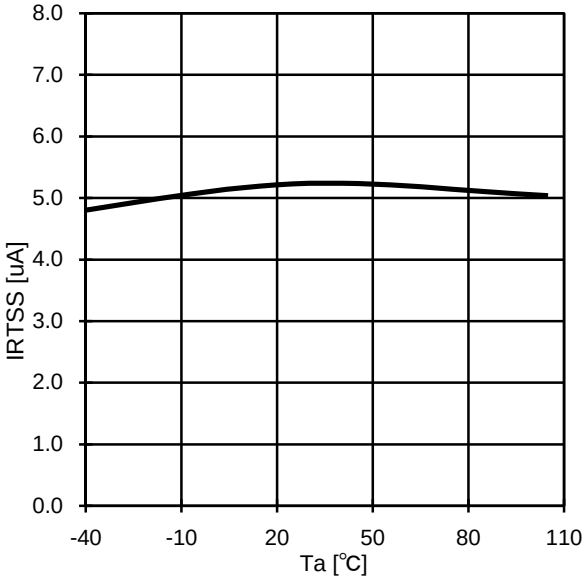


Fig.3 IRTSS-Ta (VRTSS=0V)

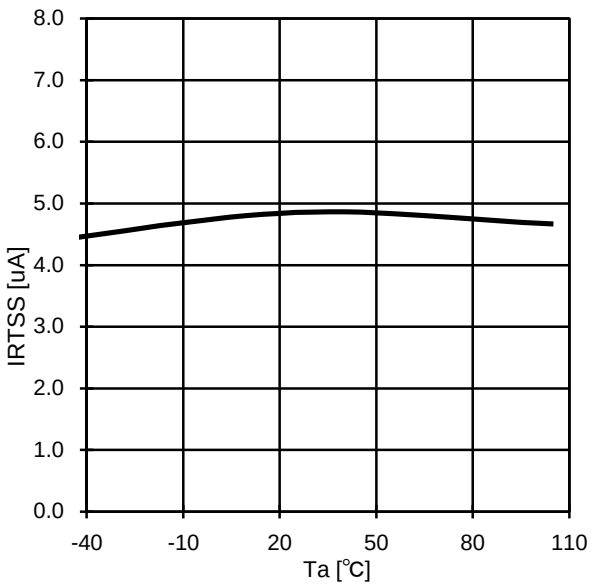


Fig.4 IRTSS-Ta (VRTSS=1V)

● **Typical Performance Curves 2**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

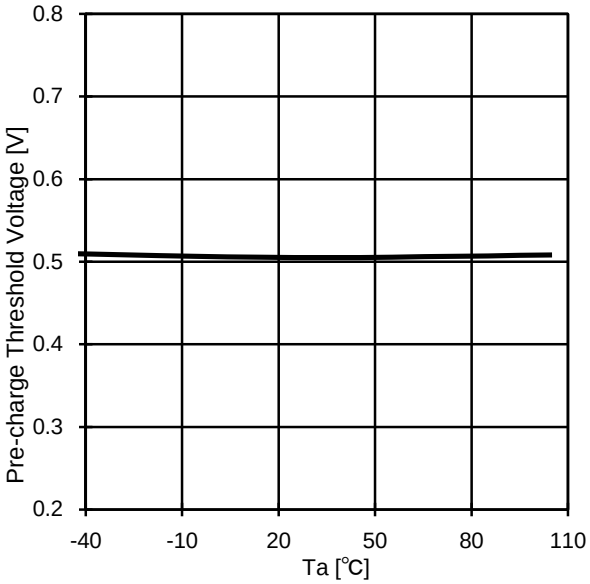


Fig.5 RTSS Pre-charge Threshold-Ta

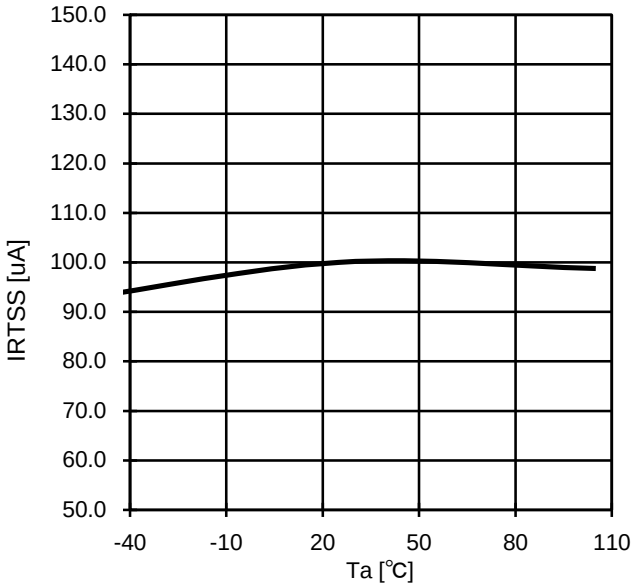


Fig.6 RTSS Pre-charge Current-Ta

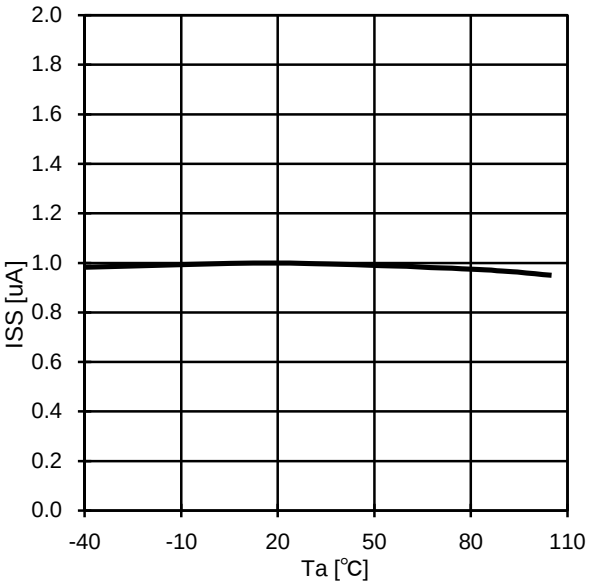


Fig.7 SS Source Current-Ta (VSS=1V)

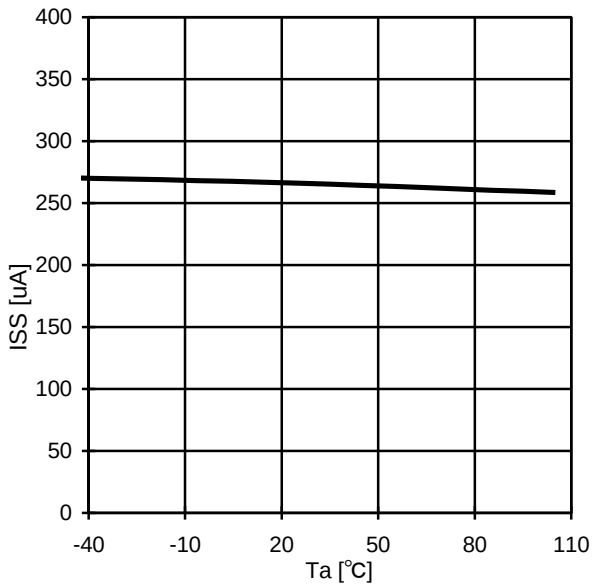


Fig.8 SS Sink Current-Ta (VSS=1V, Protection)

● **Typical Performance Curves 3**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

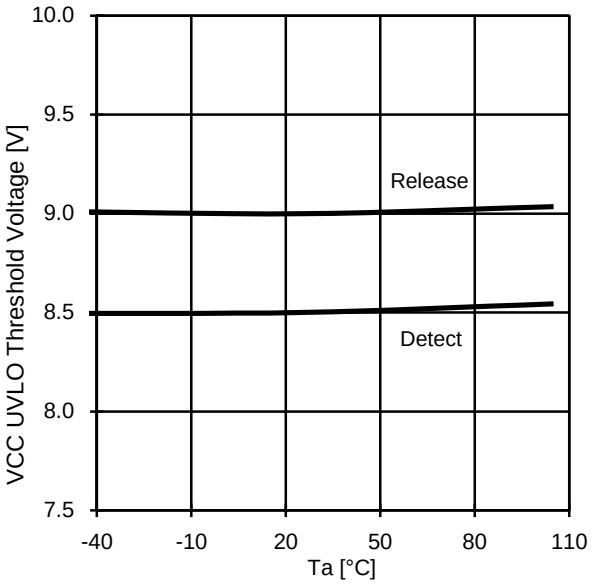


Fig.9 VCC UVLO-Ta

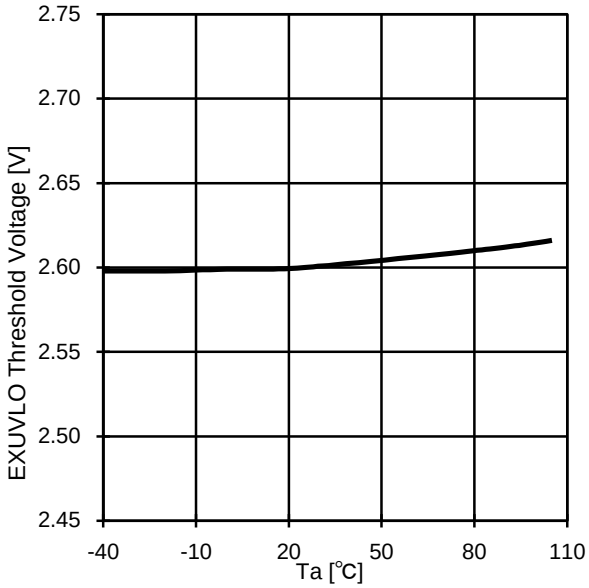


Fig.10 EXUVLO (CTL)-Ta

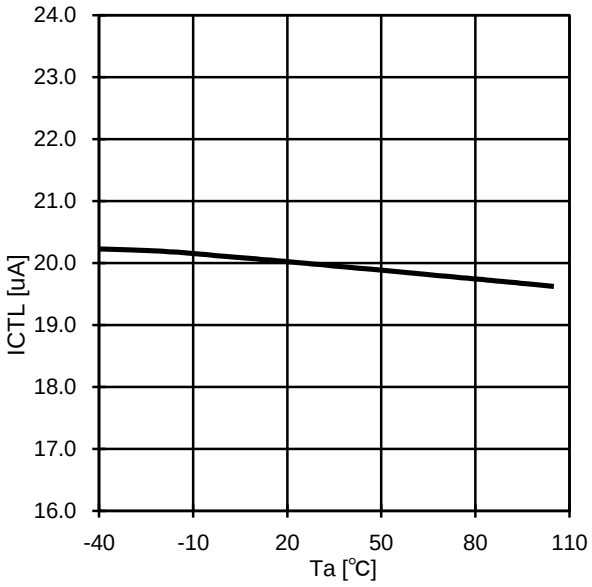


Fig.11 UVLO Hysteresis Current-Ta

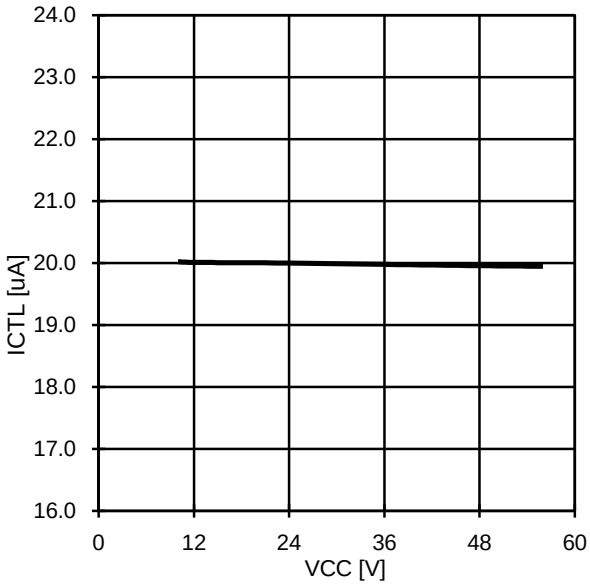


Fig.12 UVLO Hysteresis Current-VCC

● **Typical Performance Curves 4**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

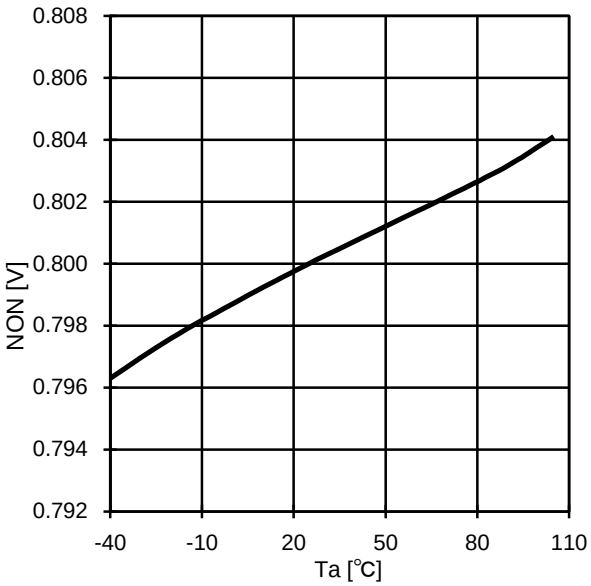


Fig.13 Reference Voltage-Ta

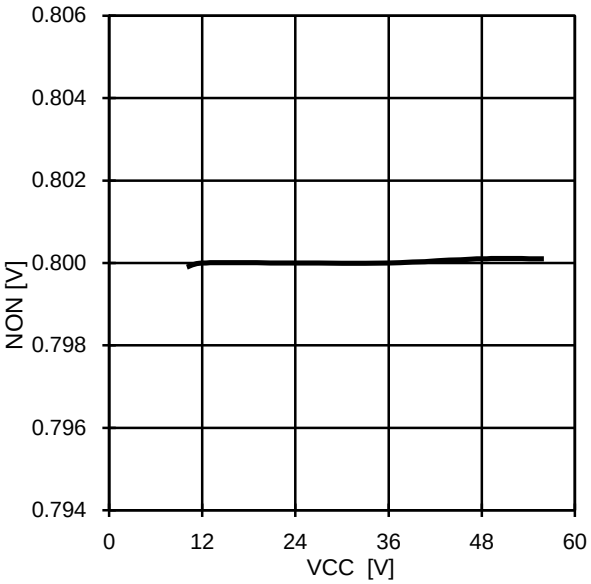


Fig.14 Reference Voltage-VCC

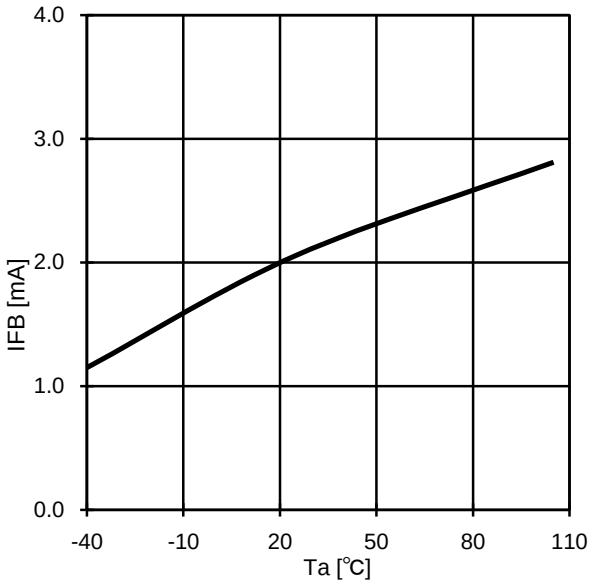


Fig.15 FB Sink current-Ta

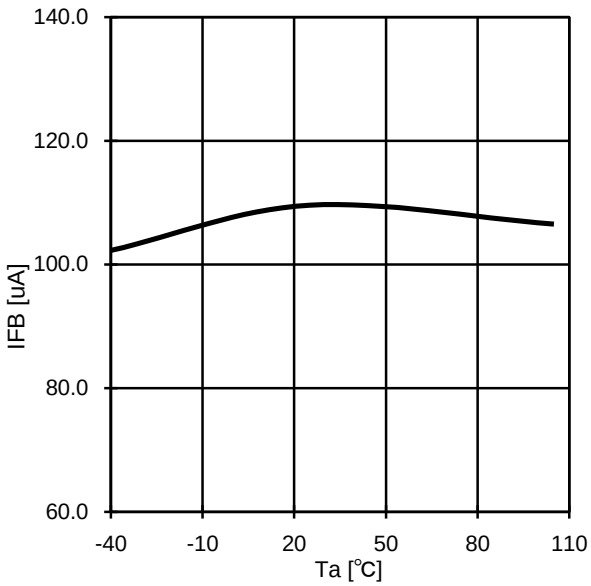


Fig.16 FB Source current-Ta

● **Typical Performance Curves 5**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

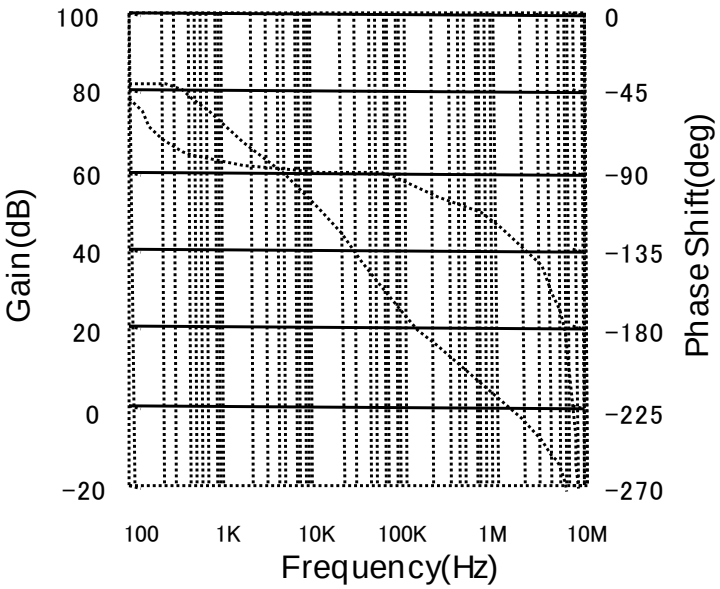


Fig.17 Error Amp Response-Frequency

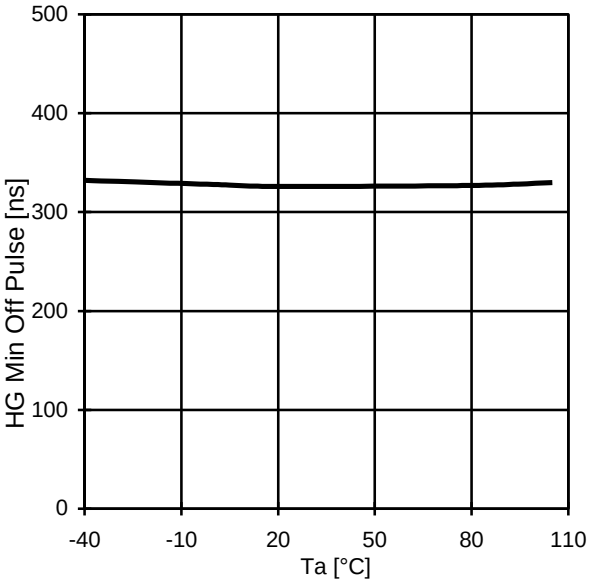


Fig.18 HG Min Off Pulse-Ta

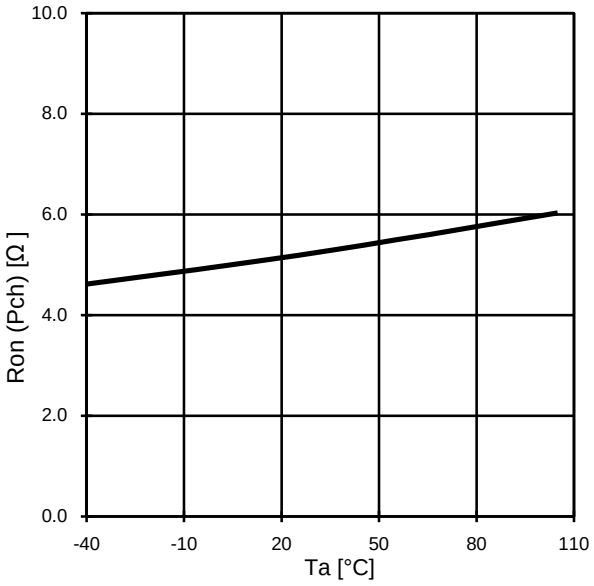


Fig.19 FET Ron –Ta (Pch)

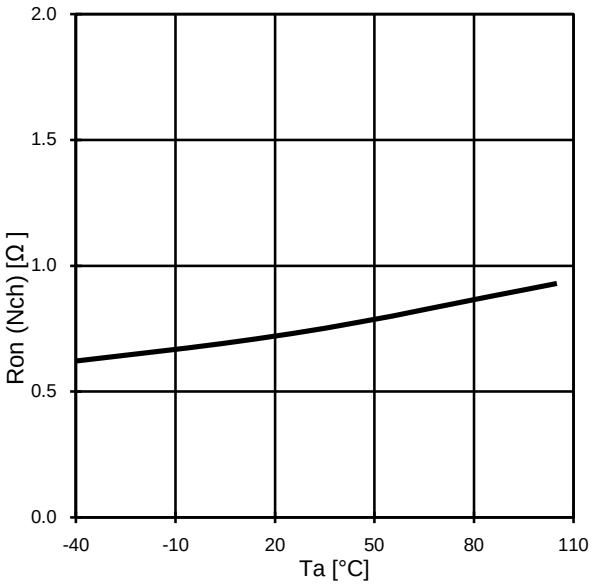


Fig.20 FET Ron –Ta (Nch)

● **Typical Performance Curves 6**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

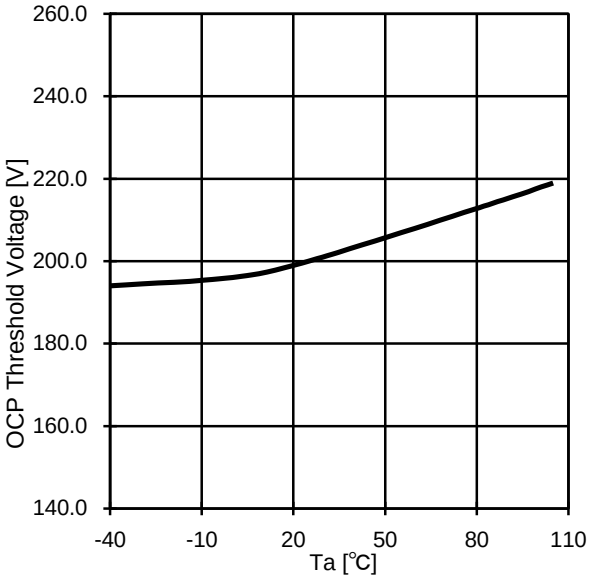


Fig.21 OCP Threshold Voltage-Ta

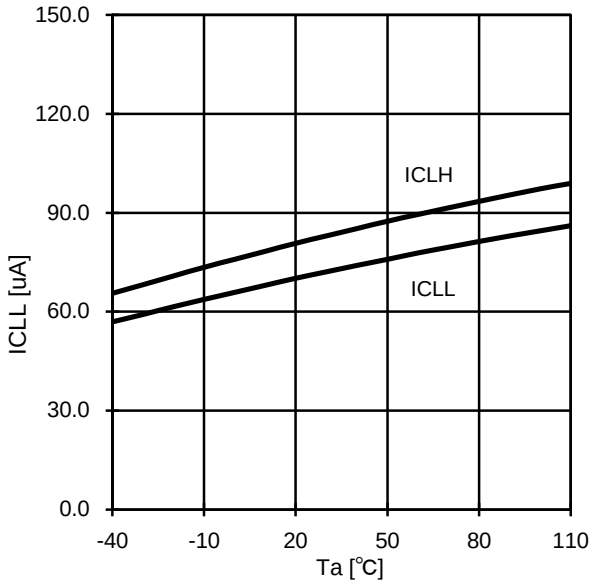


Fig.22 ICLH, ICLL-Ta

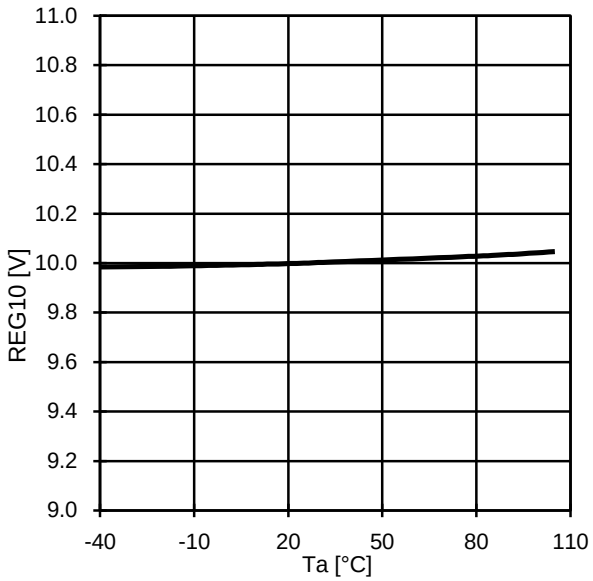


Fig.23 REG10-Ta

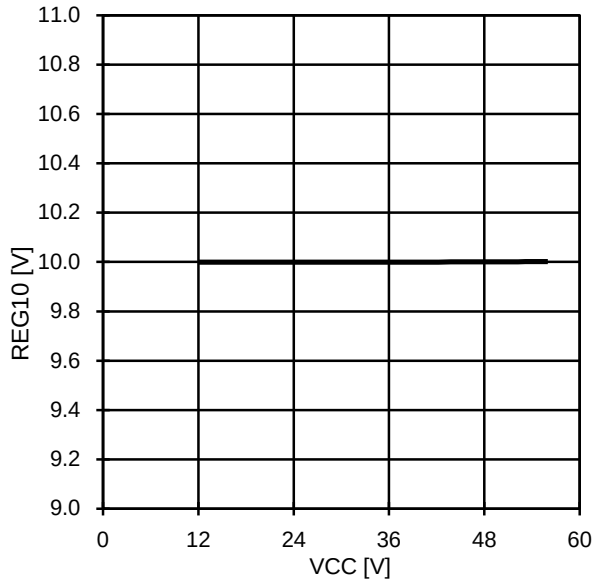


Fig.24 REG10 Line Regulation

● **Typical Performance Curves 7**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

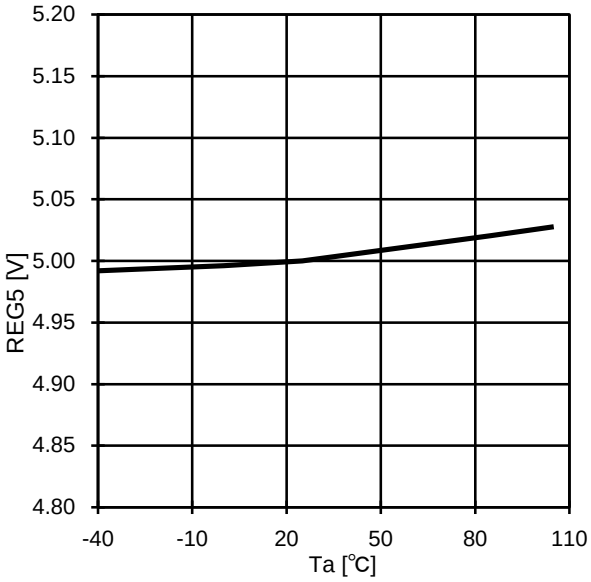


Fig.25 REG5-Ta

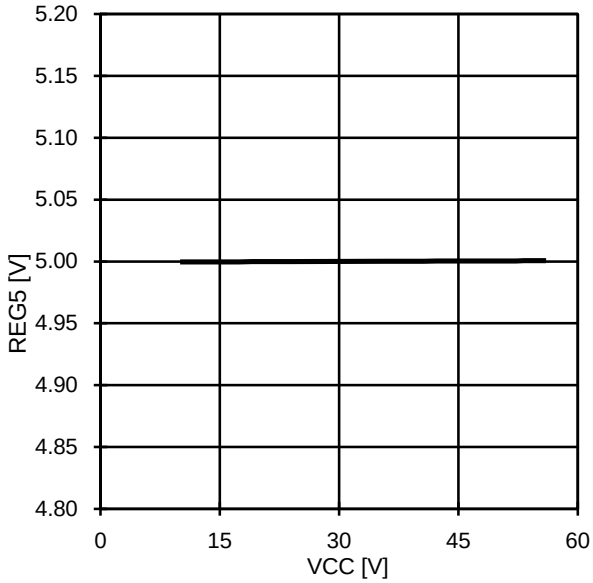


Fig.26 REG5-VCC

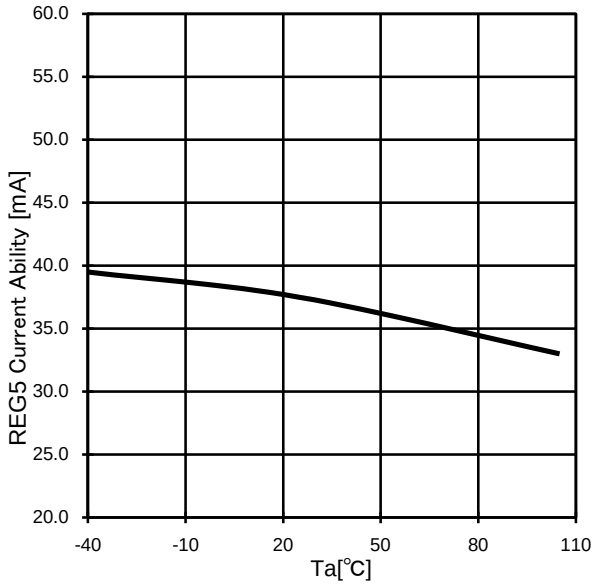


Fig.27 REG5 Current Ability -Ta

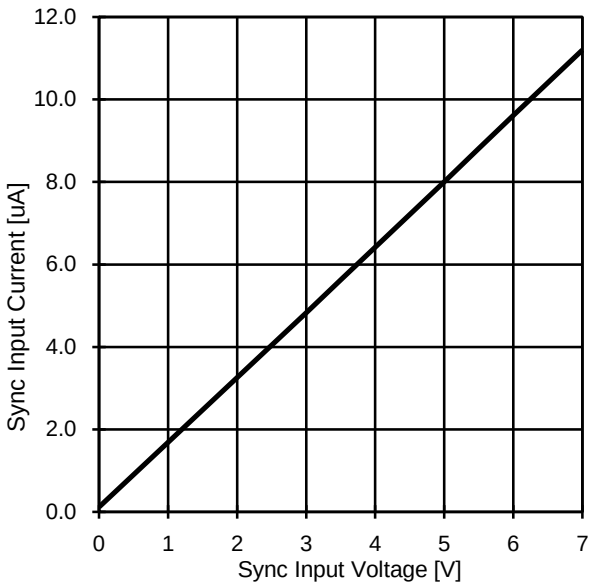


Fig.28 ISYNC-VSYNC

● **Typical Performance Curves 8**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

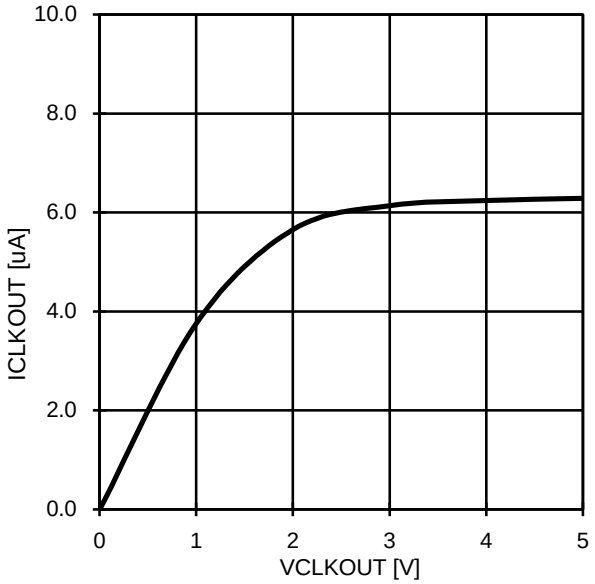


Fig.29 CLKOUT Sink Current - VCLKOUT

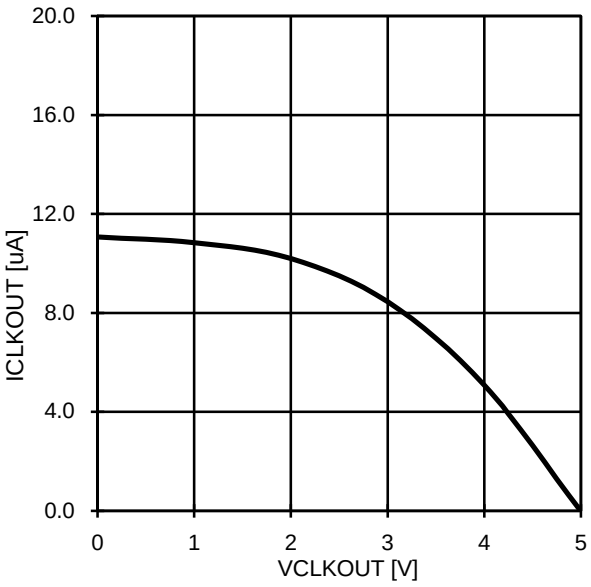


Fig.30 CLKOUT Source Current - VCLKOUT

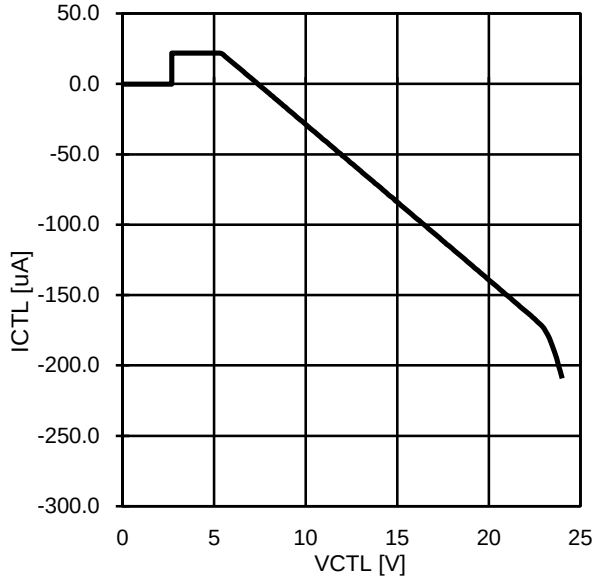


Fig.31 ICTL-VCTL

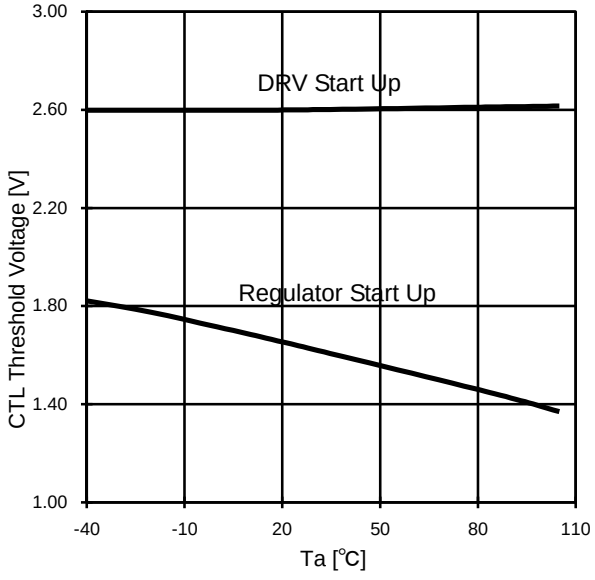


Fig.32 CTL Threshold Voltage -Ta

● **Typical Performance Curves 9**
(Unless otherwise specified: Ta=25℃, VCC=CTL=24V, RT=200kΩ)

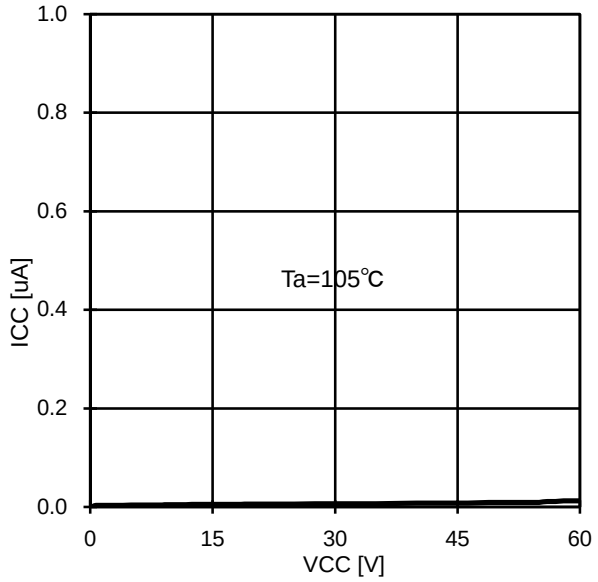


Fig.33 Stand-by Current -VCC

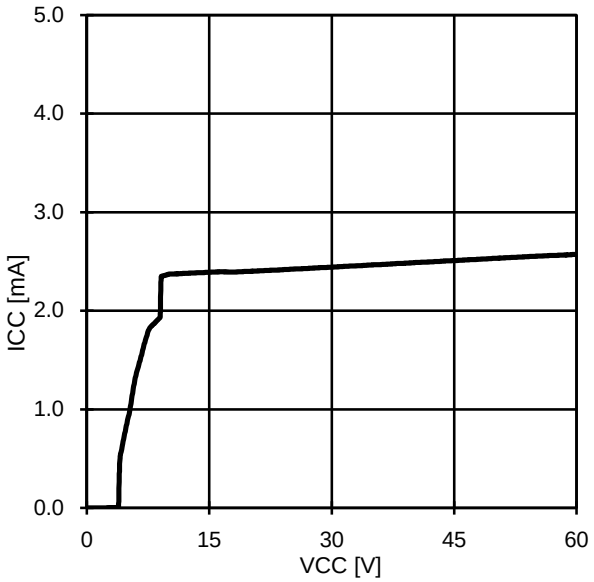


Fig.34 Quiescent Current -VCC

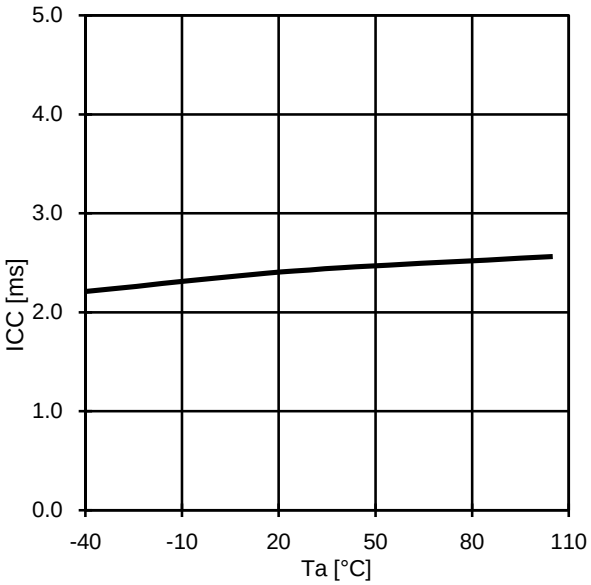
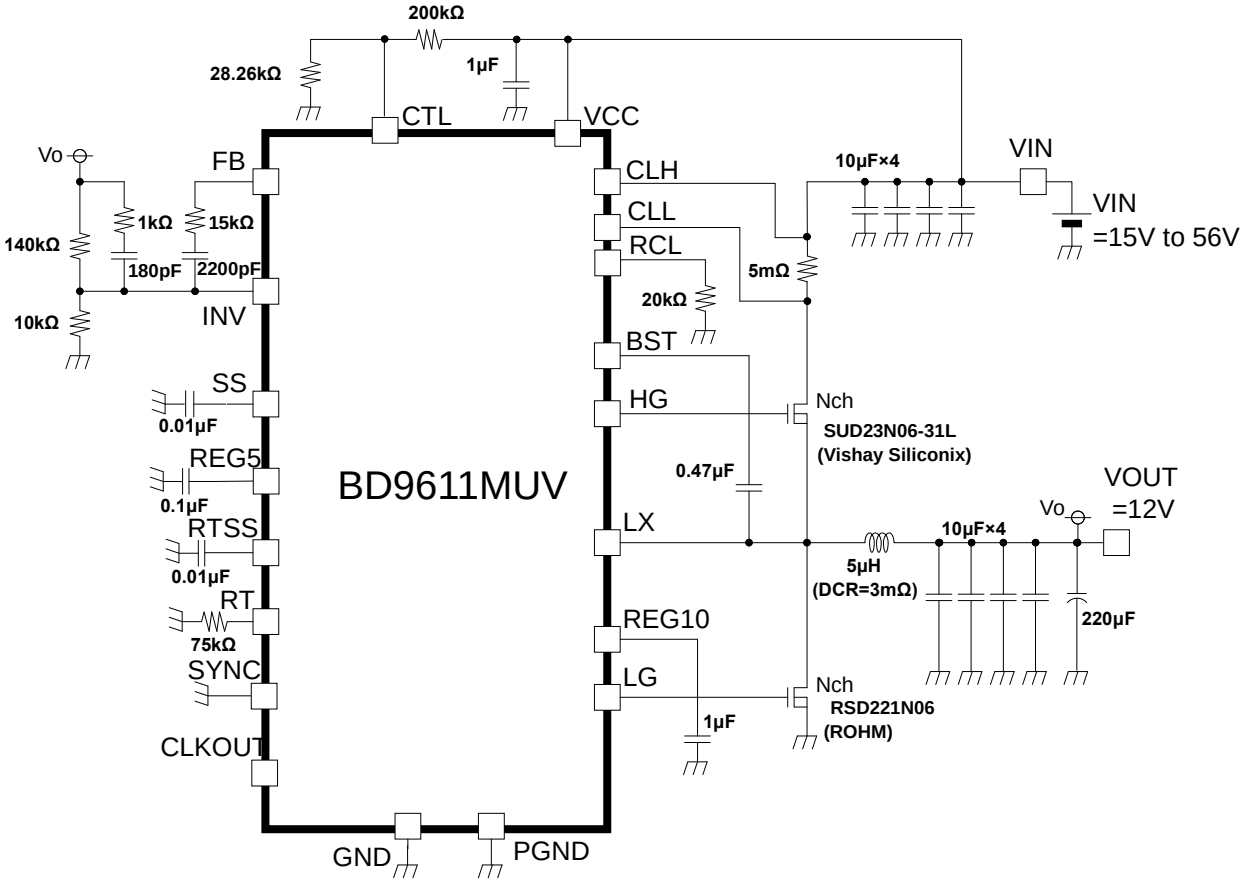


Fig.35 Quiescent Current -Ta

● **Reference Application (Vo=12V/ Io=10A)**



● **Reference Application data**
(VCC=34V, Vo=12V, Ta=25℃)

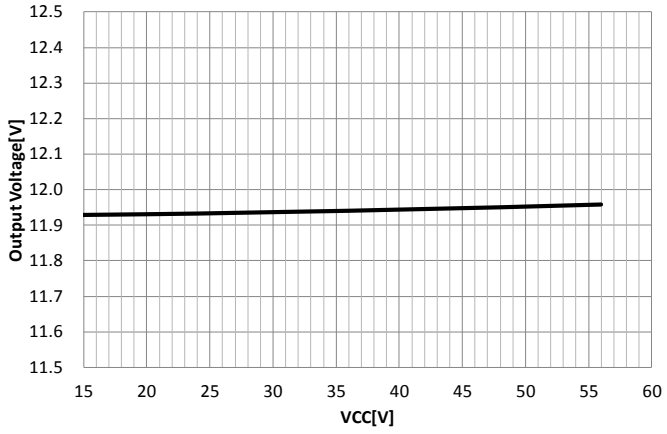


Fig.36 Line Regulation
(Io=10A)

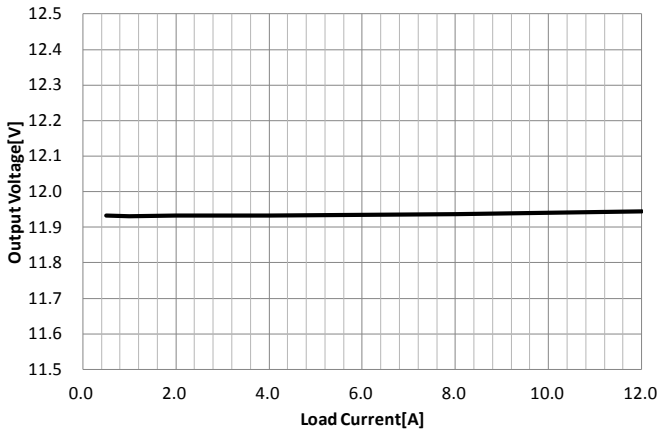


Fig.37 Load Regulation
(VCC=34V)

- **Reference Application data**
  (VCC=34V, Vo=12V, Ta=25℃)

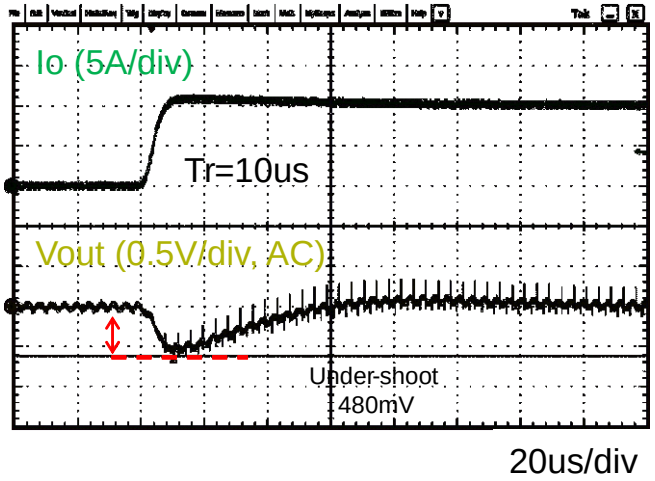


Fig.38 Load Response (Io=0A→10A)

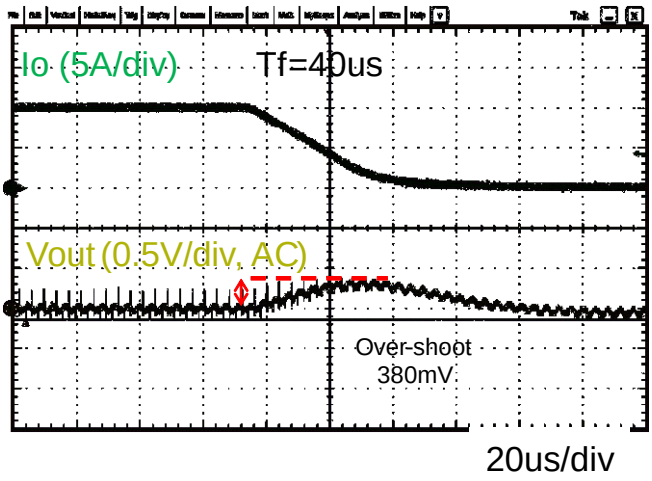


Fig.39 Load Response (Io=10A→0A)

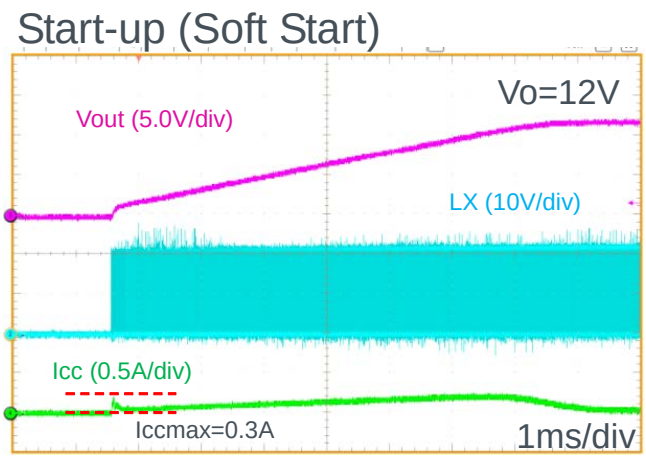


Fig.40 Start-up Waves (Soft Start)

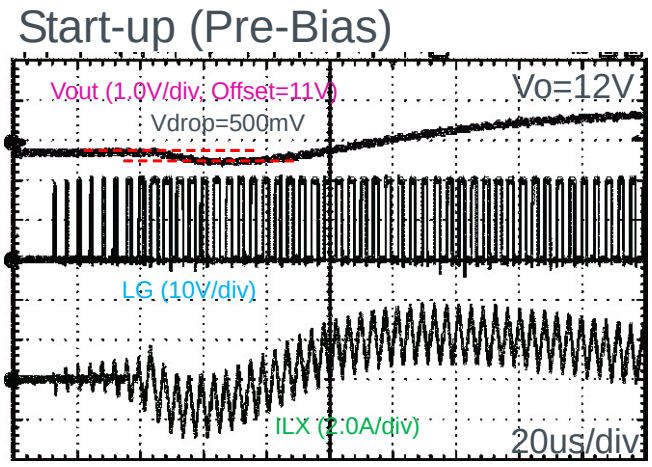


Fig.41 Start-up Waves (Pre-Bias)

● Function Description

(1) REG5 REGULATOR

REG5 is used as an internal power supply and reference voltage. Its maximum load should be less than 2mA.
Please connect a ceramic capacitor (CREG5=0.1uF) between REG5 and GND.

(2) REG10 REGULATOR

This is a regulator for the low-side DRV. It also charges the external BST-LX capacitor through an internal FET switch.
Please connect a ceramic capacitor (CREG10=1.0uF) between REG10 and GND.
When REG10 pin is shorted to GND, its short circuit detection function limits the load current to 20mA.

(3) SOFT START

To prevent in-rush current or overshoot, a reference voltage is ramped at startup.
The reference voltage comes from the voltage generated across capacitor CSS connected to the SS pin.
A ramp voltage is generated at this pin as CSS is charged by an internal constant current source (ISS=1uA).
Soft-start time (tss) is defined as the time it takes for the SS voltage to reach 0.8V:

$$tss = (CSS \times VNON) / ISS$$

(Ex.) CSS=0.01uF → tss = (0.01uF × 0.8V) / 1uA = 8 [ms]

Before soft start begins, the start-up time for RTSS takes first as described next.

(4) OSCILLATOR (RT, RTSS, CLKOUT)

The switching frequency of the oscillator is set by an external resistor RRT that is connected to pin RT and ground.
The clock frequency FOSC is related to RRT as shown in Figure 42 and is defined by the equation below.
Note that the amplitude of the generated triangle wave of the oscillator is 1.5V to 2V.

$$FOSC = 15900 \times RRT^{-0.955} \text{ [kHz]}$$ （RRT: RT resistor [kΩ] ）

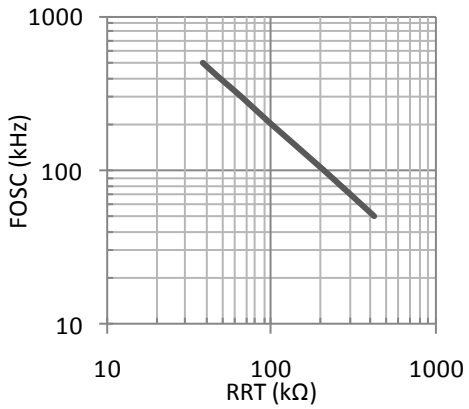


Fig.42 Switching Frequency vs RRT Resistance

In case external synchronization is not used, the RTSS terminal outputs the internal reference voltage (0.5V) through its internal voltage buffer. Terminal RT outputs the buffer of the RTSS voltage.
A 0.01uF ceramic capacitor (CRTSS) should be connected from terminal RTSS to ground.

When the UVLO is about to be released, the RTSS pin is quickly charged up to VRTSS=0.45V by an internal current source (IRTSS=100uA) due to pre-charge function. CRTSS is later discharged during UVLO.
If the voltage of pin RTSS reaches 0.45V, the UVLO is released and soft start function is started.
The CRTSS charging time (TRTSS) is the time it takes before CSS is charged at start-up of DC/DC operation.
TRTSS is given by:

(ex.) CRTSS=0.01uF
TRTSS= (0.01uF × 0.50V) / 100uA = 50 [us]

The CLKOUT pin outputs a square wave synchronized to the internal oscillator.
CLKOUT is intended to serve as clock for synchronizing master-slave configurations.

(5) EXTERNAL SYNCHRONIZATION (SYNC)

This IC can be synchronized to an external clock through the SYNC pin for noise management. It can either be used as a Master IC which outputs a clock signal through the CLKOUT terminal, or as a Slave IC which accepts an input clock signal through the SYNC terminal. The SYNC pin is connected to GND when the IC is not configured as Slave.

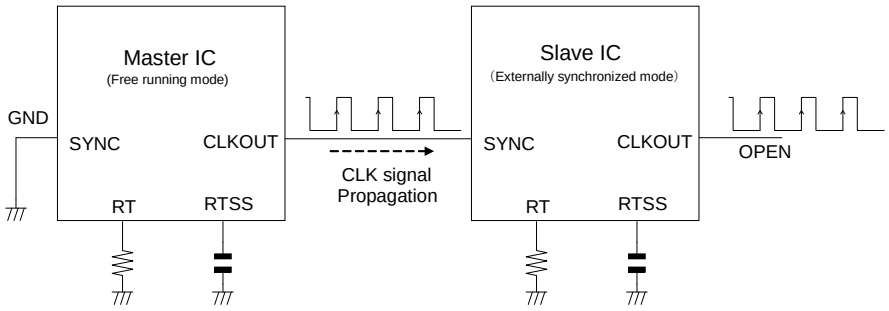


Fig.43 Example of an External Synchronization Circuit

Synchronization happens after three consecutive rising edges at the SYNC terminal. The clock frequency at the SYNC pin replaces the master clock generated by the internal oscillator circuit.
Pulling the SYNC pin low configures the BD9611MUV to freely run at the frequency programmed by RRT.

◆ Input Wave Conditions into the SYNC Pin

The synchronization frequency should be in the range of -10% to +10% in relation to the programmed free-run frequency, that is within the range of 50 to 500kHz. The input pulse width should be more than 500ns and its high level should be within 2.8V to 5.0V. There is no special sequence against VCC or CTL. Please refer to the discussion of RRT vs Frequency from the previous page in deciding the RT resistor value to be used when using fixed-frequency input signal into SYNC.

It is recommended to decide whether the BD9611MUV synchronizing function is used or not before start-up.
If synchronization is done after start-up, please consider the fluctuation of Vout caused by the momentary instability of oscillation. When the SYNC pin becomes open, the oscillator state is changed from synchronized mode to free-run mode after eight consecutive pulses had not been detected. The BD9611MUV operating frequency will gradually change to the free-run frequency programmed by RRT. The speed of transition depends on how fast the RTSS voltage stabilize to 0.5V by charging or discharging CRTSS with IRTSS (=5uA max). The frequency changes as RTSS shifts.
The RT voltage is fixed to almost 0.5V during free-run mode. In synchronized mode, the RT voltage adjusts freely between 0.25V and 1.0V for the oscillator to be able to output the synchronized frequency. The movement of the RT voltage is smoothed out by CRTSS. When the capacitance of the CRTSS is too small, the frequency fluctuates. However, if the capacitance is too large, it takes longer to synchronize the frequency. CRTSS should be adjusted accordingly to the intended circuit behavior.

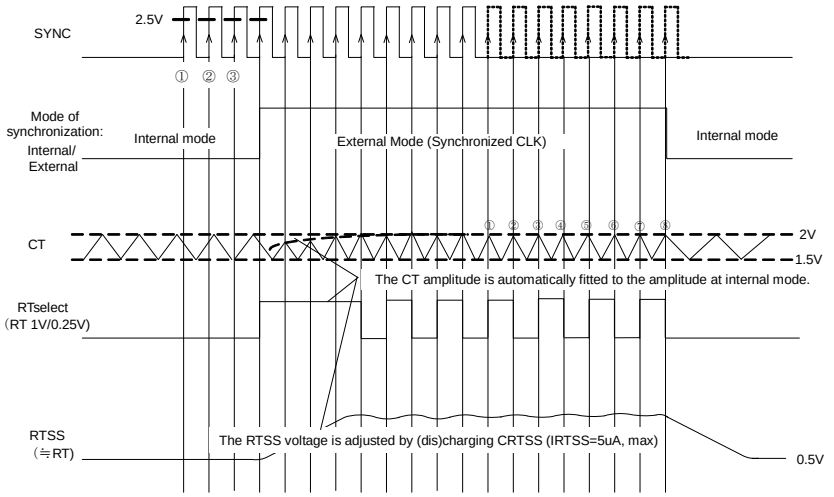


Fig.44 Timing Chart of External Synchronization

(6) PWM / BOOST (PRE-CHARGE MODE)

Charging capacitor CBST (BST-LX) is needed to drive the high-side N-channel FET.
CBST is charged to the voltage of REG10 through the internal FET switch between REG10 and BST, whenever the low side external FET is turned on.
The maximum on duty does not reach 100% because of the LG minimum ON pulse. It is possible to charge CBST even if the voltage of the FB pin is over 2.0V (high voltage of the internal ramp wave) and for terminal HG to always output HIGH. In case the voltage values of Vin and Vout are becoming close, the voltage of Vout can never become equal to the voltage of the Vin.

※ MAX DUTY

BD9611MUV turns off for almost 350nsec at every turn. This is the High-side Min Off Pulse (HGmin).
The 350ns duration of HGMIN consists of the LG Min pulse (about 100ns) and the anti-cross conduction time between HG and LG (100ns each).
The Max ON Duty is calculated in the following equation:

D(on) = (T – Toff) / T Where: T: Switching Cycle (=1/FOSC), Toff: OFF time (≒350ns Typ)

※ PRE-CHARGE MODE

The BD9611MUV operates at pre-charge mode during the time when CBST is charged at start-up. By dropping the voltage of CBST and releasing the protect functions (UVLO, TSD, OCP hiccup-mode), CBST is charged in advance. In this mode, capacitor CBST is charged by the LG ON pulse which is limited to almost 300ns at every cycle.
Pre-charge mode changes to normal switching mode after the release threshold of BSTUVLO had been detected.

(7) STAND-BY

It is possible to make the quiescent current value go as low as 0uA by turning off the IC using the CTL pin.
All IC functions such as REG5 and REG10 are terminated in this mode.

(8) UVLO

The UVLO circuits shut down HG, LG, SS and FB, when the voltage of any of the three supplies VCC, REG10 or REG5 are under their respective UVLO threshold (VCC<9V, REG10<8V, REG5<4.5V). Voltage hysteresis is also present for the supplies VCC, REG10 and REG5 (VCC: 0.5V, REG10: 0.5V, REG5: 0.2V). Whenever the UVLO is released, soft-start begins after the voltage of RTSS is over 0.5V. In case quick start-up is needed, please adjust the capacitance of CRTSS accordingly.
BST_UVLO protection exists between BST and LX. When the BST_UVLO threshold is detected, HG, SS and FB are all shut down, then BD9611MUV shifts to pre-charge mode where CBST is charged every LG pulse (t≅300ns).

(9) TSD

TSD is the protection of the IC against abnormal temperature, which starts at temperature greater than T_{JMAX} (150°C). The TSD gets triggered at almost 175°C, so it doesn't work in the normal operating temperature range. TSD is automatically released after being cooled back to 150°C or lower. Under TSD protection, HG, LG, SS and FB are all shut down similar to UVLO.

(10) LG short protection

When the LG pin short to GND, an exceptional large current flow occurs in BD9611MUV.
(Reason: The DC/DC is able to output under diode-rectifier mode by the body diode of the low side Nch-FET.)
For this case, BD9611MUV checks after the PWM low output in every cycle before turning on LG. If LG doesn't turn on, the DC/DC will be shut down.

(11) PROGRAMING OCP

This IC monitors the voltage between CLH and CLL when turning on the High-side driver (HG=ON).
When this voltage exceeds the threshold as configured by RRCL, the output is turned off immediately.
The switching current is monitored using the current sense resistor Rs, which is usually connected to the drain of the high-side FET.

The value of the OCP current is determined by the following:

$$IOCP = VOCPTH / Rs \quad (8)$$

IOCP：OCP trigger current
VOCPTH：OCP threshold voltage between CLH and CLL configured using RCL
Rs：Current sense resistor

The OCP threshold is set by the resistor RRCL connected from terminal RCL to ground.
Please refer to the graph below:
Using RRCL>12.5kΩ, take into consideration the increase of OCP variability.

$$VOCPTH = (0.8 / RRCL) \times 1850 \text{ [mV]}$$ RRCL: Resistor connected to the RCL pin [kΩ]

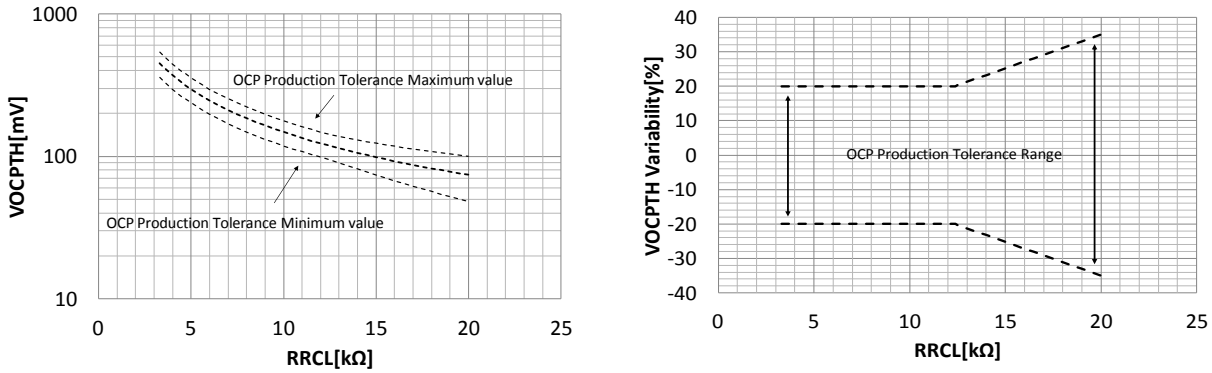


Fig.45 OCP Threshold vs RRCL

Resistor Rs senses the OCP voltage and is connected between VCC and the drain of the High-side Nch-FET.
It is recommended that sensing be improved by using an RC filter between CLH and CLL as shown Figure 46.
This filter should be available for response stability in controlling detected variation. Ensure that CLH and CLL are not connected to traces subjected to common impedance, such as when connecting it to the large-current trace far from either side of Rs. The RC filter is connected between CLH, CLL and at either ends of Rs. It is comprised of Cocp and Rocp as shown below. The impedance of Cocp should be the lowest possible under noise frequency (adjust noise frequency and self-resonant frequency if needed) and should maintain a fixed filter constant with Rocp.

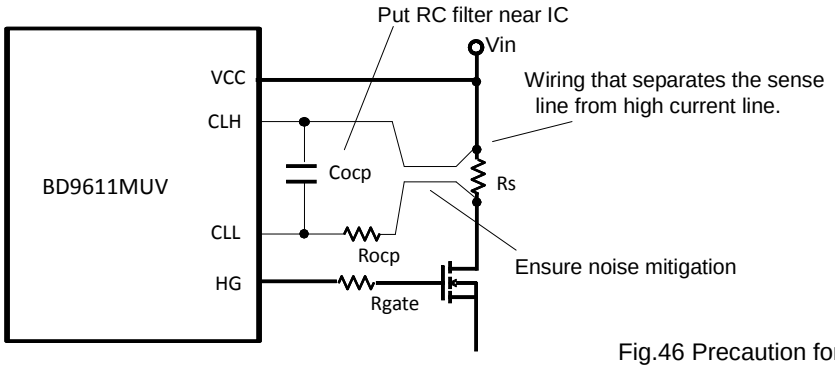


Fig.46 Precaution for CLH, CLL filter

Please take into consideration the ON resistance of the external FET and the wiring pattern when setting up OCP.
Due to variable FET ON resistance and large switching noise, false over-current detection might happen.

Please connect CLH to the VCC line and CLL to the line which connects to LX when the FET is on.

Connect RCL to REG5 and CLH/CLL to VCC without using the shortest lines with high common impedance.

＜Pulse by Pulse Protection＞
The over-current detection of OCP initially does not work for almost 60ns due to the blanking time against LX ringing noise. It also has an action delay time of almost 140ns after over-current is detected.
When the switching frequency and the ratio of Vin and Vout are both high, this IC might not detect over-current. Please take into consideration the minimum pulse width and refer to the graph of item no (13) “About Output programmed voltage range”.

＜Hiccup Protection＞
When over-current is detected twice in either two or three consecutive pulses, the outputs FB and SS are turned off within the specified OCP shut-down hold cycles (equivalent to 32768 clock cycles).
(ex.) FOSC = 300kHz

$$\text{OCP shut-down hold cycles (THICCUP)} = T = (1 / FOSC) \times 32768$$
$$= (1 / 300k) \times 32768 = 108\ [ms]$$

At the end of the OCP shut-down hold cycles, the soft start procedure begins automatically.

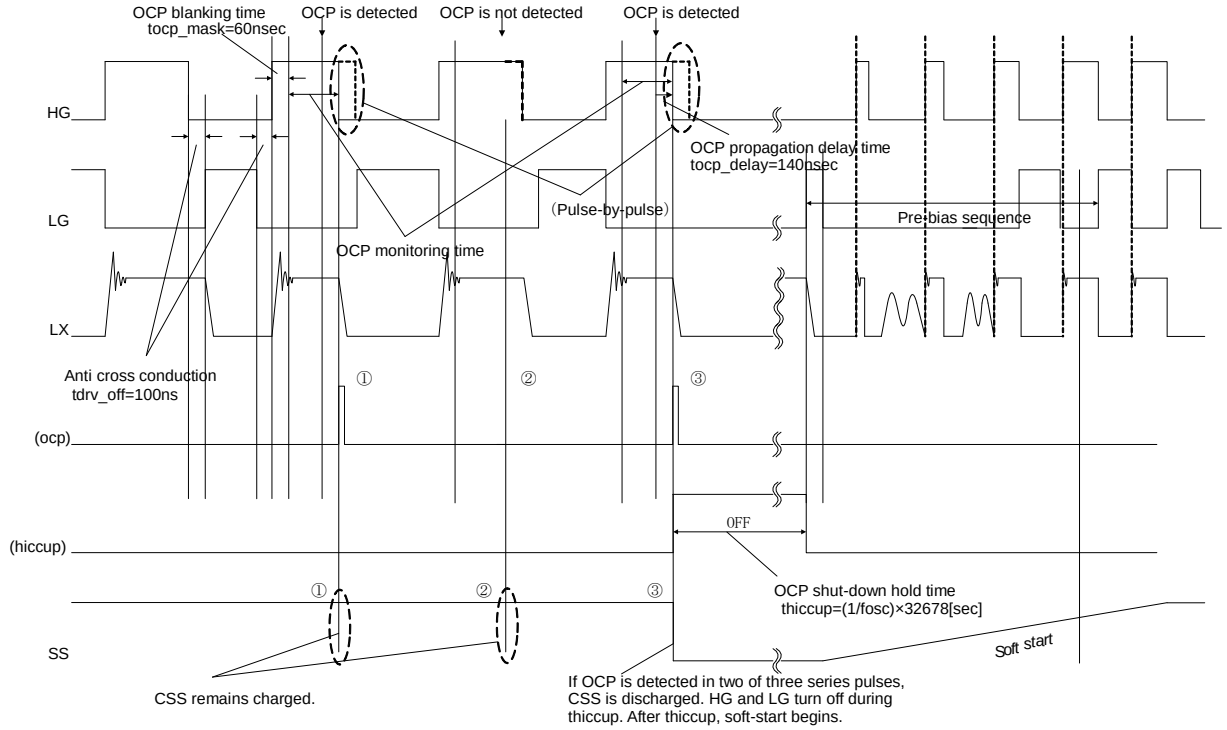


Fig.47 OCP Timing Chart (※To explain the sequences, the time axis of this graph is not scaled to actual)

(12) PRE-BIAS

This IC is designed not to sink large current from Vout, even if Vout had been biased at high voltage upon startup. However, there is a potential of an increase in output voltage through Body-Di of BST, during the charge cycle of switching. This happens when the programmed output voltage is under 10V.

To prevent this, connect a load resistor between Vo and PGND to serve as discharge path when using Vo<10V. Please use the table in Figure 49 as reference in choosing the discharge resistance value.

This issue does not exist when Vo≧10V.

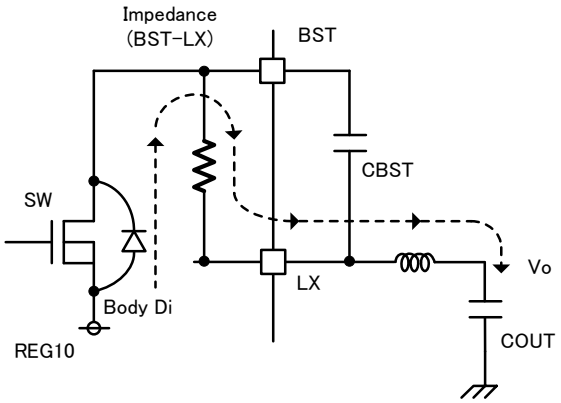
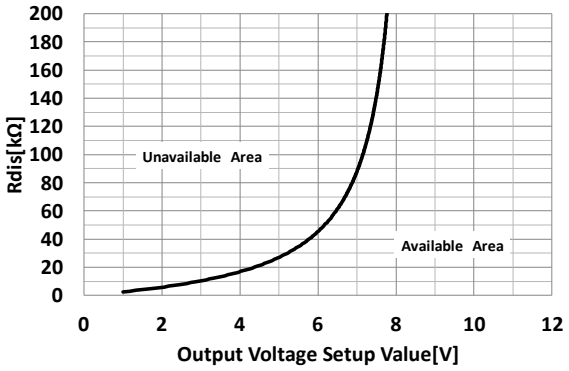


Fig.48 Current Passes Through PRE-BIAS at Low Output Voltage Setting



Vo[V]	Rdis[kΩ]
1.0	2.5
2.0	6.5
3.0	10.5
3.3	12.0
4.0	17.0
5.0	27.0
6.0	45.5
7.0	88.5
8.0	302.0

Fig.49 Output Voltage Setting vs Load Resistance

(13) Programmed Output Voltage Range

This IC's programmable output voltage is limited to the available area shown on Figure 50. In application, the programmable output voltage is restricted from the unavailable area on the graphs due to input-voltage, frequency, high-side minimum off pulse and load current.

◆ Relation Between Frequency and Input-Output Voltage Ratio

This IC has a limitation in programmed output voltage as shown on the following graphs due to the minimum pulse available for feedback control and programmed OCP detect voltage.

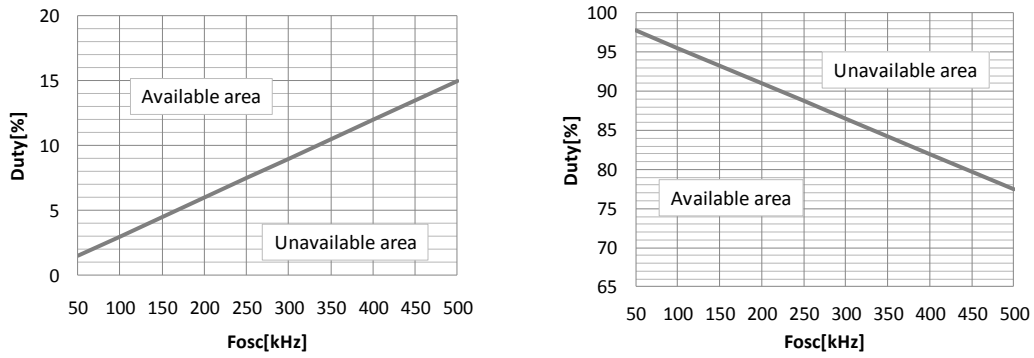


Fig.50 Frequency vs Input-Output Voltage Ratio (Duty)

◆ High-side (HG) Minimum Off Pulse

This IC has a limitation in programmed output voltage due to the Hi-side Minimum Off Pulse for charging BST capacitor (CBST) which adopts the Bootstrap system.

Consider toff=450ns as the OFF duty pulse.

In cases where the configured output voltage is near the input value, the output voltage gets affected by this off pulse.

Take into consideration the reduced output voltage limit when the programmed output voltage is near input value.

For example:

Programmed output voltage: Vo = 12V, Frequency: f = 250kHz (T = 1/f = 4us)

OFF_Duty = 1 – (Vo / Vin), Minimum OFF pulse: toff_min = T × OFF_Duty

toff_min = T × (1 - Vo /Vin) = 4us × (1 – 12V / Vin) ≧ 450ns → Vin ≧14.95V

It is necessary that the condition Vin ≧ 14.95V is satisfied to ensure that the programmed output Vo = 12V is reached.

Additionally, take into consideration the Ron voltage drop of the high-side FET, the DCR of coil and the PCB pattern impedance.

◆ Load current

There are no limitations on the load current when the programmed output voltage holds the condition Vo ≧ 10V.

However, certain limitations are imposed when Vout is under 10V because of the Pre-bias sequence.

Please refer to No. (12) PRE-BIAS on page 24.

(14) About programmed External UVLO (EXUVLO)

VCC detect and release voltages are configurable using external resistances connected to CTL as shown in Figure 51. When VCC voltage is lower than detect voltage, it is designed to stop the output (HG="L", LG="L") and discharge SS and FB.

The constant current connected to CTL (that turns the IC ON/OFF) is sourced after the release threshold voltage. A current value of (VCTL - 5.6V) / 100kΩ sinks to CTL when applying VCTL > 5.6V. This is due to a 5.6V clamping circuit connected through 100kΩ to CTL terminal as shown in Figure 52.

The IC is unable to turn off after reaching the release threshold voltage because of the constant current sourced to CTL, when the external resistances (R1, R2) are opened.

Please supply VCTL < 0.3V to put the IC back into stand-by.

(Ex.) Programmed Release Voltage: (Vuv+) = 21V, Hysteresis Voltage: (Vhys) = 4V (Detect Voltage = 17V)

Vuv+ = (R1+R2) / R2 × VEXUTH

Vhys = R1 × IUVHYS

Where: VEXUTH=2.6V (Typ), IUVHYS=20uA (Typ)

When calculating the equations above, resulting values are: R1=200kΩ, R2=28.26kΩ.

Considering production tolerance and temperature characteristics, the max release voltage threshold is 21.63V and the min detect voltage threshold is 15.37V. This is when using R1=200kΩ and R2=28.26kΩ, given that VEXUTH = 2.6V±3%, IUVHYS = 20uA±25%.

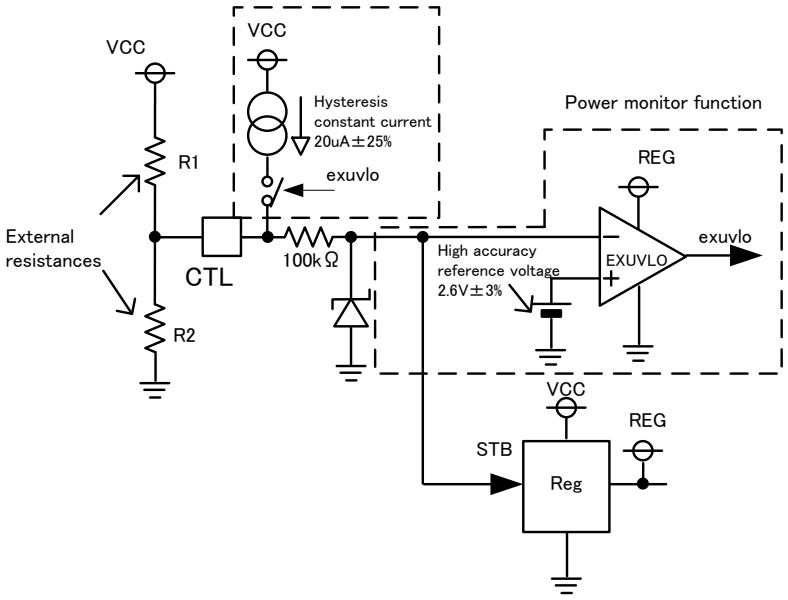


Fig.51 Circuit Configuration of EXUVLO

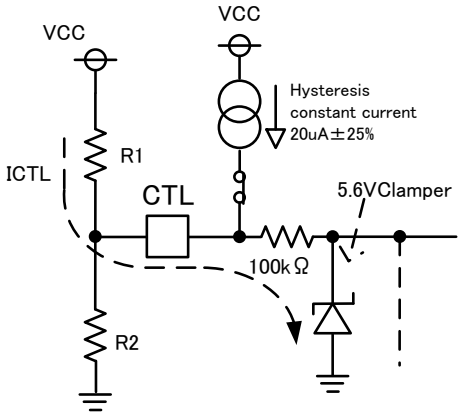
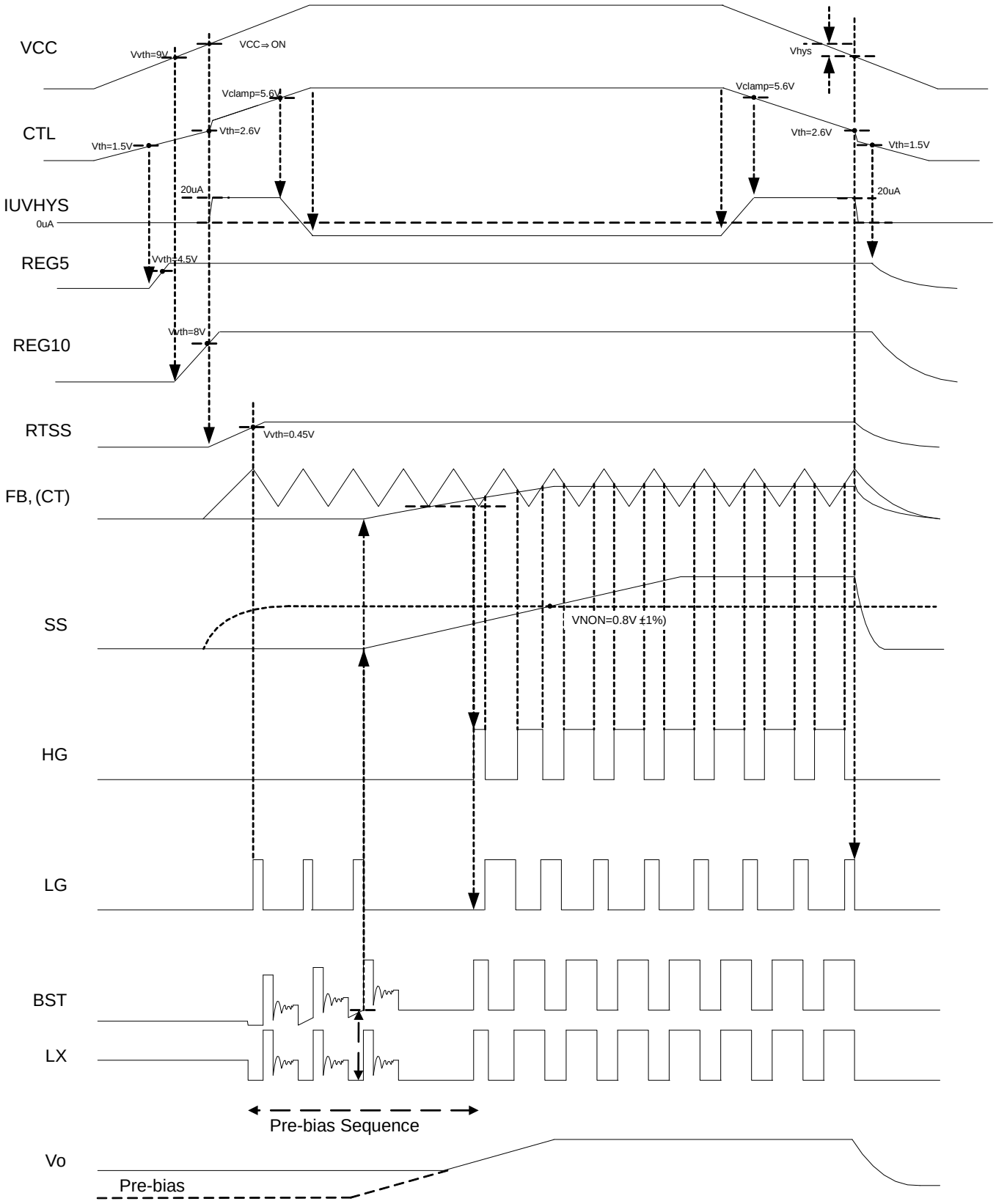


Fig.52 Current Path at CTL > 5.6V

● **TIMING CHART (START-UP)**



Note: To explain the sequences, the time axis of this graph is not scaled to actual

Fig.53 Timing Chart (Start-up)

● **Selection of Externally Connected Components**

(1) INDUCTOR

It is recommended that the inductor satisfies the absolute maximum current, has low DC resistance, and is shielded type. The inductance affects the ripple current and Vo ripple voltage. Increasing either the inductance or the switching frequency makes the ripple current small.

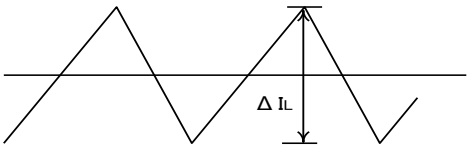


Fig.54 Inductor Current

Ipeak = Iout＋1/2 × ⊿IL [A] (1)

⊿IL = (Vin - Vout) / L × (Vout / Vin) × (1 / fosc) [A] (2)

(Where: ⊿IL: Inductor ripple current, fosc: Switching Frequency)

Generally, ⊿IL is chosen such that the converter enters discontinuous mode at 20-40% of nominal load.

If the inductor current exceeds the maximum current, the inductor may undergo saturation and the efficiency becomes poor. Sometimes, the DC/DC may cause oscillation. It is very important to select an inductor that can support the largest absolute current with enough margins.

(2) COUT

It is recommended to select a capacitor with small ESR for decreasing the Vout ripple voltage.
It is also important that the capacitor has high absolute voltage rating with regards to DC bias characteristic.
The Vout ripple voltage is calculated by the following equation:

Vripple =⊿IL × 1 / (2π × f × Cout)＋⊿IL × Resr (3)

If the capacitance of Cout is too large, it won't be able to start up. Please refer the following equation:

Cout ≦ tss × (Iocp – Iout) / Vout (4)

Where: tss: Soft Start Time, Iocp: OCP Detect Current

(3) SETTING OF VOUT

The reference voltage of the ERROR AMP is set to 0.8V.
The Vout voltage is calculated by the following equation

VOUT = (R1＋R2) / R2 × 0.8 [V] (5)

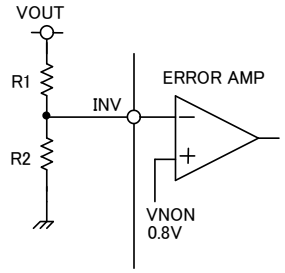


Fig.55 Vout setting

(4) FET

It is required to select high-current capability FETs because of the short-circuit current and the high switching spike noise. Please choose FETs with low Ciss or low Qg for low noise and high efficiency of application.
Consideration should also be given to the gate bias voltage, since BD9611MUV drives the FETs using 10V driver.

(5) CBST

The capacitor connected from BST to LX is the power supply for the high side FET driver.
For general applications, a 0.47uF ceramic capacitor should be connected.

(6) CIN

The absolute maximum voltage rating, ripple current and low ESR should be taken into consideration when choosing CIN. Please refer to the Irms equation below for calculating the ripple current:

Irms = Iout × √ (Vout × (Vin - Vout) / Vin) (6)

(7) Adjusting the Frequency Characteristic of the DC/DC Converter

This IC contains a voltage-mode PWM controller.

For the entire DC/DC system's stability, lead compensation (fz1, fz2) is adjusted using the R and C around INV and FB against lag (fp2), which is comprised of L and COUT.

The target frequency of the whole system should satisfy:

- Unity gain frequency (Gain = 0dB): 1/10 to 1/30 times of switching frequency (FOSC)
- Phase margin: $\theta \geqq 30°$

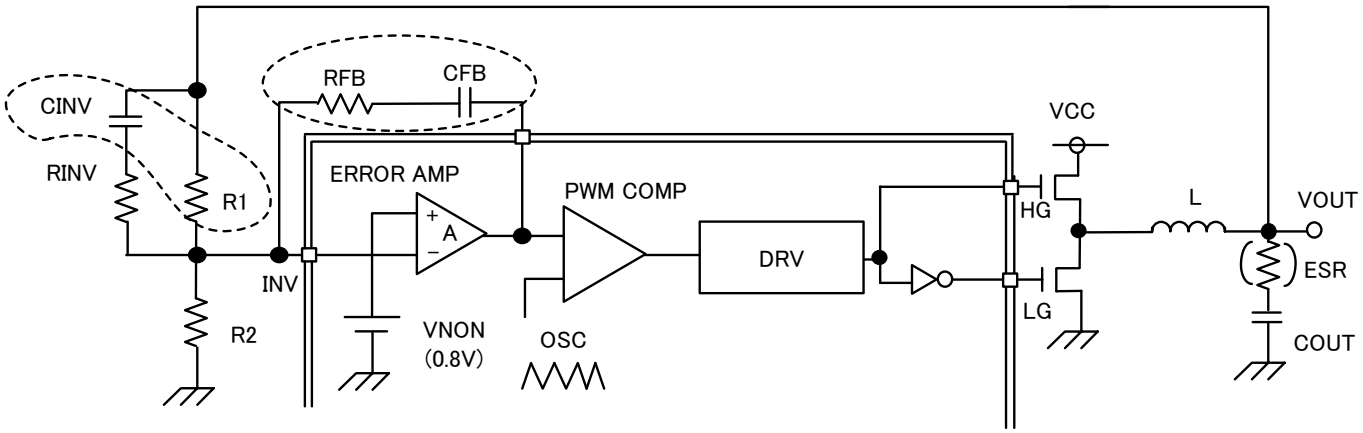


Fig.56 The phase compensation whole DC/DC system

There are two poles (phase lag) on the DC/DC behavior as shown by the system figure above:

① Pole around ERR_AMP (fp1)

$fp1 = 1 / [2 \cdot \pi \cdot (R1//R2) \cdot A \cdot CFB]$ ・・・1st lag (90°)

② Pole of LC filter (fp2)

$fp2 = 1 / [2 \cdot \pi \cdot \sqrt{(L \cdot C)}]$ ・・・2nd lag (180°)

This can be fixed by two phase-lead compensation using zero points against the 2nd lag pole (②) of the LC filter so that the total phase would not lag by 180°.

Please set the RC constant such that each frequency fz1, fz2 (and fz3) cancels fp2.

③ Zero of output capacitor ESR (fz1)

$fz1 = 1 / (2 \cdot \pi \cdot COUT \cdot ESR)$ ・・・1st lead (90°)

④ Zero around ERR_AMP (fz2)

$fz2 = 1 / (2 \cdot \pi \cdot CFB \cdot RFB)$ ・・・1st lead (90°)

⑤ ※ Zero around ERR_AMP (fz3)

$fz3 = 1 / (2 \cdot \pi \cdot CINV \cdot R1)$ ・・・1st lead (90°)

※ There is no need to set fz3 when fz1 is sufficient, particularly when using a high-ESR capacitor on the output such as an electrolytic capacitor.

In addition, fz3 needs to be set if fz1 lands at the high frequency range, particularly when using a low-ESR capacitor such as a ceramic-type.

It is possible to adjust the frequency characteristic by using a value of RINV that is around 1/10 of the value of either R1 or R2 (given same R1 and R2) to add the pole and shifted zero point.

Please confirm the actual results because capacitor ESR characteristic and DC bias characteristic change when using either ceramic-type or electrolytic-type capacitors, or when temperature varies. In such cases, output voltage may have changed.

Recommendation: Confirm the bode diagram using a Frequency Response Analyzer (FRA).

(8) Output Startup Rush Current

The three inputs of the error-amplifier shown on Figure 57 are the SS terminal, a 0.8V reference voltage, and a feedback terminal (INV). The SS terminal voltage increase in a slope as the external capacitor CSS is charged using a constant current (ISS=1uA). This is to protect against start-up rush current and overshoot.

When the SS terminal voltage is lower than 0.8V, it is used as reference by the ERR AMP to control output voltage. Switching action does not yet occur at this state and the output voltage is “L” until FB reaches 1.5V.

After reaching FB=1.5V, FB can then be used as reference by a comparator with the internal 1.5V-2.0V triangle waves, as shown in Figure 58.

The start-up output voltage at the state when SS voltage is increasing and switching is OFF can be calculated as shown below. In addition, the rush current when FB becomes 1.5V is proportional to the start-up voltage and output capacitor value. Thus, consideration should be given in choosing the external capacitor.

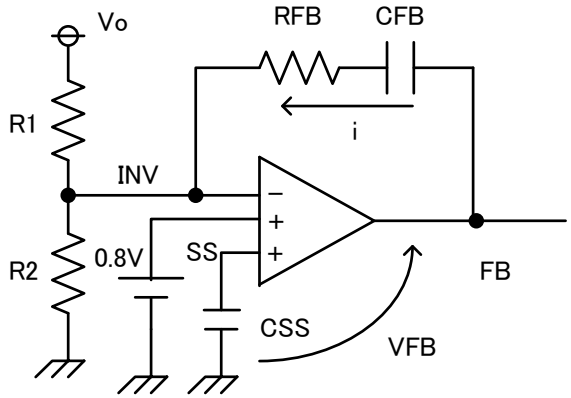


Fig.57 ERR AMP Schematic

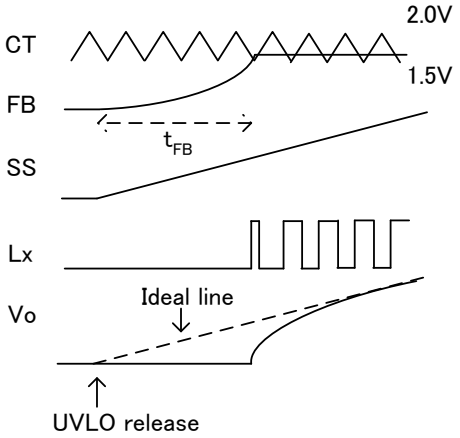


Fig.58 Startup Timing Chart

$$t_{FB} = C_{FB}\left\{\sqrt{\left(R_{FB}+R_2\right)^2+\frac{3C_{SS}R_2}{C_{FB}I_{SS}}}-\left(R_{FB}+R_2\right)\right\}$$

$$V_O = \frac{I_{SS}\left(R_1+R_2\right)}{C_{SS}R_2}\times t_{FB}$$

● **PCB Pattern and Layout Consideration**

(1) It is very important to minimize loops ① and ② to reduce the switching noise caused by parasitic inductance of the trace. Great care should also be given to the gate wiring.

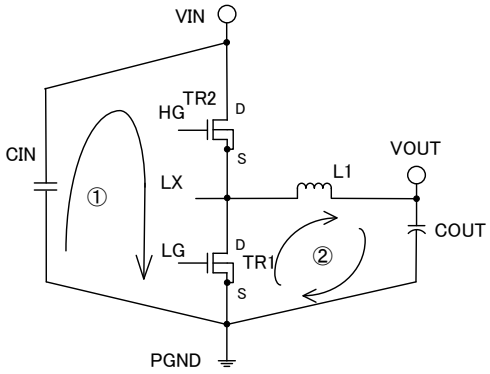


Fig.59 Current loop paths on PCB

(2) Using long traces for switching nodes like LX, HG and LG that have wide voltage fluctuations may cause low efficiency and produce large noise. Please minimize the switching node trace length and provide enough current tolerance.

(3) The FETs will most likely become the hottest device during DC/DC operation. Please take measures to manage the heat, such as using a multiple-layer board and connecting each FET source/drain patterns with multiple thermal via. The pad of the bottom of the IC which serves as thermal sink should also be connected to the GND pattern.

(4) The PGND plane should be shorted to the GND plane below the BD9611MUV. All GND connections should have low impedance with respect to the GND plane. Low impedance is important for stable operation.

(5) There are sensitive analog nodes that are prone to noise and are easily affected at switching mode. Please keep the periphery of the analog control section (REG5, SS, INV, FB, RCL, RTSS and RT) away from both the periphery of the switching power section (BST, HG, LX, REG10 and LG), and the periphery of the switching clock section (SYNC and CLKOUT).

(6) For stable operation, the capacitors of VCC, REG5, RTSS and the resistors of RT and RTSS should be connected to a stable GND plane (which is connected to the GND pin) without any common impedance due to large current.

(7) The VCC and GND nodes should both be wide to reduce line impedance and to keep the noise and voltage drop low.

● **Power Dissipation**

Shown below is the power dissipation characteristic of the IC when mounted on a 70mm × 70mm × 1.6mm, 4 layer PCB. Junction temperature must be designed not to exceed 150°C.

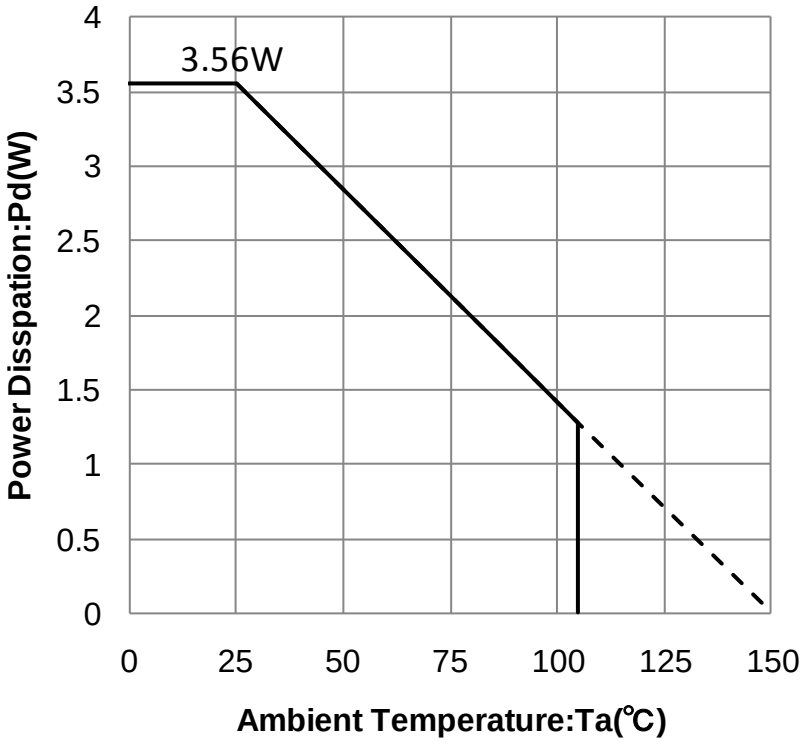
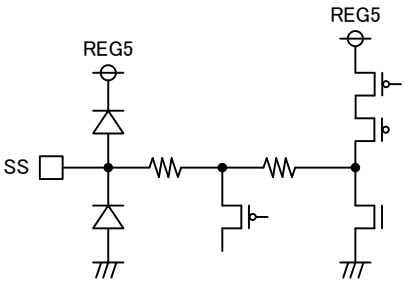
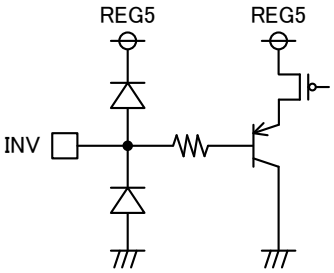
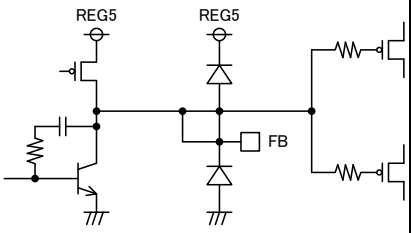
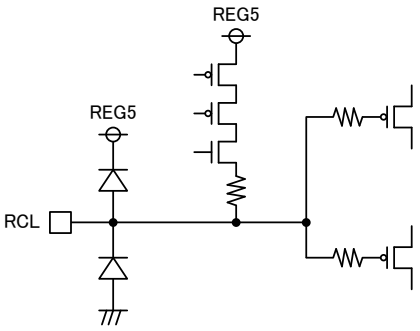
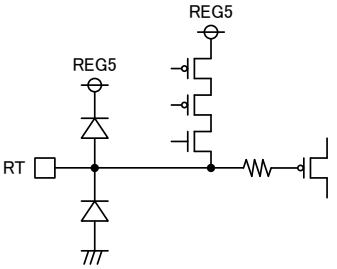
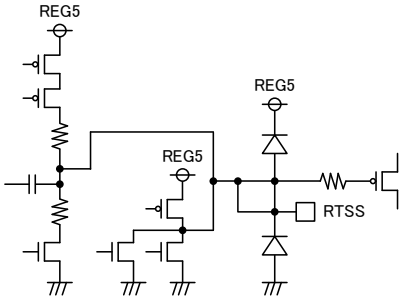
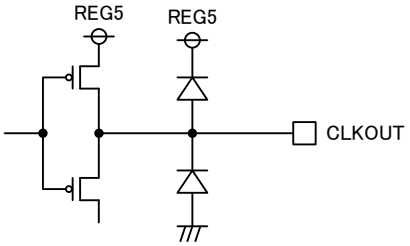
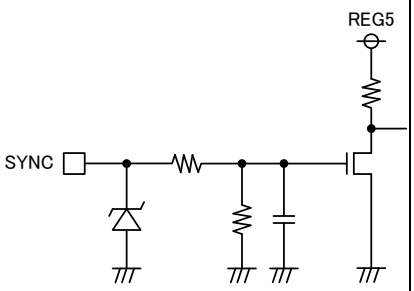
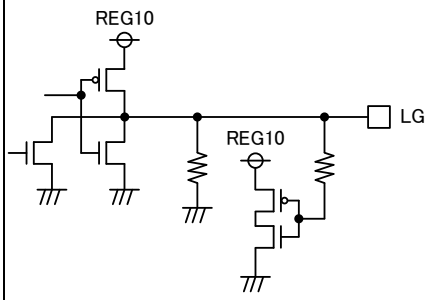
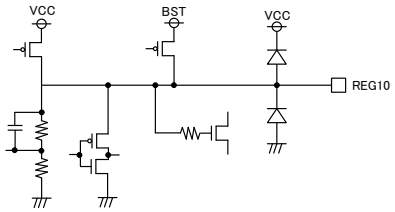
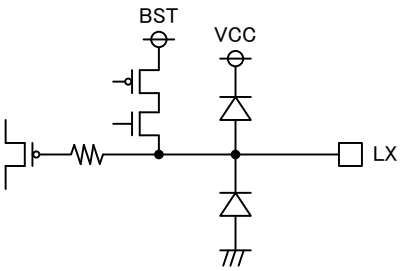
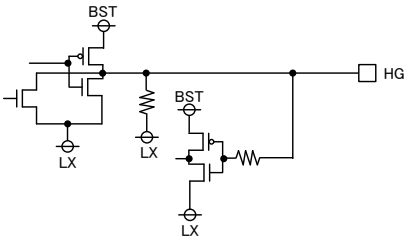
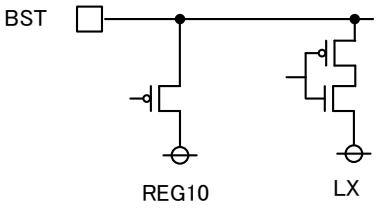
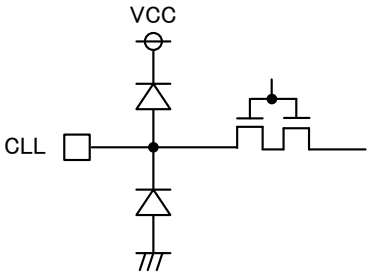
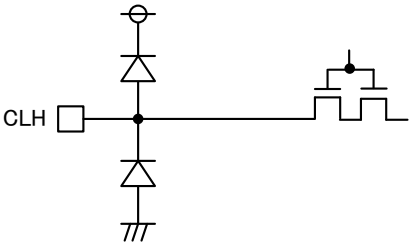
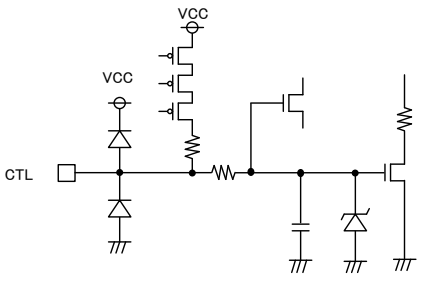
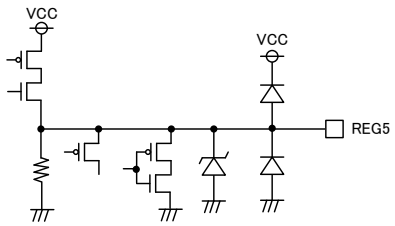


Fig.60 Power Dissipation

● **I/O Equivalent Circuit**

Pin. No	Pin Name	Equivalent Circuit	Pin. No	Pin Name	Equivalent Circuit
1	GND		2	SS	
3	INV		4	FB	
5	RCL		6	RT	
7	RTSS		8	CLKOUT	
9	PGND		10	SYNC	

Pin. No	Pin Name	Equivalent Circuit	Pin. No	Pin Name	Equivalent Circuit
11	LG		12	REG10	
13	LX		14	HG	
15	BST		16	CLL	
17	CLH		18	VCC	
19	CTL		20	REG5	

Operational Notes

(1) Absolute Maximum Ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) GND Potential

Ensure a minimum potential for the GND pin at all operating conditions.

(3) Design for Heat Dissipation

Use a thermal design that allows for a sufficient margin with respect to the power dissipation (Pd) in actual operating conditions.

(4) Short Circuit Between Pins and Erroneous Mounting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

(5) Operation within Strong Electromagnetic Field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(6) Temperature Protect Circuit (TSD Circuit)

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

(7) Testing on Application Boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

(8) Common Impedance

The power supply and GND lines should have minimal common impedance and ripple. This can be done by making the traces thick and short, and by using LC components as near to the IC as possible, along with other methods.

(9) Bypass Diode

During application, it is possible that the VCC potential becomes lower than those of other pins, causing internal circuit damage. For example, during cases when charge is given to an external capacitor, and the VCC is suddenly shorted to GND. it is recommended to insert a bypass diode in series with VCC, or between each pin-VCC connections for back current prevention.

(10) Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, with the resistor and transistor models connected to the pins as shown in Figure 61, a parasitic diode or transistor operates by inverting the pin voltage and GND voltage.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

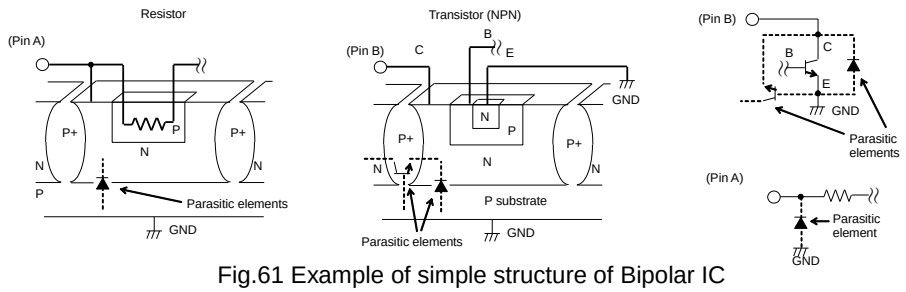


Fig.61 Example of simple structure of Bipolar IC

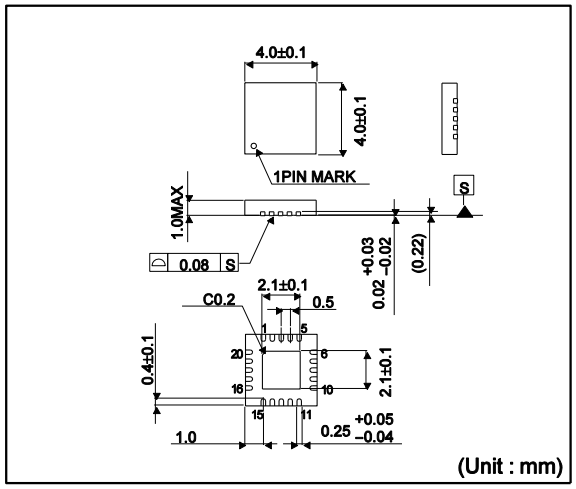
● **Ordering Information**

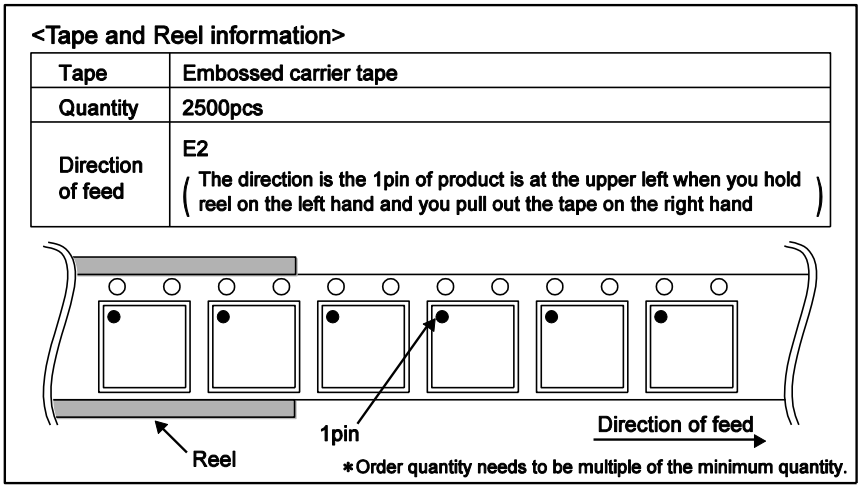
B	D	9	6	1	1	M	U	V	-	E	2

Part No.	Part No.	Package	Packaging and forming specification
		QFN: VQFN020V4040	E2: Embossed tape and reel

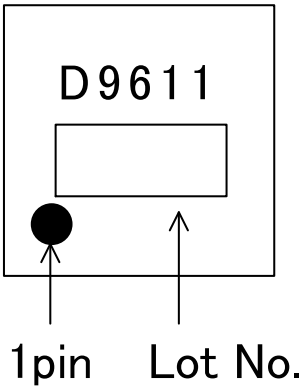
● **Physical Dimension Tape and Reel Information**

VQFN020V4040





● **Marking Diagram (Top View)**



●**Revision History**

Date	Revision	Changes
14.MAR.2013	001	New Release
15.MAY.2014	002	Correction of Typographical Error.
17.OCT.2014	003	RRCL operating rating (P.5) and add graph of OCP production tolerance(P.22)

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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