7V to 28V Input, 1.5A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9E103FJ

General Description

BD9E103FJ is a single synchronous buck DC/DC converter with built-in low on-resistance power MOSFETs. The SLLM™ control provides excellent efficiency characteristics in light-load conditions which make the product ideal for equipment and devices that demand minimal standby power consumption. BD9E103FJ is a current mode control DC/DC converter and features high-speed transient response. Phase compensation can also be set easily.

Features

- Single Synchronous Buck DC/DC Converter
- 5V Fixed Output Voltage
- SLLM™ (Simple Light Load Mode) Control
- Efficiency = 80% (@I_{OUT}=10mA)
- Over Current Protection
- Short Circuit Protection
- Thermal Shutdown Protection
- Under Voltage Lockout Protection
- Over Voltage Protection
- Internal Soft Start
- Reduced External Diode
- SOP-J8 Package

Applications

- Consumer Applications such as Home Appliance
- Secondary Power Supply and Adapter Equipment
- Telecommunication Devices
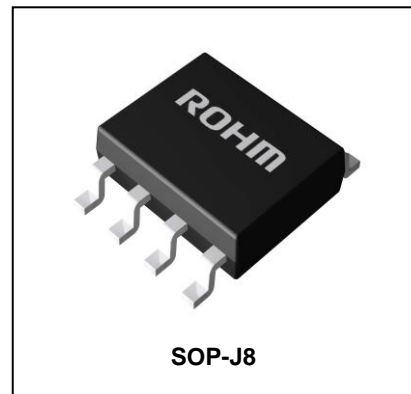
Key Specifications

- Input Voltage Range: 7V to 28V
- Fixed Output Voltage: 5.0V (Typ)
- Output Current: 1.5A (Max)
- Switching Frequency: 330kHz (Typ)
- High-Side MOSFET ON-Resistance: 250mΩ (Typ)
- Low-Side MOSFET ON-Resistance: 200mΩ (Typ)

Package

	W (Typ) x D (Typ) x H (Max)
SOP-J8	4.90 mm x 6.00 mm x 1.65 mm

SOP-J8

Typical Application Circuit
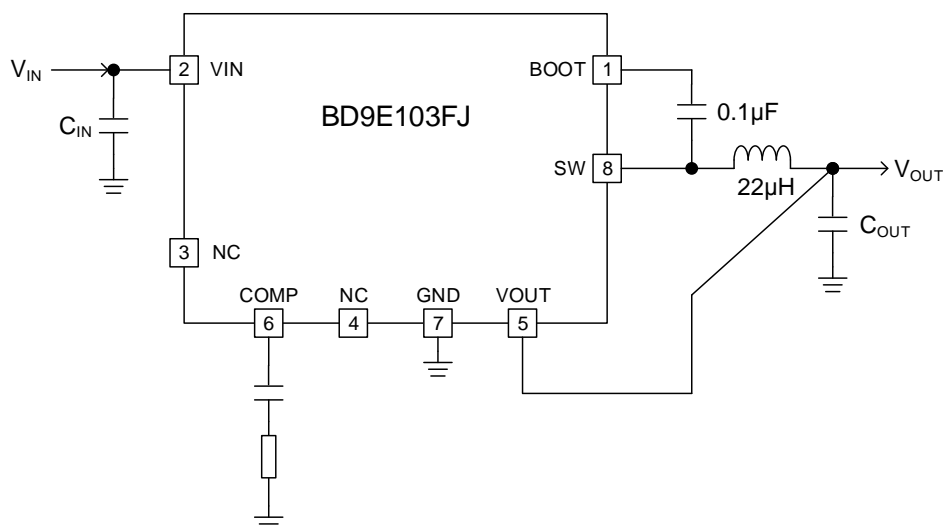
Figure 1. Application Circuit

○Product structure : Silicon monolithic integrated circuit.　○This product has no designed protection against radioactive rays.

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Pin Configuration

(TOP VIEW)

BOOT	1		8	SW
VIN	2		7	GND
NC	3		6	COMP
NC	4		5	VOUT
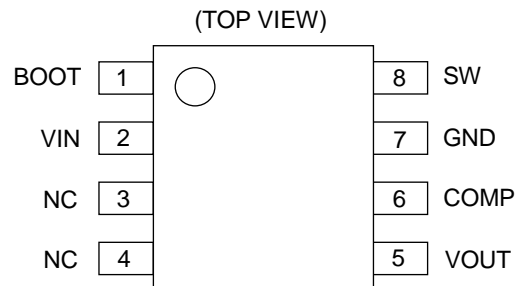
Pin Description

Pin No.	Pin Name	Description
1	BOOT	Connect a bootstrap capacitor of 0.1µF between BOOT terminal and SW terminal. The voltage of this capacitor is the gate drive voltage of the High-Side MOSFET.
2	VIN	Power supply terminal for the switching regulator and control circuit. Connecting a more than 10µF ceramic capacitor is recommended.
3	NC	No connection terminal.
4	NC	No connection terminal.
5	VOUT	Output voltage sense terminal.
6	COMP	Output terminal for the error amplifier and input terminal for PWM comparator. Connect phase compensation components to this terminal.
7	GND	Ground terminal for the control circuit and output stage of the switching regulator.
8	SW	Switch terminal. This terminal is connected to the source of the High-Side MOSFET and drain of the Low-Side MOSFET. Connect a bootstrap capacitor of 0.1µF between BOOT terminal and SW terminal. In addition, connect an inductor of 22µH considering the direct current superimposition characteristic.

Block Diagram

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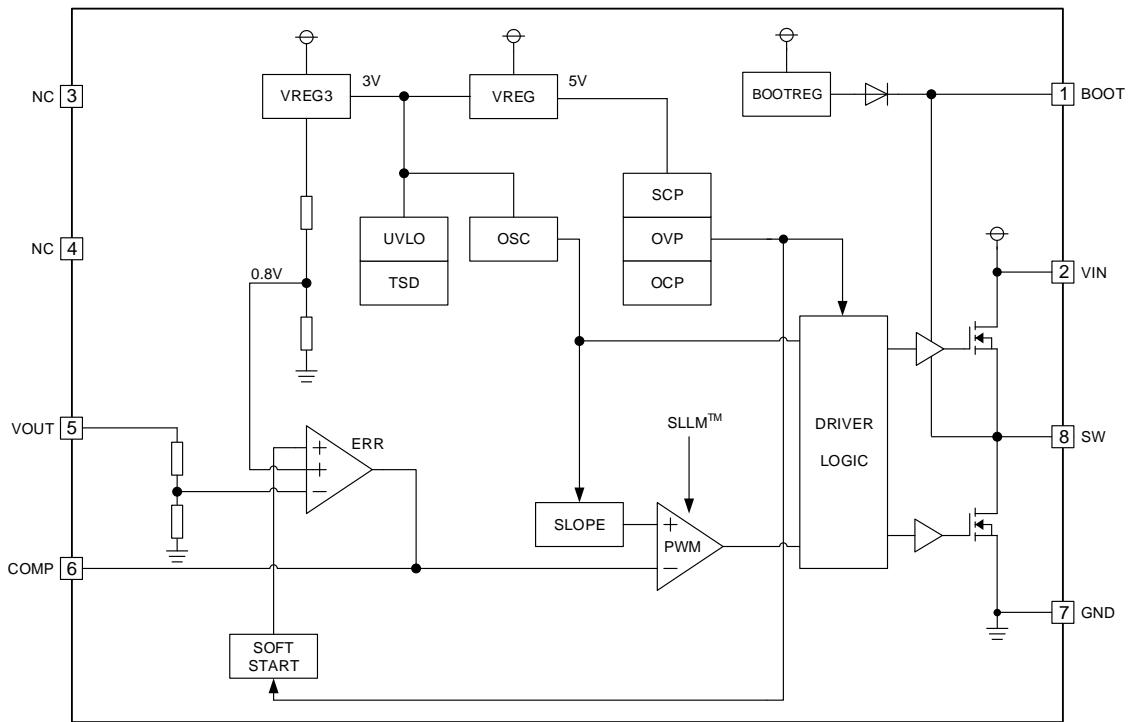
Description of Blocks

1. VREG3
   The VREG3 block generates the 3V (Typ) internal reference voltage.

2. VREG
   The VREG block generates the 5V (Typ) internal power supply.

3. BOOTREG
   The BOOTREG block generates the gate drive voltage.

4. TSD
   The TSD block is for thermal protection. It shuts down the device when the internal temperature of IC rises to 175°C (Typ) or higher. Thermal protection circuit resets when the temperature falls. The circuit has a hysteresis of 25°C (Typ).

5. UVLO
   The UVLO block is for under voltage lockout protection. It shuts down the device when the V_{IN} falls to 6.4V (Typ) or lower. The UVLO threshold voltage has a hysteresis of 200mV (Typ).

6. ERR
   The ERR amplifier compares the reference voltage with the feedback voltage of the output voltage. The ERR amplifier output voltage (the COMP terminal voltage) determine the switching duty. Also, COMP terminal voltage is controlled by internal slope voltage due to soft start function during start-up.

7. OSC
   The OSC block generates the oscillating frequency.

8. SLOPE
   The SLOPE block synthesizes slope signal generated by OSC signal and current sense signal of High-Side MOSFET. This synthesized slope signal is sent to the PWM comparator.

9. PWM
   The PWM block compares the COMP terminal voltage and the slope signal voltage to determine the switching duty.

10. DRIVER LOGIC
    The DRIVER LOGIC block generates the DC/DC driver signals. A signal from PWM comparator is applied to drive the MOSFETs.

11. SOFT START
    The SOFT START circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current. The internal soft start time is set to 4ms (Typ).

12. OCP
    Current flowing in High-Side MOSFET is controlled every cycle of switching frequency when over current protection is detected.

13. SCP
    When the output voltage has fallen below 3.5V (Typ) and remained there for 0.8ms (Typ), SCP stops the operation for 25ms (Typ) and subsequently initiates a restart.

14. OVP
    When the output voltage exceeds 6.5V (Typ), it turns off the output MOSFETs. After the output voltage drops, it returns to normal operation with hysteresis.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	-0.3 to +30	V
Voltage from GND to BOOT	V_{BOOT}	-0.3 to +35	V
Voltage from SW to BOOT	ΔV_{BOOT}	-0.3 to +7	V
VOUT Terminal Voltage	V_{OUT}	-0.3 to +7	V
COMP Terminal Voltage	V_{COMP}	-0.3 to +7	V
SW Terminal Voltage	V_{SW}	-0.5 to +30	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
SOP-J8				
Junction to Ambient	θ_{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	18	11	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70μm

(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm x 74.2mm	35μm	74.2mm x 74.2mm	70μm

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Input Voltage	V_{IN}	7	-	28	V
Output Current	I_{OUT}	-	-	1.5	A
Operating Temperature	Topr	-40	-	+85	°C

Electrical Characteristics (Unless otherwise specified Ta = 25°C, V_{IN} = 12V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Operating Supply Current	I_{OPR}	-	270	500	µA	V_{OUT}= 5.62V
Output Voltage	V_{OUT}	4.9	5.0	5.1	V	
Switching Frequency	f_{OSC}	280	330	380	kHz	
Maximum Duty Ratio	Maxduty	88	93	98	%	
High-side MOSFET ON-Resistance	R_{ONH}	-	250	-	mΩ	I_{SW} = 100mA
Low-side MOSFET ON-Resistance	R_{ONL}	-	200	-	mΩ	I_{SW} = 100mA
Over Current Limit [Note 1]	I_{LIMIT}	2.1	2.5	2.9	A	
UVLO Detection Voltage	V_{UVLO}	6.1	6.4	6.7	V	V_{IN} falling
UVLO Hysteresis Voltage	$V_{UVLOHYS}$	100	200	300	mV	
Soft Start Time	t_{SS}	2	4	8	ms	

(Note 1) No tested on outgoing inspection.

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Typical Performance Curves
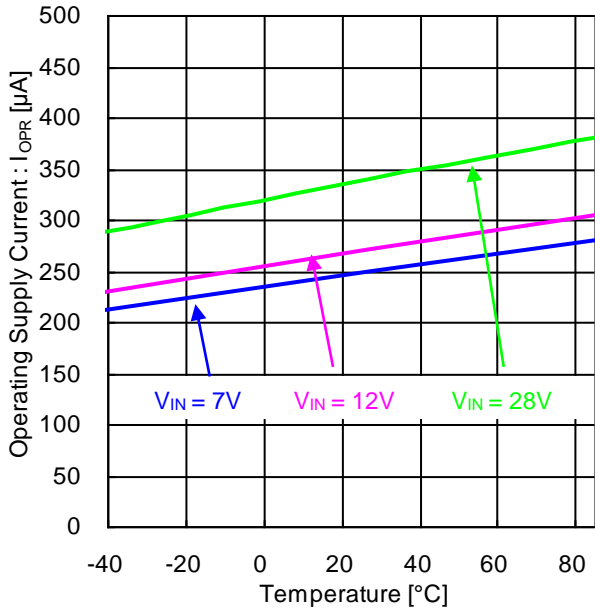
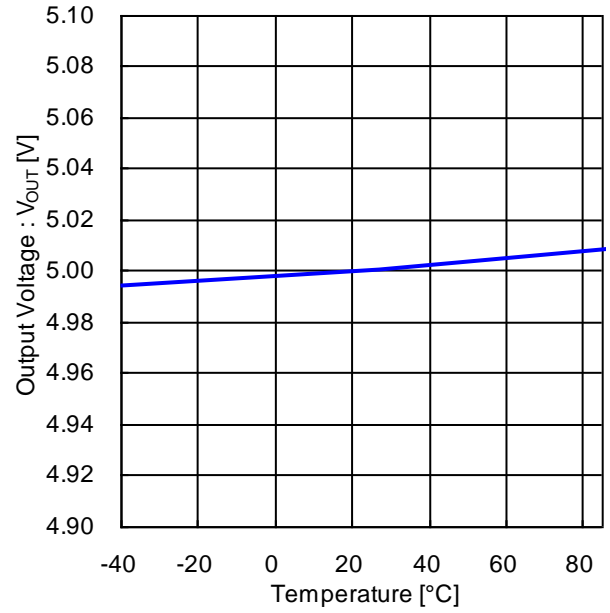Figure 2. Operating Supply Current vs Temperature
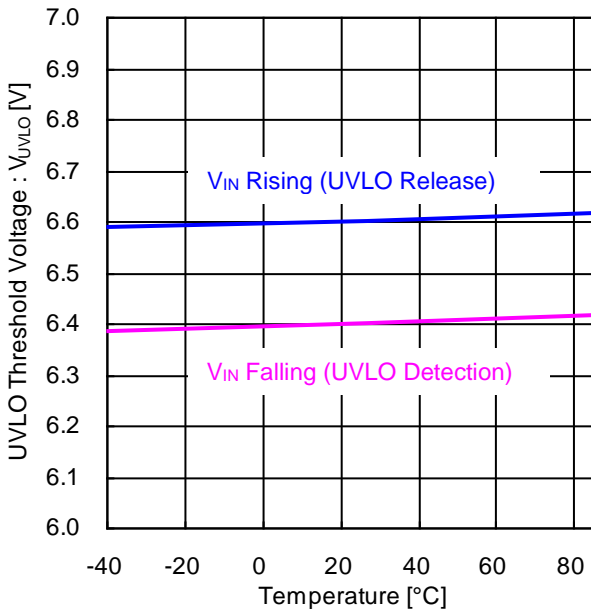

Figure 3. Output Voltage vs Temperature
(V_{IN} = 12V)
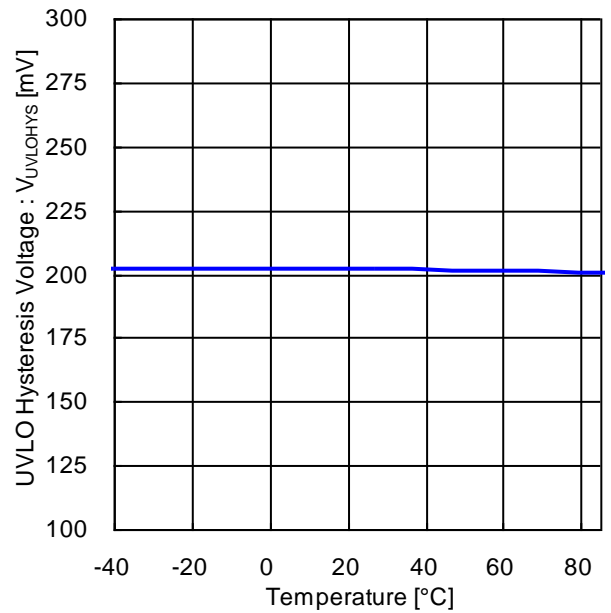

Figure 4. UVLO Threshold Voltage vs Temperature

Figure 5. UVLO Hysteresis Voltage vs Temperature

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Typical Performance Curves - continued
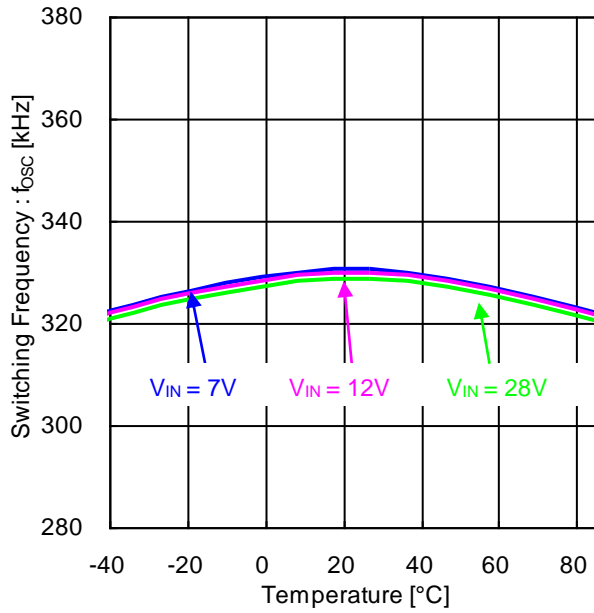
Figure 6. Switching Frequency vs Temperature
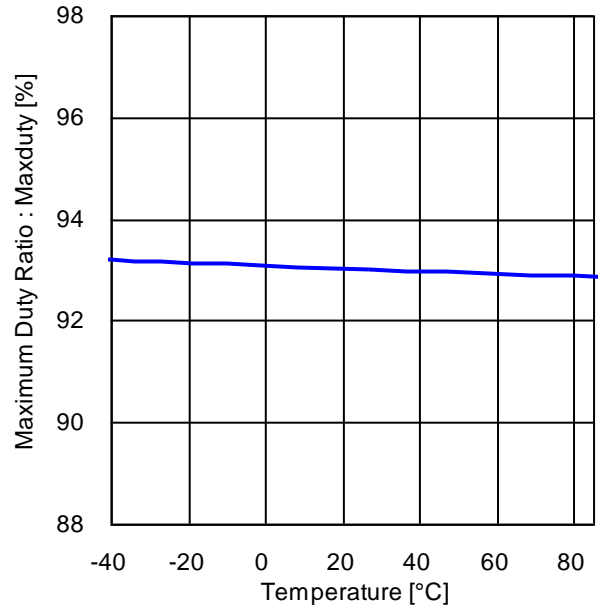
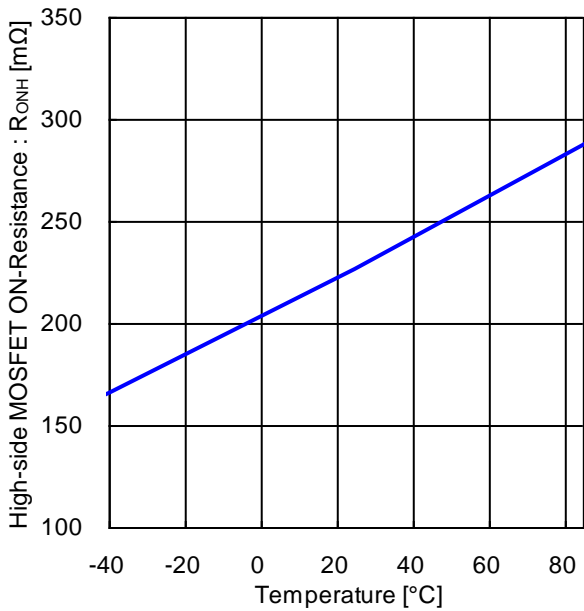Figure 7. Maximum Duty Ratio vs Temperature
(V_{IN} = 12V)

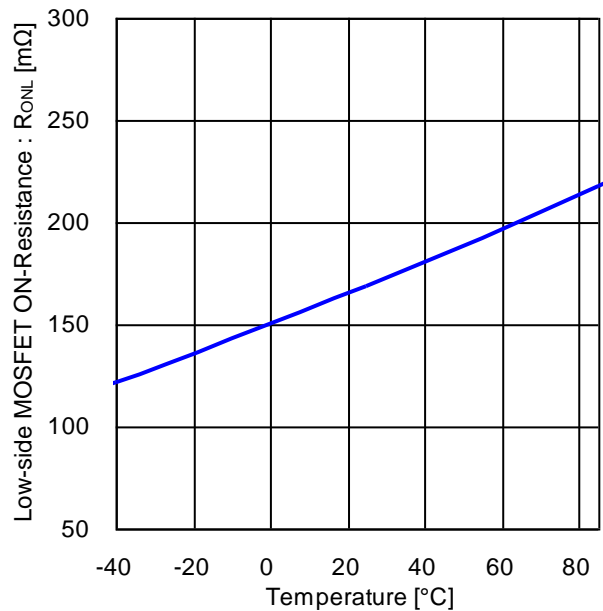Figure 8. High-side MOSFET ON-Resistance vs Temperature
(V_{IN} = 12V)

Figure 9. Low-side MOSFET ON-Resistance vs Temperature
(V_{IN} = 12V)

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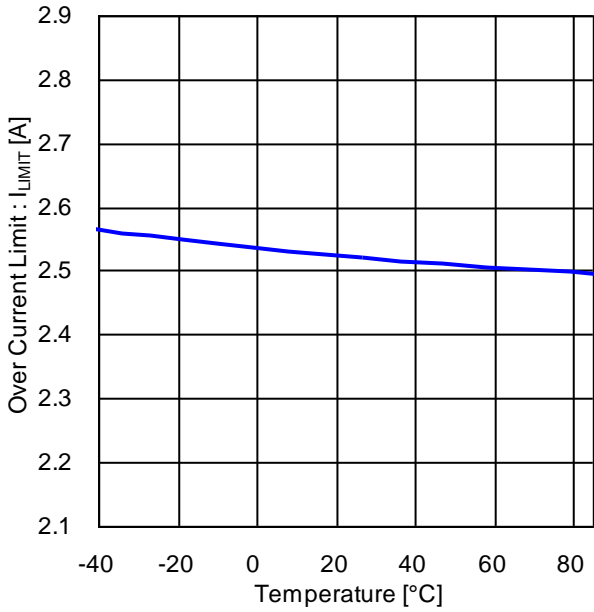## Typical Performance Curves   - continued

Figure 10. Over Current Limit vs Temperature
(V_{IN} = 12V)
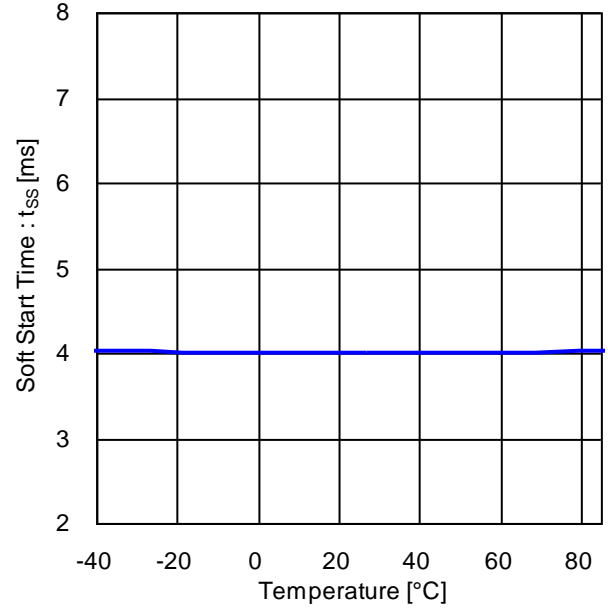

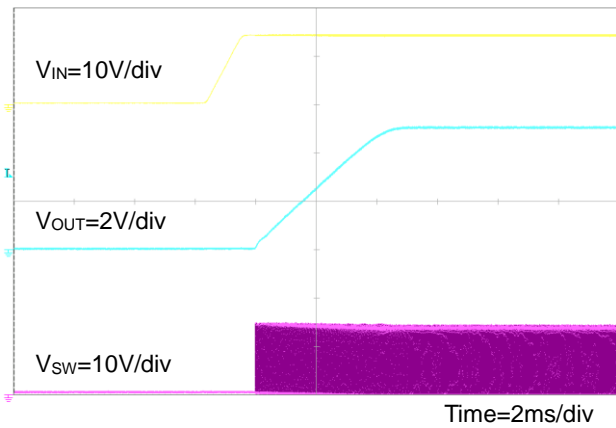
Figure 11. Soft Start Time vs Temperature
(V_{IN} = 12V)
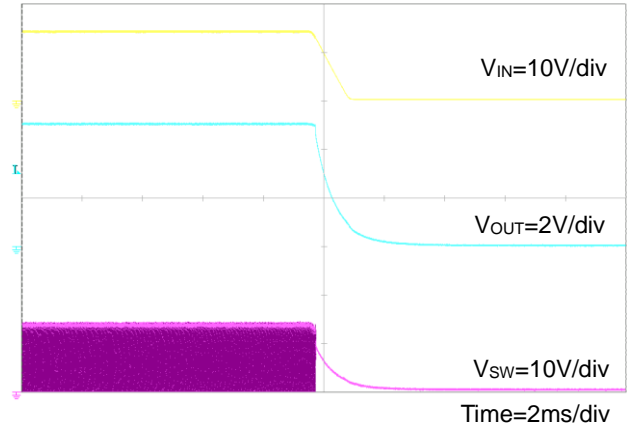

Figure 12. Start-up Waveform
(V_{IN} = 0V to 12V)

Figure 13. Shutdown Waveform
(V_{IN} = 12V to 0V)

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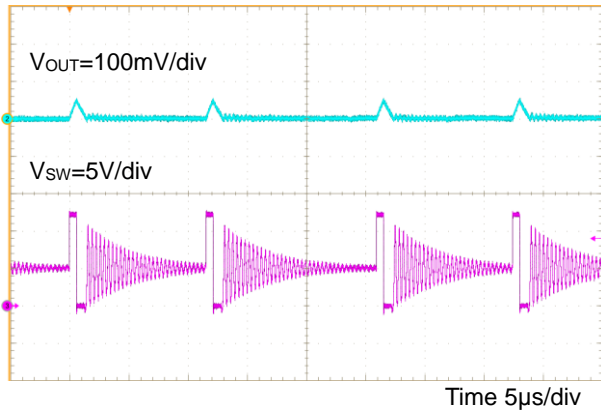## Typical Performance Curves   - continued

Figure 14. V$_{OUT}$ Ripple (V$_{IN}$ = 12V, I$_{OUT}$ = 10mA)
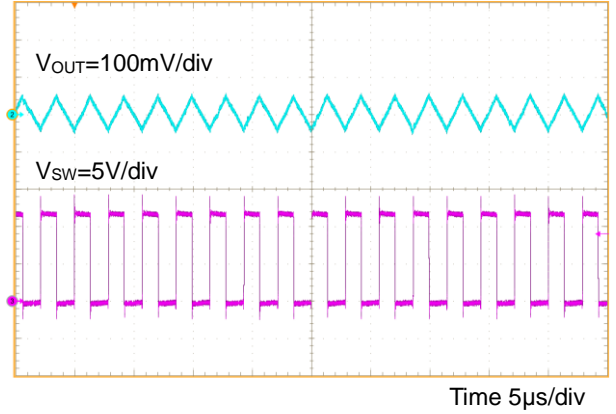

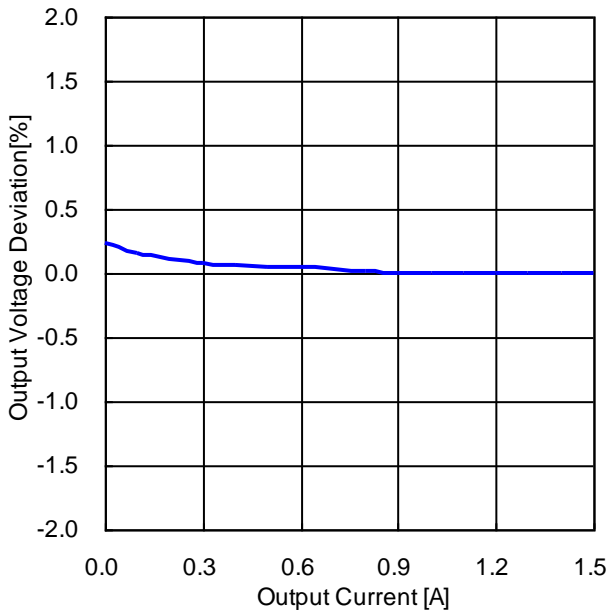Figure 15. V$_{OUT}$ Ripple (V$_{IN}$ = 12V, I$_{OUT}$ = 1.5A)

Figure 16. Load Regulation (V$_{IN}$ = 12V)
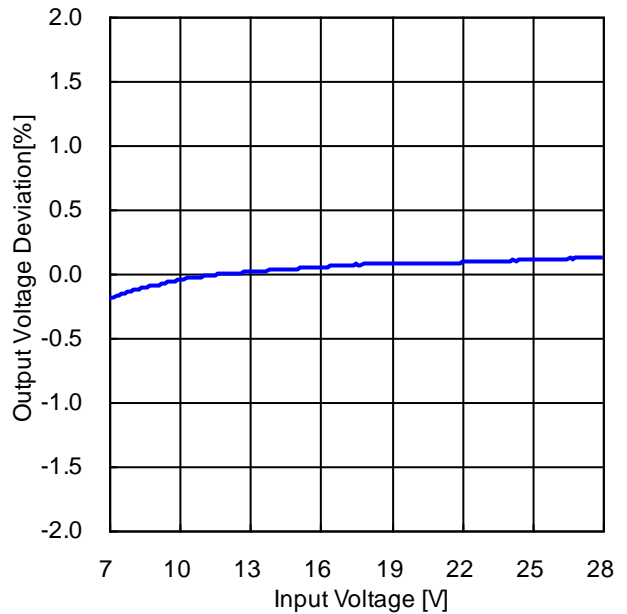

Figure 17. Line Regulation (I$_{OUT}$ = 1.5A)

Function Description

1. **DC/DC Converter Operation**

    BD9E103FJ is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM (Simple Light Load Mode) control for lighter load to improve efficiency.
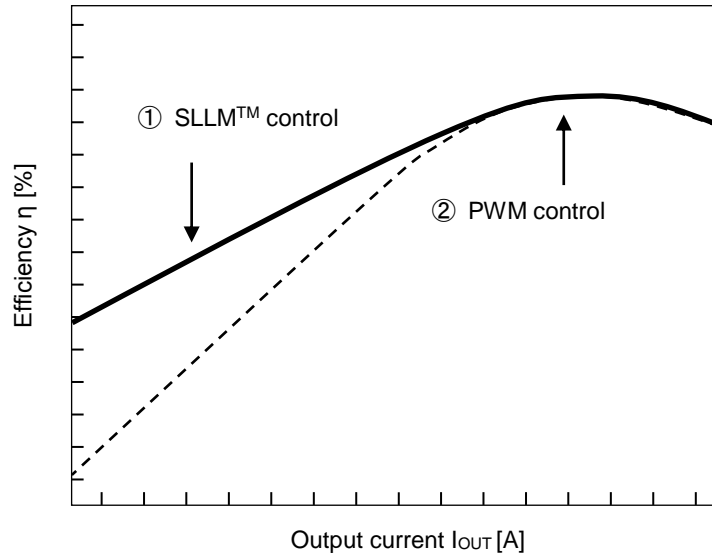

Figure 18. Efficiency (SLLM^TM control and PWM control)
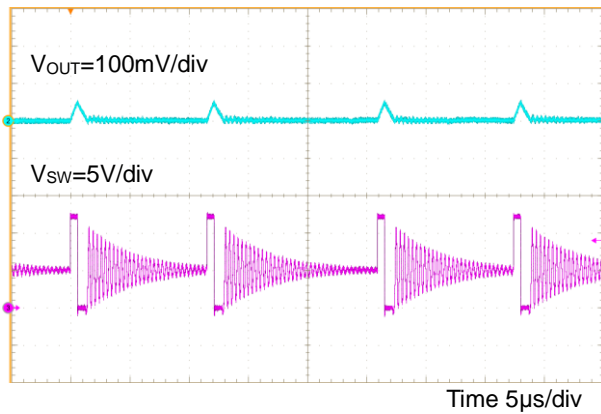
①SLLM^TM Control

Figure 19. SW Waveform at SLLM^TM Control
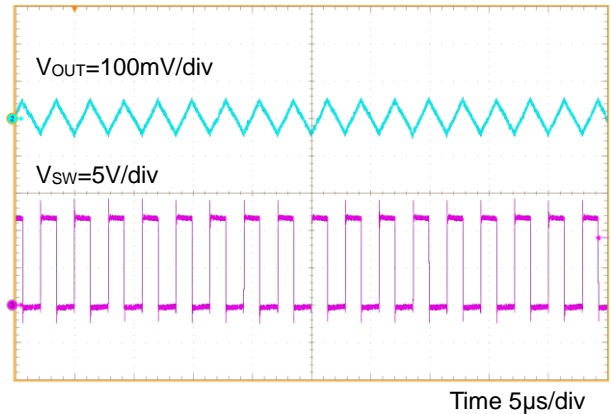(V_{IN} = 12V, I_{OUT} = 10mA)

②PWM Control

Figure 20. SW Waveform at PWM Control
(V_{IN} = 12V, I_{OUT} = 1.5A)

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Function Description – continued

2. Soft Start

When V_{IN} reaches 6.6V (Typ), Soft Start function operates and the output voltage V_{OUT} gradually rises. With the Soft Start function, output voltage overshoot and in-rush current can be prevented. The rising time of output voltage is 4ms (Typ).
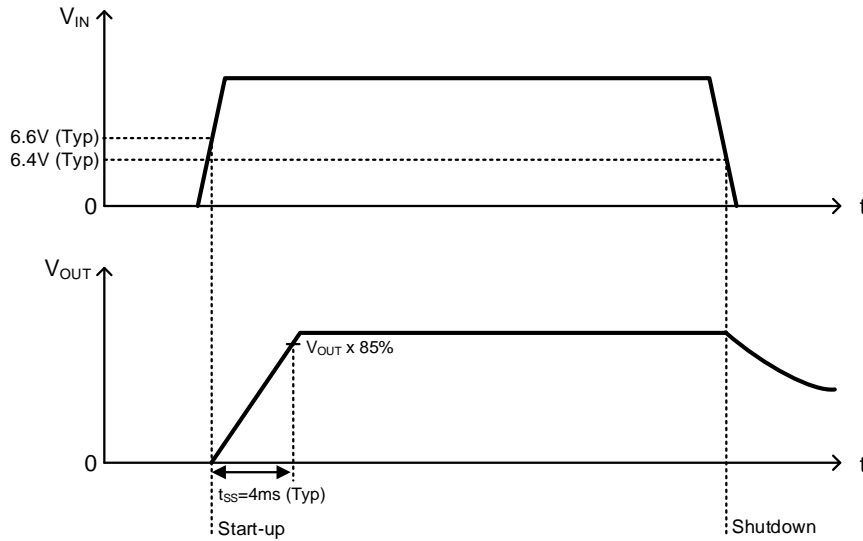
Figure 21. Soft Start Timing Chart

3. Protection

The protective circuits are intended for prevention of damage caused by unexpected accidents. Do not use them for continuous protective operation.

(1) Short Circuit Protection (SCP)

The short circuit protection block compares the output voltage of VOUT terminal with the internal reference voltage. When the VOUT terminal voltage has fallen below 3.5V (Typ) and remained there for 0.8ms (Typ), SCP function stops the IC operation for 25ms (Typ) and subsequently initiates a restart.

Table 1. Short Circuit Protection Function

VIN terminal	VOUT terminal	Short Circuit Protection	Short Circuit Protection Operation
6.6V or higher (UVLO Release)	< 3.5V (Typ)	Enabled	ON
	> 3.5V (Typ)		OFF
6.4V or lower (UVLO Detect)	-	Disabled	OFF
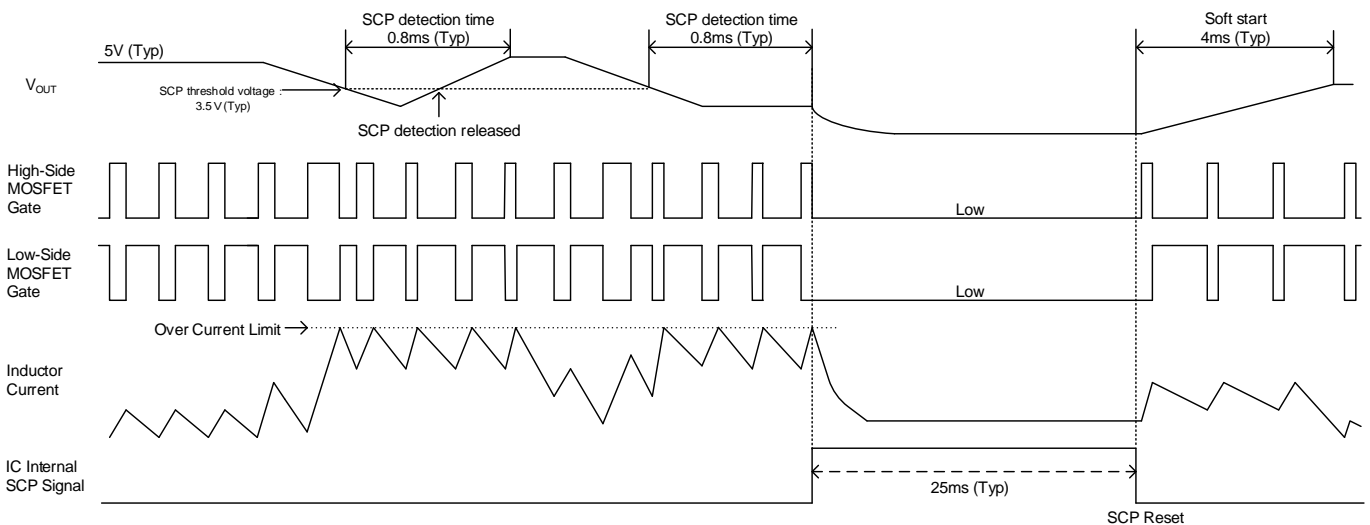
Figure 22. Short Circuit Protection (SCP) Timing Chart

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Function Description - continued

(2) Under Voltage Lockout Protection (UVLO)
The under voltage lockout protection circuit monitors the VIN terminal voltage.
The operation enters standby when the VIN terminal voltage is 6.4V (Typ) or lower.
The operation starts when the VIN terminal voltage is 6.6V (Typ) or higher.
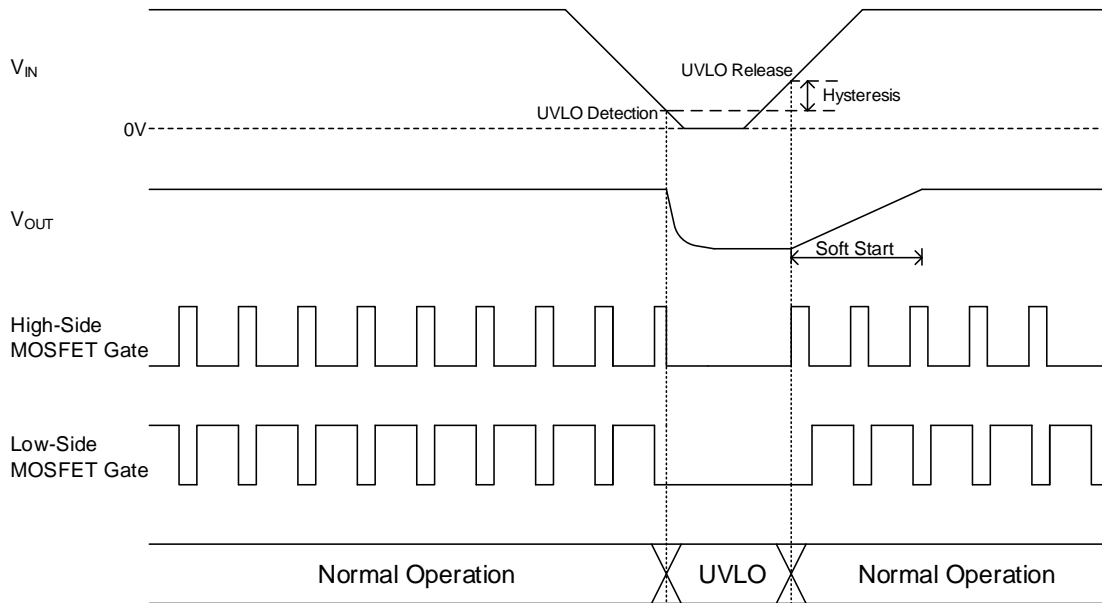

Figure 23. UVLO Timing Chart

(3) Thermal Shutdown (TSD)
When the chip temperature exceeds Tj=175°C (Typ), the DC/DC converter output is stopped. Thermal protection circuit resets and the output voltage returns to the normal operation level when the temperature falls. The circuit has a hysteresis of 25°C (Typ). The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding Tjmax=150°C. It is not meant to protect or guarantee the reliability of the application. Do not use this function of the circuit for application protection design.

(4) Over Current Protection (OCP)
The Over Current Protection function is realized by using the current mode control to limit the current that flows through the High-Side MOSFET at each cycle of the switching frequency. The designed over current limit value is 2.5A (Typ).

(5) Over Voltage Protection (OVP)
Over Voltage Protection function compares VOUT terminal voltage with internal reference voltage and when the VOUT terminal voltage exceeds 6.5V (Typ), the OVP function turns off the output MOSFETs. When the output voltage drops, the device returns to normal operation with hysteresis.

Application Example

Parameter	Symbol	Value
Input Voltage	V_{IN}	12V
Output Voltage	V_{OUT}	5V
Switching Frequency	f_{OSC}	330kHz (Typ)
Maximum Output Current	I_{OUTMAX}	1.5A
Operating Temperature Range	Topr	-40°C to +85°C
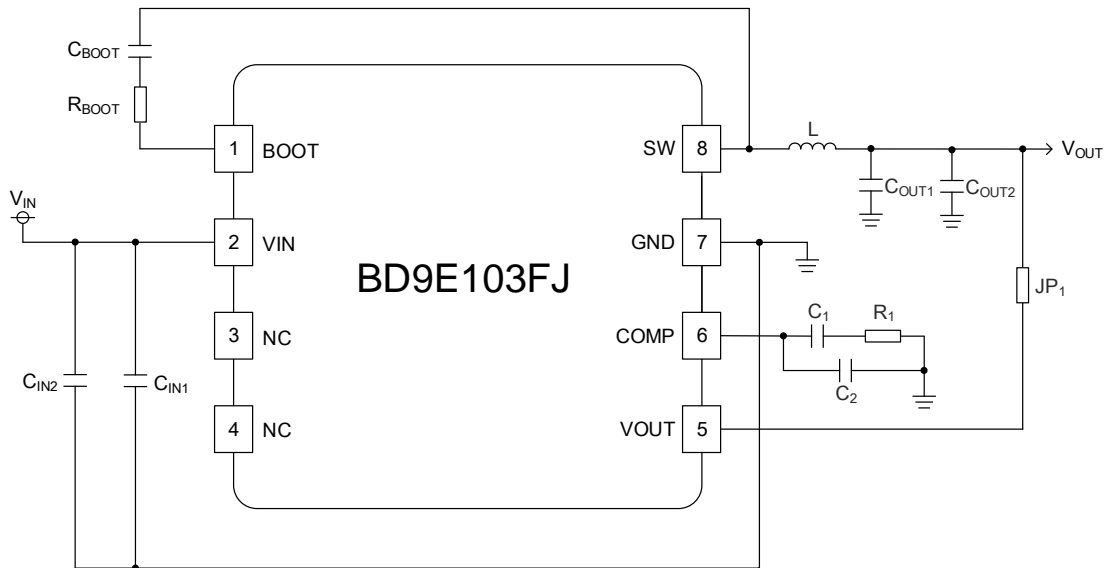
Figure 24. Application Circuit

Table 2. Recommended Component Values

Part No.	Value
C_{IN1} (Note 1)	0.1µF
C_{IN2} (Note 2)	470µF
C_{BOOT} (Note 3)	0.1µF
R_{BOOT} (Note 4)	Short
L	22µH
C_{OUT1} (Note 5)	0.1µF
C_{OUT2} (Note 5)	220µF
R_1	30kΩ
C_1	2200pF
C_2	100pF
JP_1 (Note 6)	Short

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1µF ceramic capacitor as close as possible to the VIN terminal and the GND terminal.

(Note 2) For the capacitance of input capacitor, take temperature characteristics, DC bias characteristics, etc. into consideration and set to a minimum value of no less than 10µF.

(Note 3) For the capacitance of bootstrap capacitor, take temperature characteristics, DC bias characteristics, etc. into consideration to set minimum value to no less than 0.047µF.

(Note 4) Avoid short-circuiting between VIN terminal and VOUT terminal or SW terminal. Short-circuiting between these terminals may result in damage to the IC or smoke generation. In a case that has been applied V_{IN} = 20V or more, when there is a possibility the BOOT terminal and SW terminal is short-circuited, please insert a R_{BOOT} resistor of 10Ω between the bootstrap capacitor 0.1µF and BOOT terminal. Short-circuiting without inserting this resistance may result in damage to the IC or smoke generation.

(Note 5) In case capacitance value fluctuates due to temperature characteristics, DC bias characteristics, etc. of output capacitor, Loop Response may oscillate. Please confirm on actual equipment. When selecting a capacitor, confirm the characteristics of the capacitor in its datasheet.

(Note 6) JP_1 is an option, used for feedback's frequency response measurement. By inserting a resistor at JP_1, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor will not be used in actual application, please use this resistor pattern in short-circuit mode.
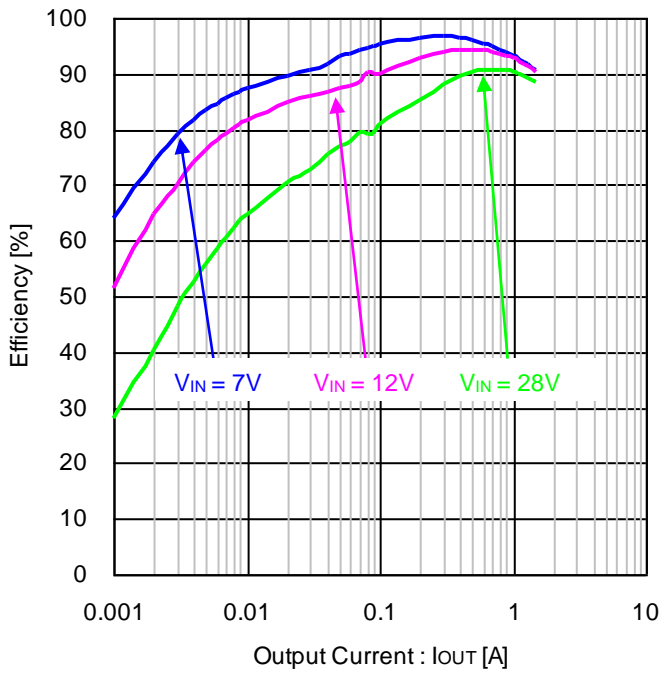
Figure 25. Efficiency vs Output Current

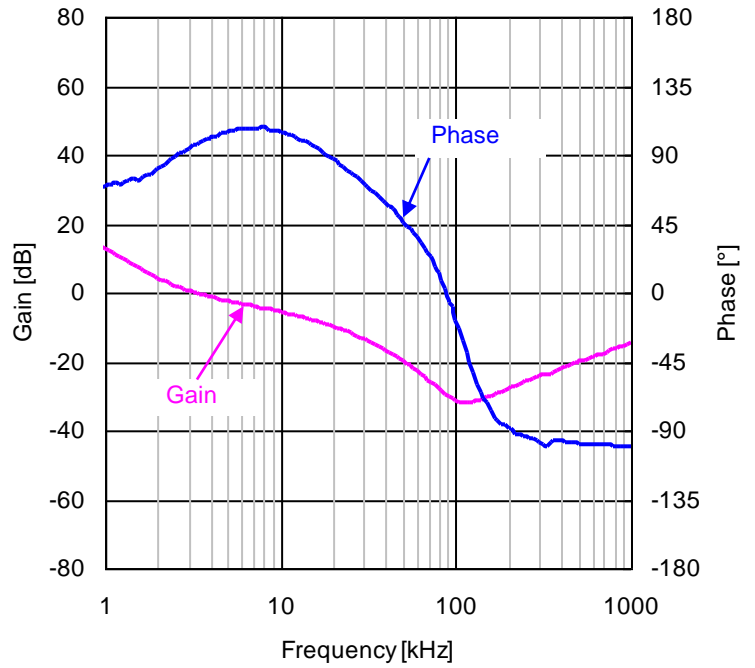Figure 26. Closed Loop Response I_{OUT} = 1.5A
(V_{IN} = 12V, L = 22μH, C_{OUT} = Ceramic0.1μF and Electrolytic220μF)
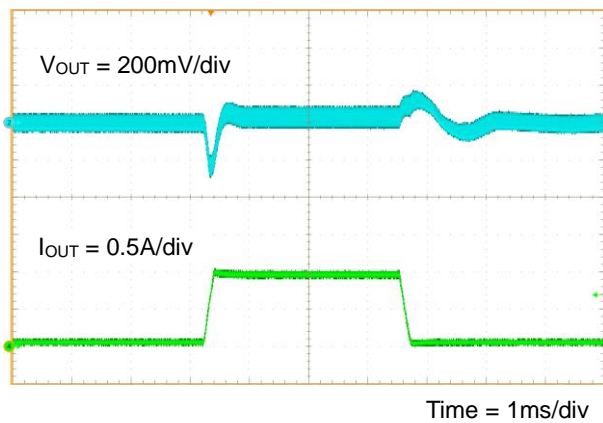

Figure 27. Load Transient Response
I_{OUT} = 0.1A – 1.0A
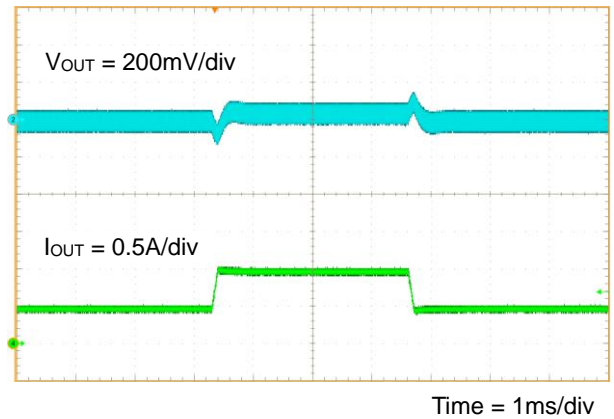(V_{IN} = 12V, L = 22μH, C_{OUT} = Ceramic0.1μF and Electrolytic220μF)

Figure 28. Load Transient Response
I_{OUT} = 0.5A – 1.0A
(V_{IN} = 12V, L = 22μH, C_{OUT} = Ceramic0.1μF and Electrolytic220μF)

Selection of Components Externally Connected

About the application except the recommendation, please contact us.

1. Output LC Filter
The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. I_L ripple current flowing through the inductor is returned to the device for SLLM™ control. It is recommended to use 22µH inductor since the feedback current has the best behavior in the specified inductance value.
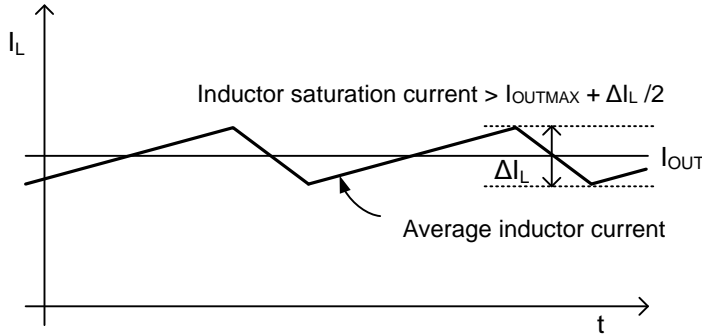

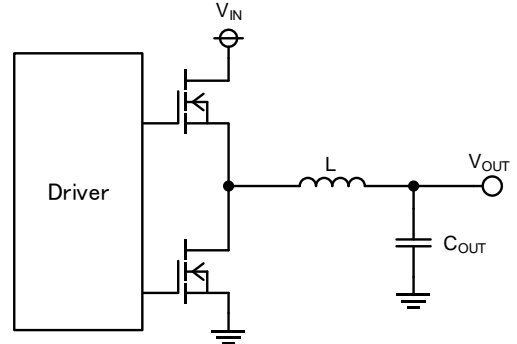Figure 29. Waveform of Current through Inductor

Figure 30. Output LC Filter Circuit

Calculation with V_{IN} = 12V, V_{OUT} = 5V, L = 22µH, and switching frequency f_{OSC} = 330kHz is expressed as below.

Inductor ripple current ΔI_L,

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{OSC} \times L} = 402\,[\text{mA}]$$

The saturation current of the inductor must be larger than the sum of the maximum output current and one-half (1/2) of the inductor ripple current ΔI_L.

The output capacitor C_{OUT} affects the output ripple voltage characteristics. The output capacitor C_{OUT} must satisfy the required ripple voltage characteristics.

The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{OSC}})$$

R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.
With C_{OUT} = 220µF, R_{ESR} = 100mΩ the output ripple voltage is calculated as below.

$$\Delta V_{RPL} = 0.402 \times (100m + \frac{1}{8 \times 220\mu \times 330k}) = 41\,[\text{mV}]$$

Be careful of the total capacitance value when additional capacitor C_{LOAD} is connected to the output capacitor C_{OUT}. Use maximum additional capacitor C_{LOAD} (Max) condition which satisfies the following method.

Maximum starting inductor ripple current I_{LSTART} <   Over Current Limit 2.1A (Min)

Maximum starting inductor ripple current I_{LSTART} can be expressed in the following method.

I_{LSTART} =   Maximum starting output current (I_{OUTMAX}) +   Charge current to output capacitor(I_{CAP}) + $\dfrac{\Delta I_L}{2}$

Charge current to output capacitor I_{CAP} can be expressed in the following method

$$I_{CAP} = \frac{(C_{OUT} + C_{LOAD}) \times V_{OUT}}{t_{SS}}$$

Calculation with V_{IN} = 12V, V_{OUT} = 5V, L = 22µH, I_{OUTMAX} = 1.5A, switching frequency f_{OSC} = 330kHz (Typ), Output capacitor C_{OUT} = 220µF, Soft Start time t_{SS} = 4ms (Typ), the method is as below.

$$C_{LOAD}(Max) \leq \frac{(2.1 - I_{OUTMAX} - \frac{\Delta I_L}{2}) \times t_{SS}}{V_{OUT}} - C_{OUT} = 99.2 \, [\mu F]$$

* C_{LOAD} has an effect on the stability of the DC/DC converter. To ensure the stability of the DC/DC converter, make sure that a sufficient phase margin is provided.

2. Phase Compensation

A current mode control buck DC/DC converter is a two-pole, one-zero system two poles formed by an error amplifier and load and one zero point added by phase compensation. The phase compensation resistor R_{CMP} determines the crossover frequency f_{CRS} where the total loop gain of the DC/DC converter is 0 dB. High value for this crossover frequency f_{CRS} provides a good load transient response characteristic but inferior stability. Conversely, specifying a low value for the crossover frequency f_{CRS} greatly stabilizes the characteristics but the load transient response characteristic is impaired.

(1) Selection of Phase Compensation Resistor R_{CMP} (R_1)

The phase compensation resistance R_{CMP} can be determined by using the following equation.

$$R_{CMP} = \frac{2\pi \times V_{OUT} \times f_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}}$$

Where:

V_{OUT} is the output voltage (5V (Typ))
f_{CRS} is the crossover frequency [Hz]
C_{OUT} is the output capacitance [F]
V_{FB} is the feedback reference voltage (0.8V (Typ))
G_{MP} is the current sense gain (7 A/V (Typ))
G_{MA} is the error amplifier transconductance (82 µA/V (Typ))

(2) Selection of Phase Compensation Capacitance C_{CMP} (C_1)

For stable operation of the DC/DC converter, inserting a zero point at 1/6 of the zero crossover frequency cancels the phase delay due to the pole formed by the load often provides favorable characteristics.

The phase compensation capacitance C_{CMP} can be determined by using the following equation.

$$C_{CMP} = \frac{1}{2\pi \times R_{CMP} \times f_Z}$$

Where:

f_Z is Zero point inserted

(3) Loop Stability

In order to ensure stability of DC/DC converter, confirm there is enough phase margin on actual equipment. Under the worst condition, it is recommended to ensure phase margin is 45° or more. In fact, the characteristics may variable due to PCB layout, routing of wiring, types of used components and operating environments (temperature etc.). Use gain-phase analyzer or FRA to confirm frequency characteristics on actual equipment. Contact the manufacturer of each equipment to check its measuring method, etc.

PCB Layout Design

PCB layout design for DC/DC converter power supply IC is as important as the circuit design. Appropriate layout can avoid various problems caused by power supply circuit. Figure 31-a to 31-c show the current path in a buck converter circuit. The Loop1 in Figure 31-a is a current path when H-side switch is ON and L-side switch is OFF, the Loop2 in Figure 31-b is when H-side switch is OFF and L-side switch is ON. The thick line in Figure 31-c shows the difference between Loop1 and Loop2. The current in thick line changes sharply each time the switching element H-side and L-side switch change from OFF to ON, and vice versa. These sharp changes induce several harmonics in the waveform. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more detail, refer to application note of switching regulator series "PCB Layout Techniques of Buck Converter".
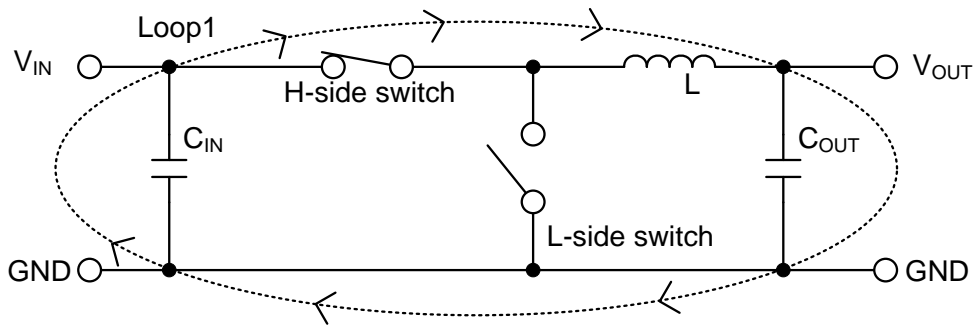
Figure 31-a. Current path when H-side switch = ON, L-side switch = OFF
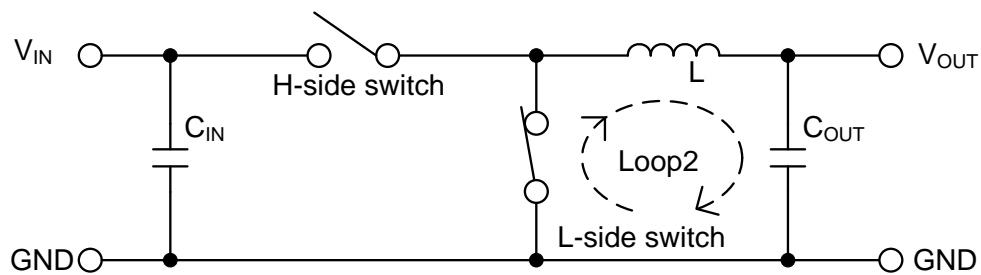
Figure 31-b. Current path when H-side switch = OFF, L-side switch = ON
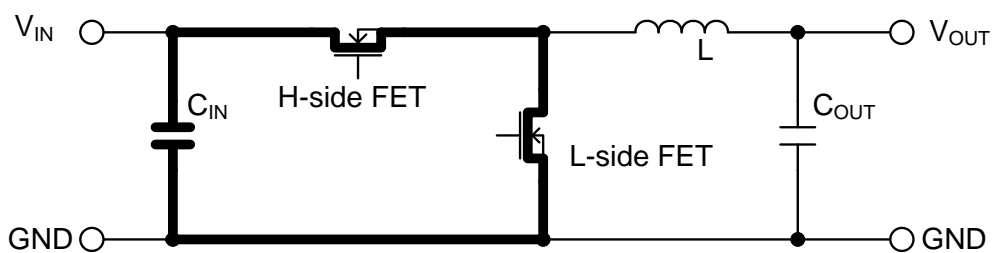
Figure 31-c. Difference of current and critical area in layout

PCB Layout Design - continued

When designing the PCB layout, please pay extra attention to the following points:

- Place input capacitor on the same PCB surface as the IC and as close as possible to the IC's VIN terminal.
- Switching nodes should be traced as thick and short as possible to the inductor, because they may induce the noise to the other nodes due to AC coupling.
- Please keep the lines connected to VOUT sense away from the SW node as far as possible.
- Please place output capacitor away from input capacitor to avoid harmonics noise from the input.

I/O Equivalence Circuits
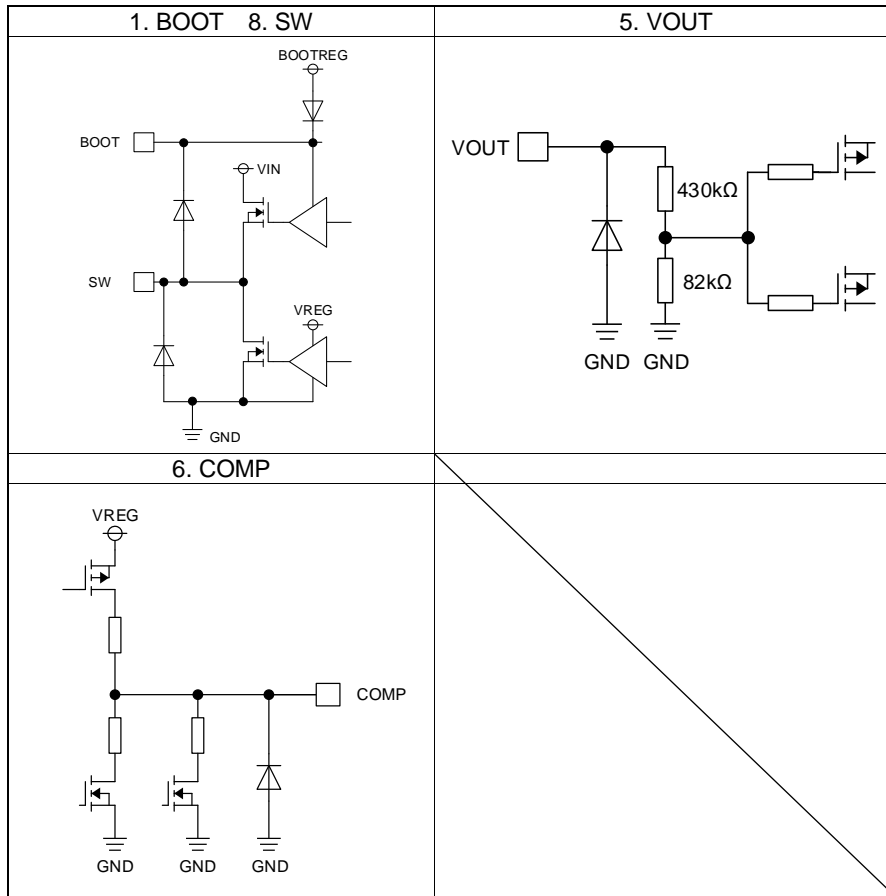
Figure 32. I/O Equivalence Circuits

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. **Regarding the Input Pin of the IC**
    This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

    When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
    When GND > Pin B, the P-N junction operates as a parasitic transistor.

    Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.
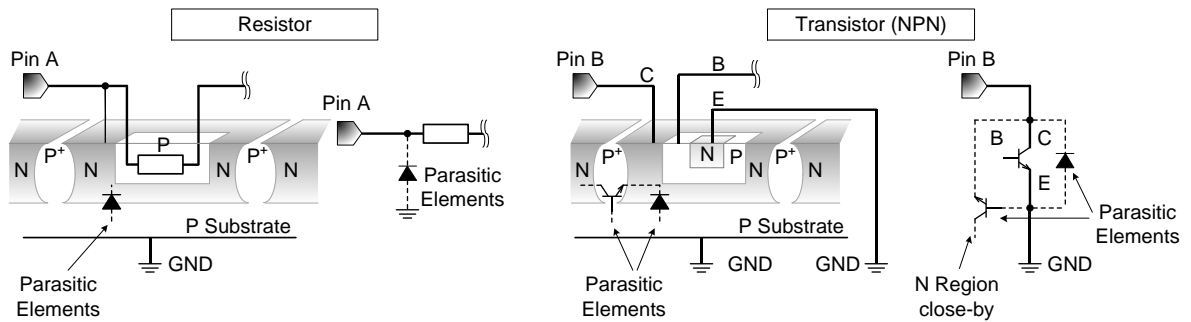
Figure 33. Example of monolithic IC structure

12. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. **Area of Safe Operation (ASO)**
    Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

14. **Thermal Shutdown Circuit(TSD)**
    This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
    Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. **Over Current Protection Circuit (OCP)**
    This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

16. **Disturbance Light**
    In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information

| B | D | 9 | E | 1 | 0 | 3 | F | J | - | E 2 |

Part Number

Package
FJ: SOP-J8

Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram

SOP-J8 (TOP VIEW)

9 E 1 0 3 ← Part Number Marking

← LOT Number

← Pin 1 Mark
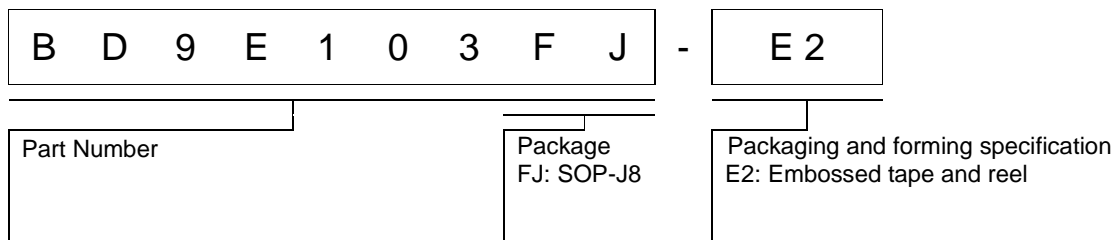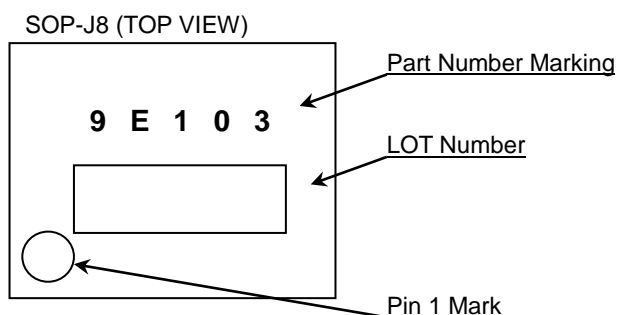
Physical Dimension and Packing Information

Package Name	SOP-J8

4. 9±0. 2

Max5. 25 (include. BURR)

8　7　6　5

6. 0±0. 3

3. 9±0. 2

1　2　3　4

0. 545

4°　+6°/−4°

0. 45MIN

0. 2±0. 1

S

1. 375±0. 1

0. 175

1. 27

0. 42±0. 1

0. 1　S

(UNIT : mm)
PKG : SOP−J8
Drawing No. EX111−5002

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

E2	TR
TL	E1

Reel

Pocket Quadrants

Direction of feed

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TSZ22111 • 15 • 001

23/24

TSZ02201-0F3F0AJ00140-1-2
25.Sep.2017 Rev.001

Revision History

Date	Revision	Changes
25. Sep. 2017	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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    - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
    - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
    - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
    - [f] Sealing or coating our Products with resin or other coating materials
    - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
    - [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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