ROHM Switching Regulator Solutions

Evaluation Board: High Voltage 3A Buck Converter With Integrated FET

BD9G341AEFJ-EVK-101 (5V/3A Output)

AEY60-D1-0002

- **Introduction**

  This application note will provide the steps necessary to operate and evaluate ROHM's non-synchronous buck DC/DC converter using the BD9G341AEFJ evaluation boards. Component selection, board layout recommendations, operation procedures and application data is provided.

- **Description**

  This evaluation board has been developed for ROHM's non-synchronous buck DC/DC converter customers evaluating BD9G341AEFJ. While the BD9G341AEFJ accepts a power supply input range of 12V to 76V, and generates output voltages from 1V to Vcc, this evaluation board is setup for the same input voltage range and a fixed output of 5V can be produced. The IC has internal 150mΩ N-channel MOSFET and the operating frequency is programmable from 50kHz to 750kHz. A fixed Soft Start circuit prevents inrush current during startup along with UVLO (under voltage lock out) and TSD (thermal shutdown detection), OCP (over current protection), OVP (over voltage protection) protection circuits. The under voltage lock out and hysteresis can be set by external resistor using EN pin. EN pin allows for simple ON/OFF control of the IC to reduce standby current consumption.

- **Applications**

  Industrial distributed power applications.
  Battery powered equipment.

- **Evaluation Board Operating Limits**

Parameter		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
Supply Voltage							
	BD9G341AEFJ	VCC	12	-	76	V	
Output Voltage / Current							
	BD9G341AEFJ	VOUT	-	5	-	V	
		IOUT	-	-	3	A	

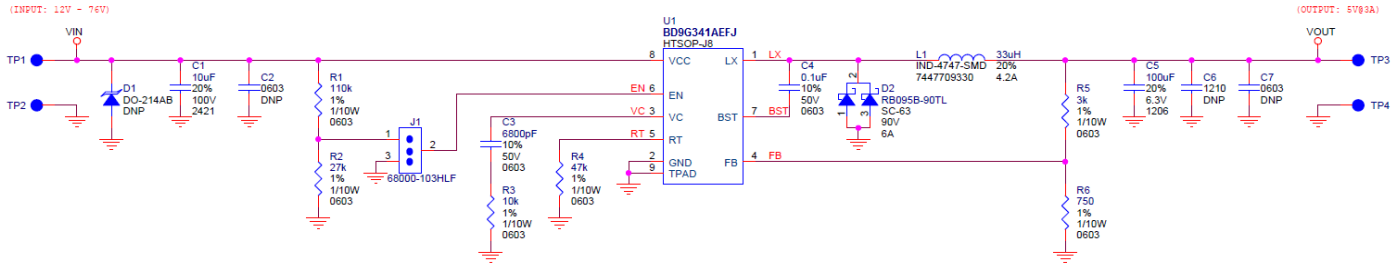
- **Evaluation Board**

  Below is evaluation board with the BD9G341AEFJ.

Figure 1. BD9G341AEFJ Evaluation Board

- **Evaluation Board Schematic**

Below is evaluation board schematic for BD9G341AEFJ.



BD9G341AEFJ EVM Jumper Positions

Reference Designator	Position	Description
J1	Open	Configure U1 fully operational
	2 - 1	
	2 - 3	Configure U1 in low power state

VOUT = (R5+R6)/R6

Figure 2. BD9G341AEFJ Evaluation Board Schematic

- **Evaluation Board Operation Procedures**

Below is the procedure to operate the evaluation board.

1. Connect power supply's GND pin to GND test point TP2 on the evaluation board.
2. Connect power supply's V_{CC} pin to VIN test point TP1 on the evaluation board. This will provide VCC to the IC U1. Please note that the VCC should be in range of 12V to 76V.
3. Check if shunt jumper of J1 is at position ON (Pin2 connect to Pin1, EN pin of IC U1 is pulled high).
4. Connect electronic load to TP3 and TP4. Do not turn on load (electronic load is off power).
5. Turn on power supply. The output voltage V_{OUT}(+5V) can be measured at the test point TP3. Now turn on the load. The load can be increased up to 3A MAX.

Notes:
The board does not support hot plugging protection. Do not perform hot plugging on this board.

- **Evaluation Board BOM**

  Below is a table with the build of materials. Part numbers and supplier references are provided.

Table 1. Bill of Materials

Item	Qty.	Ref	Description	Manufacturer	Part Number
1	1	C1	CAP CER 10µF 100V 20% X7R SMD	Murata	KRM55TR72A106MH01K
2	1	C3	CAP CER 6800PF 50V 10% X7R 0603	Murata	GRM188R71H682KA01D
3	1	C4	CAP CER 0.1µF 50V 10% X7R 0603	Murata	GRM188R71H104KA93D
4	1	C5	CAP CER 100µF 6.3V 20% X5R 1206	Murata	GRM31CR60J107ME39L
5	1	D2	DIODE SCHOTTKY 90V 3A CPD	Rohm	RB095B-90TL
6	1	J1	CONN HEADER VERT .100 3POS 15AU	FCI	68000-103HLF
7	1	L1	INDUCTOR POWER 33µH 4.2A SMD	Wurth Electronics Inc	7447709330
8	1	R1	RES 110K OHM 1/10W 1% 0603 SMD	Rohm	MCR03EZPFX1103
9	1	R2	RES 27K OHM 1/10W 1% 0603 SMD	Rohm	MCR03EZPFX2702
10	1	R3	RES 10K OHM 1/10W 1% 0603 SMD	Rohm	MCR03EZPFX1002
11	1	R4	RES 47K OHM 1/10W 1% 0603 SMD	Rohm	MCR03EZPFX4702
12	1	R5	RES 3K OHM 1/10W 1% 0603 SMD	Rohm	MCR03EZPFX3001
13	1	R6	RES 750 OHM 1/10W 1% 0603 SMD	Rohm	MCR03EZPFX7500
14	2	TP1,TP3	TEST POINT PC MULTI PURPOSE RED	Keystone Electronics	5010
15	2	TP2,TP4	TEST POINT PC MULTI PURPOSE BLK	Keystone Electronics	5011
16	1	U1	IC REG BUCK SYNC ADJ 3A HTSOP-J8	Rohm	BD9G341AEFJ-E2

- **Reference Application Data for BD9G341AEFJ-EVK-101**

  Following graphs show quiescent current, efficiency, load response, output voltage ripple response of the BD9G341AEFJ evaluation board.

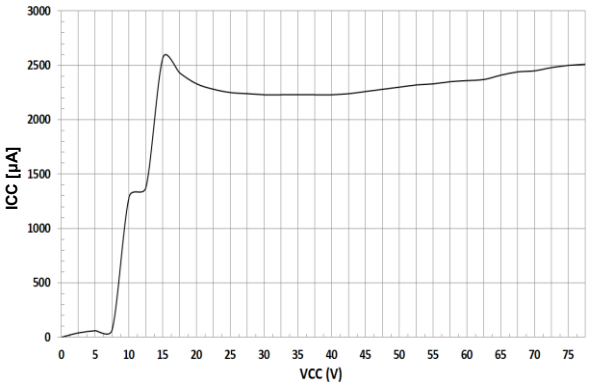


Figure 3. Circuit Current vs Power Supply Voltage Characteristics(Ta=25℃)

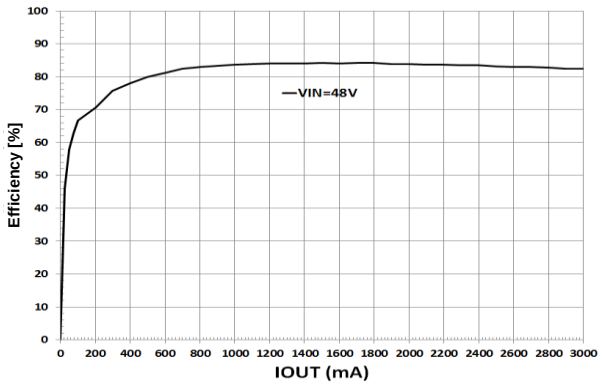


Figure 4. Efficiency vs Load Current (VIN=48V, VOUT=5V)

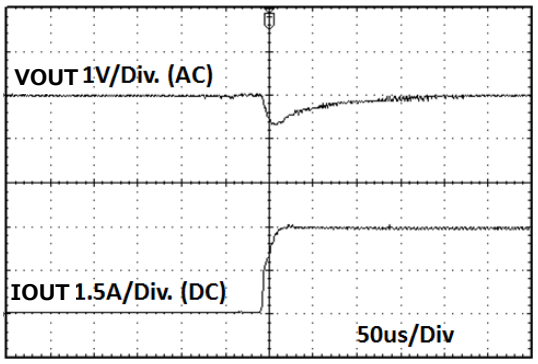


Figure 5. Load Response Characteristics (VIN=48V, VOUT=5V, I_{OUT}=0A→3A)

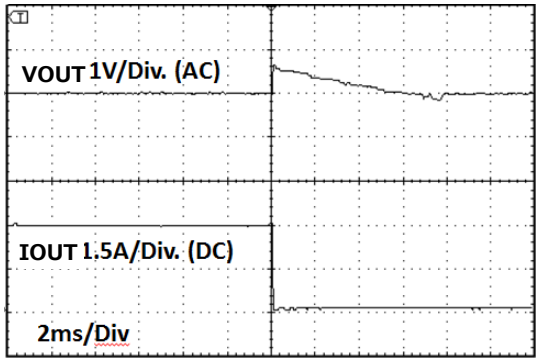


Figure 6. Load Resopnse Characteristics (VIN=48V, VOUT=5V, IOUT=3A→0A)

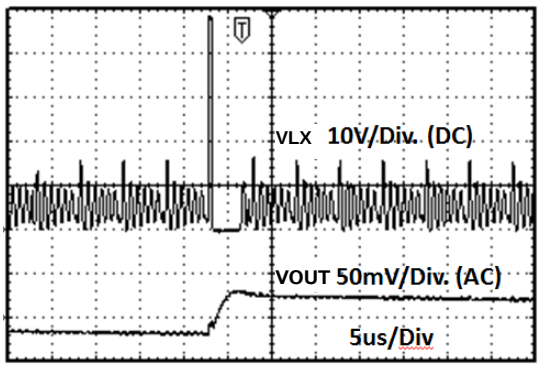


Figure 7. Output Ripple Voltage Characteristics (VIN=48V, VOUT=5V, IOUT=0A)

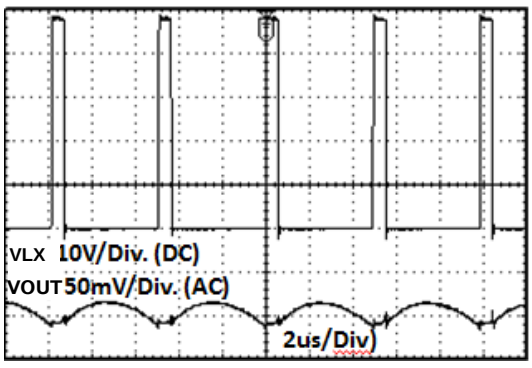
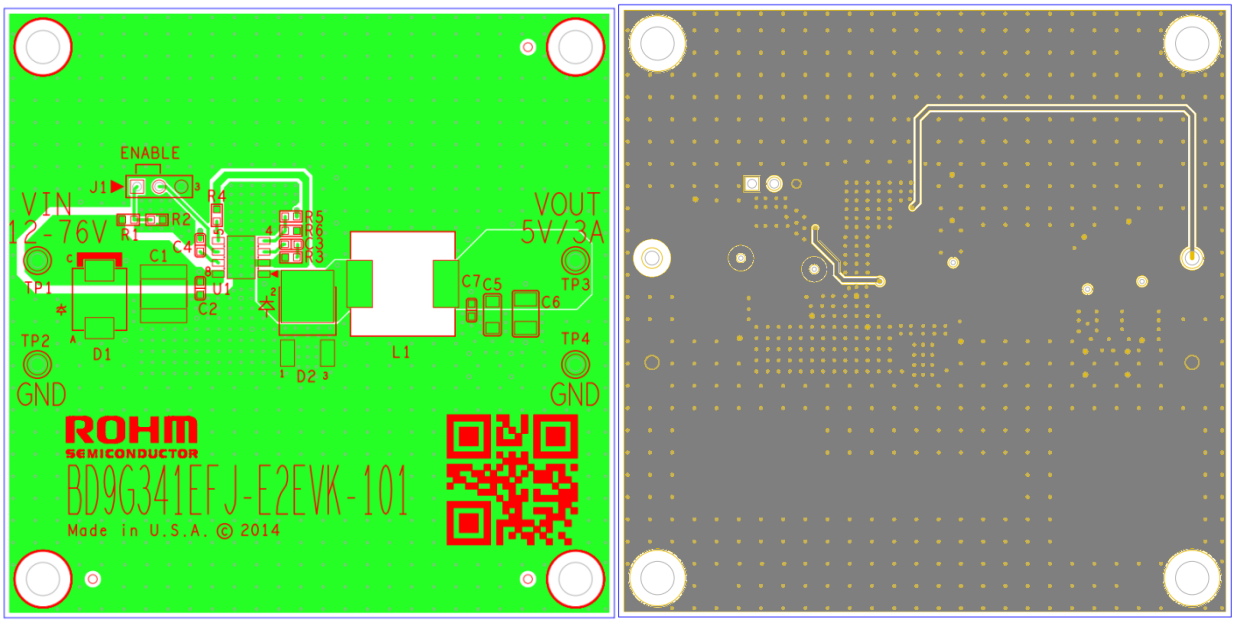


Figure 8. Output Ripple Voltage Characteristics (VIN=48V, VOUT=5V, IOUT=0A)

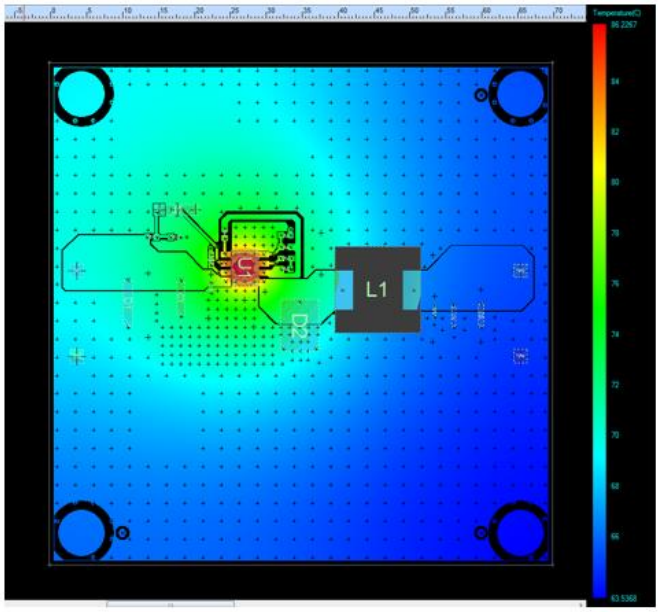
- **Evaluation Board Layout Guidelines**

  Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing current or voltage that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supply's performance. To help eliminate these problems, the VCC pin should be bypassed to ground with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VCC pin, and the anode of the catch diode.
  The GND pin should be tied directly to the thermal pad under the IC and the thermal pad.
  In order to reduce the influence of the parasitic impedance and inductance, the path of high current should be thick and short.
  Input decoupling capacitor should be located as close to the VCC pins.
  In order to minimize the parasitic capacitor and impedance of pattern, the catch diode and inductor should be located as close to the LX pin.
  The thermal pad should be connected to any internal PCB ground planes using multiple VIAs directly under the IC.
  Take care not to give the GND of feedback resistor, phase compensation elements and RT resistor the common impedance with high current path.
  Place the phase compensation capacitor between VC and GND pins as possbile as close to the IC.



Top Layer Bottom Layer

Figure 9. BD9G341AEFJ-EVK-101 Board PCB layout



U1: BD9G341AEFJ
- **Max. power dissipation: 3.825W @VIN=76V**
- **Component temperature = 86.2 ^{0}C**

L1: 7447709330
- **Max. power dissipation: 0.405W**
- **Component temperature = 70.4 ^{0}C**

Figure 10. BD9G341AEFJ-EVK-101 Thermal Characteristics
(Ta=25℃, No air flow, VIN=76V, VOUT=5V, IOUT=3A)

Thermal note: If the board is operated above room temperature (T>25ºC), an active cooling source (fan) or heat sink (soldered to bottom of PCB) need to be added.

Additional layout notes:

- The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plane as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective.
- The input capacitors should be connected to GND as close as possible to the VCC pin.
- The inductor and the output capacitors should be placed close to LX pin as much as possible.
- For applications operating at or near maximum voltage conditions (76V max), additional precautions regarding heat dissipation need to be considered during board layout. The provided evaluation board is a 4-layer board meant for evaluation purposes only. At maximum conditions, the IC's internal thermal shutdown detection circuit will be potentially initiated and the output disabled until the junction temperature falls. For final designs operating near these conditions, we recommend using one of the below PCB options for better heat dissipation of the IC.

  1) Use of a 4-layer PCB with internal GND planes connected to the IC GND pins.
  2) Use of a 2-layer PCB with a heat sink attached to the IC package.
  3) Use of a 2-layer PCB with a copper plane (>1oz) attached to the IC.

- **Calculation of Application Circuit Components**

1. Inductors

Something of the shield type that fulfills the current rating (Current value I_{peak} below), with low DCR is recommended.
Value of Inductance influences inductor ripple current and becomes the cause of output ripple.
In the same way as the formula below, this ripple current can be made small for as big as the L value of coil or as high as the switching frequency.

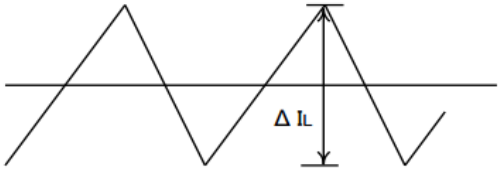


Figure 11. Inductor Current

$$\mathbf{I_{peak}} = \mathbf{IOUT} + \frac{\Delta \mathbf{I_L}}{\mathbf{2}} \ldots (\mathbf{1})$$

$$\Delta \mathbf{I_L} = \frac{\mathbf{VCC - VOUT}}{\mathbf{L}} \times \frac{\mathbf{VOUT}}{\mathbf{VCC}} \times \frac{\mathbf{1}}{\mathbf{f}} \ldots (\mathbf{2})$$

(ΔI_L: Output Ripple Current, VCC: Input Voltage, VOUT: Output Voltage, f: Switching Frequency)

For design value of inductor ripple current, please carry out design tentatively with about 20% to 50% of maximum input current.
In the BD9G341AEFJ, it is recommended the below series of 4.7μH to 33μH inductance value.
Recommended Inductors：

Wurth Electronics Inc. 7447709XXX Series
SUMIDA CDRH129HF Series

2. Output Capacitor

In order for capacitor to be used in output to reduce output ripple, Low ceramic capacitor of ESR is recommended.
Also, for capacitor rating, on top of putting into consideration DC Bias characteristics, please use something whose maximum rating has sufficient margin with respect to the Output Voltage.
Output ripple voltage is looked for using the following formula.

$$\mathbf{V_{PP}} = \Delta \mathbf{I_L} \times \frac{\mathbf{1}}{\mathbf{2\pi \times f \times COUT}} + \Delta \mathbf{I_L} \times \mathbf{R_{ESR}} \ldots (\mathbf{3})$$

Please design in a way that it is held within Capacity Ripple Voltage.
In the BD9G341AEFJ, it is recommended a ceramic capacitor over 10μF.

3. Output voltage setting

The internal reference voltage of ERROR AMP is 1.0V.
Output voltage is determined like (4) types

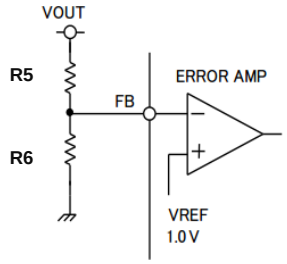


Figure 12. Output voltage setting

$$\mathbf{VOUT} = \frac{\mathbf{R5} + \mathbf{R6}}{\mathbf{R6}} \ldots (\mathbf{4})$$

The available minimum output voltage is restricted by minimum duty shown as the following.

MinDuty = f × MinOnTime(MinDuty: minimum duty, f: frequency, MinOnTime: minimum on time)

When the calculated voltage, VCC × MinDuty, is higher than 1V, the minimum output voltage is determined by VCC × MinDuty.

The available maximum output voltage is restricted by maximum duty shown as the following.

MaxDuty =1 - f × Toff_f (MaxDuty : maximum duty, Toff _f : Forced off time)

The available maximum output is shown as the following.

Maximum output voltage = VCC × MaxDuty – Iout ×Ron (Iout : load current, Ron : NMOS ON resistance)

4. Bootstrap Capacitor

Please connect from 0.1μF (Laminate Ceramic Capacitor) between BST Pin and LX Pins.

5. Catch Diode

BD9G341AEFJ should be taken to connect external catch diode between Lx Pin and GND Pin. The diode require adherence to absolute maximum Ratings of application. Opposite direction voltage should be higher than maximum voltage of LX Pin (V_{CCMAX} + 0.5V). The peak current is required to be higher than I_{OUTMAX} +ΔI_L.

6. Input Capacitor

BD9G341AEFJ needs an input decoupling capacitor. A low ESR ceramic capacitor over 4.7μF is recommended. Additionally, it should be located as close to the VCC pin as possible.

Capacitor should be selected under consideration of the rating not maximum input voltage with input ripple voltage exceed that and the degradation of capacitance by DC bias effect.

Input ripple voltage is calculated by using the following formula.

$$\mathbf{\Delta VCC} = \frac{\mathbf{IOUT}}{\mathbf{f} \times \mathbf{CVCC}} \times \frac{\mathbf{VOUT}}{\mathbf{VCC}} \times \left[\mathbf{1} - \frac{\mathbf{VOUT}}{\mathbf{VCC}}\right] \ldots (\mathbf{5})$$

CVCC: Input capacitor

RMS ripple current is calculated by using the following formula.

$$\mathbf{I_{CVCC}} = \mathbf{IOUT} \times \sqrt{\frac{\mathbf{VOUT}}{\mathbf{VCC}} \times \left(\mathbf{1} - \frac{\mathbf{VOUT}}{\mathbf{VCC}}\right)} \ldots (\mathbf{6})$$

If VCC=2 × VOUT, RMS ripple current is maximum. That is determined by (7).

$$\mathbf{I_{CVCC\_max}} = \frac{\mathbf{IOUT}}{\mathbf{2}} \ldots (\mathbf{7})$$

7. About Adjustment of DC/DC Comparator Frequency Characteristics

Role of Phase compensation element C3, C8, R3.

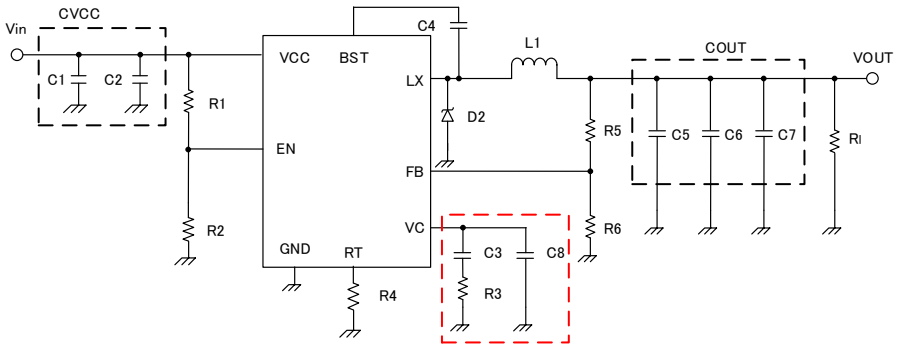


Figure 13. Feedback voltage resistance setting method

Stability and Responsiveness of Loop are controlled through VC Pin which is the output of Error Amp.
The combination of zero and pole that determines stability and responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the VC pin.
DC Gain of voltage return loop can be calculated for using the following formula.

$$\mathbf{A_{dc} = R_I \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{Vout}} \quad \dots(8)$$

Here, V_{FB} is Feedback Voltage (1.0V). A_{EA} is Voltage Gain of Error amplifier (typ: 100dB), Gcs is the transconductance of current detect(typ: 10A/V), and R_I is the output load resistance value.

There are 2 important poles in the control loop of this DC/DC.
The first occurs with/ through the output resistance of phase compensation capacitor(C3)and Error amplifier.The other one occurs with/through the output capacitor and load resistor.
These poles appear in the frequency written below.

$$\mathbf{f_{p1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}} \quad \dots(9)$$

$$\mathbf{f_{p2} = \frac{1}{2\pi \times C_{OUT} \times R_I}} \quad \dots(10)$$

Here, G_{EA} is the transconductance of Error amplifier(typ: 300μA/V).
In this control loop, one zero which occurs because of phase compensation capacitor C3 and phase compensation resistor R3 at the frequency calculated below is important.

$$\mathbf{f_{z1} = \frac{1}{2\pi \times C3 \times R3}} \quad \dots(11)$$

Also, if the output capacitance and ESR value are large, in this control loop, there are cases when it has an important, separate zero (ESR zero).
This ESR zero occurs due to ESR of output capacitor and capacitance, and exists in the frequency below.

$$\mathbf{fz_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}} \quad \dots(12) \qquad \text{(ESR zero)}$$

In this case, the 3rd pole determined with the 2nd phase compensation capacitor(C8) and phase compensation resistor(R3) is used in order to correct the ESR zero results in loop gain.This pole exists in the frequency shown below.

$$\mathbf{f_{p3} = \frac{1}{2\pi \times C8 \times R3}} \quad \dots(13) \qquad \text{(pole that corrects ESR zero)}$$

The target of phase compensation design is to create a communication function in order to acquire necessary band and phase margin.
Cross-over frequency (band) at which loop gain of return loop becomes “0” is important. When cross-over frequency becomes low, power supply fluctuation response, load response, etc worsens. On the other hand, when cross-over frequency is too high, instability of the loop can occur. Tentatively, cross-over frequency is targeted to be made 1/20 or below of switching frequency.

Selection method of phase compensation constant is shown below.

1. Phase compensation resistor(R3) is selected in order to set to the desired cross-over frequency.
   Calculation of RC is done using the formula below.

$$\mathbf{R3} = \frac{2\pi \times C_{OUT} \times f_c}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad \ldots(\mathbf{14})$$

   Here, fc is the desired cross-over frequency. It is made about 1/20 and below of the normal switching frequency (fs).

2. Phase compensation capacitor(C3) is selected in order to achieve the desired phase margin.
   In an application that has a representative inductance value(about several 4.7μH to 33μH), by matching zero of compensation to 1/4 and below of the cross-over frequency, sufficient phase margin can be acquired. C3 can be calculated using the following formula.

$$\mathbf{C3} > \frac{4}{2\pi \times R3 \times f_c} \quad \ldots(\mathbf{15})$$

3. Examination whether the second phase compensation capacitor C8 is necessary or not is done.
   If the ESR zero of output capacitor exists in a place that is smaller than half of the switching frequency, a second phase compensation capacitor is necessary. In other words, it is the case wherein the formula below happens.

$$\frac{1}{2\pi \times C_{OUT} \times R_{ESR}} < \frac{f_s}{2} \quad \ldots(\mathbf{16})$$

   In this case, add the second phase compensation capacitor C8, and match the frequency of the third pole to the frequency fp3 of ESR zero.

$$C8 = \frac{C_{OUT} \times R_{ESR}}{R3} \quad \ldots(\mathbf{17})$$

8. Frequency setting

Arbitrary internal oscillator frequency setup is possible by connecting R4 resistance at RT pin in Figure 13. Recommended frequency range is 50 kHz to 750 kHz.
For setting frequency f [Hz], R4 resistance is looked for using the following formula.

$$R4 = \frac{\frac{1}{f} - 400 \times 10^{-9}}{96.48 \times 10^{-12}} \ [\Omega] \ldots(18)$$

If the setting frequency is 200kHz, R4 is 47kΩ.
R4 resistance is related to frequency as shown in Figure14.

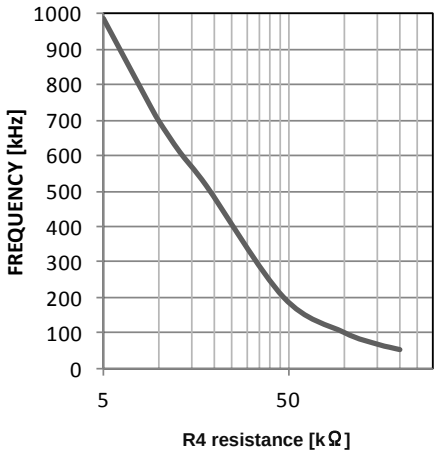


Figure 14. Oscillator Frequency vs R4 resistance

9. External UVLO threshold

The high precision reset function is built in EN pin of BD9G341AEFJ, and arbitrary low-voltage malfunction prevention setup is possible by connecting EN pin to resistance division of input voltage.
When you use, please set R1 and R2 in Figure. 13 to arbitrary voltage of IC turned on(Vuv) and hysteresis(Vuvhys) like below.

$$\mathbf{R1} = \frac{\mathbf{V_{UVHYS}}}{\mathbf{IEN}}\ [\mathbf{\Omega}]$$

$$\mathbf{R2} = \frac{\mathbf{VEN} \times \mathbf{R1}}{\mathbf{V_{UV}} - \mathbf{VEN}}\ [\mathbf{\Omega}]$$

IEN: EN pin source current 10uA(typ) VEN: EN pin output on threshold 2.6V(typ)
As an example in typical sample, When Vcc voltage which IC turned on 15V, Hysteresis width 1V, The resistance divider set to R1=100kΩ,R2=20kΩ.

Notes

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