3.0 V to 36 V Input, 2.0 A Integrated FET Single Synchronous Quiescent Operating Current Buck DC/DC Converter for Automotive

BD9P233MUF-C

General Description

BD9P233MUF-C is an ultra-low I_Q Buck converter for 3.3 V output. The LLM (Light Load Mode) control ensures an ultra-low quiescent current and high efficiency at light load situation as well as at high load situations while maintaining a regulated output voltage.

Features

- Nano Pulse Control™
- AEC-Q100 Qualified *(Note 1)*
- Low Dropout: 100 % ON Duty Cycle
- Light Load Mode (LLM)
- Spread Spectrum Function
- Adjustable Frequency
- Synchronization by External Clock
- Thermal Shutdown Protection
- Input Under Voltage Lockout Protection
- Over Current Protection
- Output Over Voltage Protection
- Power Good Output

(Note 1) Grade 1

Applications

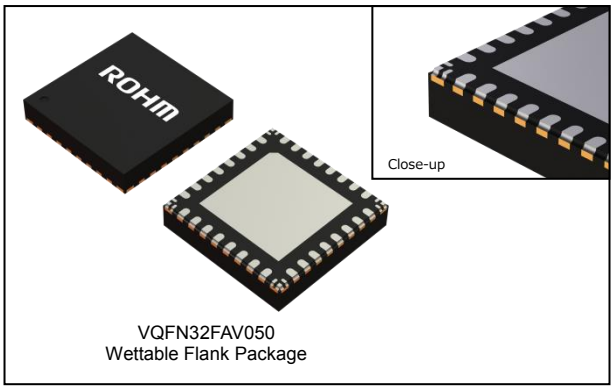
- Automotive Battery Powered Supplies (Cluster Panel, Car infotainment)
- Industrial/Consumer Supplies

Key Specifications

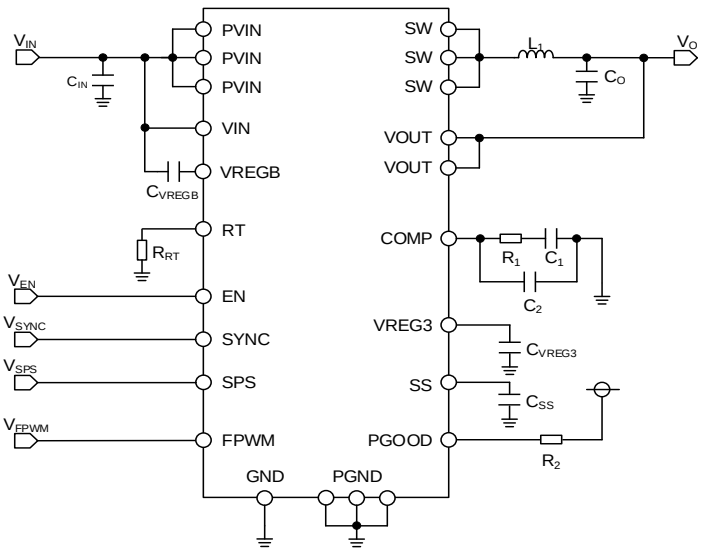
- Input Voltage Range: 3.0 V to 36 V (initial startup is 3.6 V or more)
- Output Voltage: 3.3 V
- Switching Frequency: 200 kHz to 2.4 MHz
- Output Current: 2 A (Max)
- Shutdown Circuit Current: 10 µA (Max) (25 °C)
- Quiescent Operating Current: 26 µA (Typ) (25 °C)
- Operating Temperature Range: -40 °C to +125 °C

Package

	W (Typ) x D (Typ) x H (Max)
VQFN32FAV050:	5.0 mm x 5.0 mm x 1.0 mm

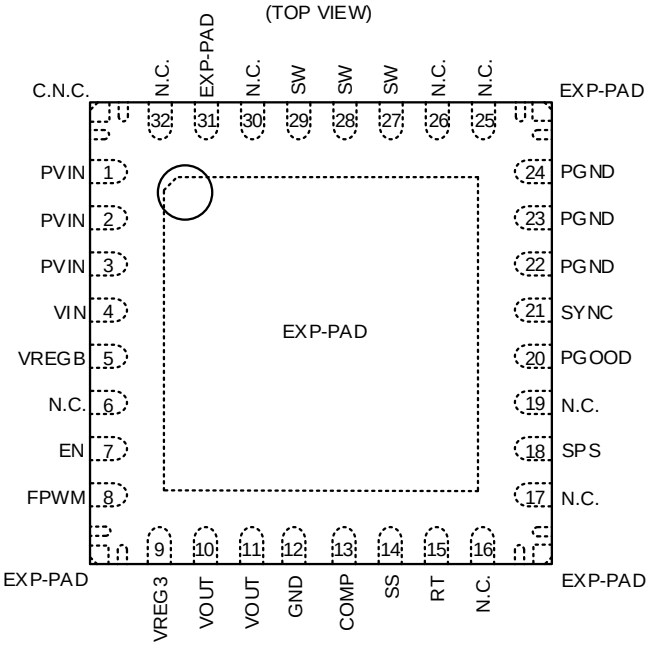


Typical Application Circuit



"Nano Pulse Control™" is a trademark of ROHM Co., Ltd.

Pin Configuration

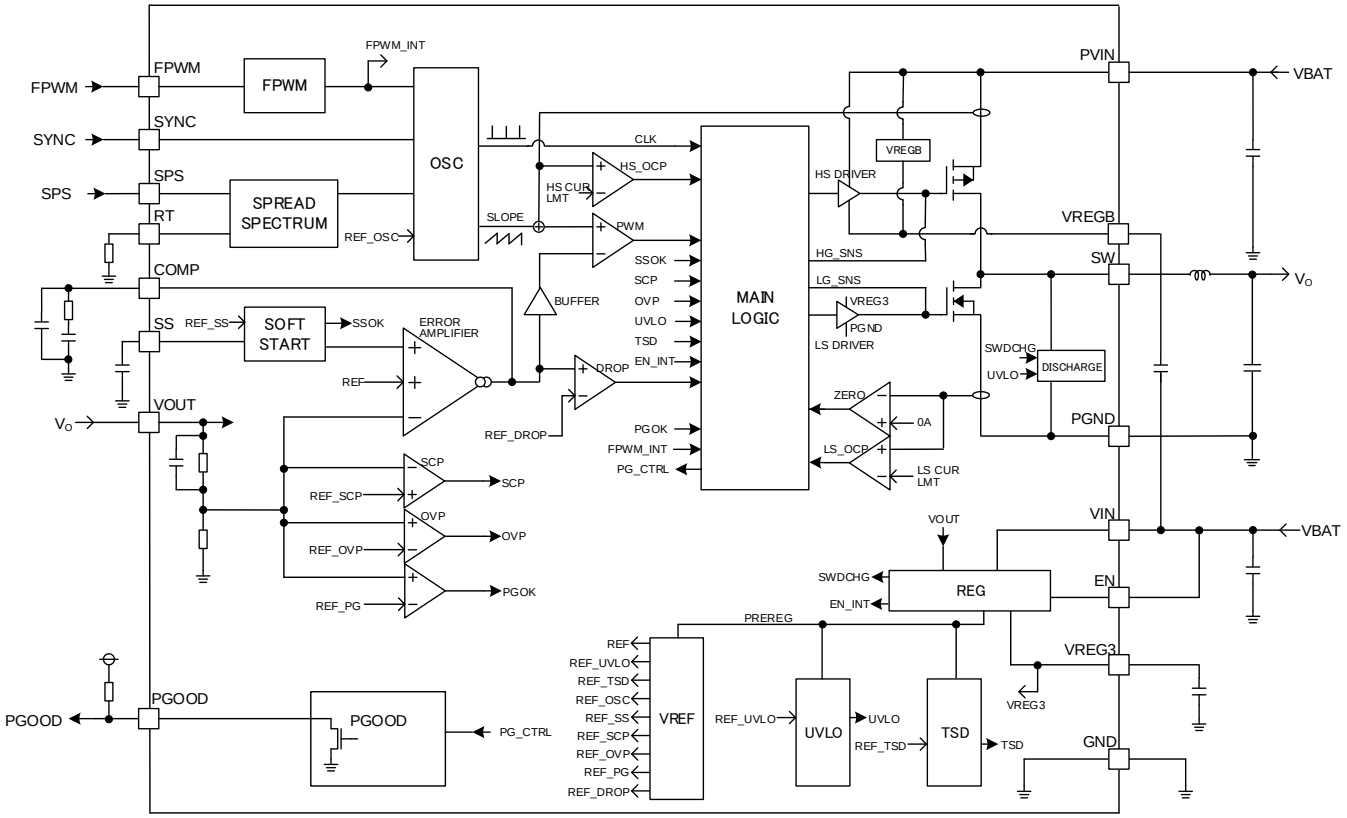


Pin Description

Pin No.	Pin Name	Function
1,2,3	PVIN	Power supply input for output FET.
4	VIN	Power supply input.
5	VREGB	Internal regulator output. Used as supply to driver circuits for high side FET. Do not connect to any external loads. Connect a 1.0 µF ceramic capacitor from this pin to the VIN pin. The voltage between the VIN pin and the VREGB pin is 4.8 V (Typ).
6	N.C.	No internal connection pin.
7	EN	Enable input. The device is active when this pin is high and shutdown when this pin is low. EN slew rate should be faster than 1 V/ms.
8	FPWM	Forced PWM mode select pin.
9	VREG3	Internal regulator output. It supplies power to internal blocks. It cannot connect to external loads except FPWM, SPS and a pull-up resistor to PGOOD. Connect a 1.0 µF ceramic capacitor from this pin to GND.
10,11	VOUT	Feedback input to regulator. Connect to the output voltage sense point.
12	GND	Reference ground.
13	COMP	Error amplifier output. Connect frequency compensation parts.
14	SS	Soft start time set pin. Connect a ceramic capacitor between this pin and GND.
15	RT	Switching frequency setting pin. Connect a resistor between this pin and GND.
16,17	N.C.	No internal connection pin.
18	SPS	Spread spectrum select pin. It should be connected to GND when this pin is not used.
19	N.C.	No internal connection pin.
20	PGOOD	An open drain output. Connect a pull-up resistor. Output “high” indicates normal state of regulator output and “low” indicates the error state.
21	SYNC	Synchronization signal input pin. Used to synchronize the switching frequency with the system clock. It should be connected to GND when this pin is not used.
22,23,24	PGND	Power ground pin. It is connected to internal low side FET. Connect to GND.
25,26	N.C.	No internal connection pin.
27,28,29	SW	The output of internal MOSFET. Connect to power inductor.
30	N.C.	No internal connection pin.
31	EXP-PAD	Exposed pad. This pin can be connected to PGND through the center EXP-PAD. For details, refer to directions for pattern layout of PCB on page 36.
32	N.C.	No internal connection pin. This pin can be connected to PGND through the center EXP-PAD. For detail, refer to directions for pattern layout of PCB on page 36.
-	C.N.C.	Corner no internal connection pin. This pin should not be connected to any other lines.
-	EXP-PAD	Exposed pad. Connect center EXP-PAD to the internal PCB ground plane using multiple via, it will provide excellent heat dissipation characteristics. Three corner EXP-PADs and pin 31 are connected to center EXP-PAD with internal frame.

The N.C. pin 6, 26 and 30 should not be connected to any other lines for the safety against adjacent inter-pin shorts.
The N.C. pin 16, 17, 19 and 25 can be connected to GND or opened.

Block Diagram



Description of Blocks

1. REG (for internal power supply)
   The REG block generates the power supply for the internal circuits and low side driver. After the completion of the soft start function, this power supply is sourced through switches from the VOUT pin connected to V_O voltage. Placing a 1 µF ceramic capacitor between the VREG3 pin and the GND pin is recommended for decouple.
   By connecting the VOUT pin to the V_O, almost internal circuits are powered from the VOUT and the power consumption from VIN is reduced after the soft start function is completed.

2. VREF
   The VREF block generates internal reference voltages for ERROR AMPLIFIER and circuits for protection.

3. UVLO
   The UVLO function is for under voltage lockout protection.
   The operation of this device is available when VIN rises 2.8 V (Typ) or more. When VIN falls 2.5 V (Typ) or below, the device is shut down. The threshold voltage has a hysteresis of 300 mV (Typ).

4. TSD
   This is the thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. However, if the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit [Tj ≥ 175 °C (Typ)] that will turn OFF output FET and VREG3 output. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

5. SCP
   The SCP comparator is for detection of short circuit. When the output voltage falls 70 % (Typ) or below after the completion of the soft start, this comparator outputs the detect signal.

6. OVP
   The OVP comparator is for protection of over voltage. When the output voltage goes 110 % (Typ) or more, High Side FET and Low Side FET are turned off. When the output voltage falls 105 % (Typ) or below, the operation will recover.

Description of Blocks – continued

7. SOFTSTART
   The SOFTSTART block slows down the rise of output voltage during startup. This function allows the prevention of output voltage overshoot and inrush current.

8. ERROR AMPLIFIER
   The ERROR AMPLIFIER block is an error amplifier and its inputs are the reference voltage, the SS pin voltage and the feedback voltage of the VOUT pin. Phase compensation can be set by connecting a resistor and a capacitor to the COMP pin. See selection of the phase compensation circuit R_1, C_1, and C_2 on page 27.

9. MAIN LOGIC
   The MAIN LOGIC block controls main operation of this device.

10. PGOOD
    When the VOUT pin voltage reaches to 95 % (Typ) of the regulated voltage, the Nch FET for power good indication turns off. When the output voltage falls below 90 % (Typ) for 25 µs (Typ) or more, the Nch FET turns on. This function is available after the completion of the soft start function. An external pull-up resistor is required for a logic supply at the PGOOD pin.

11. FPWM
    By setting the FPWM pin 2.5 V or more, the device switches to forced PWM mode. By setting the FPWM pin 0.8 V or less, the device switches to forced LLM. For the method of the mode change using this pin, refer to page 16.

12. OSC
    The OSC block generates clock signal for the switching operation and slope waveform for PWM control. The switching frequency is determined by the R_{RT} connected to the RT pin. See Figure 32, Table 4 and Table 5 on page 26.

13. SPREAD SPECTRUM
    By setting the SPS pin 2.5 V or more, the device starts to spread spectrum function. See the Spread Spectrum on page 16.

14. HS/LS DRIVER
    The HS/LS Driver blocks drive Power FETs connected to the SW pin.

15. ZERO
    The ZERO block detects that the current of inductor reverses from the SW pin to the PGND pin when Low Side FET is turned on. The detected signal input to the internal logic and used for the diode emulation function in LLM.

16. HS/LS OCP
    The HS/LS OCP block detects whether the current passes through FETs reaches to the limited value. See the operation description on page 19.

17. PWM
    The PWM comparator adjusts duty for switching operation.

18. DROP
    The DROP comparator generates the signal for LLM.

19. DISCHARGE
    The DISCHARGE block is for discharging output capacitor through the SW pin when the TSD, UVLO or EN OFF.

20. VREGB
    The VREGB block generates the power supply for the high-side driver. VREGB voltage is VIN voltage -4.8 V (Typ) when VIN voltage is 13 V. Place a 1 µF ceramic capacitor between the VIN pin and the VREGB pin.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Input Voltage	V_{PVIN},V_{VIN}	-0.3 to +42	V
PVIN – VREGB, VIN – VREGB Pin Voltage	$V_{PVIN - VREGB}$, $V_{VIN - VREGB}$	-0.3 to +7	V
EN Pin Voltage	V_{EN}	-0.3 to V_{VIN}	V
VREG3, SYNC, FPWM, SPS, VOUT, PGOOD Pin Voltage	V_{VREG3} , V_{SYNC} , V_{FPWM} , V_{SPS} , V_{VOUT}, V_{PGOOD}	-0.3 to +7	V
Junction Temperature Range	Tj	-40 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
VQFN32FAV050				
Junction to Ambient	θ_{JA}	125.5	29.9	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	11	6	°C/W

(Note 1) Based on JESD51-2A (Still-Air). Using a BD9P233MUF-C chip.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Power Supply Voltage	V_{VIN}	3 *(Note 1)*	36	V
Output Current	I_{OUT}	-	2	A
Switching Frequency	f_{OSC}	200	2400	kHz
Min ON Pulse Width	t_{ONMIN}	-	60	ns
Synchronous Operation Frequency Range	f_{SYNC}	200	2400	kHz
Operating Temperature	Topr	-40	+125	°C

(Note 1) Initial startup is 3.6 V or more.

Electrical Characteristics (Unless otherwise specified, Ta = - 40 °C to +125 °C, V_{VIN} = 13 V, V_{EN} = 3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Shutdown Current	I_{SDN}	-	7	10	µA	V_{EN} = 0 V, Ta = 25 °C
Quiescent Current	I_Q	-	26	60	µA	I_{OUT} = 0 A, V_{FPWM} = V_{SPS} = 0 V
Under Voltage Lockout Threshold Voltage	$V_{UVLO-TH}$	-	2.50	2.99	V	V_{VIN}: falling
Under Voltage Lockout Hysteresis Voltage	$V_{UVLO-HYS}$	150	300	600	mV	
Output Voltage	V_{OUT}	3.234	3.300	3.366	V	V_{VIN} = 4 V to 36 V, PWM mode
		3.20 *(Note 1)*	3.30 *(Note 1)*	3.40 *(Note 1)*	V	V_{VIN} = 13 V, LLM, I_{OUT} = 0 A Including output ripple
High Side FET ON Resistance	R_{ONH}	-	190	375	mΩ	I_{SW} = -50 mA, V_{VIN} = 13 V
Low Side FET ON Resistance	R_{ONL}	-	120	244	mΩ	I_{SW} = -50 mA, V_{VIN} = 13 V
High Side FET Current Protection *(Note 1)*	I_{HSOCP}	3.5	5.0	6.5	A	
Low Side FET Current Protection *(Note 1)*	I_{LSOCP}	2.5	3.8	-	A	
Error Amplifier Transconductance	G_{EA}	140	280	420	µA/V	V_{COMP} = 1 V
Oscillator Frequency1	f_{OSC1}	2.0	2.2	2.4	MHz	R_{RT} = 27 kΩ, V_{VIN} = 7 V to 18 V, V_{FPWM} = 3 V, I_{OUT} = 0 A
Oscillator Frequency2 (Spread Spectrum)	f_{OSC2}	1.95	2.25	2.55	MHz	R_{RT} = 24 kΩ, V_{VIN} = 7 V to 18 V, V_{FPWM} = V_{SPS} = 3 V, I_{OUT} = 0 A
Oscillator Frequency3 *(Note 1)*	f_{OSC3}	328	400	472	kHz	R_{RT} = 210 kΩ, V_{VIN} = 5 V to 36 V, V_{FPWM} = 3 V, I_{OUT} = 0 A
SYNC High Threshold Voltage	$V_{IH-SYNC}$	2.5	-	-	V	SYNC State High
SYNC Low Threshold Voltage	$V_{IL-SYNC}$	-	-	0.8	V	SYNC State Low
SYNC Sink Current	I_{SYNC}	3	6	12	µA	V_{SYNC} = 3 V
SYNC Input Pulse High Width	t_{H-SYNC}	100	-	-	ns	
SYNC Input Pulse Low Width	t_{L-SYNC}	100	-	-	ns	
FPWM ON Threshold Voltage	$V_{IH-FPWM}$	2.5	-	-	V	Forced PWM mode
FPWM OFF Threshold Voltage	$V_{IL-FPWM}$	-	-	0.8	V	LLM
FPWM Sink Current	I_{FPWM}	-	0.1	1.0	µA	V_{FPWM} = 3 V
SPS ON Threshold Voltage	V_{IH-SPS}	2.5	-	-	V	Spread Spectrum ON
SPS OFF Threshold Voltage	V_{IL-SPS}	-	-	0.8	V	Spread Spectrum OFF
SPS Sink Current	I_{SPS}	-	0.1	1.0	µA	V_{SPS} = 3 V
Soft Start Charge Current	I_{SS}	1.3	1.9	2.4	µA	

(Note 1) Not production tested.

Electrical Characteristics – continued
(Unless otherwise specified, Ta = - 40 °C to +125 °C, V_{VIN} = 13 V, V_{EN} = 3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
EN ON Threshold Voltage	V_{IH-EN}	2.5	-	-	V	
EN OFF Threshold Voltage	V_{IL-EN}	-	-	0.8	V	
EN Sink Current	I_{EN}	-	0.1	1.0	µA	V_{EN} = 3 V
PGOOD Threshold Voltage	V_{PGD}	-15	-10	-5	%	% of V_{OUT} at PWM mode, V_{OUT}: falling
PGOOD ON Sink Current	I_{PGD}	0.5	2	-	mA	V_{PGOOD} = 0.5 V
PGOOD Leak Current	$I_{PGDLEAK}$	-	0	1.0	µA	V_{PGOOD} = 3.3 V
SCP Threshold Voltage	V_{SCP}	-35	-30	-25	%	% of V_{OUT} at PWM mode, V_{OUT}: falling
OVP Threshold Voltage	V_{OVP}	5	10	15	%	% of V_{OUT} at PWM mode, V_{OUT}: rising
SW OFF Shut Sink Current	I_{SWSHUT}	4.7	8.2	-	mA	V_{EN} = 0 V, V_{SW} = 3.3 V

Typical Performance Curves
(Unless otherwise specified, Ta = - 40 °C to +125 °C, V_{VIN} = 13 V, V_{EN} = 3 V)

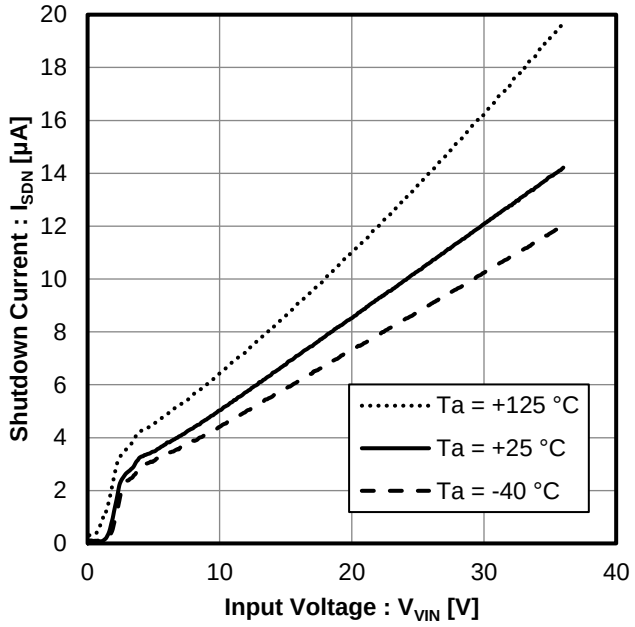


Figure 1. Shutdown Current vs Input Voltage

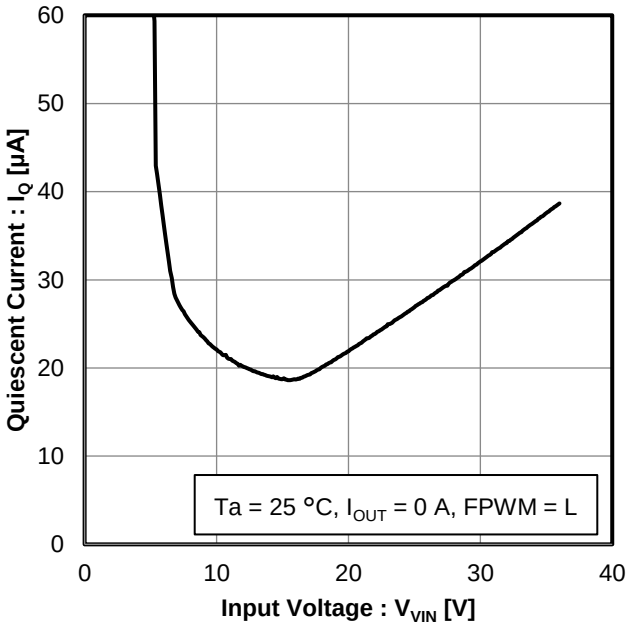


Figure 2. Quiescent Current vs Input Voltage

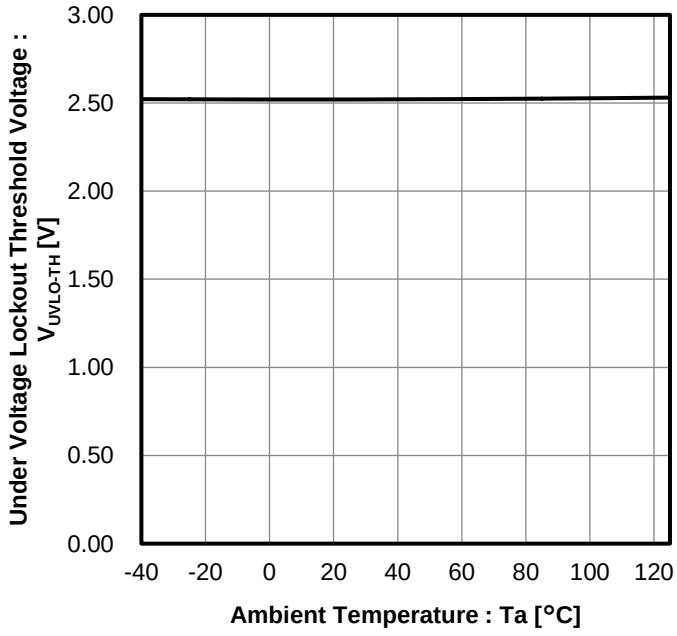


Figure 3. Under Voltage Lockout Threshold Voltage vs Ambient Temperature

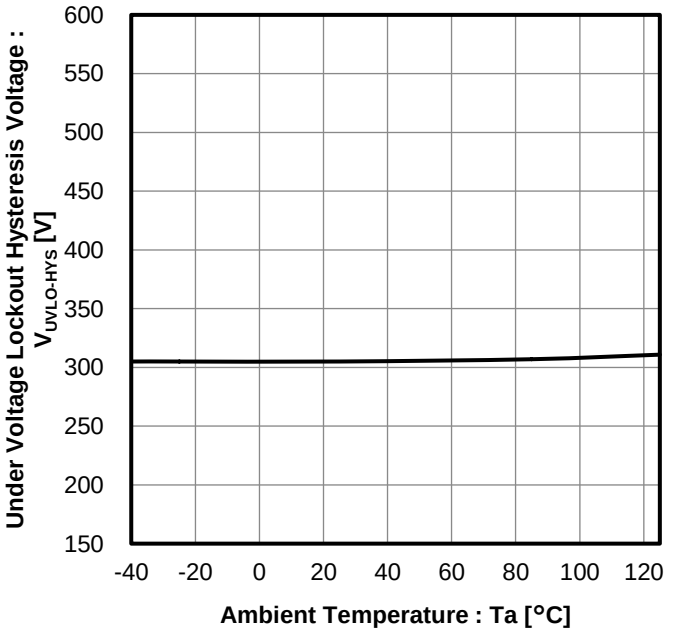


Figure 4. Under Voltage Lockout Hysteresis Voltage vs Ambient Temperature

Typical Performance Curves – continued
(Unless otherwise specified, Ta = - 40 °C to +125 °C, V_{VIN} = 13 V, V_{EN} = 3 V)

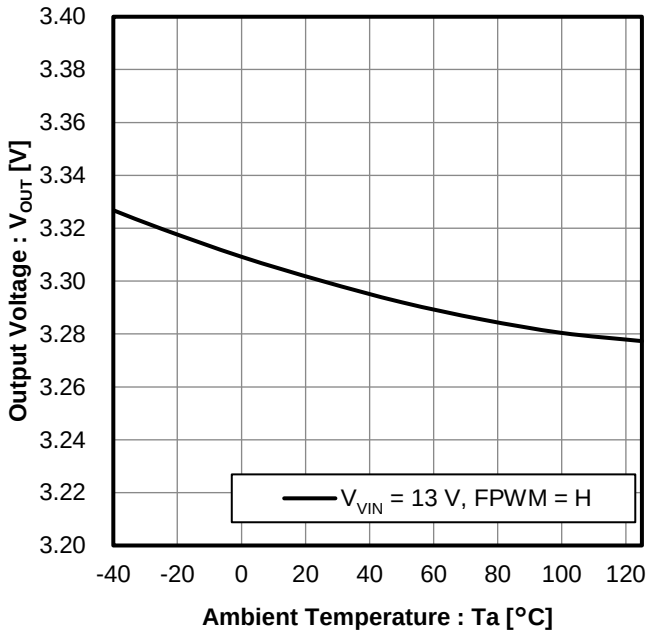


Figure 5. Output Voltage vs Ambient Temperature

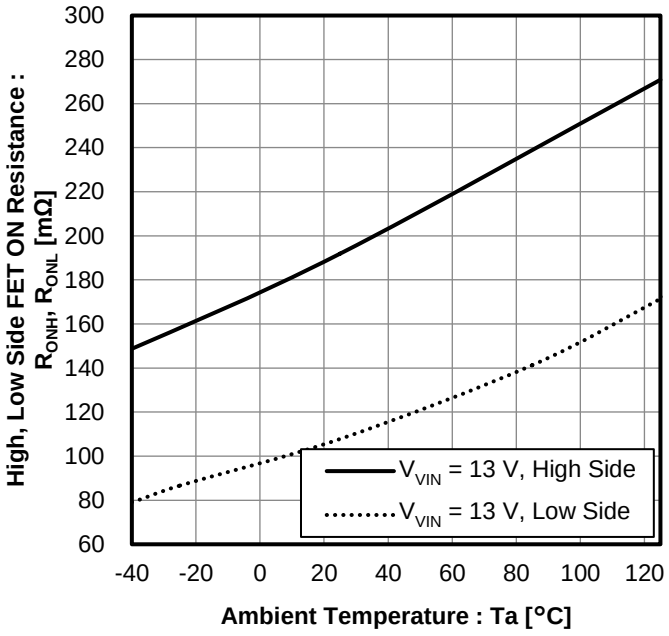


Figure 6. High/Low Side FET ON Resistance vs Ambient Temperature

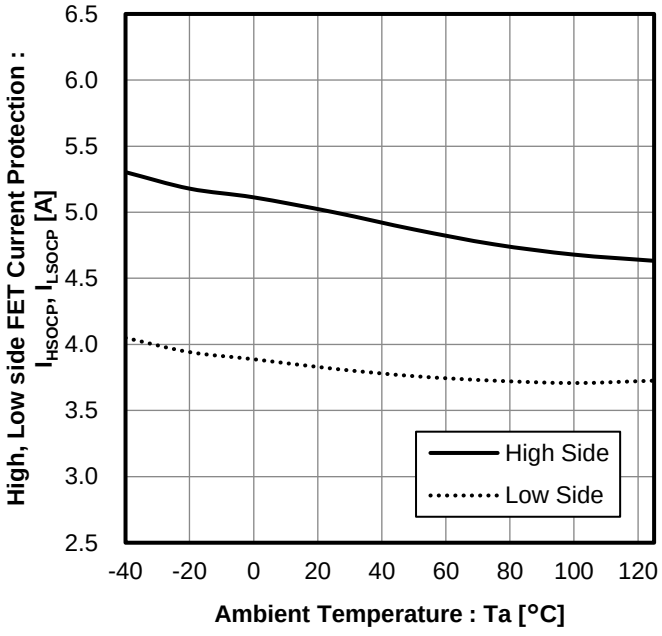


Figure 7. High/Low Side FET Current Protection vs Ambient Temperature

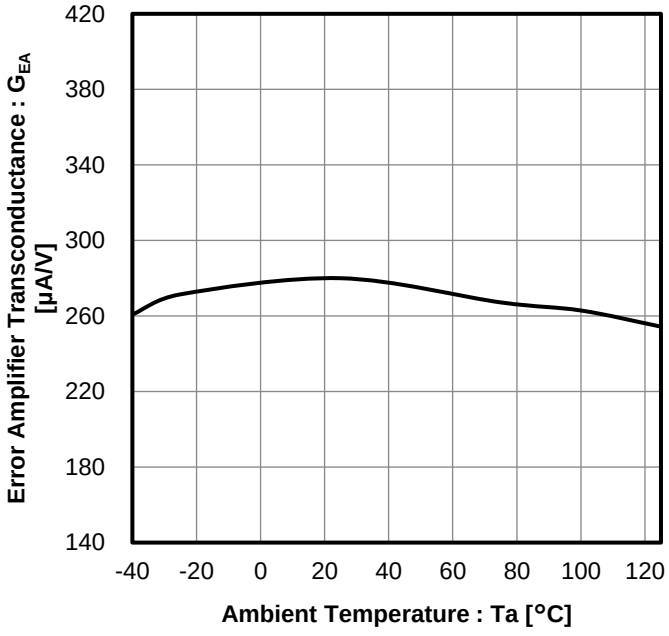


Figure 8. Error Amplifier Transconductance vs Ambient Temperature

Typical Performance Curves – continued
(Unless otherwise specified, Ta = - 40 °C to +125 °C, V_{VIN} = 13 V, V_{EN} = 3 V)

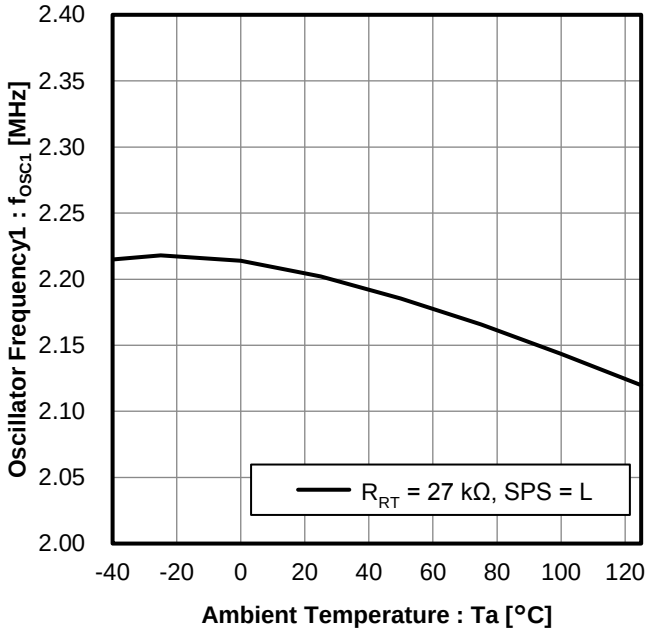


Figure 9. Oscillator Frequency1 vs Ambient Temperature

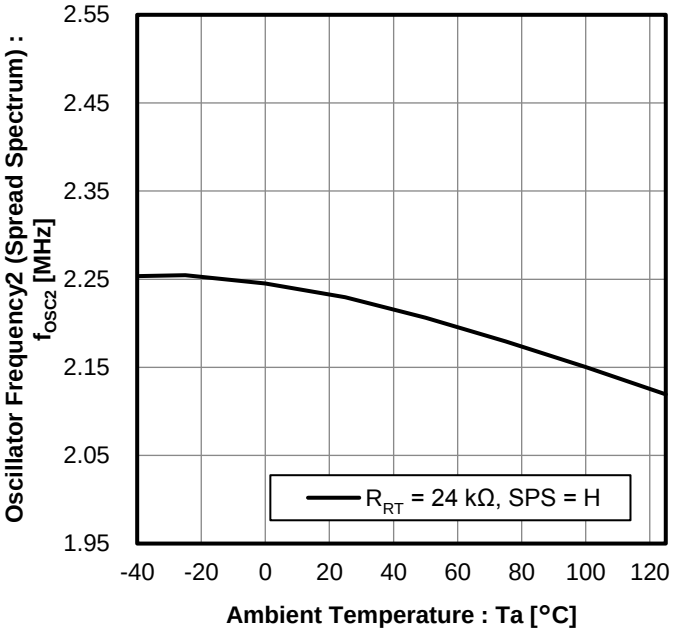


Figure 10. Oscillator Frequency2 (Spread Spectrum) vs Ambient Temperature

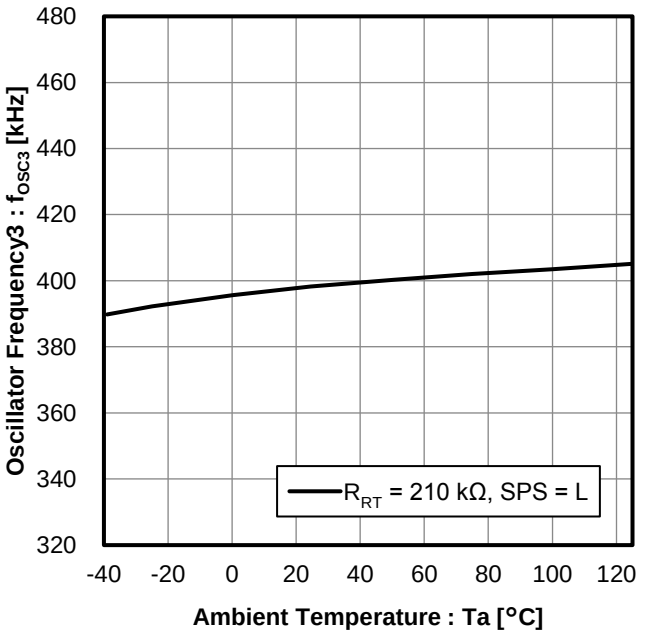


Figure 11. Oscillator Frequency3 vs Ambient Temperature

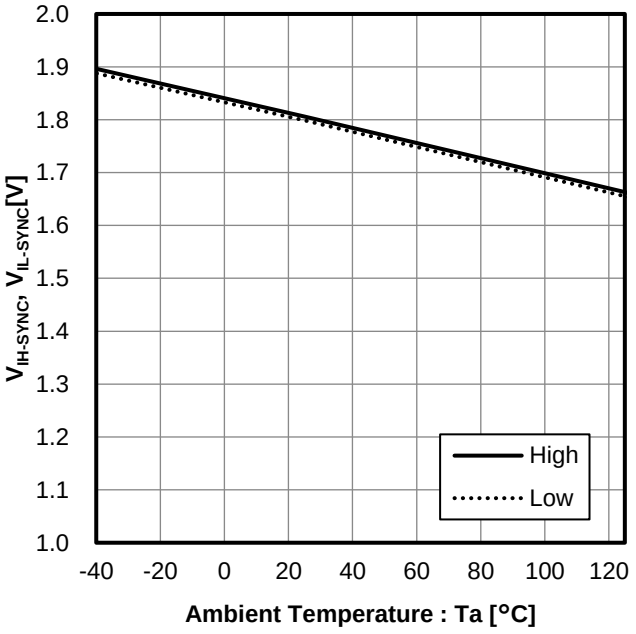


Figure 12. SYNC High/Low Threshold Voltage vs Ambient Temperature

Typical Performance Curves – continued
(Unless otherwise specified, Ta = - 40 °C to +125 °C, V_{VIN} = 13 V, V_{EN} = 3 V)

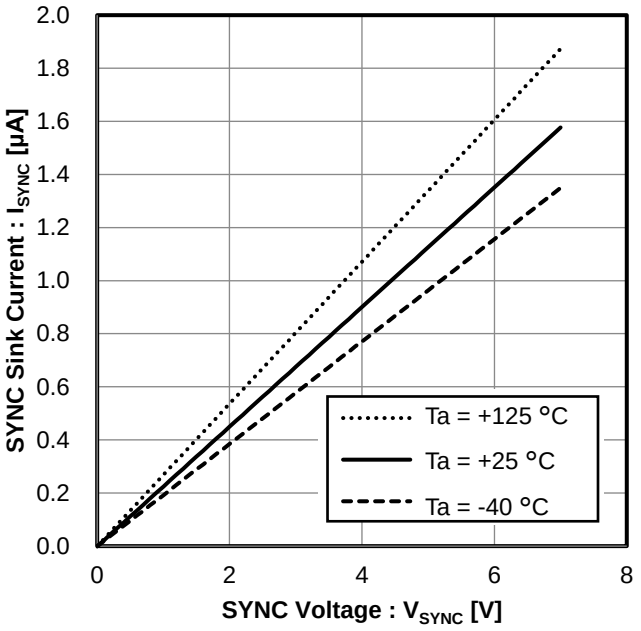


Figure 13. SYNC Sink Current vs SYNC Voltage

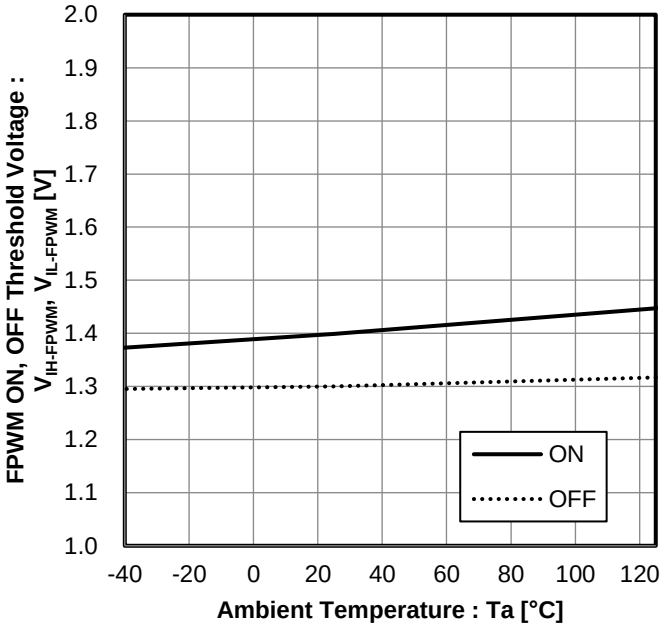


Figure 14. FPWM ON/OFF Threshold Voltage vs Ambient Temperature

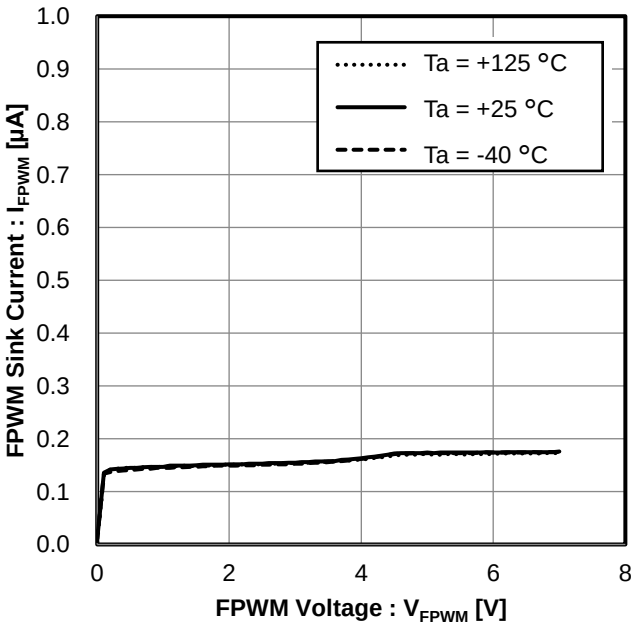


Figure 15. FPWM Sink Current vs FPWM Voltage

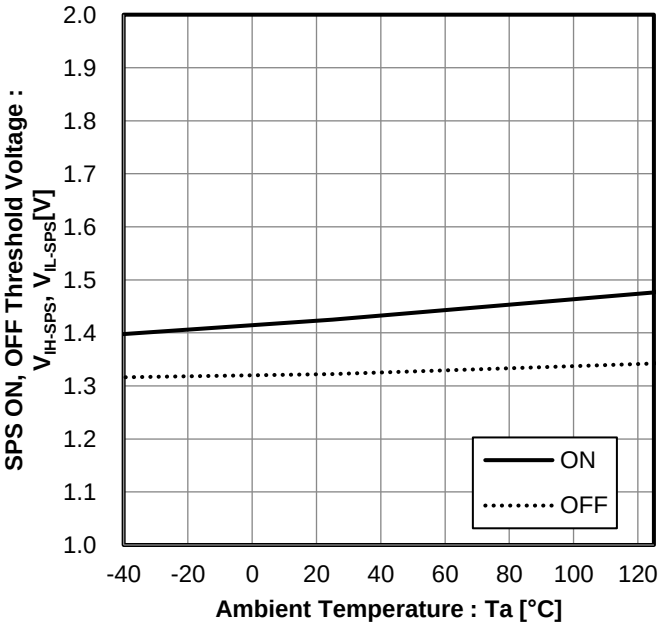


Figure 16. SPS ON/OFF Threshold Voltage vs Ambient Temperature

Typical Performance Curves – continued
(Unless otherwise specified, Ta = - 40 °C to +125 °C, V_{VIN} = 13 V, V_{EN} = 3 V)

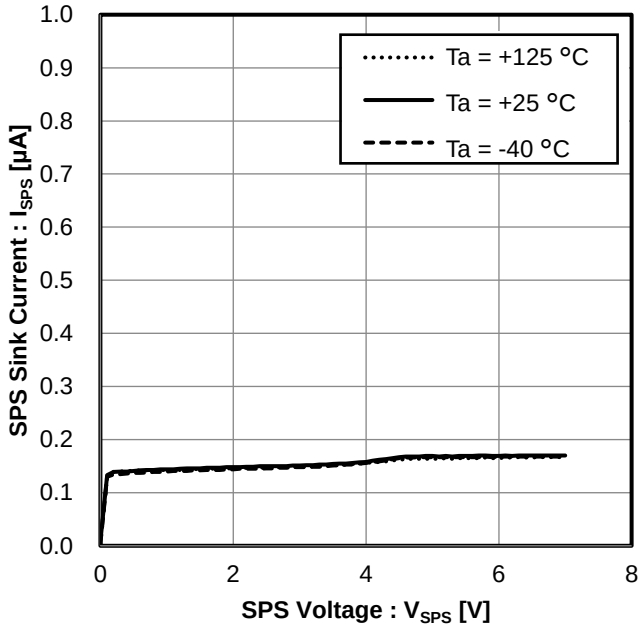


Figure 17. SPS Sink Current vs SPS Voltage

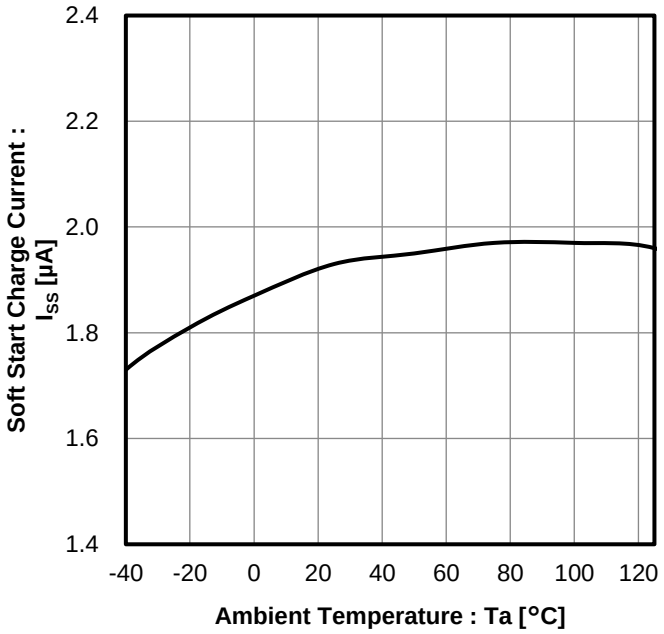


Figure 18. Soft Start Charge Current vs Ambient Temperature

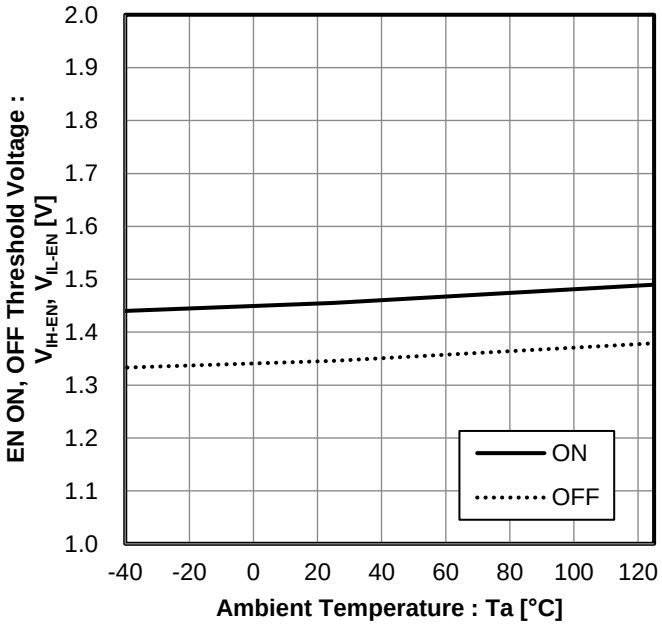


Figure 19. EN ON/OFF Threshold Voltage vs Ambient Temperature

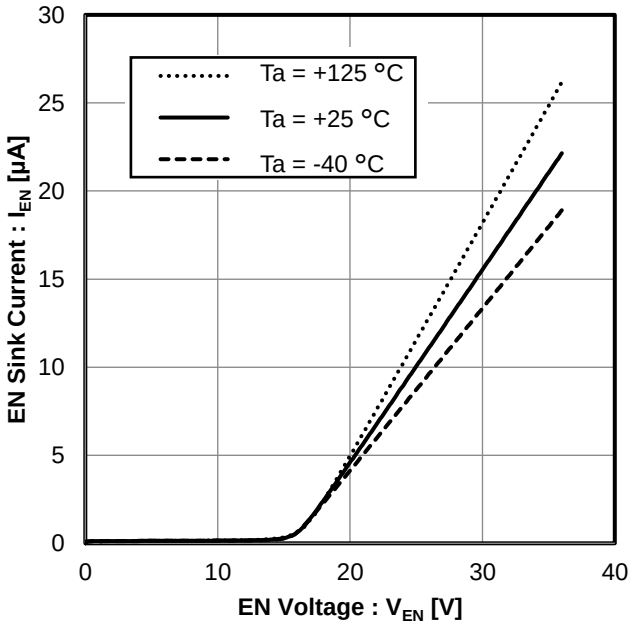


Figure 20. EN Sink Current vs EN Voltage

Typical Performance Curves – continued
(Unless otherwise specified, Ta = - 40 °C to +125 °C, V_{VIN} = 13 V, V_{EN} = 3 V)

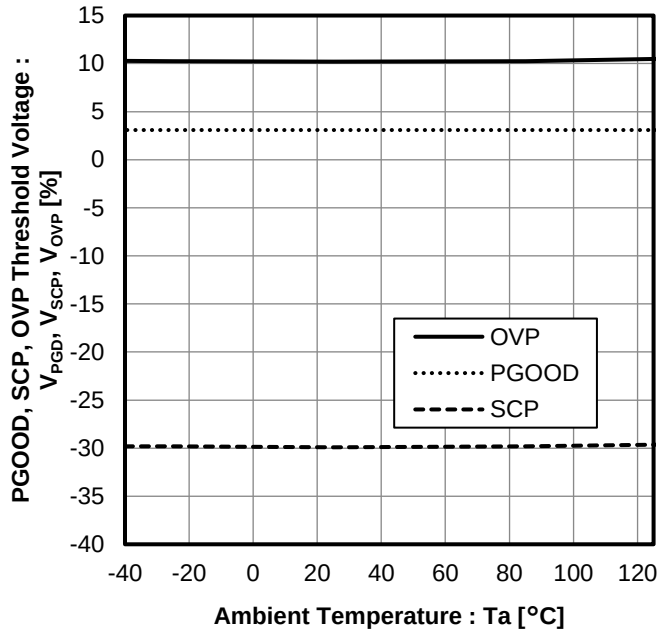


Figure 21. PGOOD/SCP/OVP Threshold Voltage vs Ambient Temperature

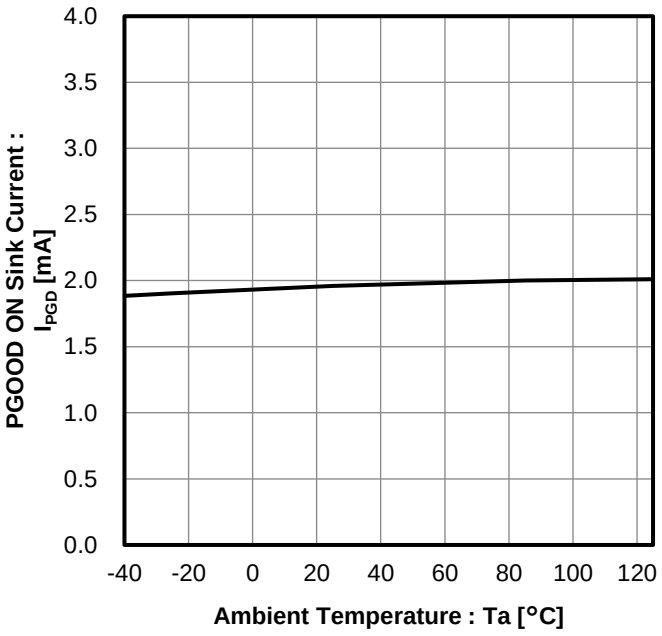


Figure 22. PGOOD ON Sink Current vs Ambient Temperature

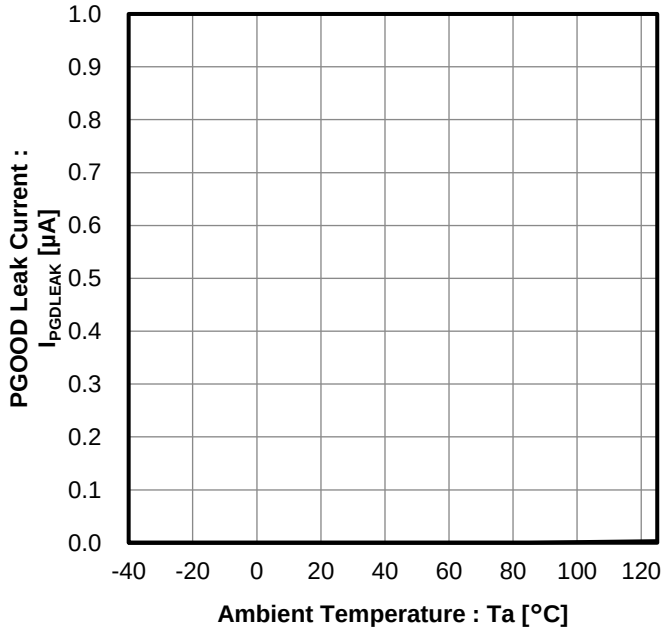


Figure 23. PGOOD Leak Current vs Ambient Temperature

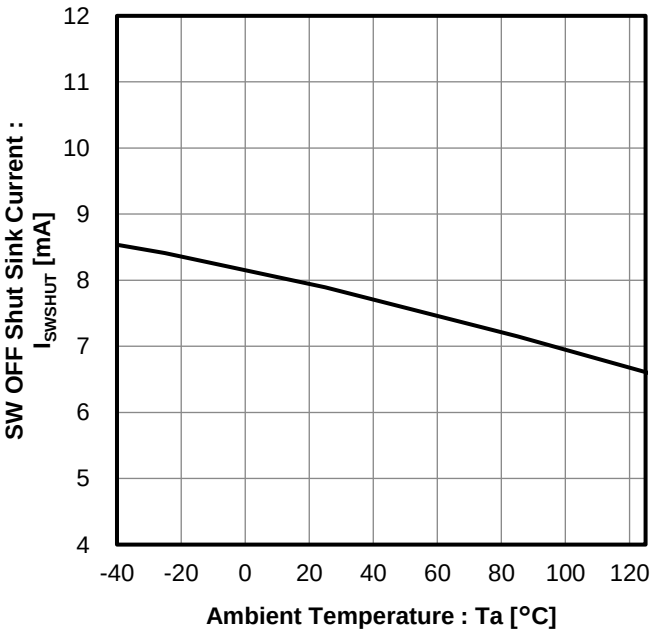


Figure 24. SW OFF Shut Sink Current vs Ambient Temperature

Function Explanations

1. Start Up/Shutdown Operation

Start up and shutdown are controlled by the voltage applied to the EN pin. The device starts up with an input voltage of 2.5 V or more and shuts down with a voltage of 0.8 V or less. If this function is unnecessary, the EN pin can directly connect to the VIN pin. However, the EN pin is recommended to pull-up to the VIN pin with the resistance for the safety against adjacent inter-pin shorts between the EN pin and the FPWM pin. The EN pin must not be left floating. This device prevents the output voltage overshoot and inrush current by soft start operation at start up. The switching frequency during start up rises in proportion to the SS pin voltage. A timing chart of typical startup and shutdown is shown in Figure 25.

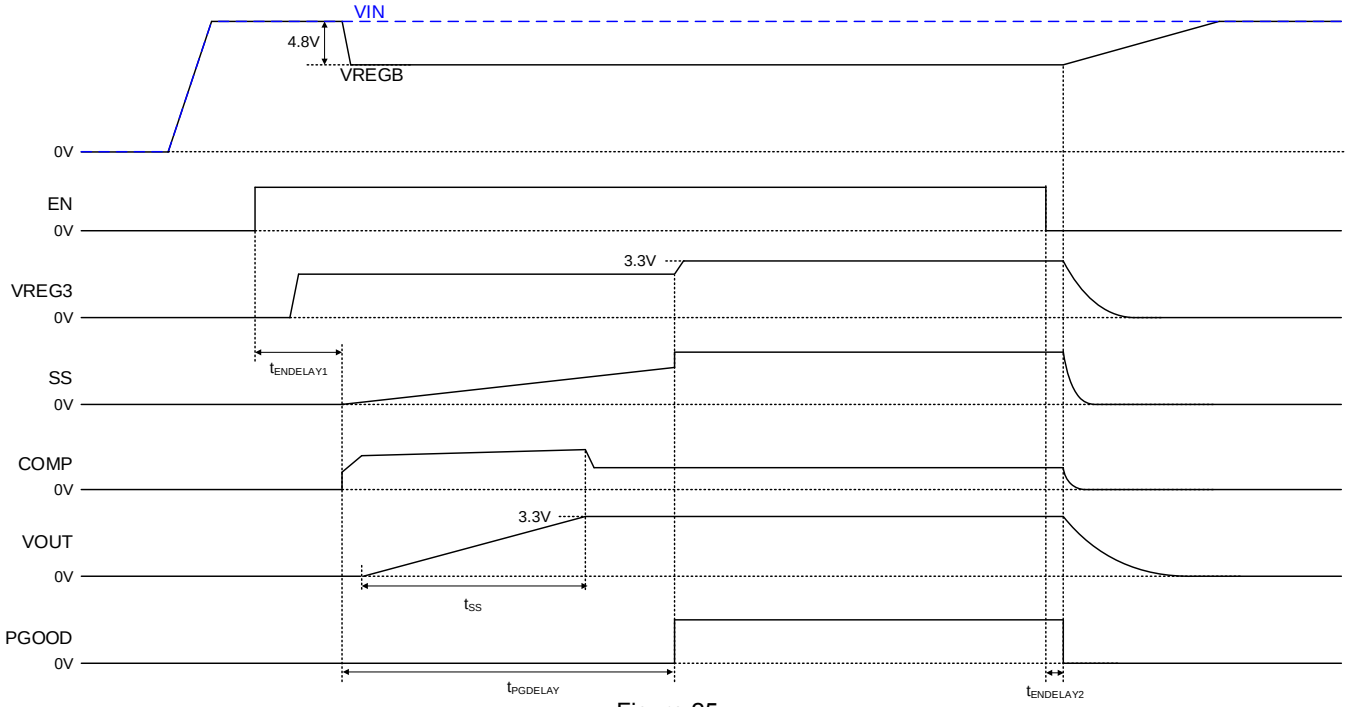


Figure 25

Typical timing characteristics
$t_{ENDELAY1}$: 165 µs (Typ)
$t_{ENDELAY2}$: 10 µs (Typ)

The soft start function is completed when the time $t_{PGDELAY}$ is passed after the time of $t_{ENDELAY1}$. $t_{PGDELAY}$ is about 1.5 times of t_{SS} (Refer to setting of soft start time on page 28) and obtained by the following equation.

$$t_{PGDELAY} = \frac{C_{SS}(nF)\times 1.2(V)}{I_{SS}(\mu A)} \text{ [ms]}$$

The power good output is available after the completion of this function.

2. LLM and Forced PWM mode

This device has two modes as shown in Table 1. These modes are controlled by the FPWM input.
The FPWM pin should not be allowed to float.

Table 1

FPWM INPUT	Mode name	Description
H : ≥ 2.5 V	Forced PWM (FPWM)	The device is locked in FPWM mode with a constant frequency and current mode synchronous converter for all loads.
L : ≤ 0.8 V	LLM	The device operates as LLM. The switching frequency depends on the load current state in LLM.

2. LLM and Forced PWM mode – continued

In FPWM mode, the device is locked in PWM mode. PWM control is maintained by allowing the inductor current to flow from the output to the IC even in no load. The switching frequency is constant in this mode, but reduces efficiency in the light load.

In PWM, the device operates as the current mode synchronous converter that adjusts the pulse width at a fixed cycle and controls the output voltage depending on the load current. This provides excellent line and load regulation and low output voltage ripple.

In LLM, the high side FET is turned on intermittently to supply energy to the load. The cycle is determined by the load current and the efficiency is increased by the diode emulation. This operation reduces the input current supplied for the output voltage regulation and provides a high efficiency. However, the output ripple voltage increases and switching cycle is not constant in LLM. Therefore, in LLM it may not get good EMI performance in AM band by the load condition. To avoid this, use FPWM mode.

LLM is available in frequency setting of 2.2 MHz or more (refer to Table 4 and Table 5 on page 26) and load current of less than 50 mA. If load current is 50 mA or more, turn the FPWM pin to H then apply the load. To disable FPWM, turn the FPWM pin to L after the load drops less than 50 mA (refer to Figure 26).

During soft start operation, the device is locked in FPWM mode. LLM is available after the completion of the soft start function.

When switching frequency setting is lower than 2.2 MHz, connect the FPWM pin to the VREG3 or the VOUT pin and use only FPWM mode.

Low pulse width for the FPWM input t_{PWL} should be more than following equation determined by the value of capacitance with output line C_O.

$$t_{PWL} > C_O(F) \times 2200 \text{ [s]}$$

C_O : Total value of capacitance with output line

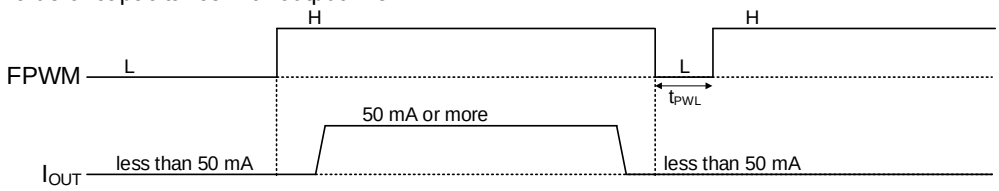


Figure 26

3. Spread Spectrum

This device has the function to spread spectrum on EMI performance. This function is enabled by the SPS input as shown in Table 2.

Table 2

SPS INPUT	SPS Mode	Description
≥ 2.5 V	Enable	The frequency decreases by 6.25 % (Typ) from the frequency set by the resistor connected to the RT pin. It spreads from -4% to + 4% (Typ) around the frequency of -6.25%.
≤ 0.8 V	Disable	The frequency is determined by the resistor connected to the RT pin.

The RT voltage changes as a triangular wave with a period of 22 µs. Therefore, the switching frequency ramps down 4 % and back to center frequency in 11 µs and also ramps up 4 % and back to center frequency in 11 µs. The cycle repeats.
A typical timing chart of input/output of this function is shown in Figure 27. SPS mode is available after the completion of the soft start function. The SPS pin can be connected to the VREG3 pin or the VOUT pin.

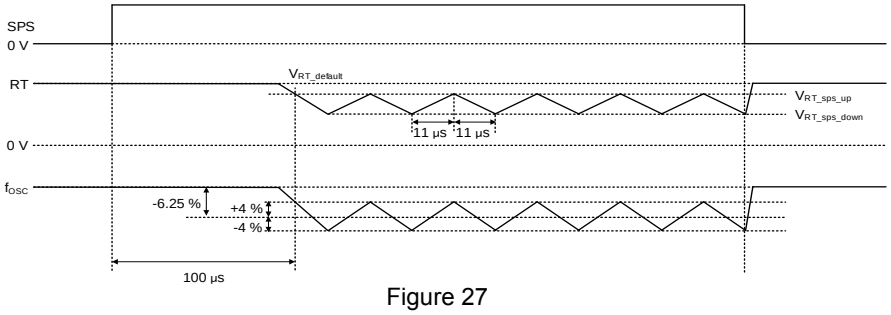


Figure 27

Function Explanations – continued

4. Synchronizing Input

This device has synchronizing function by PLL (Phase Locked Loop) using a clock input from the SYNC pin.

In order to activate the synchronizing function, set to the FPWM mode and then input a synchronizing signal from the SYNC pin. In LLM, input to the SYNC pin is ignored. If five positive edges are inputted and 128 times of cycle time passed, the device starts the synchronize function by PLL mode.
If input to the SYNC pin is fixed to Low or High state for four times of cycle time, PLL mode is disabled.

The “cycle time” in this function indicates the period determined by the R_{RT} connected to the RT pin.

The range of switching frequency of the external synchronization is limited within ±30 % of the switching frequency determined by the R_{RT}.

i.e. When R_{RT} is 300 kΩ (f_{OSC} = 290 kHz), the switching frequency range of the external synchronization is 203 kHz to 377 kHz.

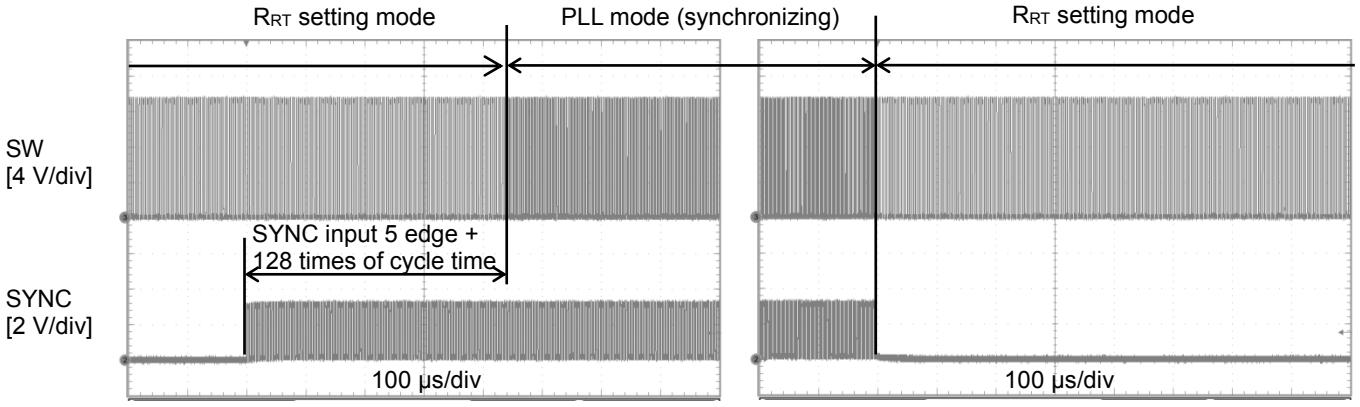


Figure 28. PLL OFF to ON waveform
(R_{RT} setting : 290 kHz, SYNC : 377 kHz)

Figure 29. PLL ON to OFF waveform
(R_{RT} setting : 290 kHz, SYNC : 377 kHz)

5. Power Good

This device has the function to watch the state of the output voltage. The PGOOD output consists of an open drain Nch FET. This output pin is required that an external pull-up resistor placed between this pin and either VOUT or VREG3 for a logic supply. When the VOUT voltage reaches to 95 % (Typ) or more of the regulating output voltage, Nch FET is turned off and the PGOOD indicates High state. When the VOUT voltage falls below 90 % (Typ), Nch FET is turned on and the PGOOD indicates Low state. This function is available after the completion of the soft start function.

Function Explanations – continued

6. Power supply from the output

This device has the function to supply power for the control circuits from the output through the VOUT pin. This function is available when PGOOD is detected after the completion of the soft start function. The current for the control of circuits is reduced by the ratio of V_O/VIN. It is helpful to improve the efficiency at light loads.

The difference of the current path at startup and the state after the soft start function is shown in Figure 30 and Figure 31.

At the startup, the power supply of VREG3 and PREREG comes from the VIN. After the completion of the soft start function and the detection of PGOOD, the almost power for control circuits is sourced through switches from the VOUT pin connected to V_O voltage.

At the startup

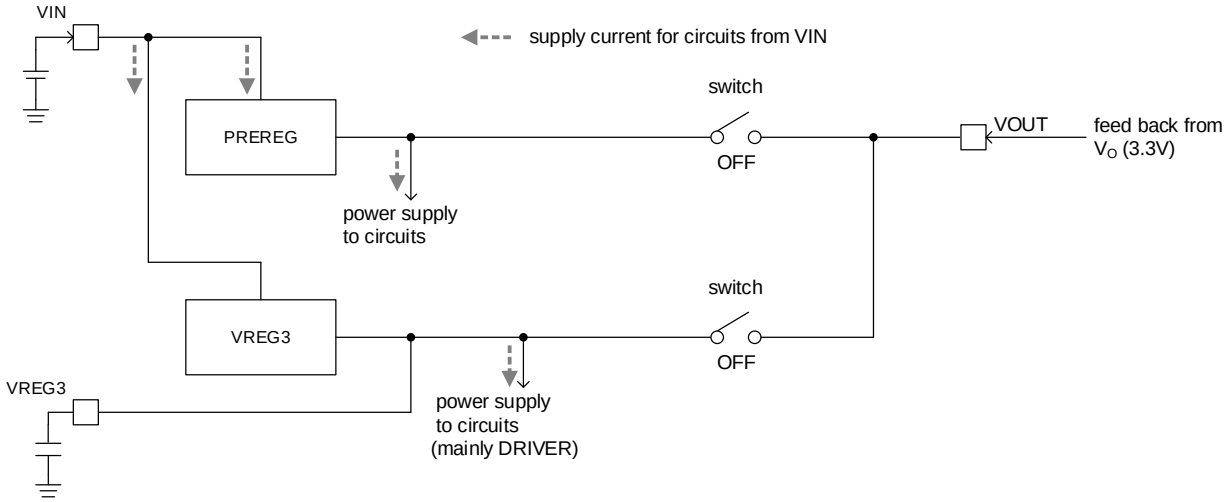


Figure 30

At the state after the soft start function

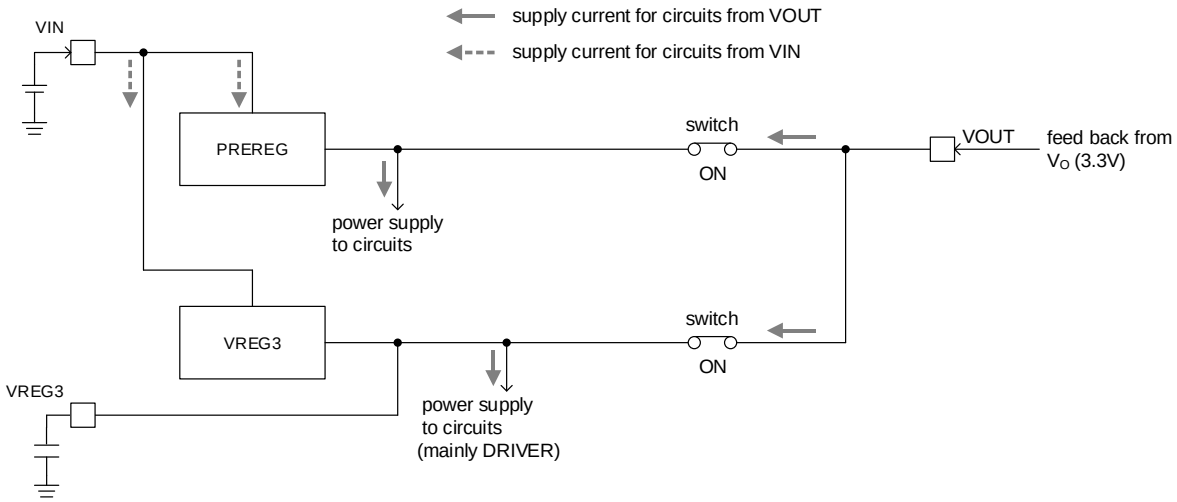


Figure 31

Protection

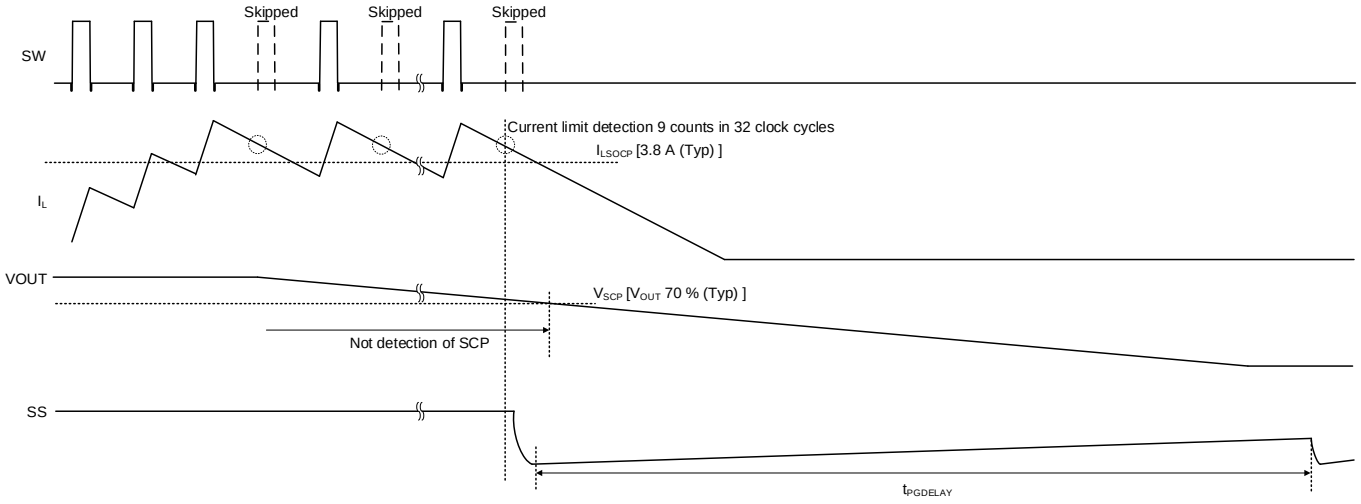
1. Over Current Protection (OCP) and Short Circuit Protection (SCP)

The device has valley current limit with low side FET and peak current limit with high side FET to detect the inductor current against over current load and output short circuit.

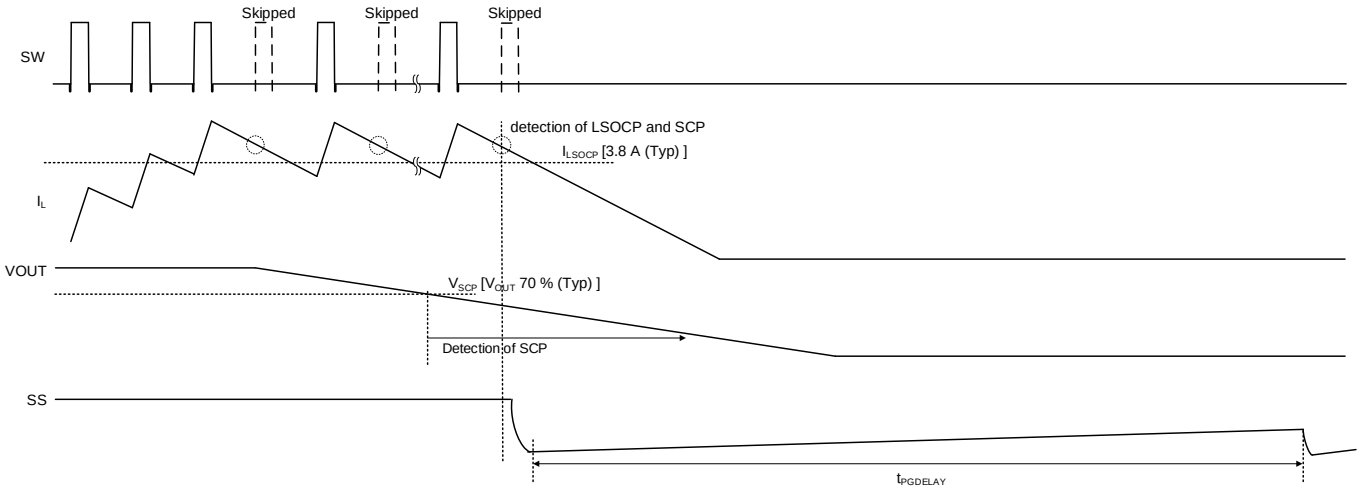
The inductor current decreases when the low side FET is turned on. If the inductor current does not drop below 3.8 A (Typ) before the next turn-on, the turn-on operation is skipped by the low side FET current limit. Then, the low side FET keeps on until the inductor current drops below 3.8 A (Typ).
If this situation is detected in 9 times during 32 switching cycles, the device turns off both high and low side FETs for the time that corresponds to 7 times of $t_{PGDELAY}$. It is called “HICCUP” action. After that, startup operation by soft-start function will be done. In addition, if the valley current limit is detected with the detection of SCP, the voltage of output drops under 70 %, the device also turns off both switches for the “HICCUP” time.
A timing chart about valley current limit and skip pulse is shown in Case1 and Case2.

When the peak inductor current reaches 5 A (Typ), the inductor current is limited by the high side FET. This limit is a cycle-by-cycle.
If this situation occurs 9 times during 32 clock cycles, the device turns off both switches as same as valley current limit for the “HICCUP” time. A timing chart about peak current limit is shown in Case3.
In addition, if the high side current limit is detected with the detection of SCP, the device also turns off both switches for the “HICCUP” time. A timing chart of typical short circuit transient is shown in Case4, and “HICCUP” time and recovery is shown in Case5.

Case1: Detecting valley current limit 9 times

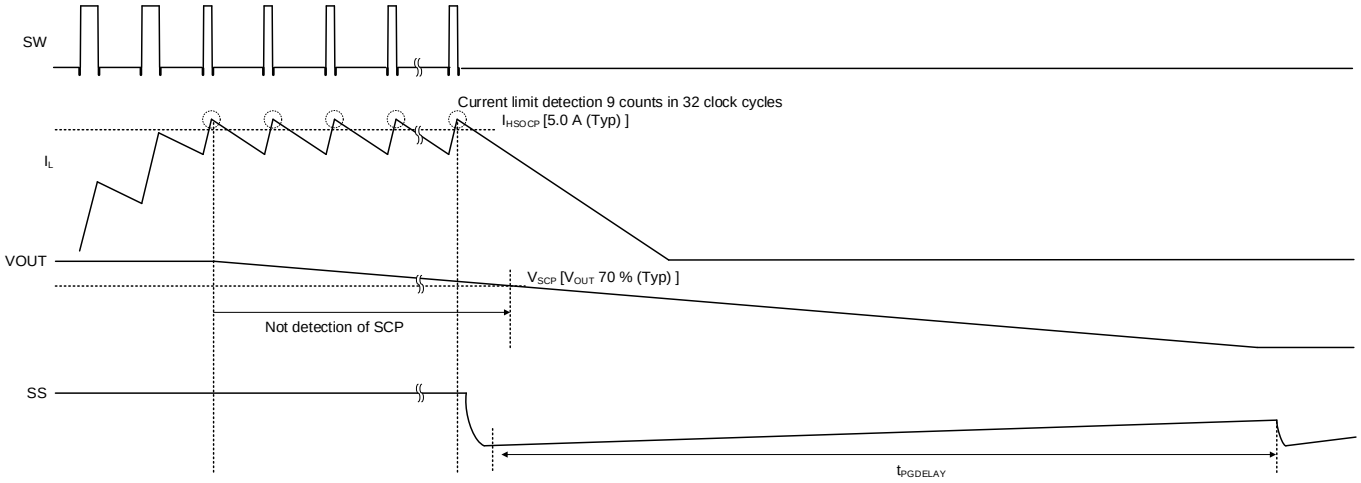


Case2: Detecting valley current limit when SCP is detected

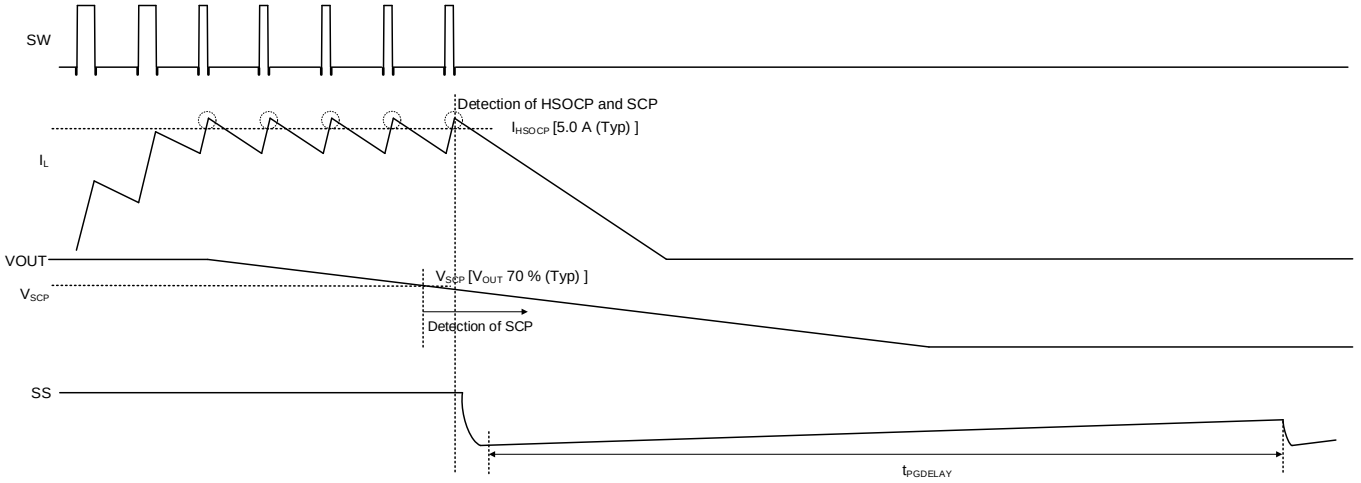


Protection – continued

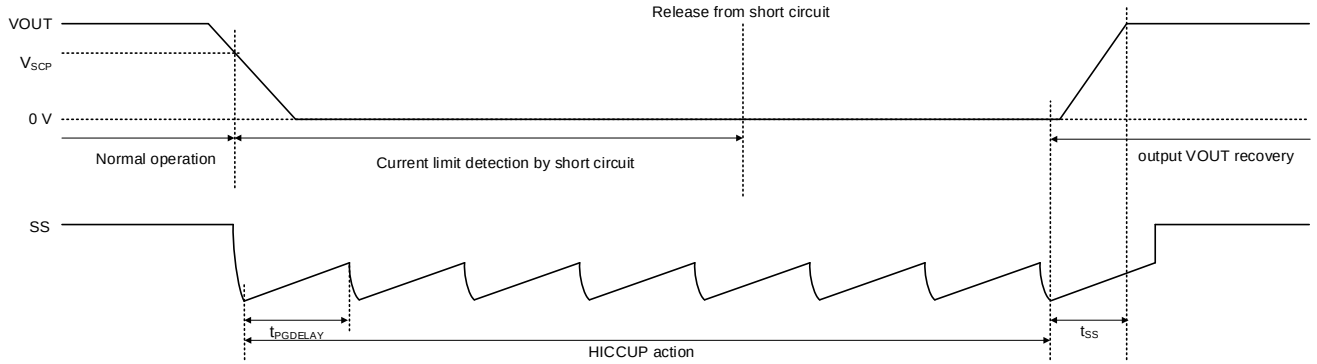
Case3: Detecting peak current limit 9 times



Case4: Detecting peak current limit when SCP is detected



Case5: “HICCUP” time and recovery



Protection – continued

2. Over Voltage Protection (OVP)

This device has the function to detect the over voltage of the VOUT.
This function compares internal node voltage divided VOUT voltage with the internal reference voltage. When the VOUT voltage goes 110 % (Typ) or more of the regulated output, High Side FET and Low Side FET turn off. When the VOUT voltage falls 105 % (Typ) or less, it returns to the normal operation.

3. Thermal Shutdown (TSD)

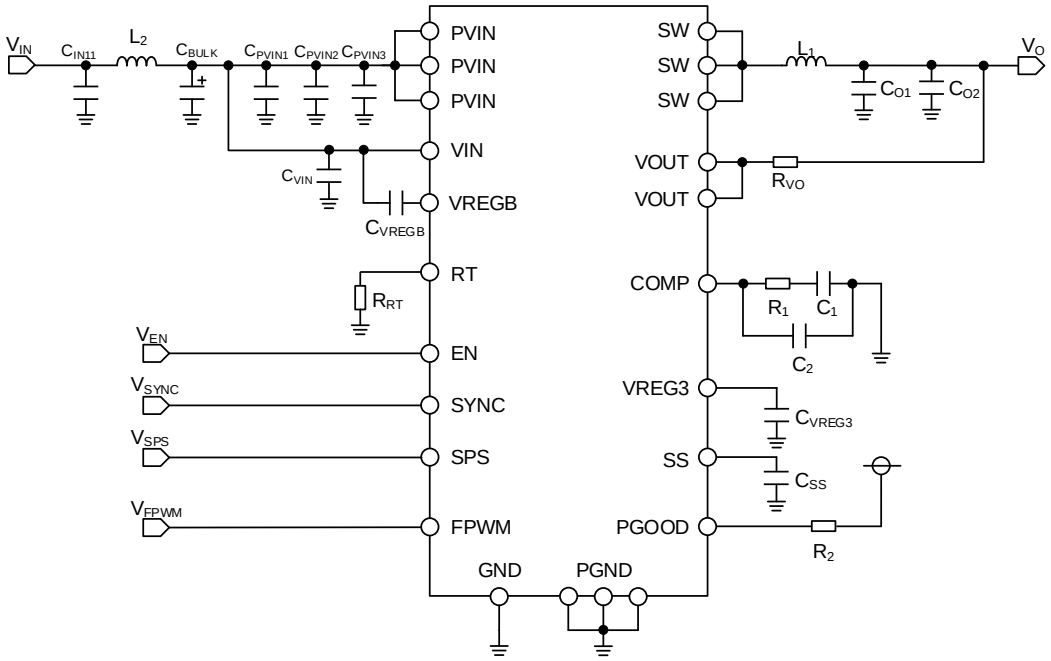
This device has the function to protect itself from excessive temperature.
Normal operation should always be within the IC's power dissipation rating. However, if the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit [Tj ≥ 175 °C (Typ)] that will turn OFF output FETs and VREG3 output. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

4. Under Voltage Lock-Out (UVLO)

This device has the function for an input under voltage lockout (UVLO).
The operation of this device is available when the VIN voltage rises 2.8 V (Typ) or more. When the VIN voltage falls below 2.5 V (Typ), the device is shut down. The threshold voltage has a hysteresis of 300 mV (Typ).

Application Example

The figure below is the application sample circuit.



Selection of Components Externally Connected

1. Selection of the inductor L_1 value

When the switching regulator supplies current continuously to the load, the LC filter is necessary for the smoothness of the output voltage. The Inductor ripple current ΔI_L that flows to the inductor becomes small when an inductor with a large inductance value is selected. Consequently, the voltage of the output ripple also becomes small. It is the trade-off between the size and the cost of the inductor.

The recommended inductance value of the inductor is shown in the following table:

Table 4

Frequency setting	L_1
200 kHz ≤ f_{OSC} < 1 MHz	6.8 µH to 10 µH
1 MHz ≤ f_{OSC} ≤ 2.4 MHz	2.2 µH to 6.8 µH

Maximum ΔI_L and ΔV_{PP} are shown in the following equation.

$$\Delta I_L = \frac{(V_{VIN(Max)} - VOUT) \times VOUT}{V_{VIN(Max)} \times f_{OSC} \times L_1} \quad [A]$$

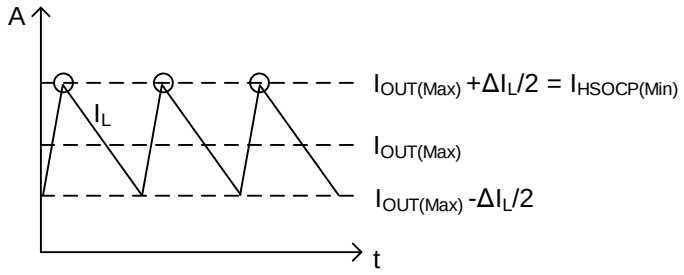
$$\Delta V_{PP} = \Delta I_L \times ESR + \frac{\Delta I_L}{8 \times C_O \times f_{OSC}} \quad [V] \quad \cdots\cdots (a)$$

Where:
$V_{VIN(Max)}$ is the maximum input voltage
ESR is the equivalent series resistance of output capacitor
C_O is the output capacitor

Generally, even if ΔI_L is somewhat large, the ΔV_{PP} target is satisfied because the ceramic capacitor has a very-low ESR. It also contributes to the miniaturization of the application board. Also, because of the lower rated current, smaller inductor is possible since the inductance is small. The disadvantages are increase in core losses in the inductor and the decrease in maximum output current. When other capacitors (electrolytic capacitor, tantalum capacitor, and electro conductive polymer etc.) are used for output capacitor C_O, check the ESR from the manufacturer's data sheet and determine the ΔI_L to fit within the acceptable range of ΔV_{PP}. Especially in the case of electrolytic capacitor, because the decrease in capacitance at low temperatures is significantly large, this will make ΔV_{PP} increase.
The maximum output electric current is limited to the overcurrent protection as shown in the following equation.

$$I_{OUT(Max)} = I_{HSOCP(Min)} - \frac{\Delta I_L}{2} \quad [A]$$

Where:
$I_{OUT(Max)}$ is the maximum output current
$I_{HSOCP(Min)}$ is the OCP operation current (Min)



Selection of Components Externally Connected – continued

2. Selection of output Capacitor C_O

The output capacitor is selected based on the ESR that is required from the equation (a).

$$Co > \frac{\Delta I_L}{8 \times f_{OSC} \times (\Delta V_{PP} - \Delta I_L \times ESR)} \quad [F]$$

ΔV_{PP} can be reduced by using a capacitor with a small ESR. The ceramic capacitor is the best option that meets this requirement. It is because not only does it has a small ESR but the ceramic capacitor also contributes to the size reduction of the application circuit. Please confirm the frequency characteristics of ESR from the datasheet of the manufacturer, and consider a low ESR value for the switching frequency being used. It is necessary to consider the ceramic capacitor because the DC biasing characteristic is important. For the voltage rating of the ceramic capacitor, twice or more than the maximum output voltage is usually required. By selecting a high voltage rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristics of X7R or better is recommended. Because the voltage rating of a large ceramic capacitor is low, the selection becomes difficult for an application with high output voltage. In that case, please connect multiple ceramic capacitors in series or select electrolytic capacitor. Consider having a voltage rating of 1.2 times or more of the output voltage when using electrolytic capacitor. Electrolytic capacitors have a high voltage rating, large capacitance, small amount of DC biasing characteristics, and are generally reasonable. Since the electrolytic capacitor is usually OPEN when it fails, it is effective to use for applications when reliability is required such as automotive. But there are disadvantages such as, ESR is relatively high, and decreases capacitance value at low temperatures. In this case, please take note that ΔV_{PP} may increase at low temperature conditions. Moreover, consider the lifetime characteristic of this capacitor because it has a possibility to dry up. A tantalum capacitor and a conductive polymer hybrid capacitor have excellent temperature characteristics unlike the electrolytic capacitor. Moreover, since their ESR is smaller than an electrolytic capacitor, the ripple voltage is relatively-small over a wide temperature range. Since these capacitors have almost no DC bias characteristics, design will be easier. Regarding voltage rating, the tantalum capacitor is selected such that its capacitance is twice the value of the output voltage, and for the conductive polymer hybrid capacitor, it is selected such that the voltage rating is 1.2 times the value of the output voltage. The disadvantage of a tantalum capacitor is that it is SHORTED when it is destroyed, and its breakdown voltage is low. It is not generally selected in an application that reliability is a demand such as in automotive. An electro conductive polymer hybrid capacitor is OPEN when destroyed. Though it is effective for reliability, its disadvantage is that it is generally expensive.
To improve the performance of ripple voltage in this condition, following is recommended:

1. Use low ESR capacitor like ceramic or conductive polymer hybrid capacitor.
2. Use a capacitor C_O with a higher capacitance value.

These capacitors are rated in ripple current. The RMS values of the ripple current that can be obtained in the following equation must not exceed the ripple current rating.

$$I_{CO(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \quad [A]$$

Where:
$I_{CO(RMS)}$ is the value of the ripple electric current

In addition, for the total value of capacitance in the output line C_O(Max), choose a capacitance value less than the value obtained by the following equation:

$$C_{O(Max)} < \frac{t_{SS(Min)} \times (I_{HSOCP(Min)} - I_{OSTART(Max)})}{V_O} \quad [F]$$

Where:
$I_{HSOCP(Min)}$ is the High side FET Current Protection (Min)
$t_{SS(Min)}$ is the Soft Start Time (Min)
$I_{OSTART(Max)}$ is the maximum output current during startup

Startup failure may happen if the limits from the above-mentioned are exceeded. Especially if the capacitance value is extremely large, over-current protection may be activated by the inrush current at startup preventing the output to turn on. Please confirm this on the actual application. For stable transient response, the loop is dependent to C_O. Please select after confirming the setting of the phase compensation circuit.
Also, in case of large changing input voltage and load current, select the capacitance accordingly by verifying that the actual application setup meets the required specification.

Also at low load conditions the output buffer capacitor is determining the output voltage ripple but via a different mechanism. Generally, this leads to a somewhat larger voltage ripple as in higher load conditions.

Selection of Components Externally Connected – continued

3. Selection of capacitor C_{VIN}/C_{PVIN2}/C_{PVIN3}/C_{BULK} input

The input capacitor is usually required for two types of decoupling capacitors C_{IN} and bulk capacitors C_{BULK}. At least three ceramic capacitors need for the decoupling capacitors. Ceramic capacitors with values of 4.7 µF or more for C_{PVIN2} and 0.1 µF or more for C_{PVIN3} are recommended for the PVIN pin. Ceramic capacitor with value of 0.1 µF or more for C_{VIN} is recommended for the VIN pin.
Ceramic capacitors are effective by being placed as close as possible to the PVIN pin and the VIN pin. Voltage rating is recommended to more than or equal to 1.2 times the maximum input voltage, or more than or equal to twice the normal input voltage. The C_{PVIN2} value including temperature change, DC bias change, and aging change must be larger than 2.5 µF. In addition, the IC might not function properly when the PCB layout or the position of the capacitor is not good. Check “Directions for Pattern Layout of PCB” on page 36.

The bulk capacitor is an option. The bulk capacitor prevents the decrease in the line voltage and serves a backup power supply to keep the input potential constant. The low ESR electrolytic capacitor with large capacity is suitable for the bulk capacitor. It is necessary to select the best capacitance value as per set of application. In that case, consider not to exceed the rated ripple current of the capacitor.

The RMS value of the input ripple current is obtained in the following equation.

$$I_{CIN} = \sqrt{D\left\{\frac{{\Delta I_L}^2}{12} + {I_{OUT}}^2(1-D)\right\}} \quad \text{[Arms]}$$

Where:
I_{CIN} is the Arms value of the input ripple
D is switching pulse ON Duty
I_{OUT} is the output current

In addition, in the automotive and other applications requiring high reliability, it is recommended that the multiple electrolytic capacitors are connected in parallel to avoid a dry up. In order to reduce a risk of destruction because of short in a ceramic capacitor, we recommend using 2 serials +2 parallel structure.
Since the lineup also of what packed 2 series and 2 parallel structure in 1package, respectively is carried out by each capacitor supplier, please confirm to each supplier.
When impedance on the input side is high because of wiring from the power supply to the PVIN pin and the VIN pin is long, etc., high capacitance is needed. In actual conditions, it is necessary to verify that there is no problem like IC operation is turned off or overshoot the output when the PVIN pin or the VIN pin voltage changes at transient response.

Selection of Components Externally Connected – continued

4. Selection of the switching frequency setting resistance R_{RT}

The internal switching frequency can be set by connecting a resistor between the RT pin and the GND pin.
Range of the setting is 200 kHz to 2400 kHz, and the relation between resistance and the switching frequency is decided as shown in Figure 32. Do not use a setting beyond this range.

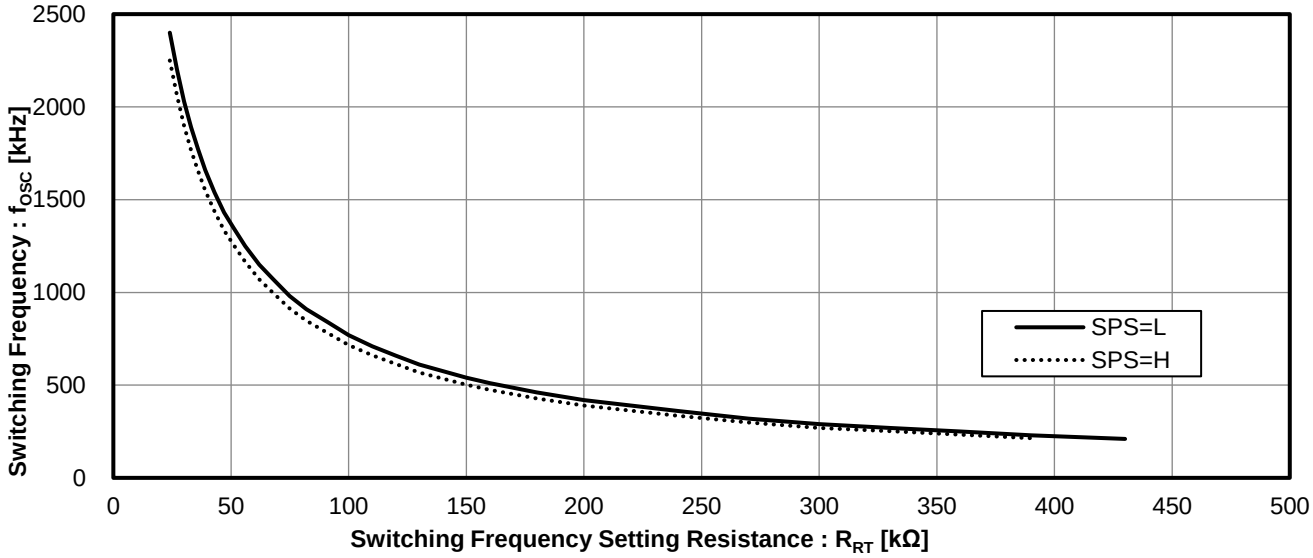


Figure 32. Switching Frequency vs Switching Frequency Setting Resistance

Table 4. Switching Frequency (SPS = L) Setting Resistance

R_{RT} [kΩ]	f_{OSC} [kHz] (SPS = L)	R_{RT} [kΩ]	f_{OSC} [kHz] (SPS = L)
24*(Note 1)*	2400	110*(Note 2)*	710
27*(Note 1)*	2200	120*(Note 2)*	660
30*(Note 2)*	2030	130*(Note 2)*	610
33*(Note 2)*	1890	150*(Note 2)*	540
36*(Note 2)*	1770	160*(Note 2)*	510
39*(Note 2)*	1660	180*(Note 2)*	460
43*(Note 2)*	1540	200*(Note 2)*	420
47*(Note 2)*	1430	220*(Note 2)*	390
51*(Note 2)*	1350	240*(Note 2)*	360
56*(Note 2)*	1250	270*(Note 2)*	320
62*(Note 2)*	1150	300*(Note 2)*	290
68*(Note 2)*	1070	330*(Note 2)*	270
75*(Note 2)*	980	360*(Note 2)*	250
82*(Note 2)*	910	390*(Note 2)*	230
91*(Note 2)*	840	430*(Note 2)*	210
100*(Note 2)*	770		

(Note 1) LLM (FPWM = L) and FPWM mode (FPWM = H) are available.
(Note 2) Only FPWM (FPWM = H) is available.

Table 5. Switching Frequency (SPS = H) Setting Resistance

R_{RT} [kΩ]	f_{OSC} [kHz] (SPS = H)	R_{RT} [kΩ]	f_{OSC} [kHz] (SPS = H)
24*(Note 1)*	2250	110*(Note 2)*	661
27*(Note 2)*	2060	120*(Note 2)*	614
30*(Note 2)*	1898	130*(Note 2)*	568
33*(Note 2)*	1766	150*(Note 2)*	502
36*(Note 2)*	1653	160*(Note 2)*	475
39*(Note 2)*	1550	180*(Note 2)*	428
43*(Note 2)*	1437	200*(Note 2)*	391
47*(Note 2)*	1333	220*(Note 2)*	363
51*(Note 2)*	1258	240*(Note 2)*	335
56*(Note 2)*	1164	270*(Note 2)*	298
62*(Note 2)*	1071	300*(Note 2)*	270
68*(Note 2)*	996	330*(Note 2)*	251
75*(Note 2)*	912	360*(Note 2)*	233
82*(Note 2)*	847	390*(Note 2)*	214
91*(Note 2)*	782		
100*(Note 2)*	717		

(Note 1) LLM (FPWM = L) and FPWM mode (FPWM = H) are available.
(Note 2) Only FPWM (FPWM = H) is available.

Selection of Components Externally Connected – continued

5. Selection of the phase compensation circuit R_1, C_1, C_2

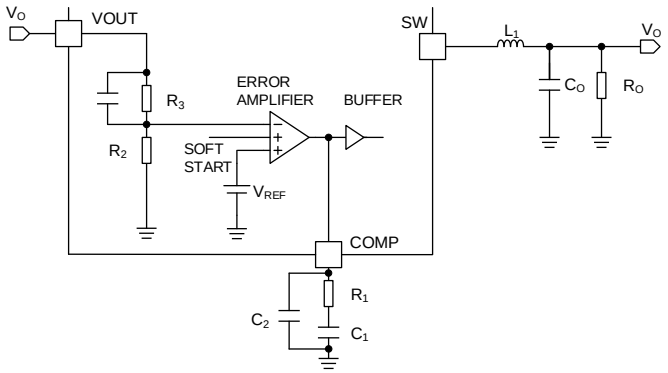


Figure 33. Setting Phase Compensation Circuit

The cross over frequency f_C (frequency at 0 dB gain) should be set lower than the frequency f_{C_MAX} shown in Figure 34.

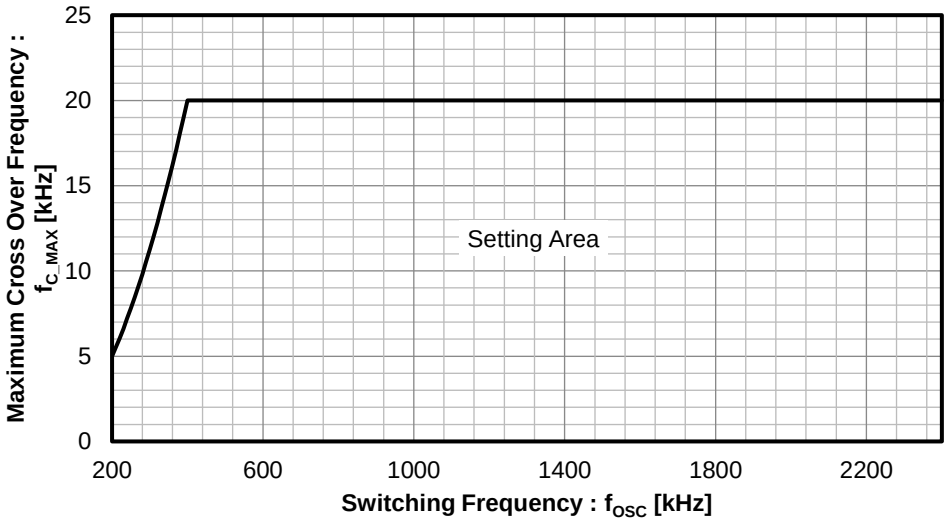


Figure 34. Maximum Cross Over Frequency vs Switching Frequency

(1) Selection of the phase compensation setting resistance R_1
R_1 is determined in the following equation.

$$R_1 = f_C \times \frac{R_2+R_3}{g_m \times R_2} \times 2\pi \times R_s \times Co \qquad [\Omega]$$

Where:

f_C is the Crossover Frequency [kHz].

$\frac{R_2+R_3}{R_2}$ is the Feedback Resistance 4.125 (Typ)

R_S is the current sense Gain 230 [mΩ] (Typ)

g_m is the Error Amplifier Trans conductance 280 [μA/V] (Typ) x Buffer Voltage Gain 2.0 [V/V] (Typ)

C_o is the output capacitor [μF]

Selection of Components Externally Connected – continued

(2) Selection of the phase compensation setting capacitor C_1

To select the compensation capacitor C_1, set the zero frequency created by R_1 and C_1.
This zero frequency is determined in the following equation.

$$f_Z = \frac{1}{2\pi \times C_1 \times R_1} \quad [\text{Hz}]$$

Set f_Z to the frequency between 0.05 times and 1.5 times of crossover frequency f_C, as the following equation.

$$0.05 \times f_C < f_Z < 1.5 \times f_C \ [\text{Hz}]$$

Therefore, C_1 is determined in the following equation.

$$\frac{1}{2\pi \times 1.5 \times f_C \times R_1} < C_1 < \frac{1}{2\pi \times 0.05 \times f_C \times R_1} \ [\text{F}]$$

(3) Selection of the phase compensation setting capacitor C_2

C_2 and R_1 form the pole f_P. Set the f_P much higher than f_C for decreasing gain at high frequency.
C_2 is determined in the following equation.

$$C_2 = \frac{1}{2\pi \times R_1 \times f_p} \quad [\text{F}]$$

6. Setting of soft start time (t_{SS})

The soft start function is necessary to prevent inrush of the inductor current and the output voltage overshoot at startup. This IC has an internal pull-up current source of I_{SS} that charges the external soft start capacitor. The soft start time can be calculated by using the equation.

$$t_{SS} = \frac{C_{SS}(nF) \times 0.8(V)}{I_{SS}(\mu A)} \ [\text{ms}]$$

Where:
C_{SS} is the capacitor connected to the SS pin.
I_{SS} is soft start charge current.

C_{SS} can be set between 2200 pF and 68000 pF.

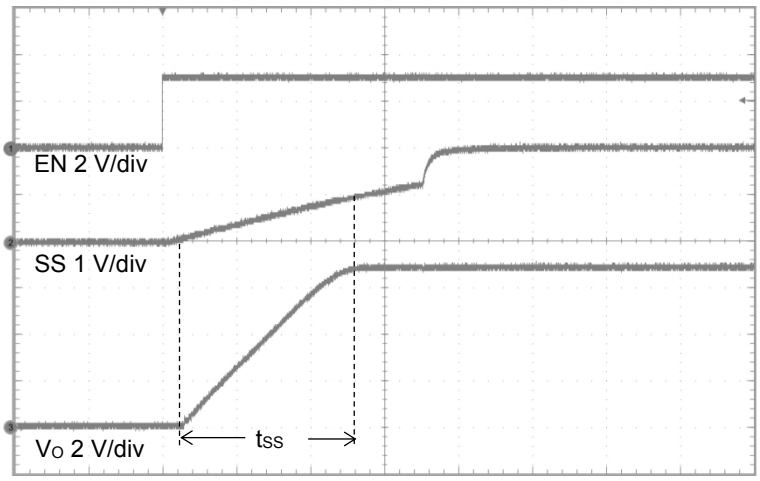
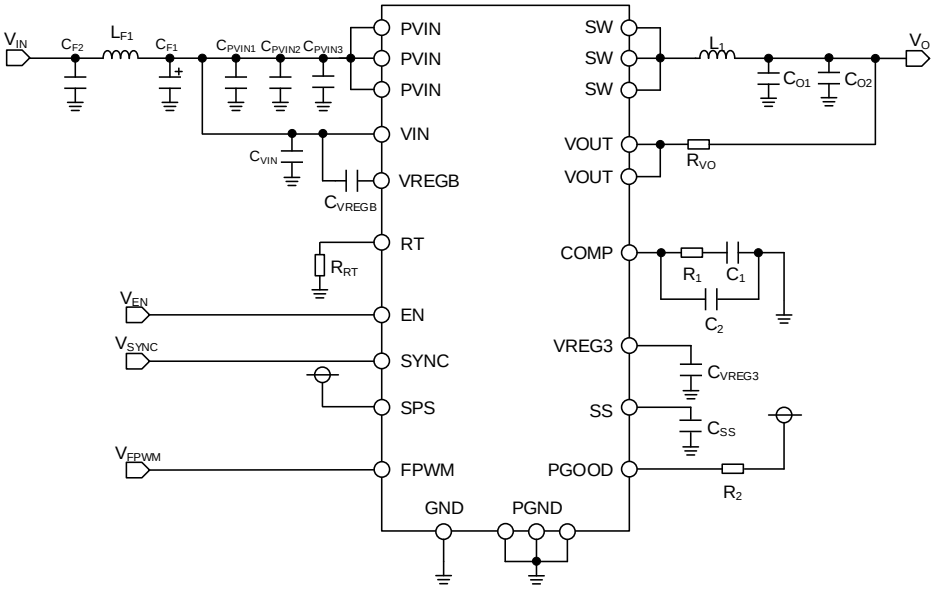


Figure 35. Soft start waveform
(V_{VIN} = 13 V, C_{SS} = 0.01 µF, 2 ms/div)

Application Example1

Parameter	Symbol	Specification case
Product Name	IC	BD9P233MUF-C
Input Voltage	V_{VIN}	8 V to 18 V
Output Voltage	V_O	3.3 V
Output Current	I_{OUT}	Min 0.5 A/Typ 1.0 A/Max 1.5 A
Switching Frequency	f_{OSC}	2.2 MHz, SPS = H
Ambient Temperature	Ta	-40 °C to +105 °C

Specification Example



Reference Circuit

No.	Size	Parameters	Part name (series)	Type	Manufacturer
C_{F1}	ϕ10 mm x L10 mm	220 µF, 50 V	UCD1H221MNL1GS	Electrolytic capacitor	NICHICON
C_{PVIN1}	3225	Open	-	-	-
C_{PVIN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475KA	Ceramic	MURATA
C_{PVIN3}	2012	0.1 µF, X7R, 50 V	CEU4J2X7R1H104K	Ceramic	TDK
C_{VIN}	2012	0.1 µF, X7R, 50 V	CEU4J2X7R1H104K	Ceramic	TDK
C_{VREGB}	1608	1.0 µF, X7R ,16 V	GCM188R71C105KA	Ceramic	MURATA
C_{VREG3}	1608	1.0 µF, X7R ,16 V	GCM188R71C105KA	Ceramic	MURATA
R_1	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip resistor	ROHM
C_1	1005	0.01 µF, R, 50 V	GCM155R11H103KA	Ceramic	MURATA
C_2	1005	10 pF, CH, 50 V	GCM1552C1H100JA	Ceramic	MURATA
C_{SS}	1005	2200 pF, R, 50 V	GCM155R11H222KA	Ceramic	MURATA
R_2	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip resister	ROHM
R_{RT}	1005	24 kΩ, 1 %, 1/16 W	MCR01MZPF2402	Chip resister	ROHM
L_1	W6.0 x H4.5 x L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK
C_{O1}	3225	22 µF, R, 10 V	GCM32ER11A226KE11	Ceramic	MURATA
C_{O2}	3225	22 µF, R, 10 V	GCM32ER11A226KE11	Ceramic	MURATA
R_{VO}	-	Short	-	-	-
C_{F2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475KA	Ceramic	MURATA
L_{F1}	W6.0 x H4.5 x L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK

Parts List

Characteristic Data (Application Example1)

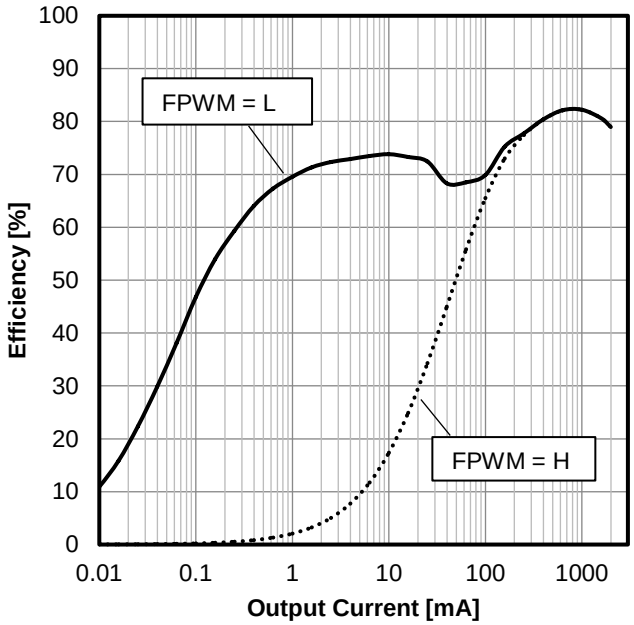


Figure 36. Efficiency vs Output Current
(V_{VIN} = 13 V, Ta = 25 °C)

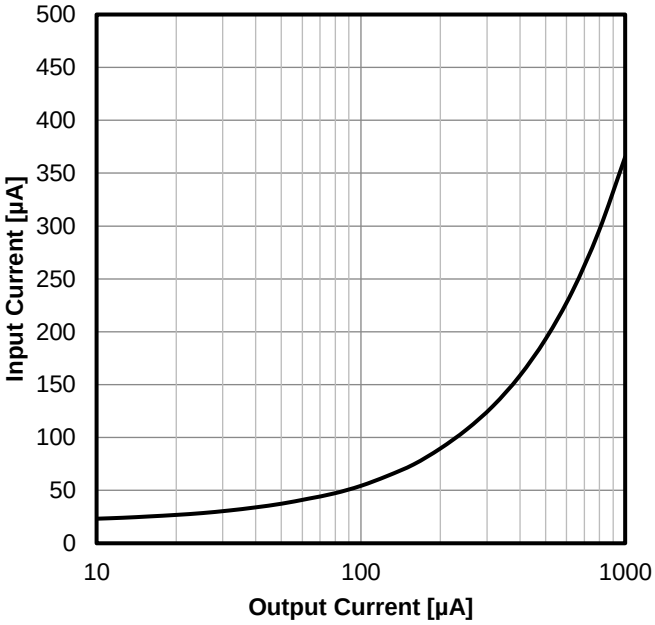


Figure 37. Input Current vs Output Current
(V_{VIN} = 13 V, Ta = 25 °C, LLM)

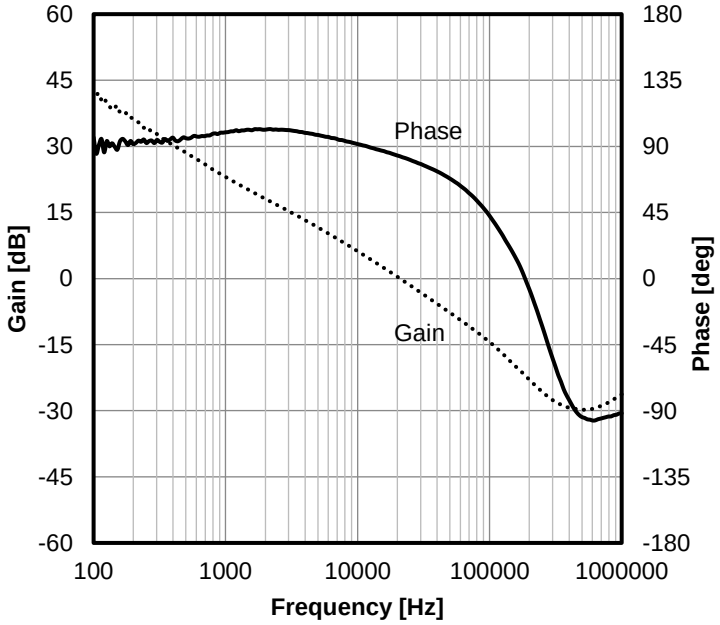


Figure 38. Frequency Characteristic
(V_{VIN} = 13 V, Ta = 25 °C, I_{OUT} = 1.0 A)

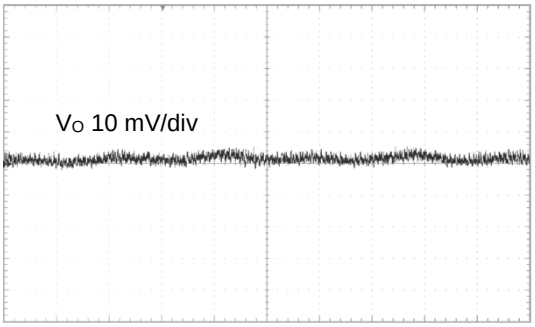


Figure 39. Output Ripple Voltage
(V_{VIN} = 13 V, Ta = 25 °C, I_{OUT} = 1.0 A, 10 µs/div)

Characteristic Data (Application Example1) - continued

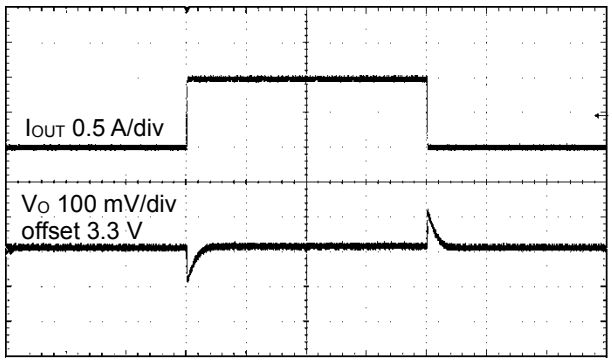


Figure 40. Load Response 1
(V_{VIN} = 13 V, Ta = 25 °C, FPWM = H,
I_{OUT} = 10 mA to 1.0 A, 1 ms/div)

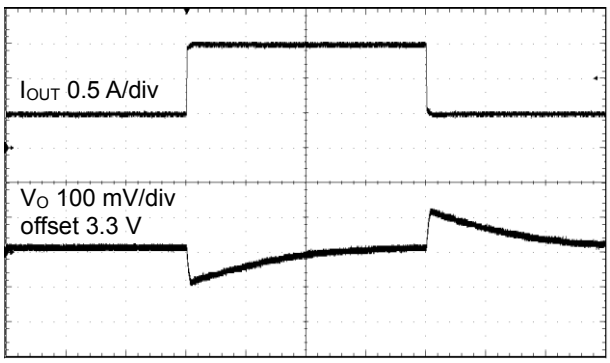


Figure 41. Load Response 2
(V_{VIN} = 13 V, Ta = 25 °C, FPWM = H,
I_{OUT} = 0.5 A to 1.5 A, 100 µs/div)

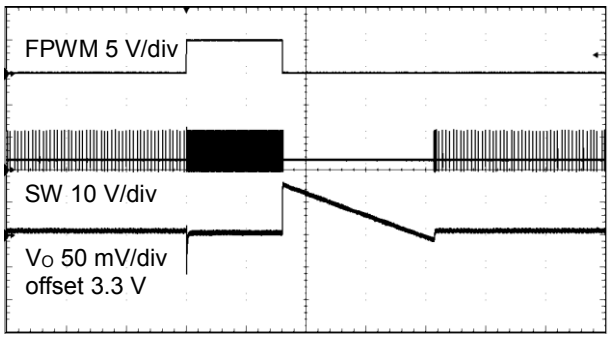
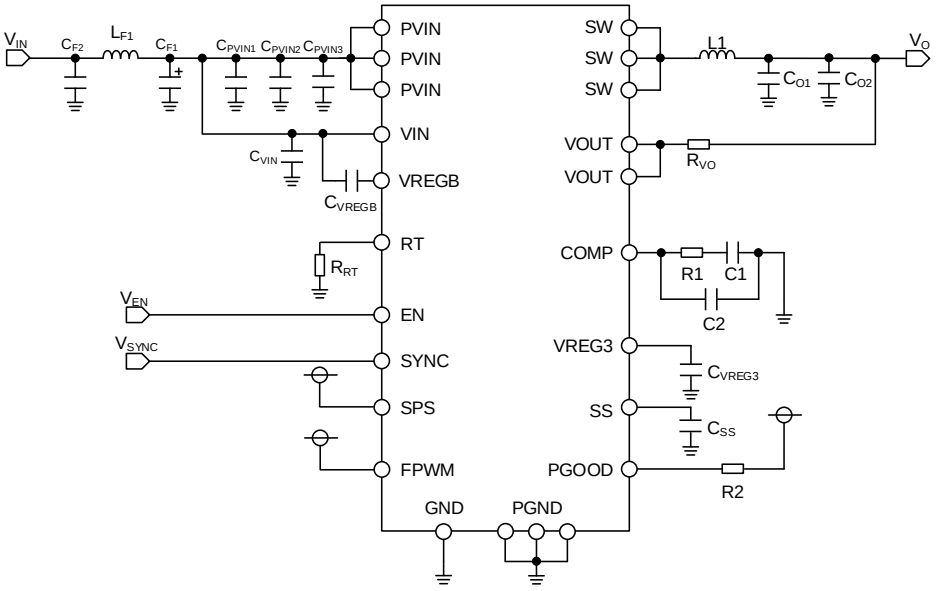


Figure 42. FPWM ON/OFF Response
(V_{VIN} = 13 V, Ta = 25 °C, I_{OUT} = 100 µA, 10 ms/div)

Application Example2

Parameter	Symbol	Specification case
Product Name	IC	BD9P233MUF-C
Input Voltage	V_{VIN}	8 V to 18 V
Output Voltage	V_O	3.3 V
Output Current	I_{OUT}	Min 0.5 A/Typ 1.0 A/Max 1.5 A
Switching Frequency	f_{OSC}	391 kHz, SPS = H, FPWM = H
Ambient Temperature	Ta	-40 °C to +105 °C

Specification Example



Reference Circuit

No.	Size	Parameters	Part name (series)	Type	Manufacturer
C_{F1}	ϕ10 mm x L10 mm	220 µF, 50 V	UCD1H221MNL1GS	Electrolytic capacitor	NICHICON
C_{PVIN1}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475KA	Ceramic	MURATA
C_{PVIN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475KA	Ceramic	MURATA
C_{PVIN3}	2012	0.1 µF, X7R, 50 V	CEU4J2X7R1H104K	Ceramic	TDK
C_{VIN}	2012	0.1 µF, X7R, 50 V	CEU4J2X7R1H104K	Ceramic	TDK
C_{VREGB}	1608	1.0 µF, X7R ,16 V	GCM188R71C105KA	Ceramic	MURATA
C_{VREG3}	1608	1.0 µF, X7R ,16 V	GCM188R71C105KA	Ceramic	MURATA
R_1	1005	4.7 kΩ, 1 %, 1/16 W	MCR01MZPF4701	Chip resistor	ROHM
C_1	1005	0.01 µF, R, 50 V	GCM155R11H103KA	Ceramic	MURATA
C_2	1005	100 pF, CH, 50 V	GCM1552C1H101JA	Ceramic	MURATA
C_{SS}	1005	2200 pF, R, 50 V	GCM155R11H222KA	Ceramic	MURATA
R_2	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip resister	ROHM
R_{RT}	1005	200 kΩ, 1 %, 1/16 W	MCR01MZPF2003	Chip resister	ROHM
L_1	W6.0 x H4.5 x L6.3 mm^3	6.8 µH	CLF6045NIT-6R8N-D	Inductor	TDK
C_{O1}	3225	22 µF, R, 10 V	GCM32ER11A226KE11	Ceramic	MURATA
C_{O2}	3225	22 µF, R, 10 V	GCM32ER11A226KE11	Ceramic	MURATA
R_{VO}	-	Short	-	-	-
C_{F2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475KA	Ceramic	MURATA
L_{F1}	W6.0 x H4.5 x L6.3 mm^3	10 µH	CLF6045NIT-100M-D	Inductor	TDK

Parts List

Characteristic Data (Application Example2)

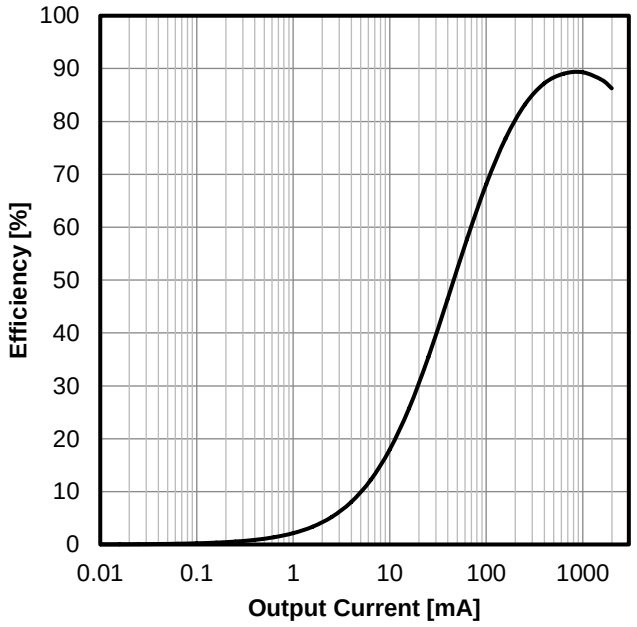


Figure 43. Efficiency vs Output Current
(V_{VIN} = 13 V, Ta = 25 °C, FPWM = H)

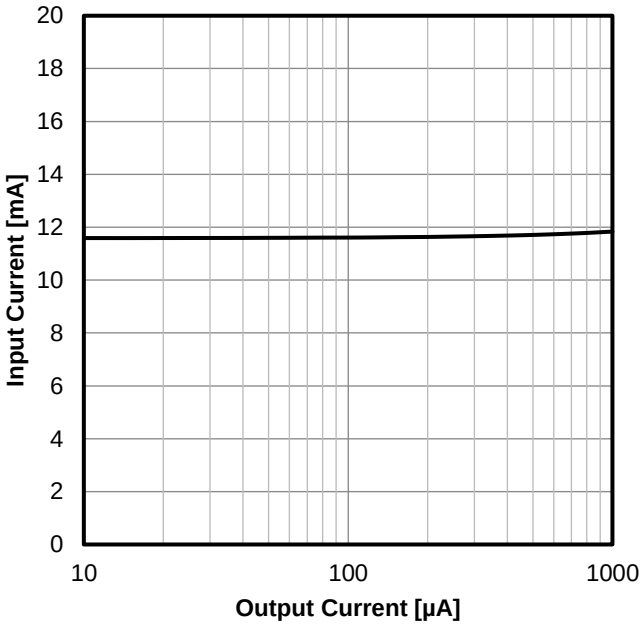


Figure 44. Input Current vs Output Current
(V_{VIN} = 13 V, Ta = 25 °C, FPWM = H)

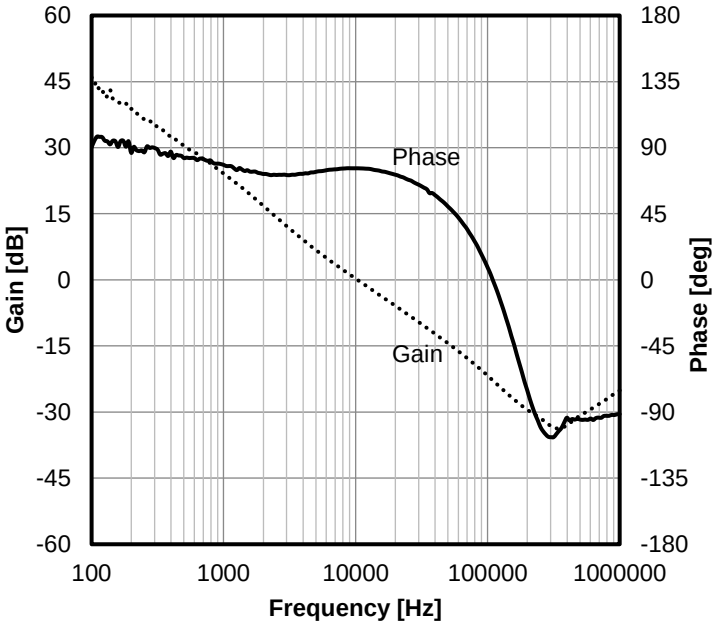


Figure 45. Frequency Characteristic
(V_{VIN} = 13 V, Ta = 25 °C, I_{OUT} = 1.0 A)

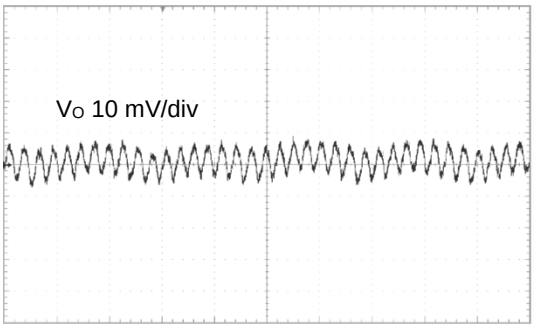


Figure 46. Output Ripple Voltage
(V_{VIN} = 13 V, Ta = 25 °C, I_{OUT} = 1.0 A, 10 µs/div)

Characteristic Data (Application Example2) - continued

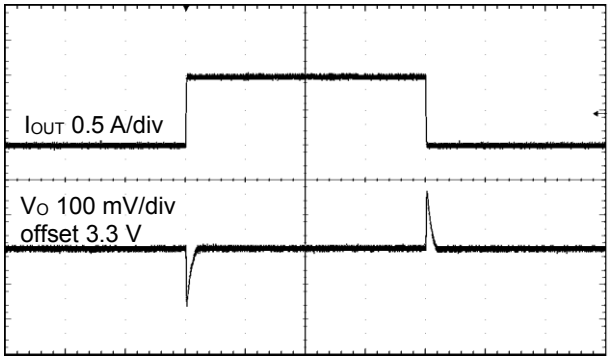


Figure 47. Load Response 1
(V_{VIN} = 13 V, Ta = 25 °C, FPWM = H,
I_{OUT} = 10 mA to 1.0 A, 1 ms/div)

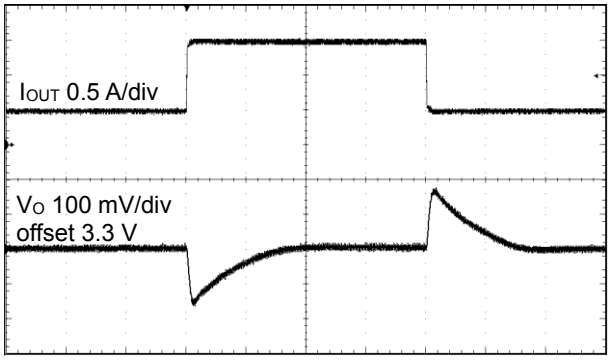


Figure 48. Load Response 2
(V_{VIN} = 13 V, Ta = 25 °C, FPWM = H,
I_{OUT} = 0.5 A to 1.5 A, 100 µs/div)

Automotive Power Supply Line Circuit

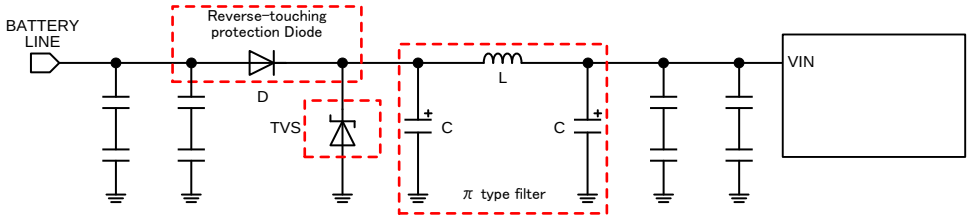


Figure 49. Automotive Power Supply Line Circuit

As a reference, the automotive power supply line circuit example is given in Figure 49.
π-type filter is a third-order LC filter. In general, it is used in combination with decoupling capacitors for high frequency. Large attenuation characteristics can be obtained and thus excellent characteristic as a EMI filter. Devices used for π-type filters should be placed close to each other.
TVS (Transient Voltage Suppressors) is used for primary protection of the automotive power supply line. Since it is necessary to withstand high energy of load dump surge, a general zener diode is insufficient. Recommended device is shown in the following table.
In addition, a reverse polarity protection diode is needed considering if a power supply such as battery is accidentally connected in the opposite direction.

Device	Part name (series)	Manufacturer	Device	Part name (series)	Manufacturer
L	CLF series	TDK	TVS	SM8 series	Vishay
L	XAL series	Coilcraft	D	S3A to S3M series	Vishay
C	UCJ series / UCZ series	NICHICON			

Parts of Automotive Power Supply Line Circuit

Recommended Parts Manufacturer List

Shown below is the list of the recommended parts manufacturers for reference.

Type	Manufacturer	URL
Electrolytic capacitor	NICHICON	www.nichicon.com
Ceramic capacitor	Murata	www.murata.com
Ceramic capacitor Inductor	TDK	www.global.tdk.com
Inductor	Coilcraft	www.coilcraft.com
Inductor	SUMIDA	www.sumida.com
Diode	Vishay	www.vishay.com
Diode/Resistor	ROHM	www.rohm.com

Directions for Pattern Layout of PCB

The PCB layout greatly influences the stable operation of the IC. Depending on the PCB layout, IC might not show its original characteristics or might not function properly. Note the following points when creation the PCB layout. Moreover, Figure 51 on page 37 shows the recommended layout pattern and component placement. 4 layers PCB is recommended for this IC.

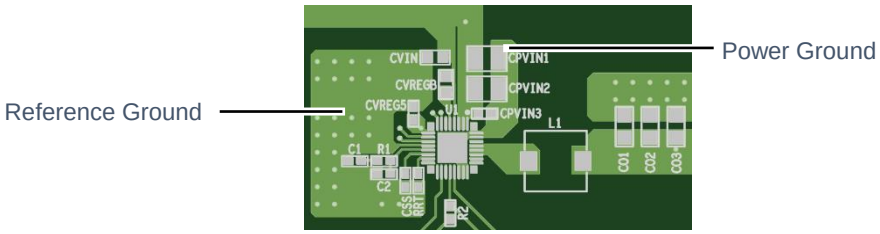


Figure 50. PCB pattern around IC

1. 4.7 µF (C_{PVIN2}) and 0.1 µF (C_{PVIN3}) decoupling capacitors should be placed closest to the PVIN pins (pin1, 2, 3) and the PGND pins (pin 22, 23, 24). As shown in the recommended layout example, both decoupling capacitors are placed closest to the PVIN pins, the shortest wiring distance to the PGND pins can be drawn by routing it to the back side of the IC via EXP-PAD (pin 31) and N.C. pin (pin 32). In addition, placing a capacitor CPVIN3 which is smaller than 4.7 µF (CPVIN2) close to the PVIN pin results in minimizing the high-frequency noise.

2. Make a slit between the PVIN pin and the VIN pin (pin 4). As the VIN pin is a power supply to the internal circuit, it needs a stable supply voltage. By making a slit, it minimizes the influence of the spike generated at the PVIN pins to the VIN pin directly. 0.1 µF decoupling capacitor of the VIN pin should be placed within the slit as shown in the recommended layout example and should be connected to the reference ground.

3. The IC, the input capacitor, the inductor and the output capacitor should be placed on the same side of the board and the connection of each part should be made on the same layer.

4. Place the ground plane in a layer closest to the surface layer where the IC is mounted.

5. The GND pin (pin 12) is the reference ground and the PGND pins are the power ground. A stable ground inside the IC can be obtained by separating these pins on the surface layer. Therefore, the GND pin should be separated from the ground line of the IC backside.

6. Separate the reference ground and the power ground on the surface layer and connect them to ground plane through VIA. Each ground connection can be summarized as follows.
   · Reference ground : the GND pin, ground of CVIN, CVREG3, C1, C2, CSS, RRT
   · Power ground : the PGND pin, center EXP-PAD, pin 31 (EXP-PAD), pin 32 (N.C. pin), ground of input decoupling capacitor (CPVIN1 to 3)

7. To minimize the emission noise from switching node, the distance between the SW pin to inductor should be as short as possible and not to expand the copper area more than necessary.

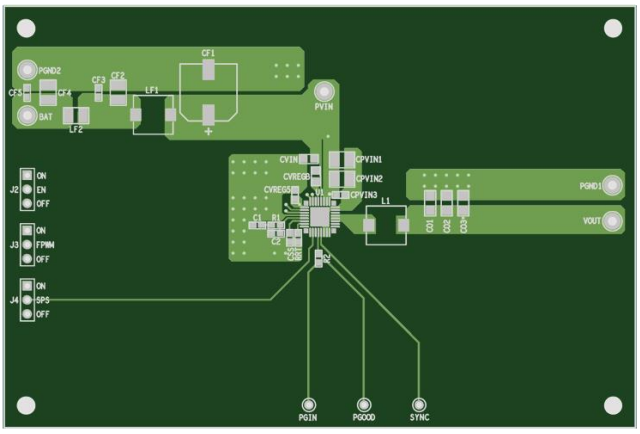
8. Make the feedback line from the output away from the inductor and the switching node. If this line is affected by external noise, an error may be occurred in the output voltage or the control may become unstable. Therefore, move the feedback line to back side layer of the board through VIA and directly connect it to the VOUT pins (pin 10, 11). The frequency characteristics (phase margin) can be measured by inserting a resistor at the location of RVO (refer to Bottom view) and using FRA. However, do not insert any components on feedback line during normal operation.

9. Connect phase compensation circuit (R1, C1 and C2) as close as possible to the COMP pin (pin 13).

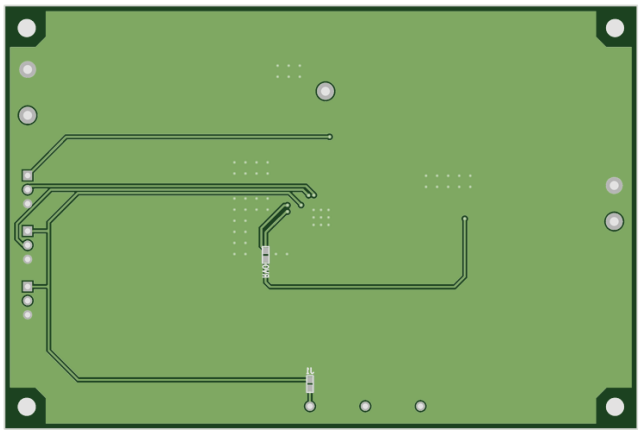
10. Connect CSS as close as possible to the SS pin (pin 14).

11. Connect RRT as close as possible to the RT pin (pin 15).

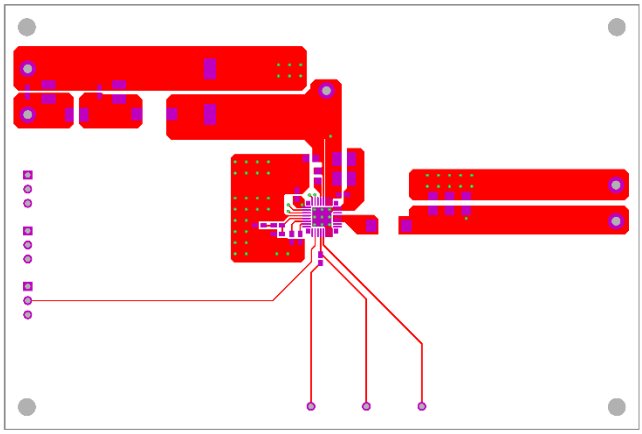
Directions for Pattern Layout of PCB – continued



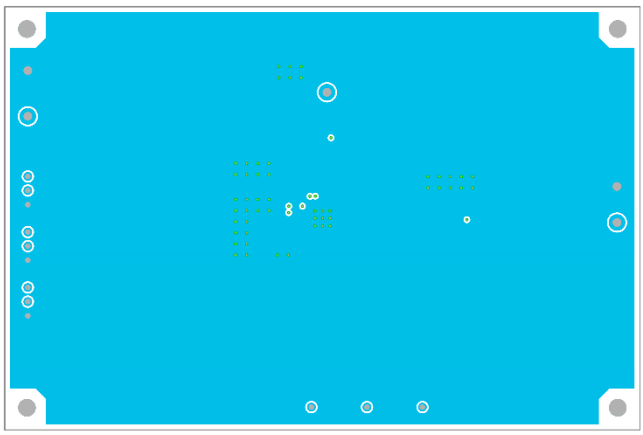
Top view



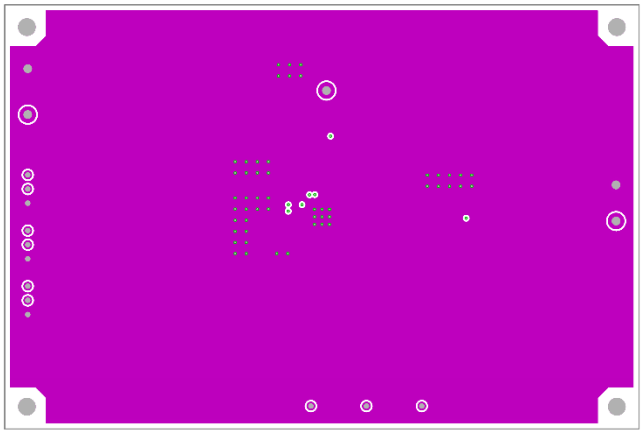
Bottom view



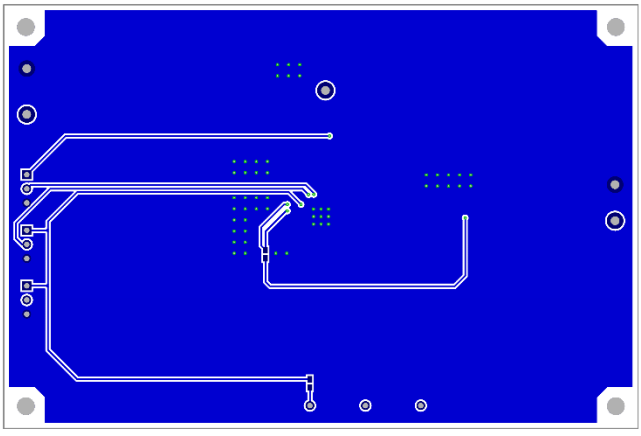
Top layer



Middle layer1



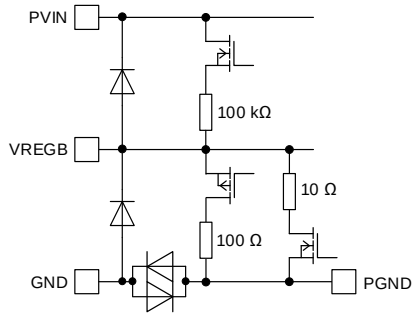
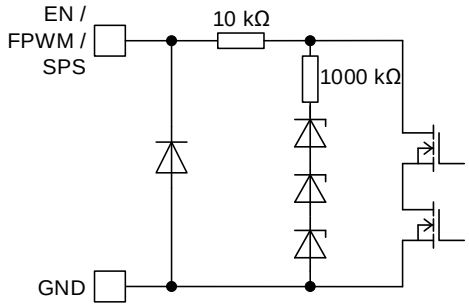
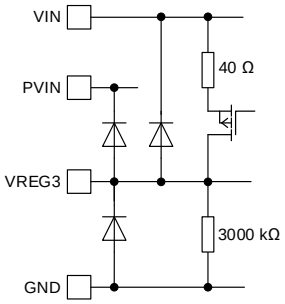
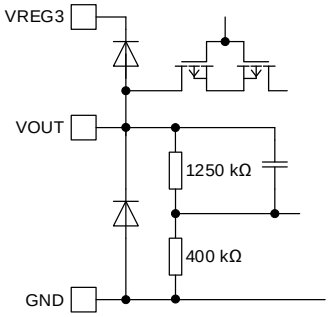
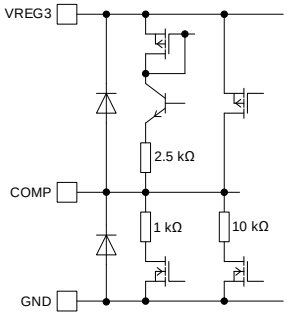
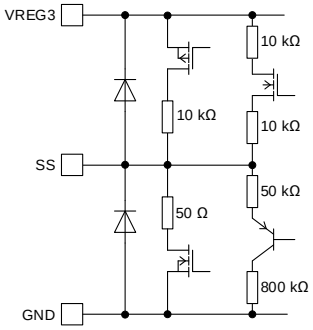
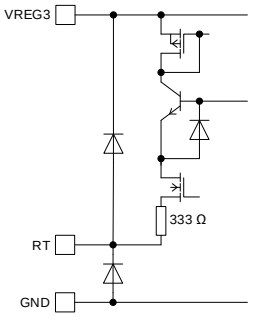
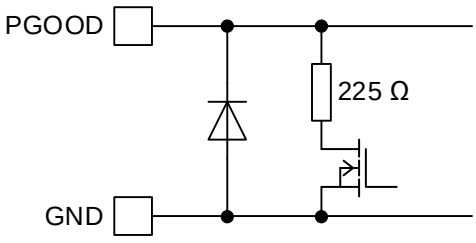
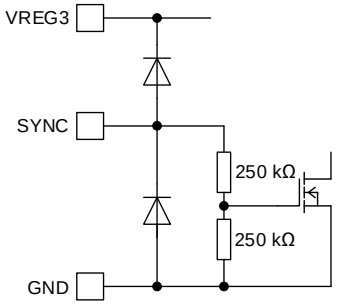
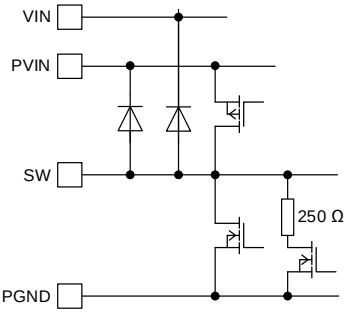
Middle layer2



Bottom layer

Figure 51. Reference PCB pattern

I/O Equivalence Circuit

5. VREGB	7. EN, 8. FPWM, 18. SPS
	
9. VREG3	**10. 11. VOUT**
	
13. COMP	**14. SS**
	
15. RT	**20. PGOOD**
	
21. SYNC	**27. 28. 29. SW**
	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

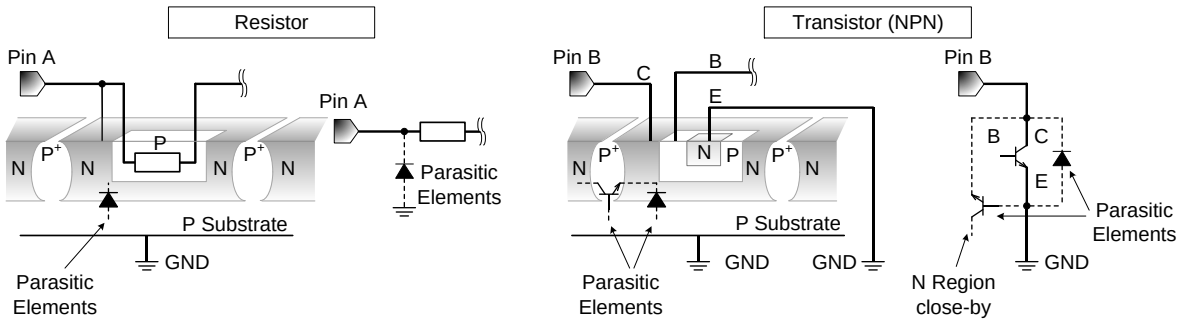


Figure 52. Example of monolithic IC structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

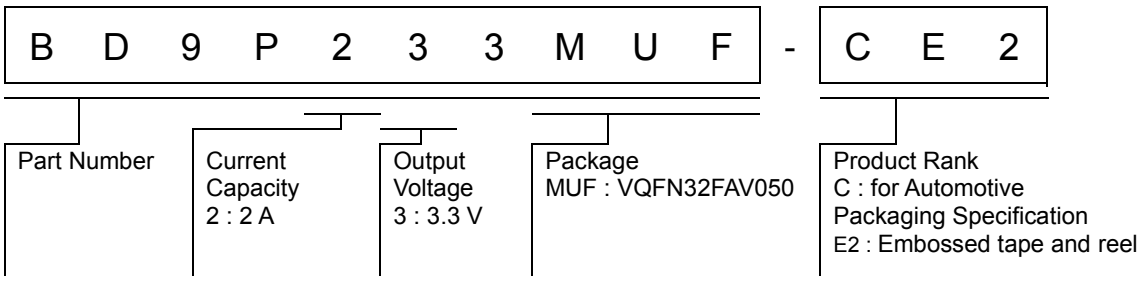
12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

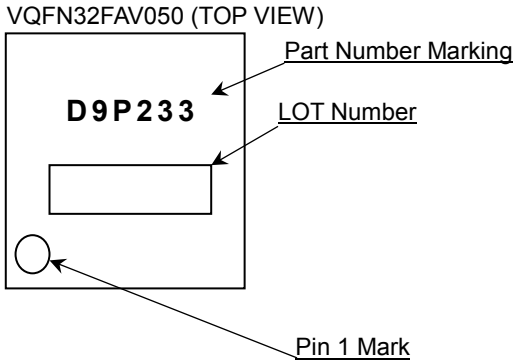
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

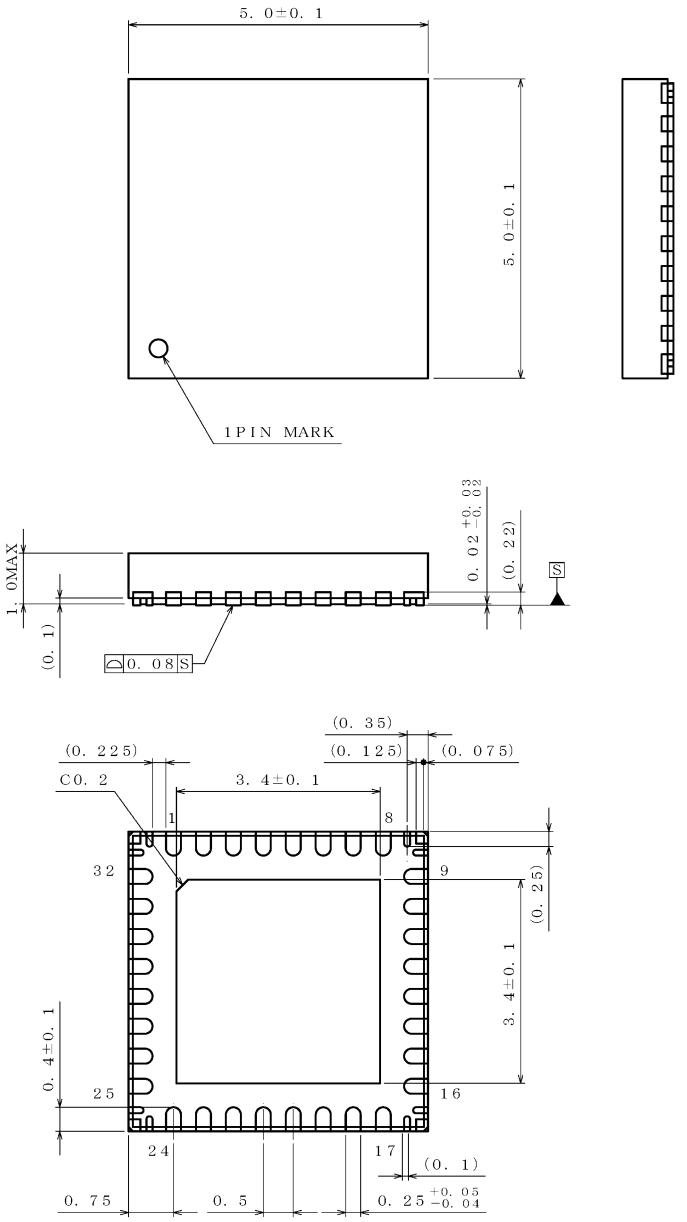


Making Diagram



Physical Dimension and Packing Information

Package Name	VQFN32FAV050



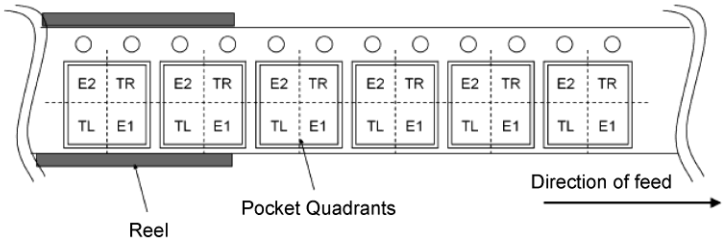
(UNIT:mm)

PKG:VQFN32FAV050
Drawing No. EX403-5001-1

NOTE: Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
19.Jul.2019	001	New Release

Notice

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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