

# Temperature Sensor IC Low Current Thermostat Output

## BDJ0600AHFV

### General Description

BDJ0600AHFV is a thermostat output temperature sensor IC with built-in temperature detection element, constant current circuit, and a high-accuracy reference voltage source in one chip. Temperature detection can be realized at  $\pm 2.5$  °C accuracy without the need for a complicated design. It is best suited for portable equipment of micro- and low-current, power down function, and battery drive.

### Key Specifications

- Power Supply Voltage Range: 2.4 V to 5.5 V
- Supply Current:
  - Normal Function Mode 7.5  $\mu$ A (Typ)
  - Power Down Mode 0.3  $\mu$ A (Typ)
- High Accuracy Thermostat:  $\pm 2.5$  °C (Max) @Ta=60 °C
- Detection Temperature Hysteresis: 10.0 °C (Typ)
- Operating Temperature Range: -30 °C to +100 °C

### Features

- Built-in Power Down Control Function (PD Input Interface Voltage is 1.5 V)
- OS Output Active L

### Applications

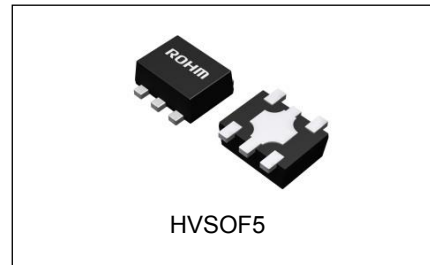
- Smart Phone (RF Module, Audio-AMP, LED Driver, etc.)
- Digital Still Camera
- Notebook PC

### Package

HVSO5F5

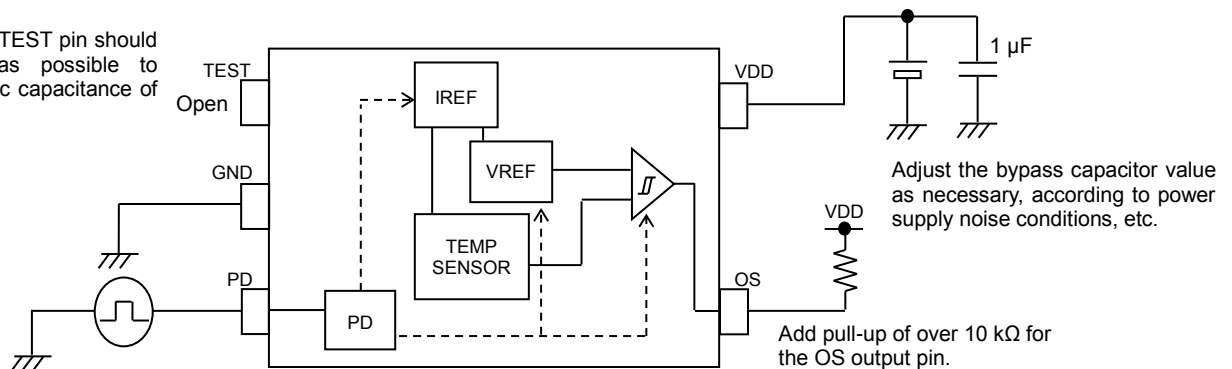
W(Typ) x D(Typ) x H(Max)

1.60 mm x 1.60 mm x 0.60 mm



### Typical Application Circuit and Block Diagram

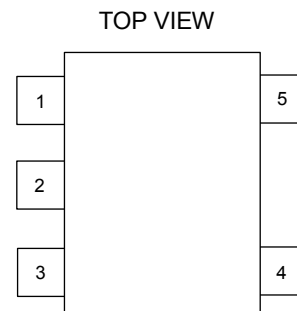
Land pattern for TEST pin should be as small as possible to minimize parasitic capacitance of the pattern.



### Pin Descriptions

Pin No.	Pin Name	Function
1	TEST	Test Pin (Open)
2	GND	Ground
3	PD	Power Down Control H: Normal Function Mode L: Power Down Mode
4	OS	Digital Thermostat Output (Open-Drain Active-Low)
5	VDD	Power Supply Voltage

### Pin Configuration



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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## Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V <sub>DD</sub>	7.0 (Note 1)	V
Input Voltage (PD)	V <sub>IN</sub>	-0.3 to (V <sub>DD</sub> +0.3) or +7.0 whichever is less	V
OS Pin Voltage	V <sub>OS</sub>	-0.3 to +7.0 (Note 1)	V
OS Pin Current	I <sub>OS</sub>	5.0	mA
Maximum Junction Temperature	T <sub>Jmax</sub>	150	°C
Storage Temperature Range	T <sub>stg</sub>	- 55 to +150	°C

(Note 1) However, not exceeding Maximum Junction Temperature.

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

## Thermal Resistance (Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 4)	2s2p (Note 5)	
HVSOF5				
Junction to Ambient	θ <sub>JA</sub>	358.2	85.3	°C/W
Junction to Top Characterization Parameter (Note 3)	Ψ <sub>JT</sub>	39	21	°C/W

(Note 2) Based on JESD51-2A(Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via (Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 6) This thermal via connects with the copper pattern of all layers.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V <sub>DD</sub>	2.4	2.8	5.5	V
Operating Temperature	T <sub>opr</sub>	-30	-	+100	°C

**Electrical Characteristics (Unless otherwise specified V<sub>DD</sub>=2.8 V Ta=25 °C)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>Supply Current</b>						
Normal Function Mode	I <sub>DD</sub>	-	7.5	12.0	μA	PD="H"
Power Down Mode	I <sub>DDPD</sub>	-	0.3	1.0	μA	PD="L"
<b>PD Input Pin</b>						
Input L Voltage	V <sub>IL</sub>	GND	-	0.2	V	
Input H Voltage	V <sub>IH</sub>	1.5	-	V <sub>DD</sub>	V	
Leakage Current	I <sub>L</sub> PD	-	-	1.0	μA	PD=2.8 V
<b>OS Output Open Drain</b>						
Leakage Current	I <sub>L</sub>	-	-	1.0	μA	V <sub>OS</sub> =5.0 V
Output L Voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OS</sub> = 1.0 mA

**Temperature Characteristics (Unless otherwise specified V<sub>DD</sub>=2.8 V)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>Thermostat</b>						
Detection Temperature	T <sub>DET</sub>	57.5	60.0	62.5	°C	
Detection Temperature Hysteresis	T <sub>HYS</sub>	7.5	10.0	12.5	°C	

Typical Performance Curves

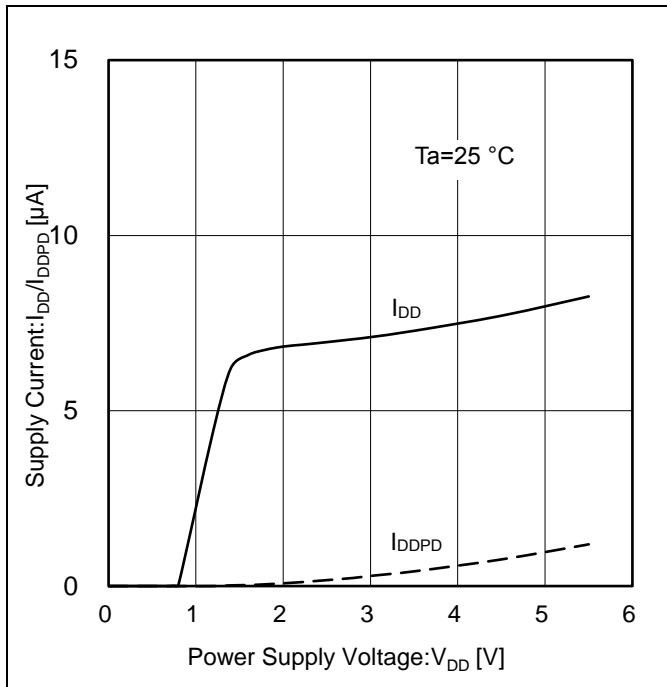


Figure 1. Supply Current vs Power Supply Voltage

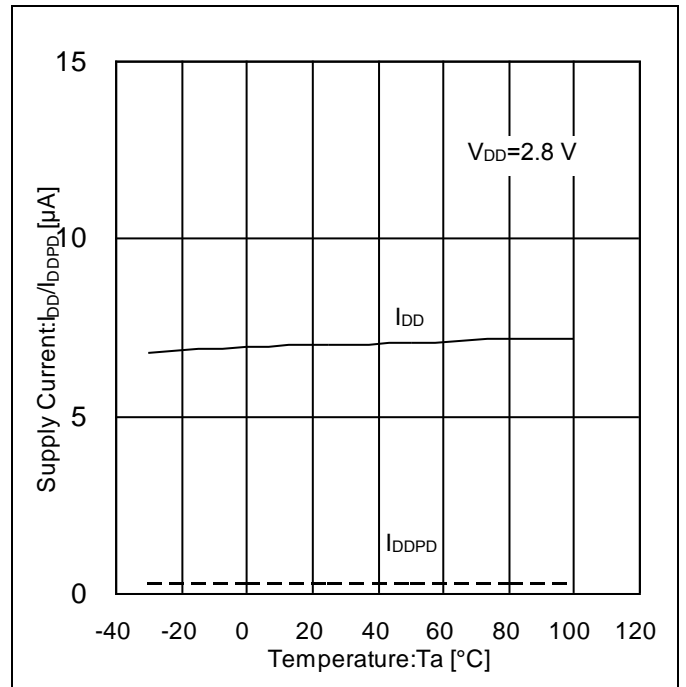
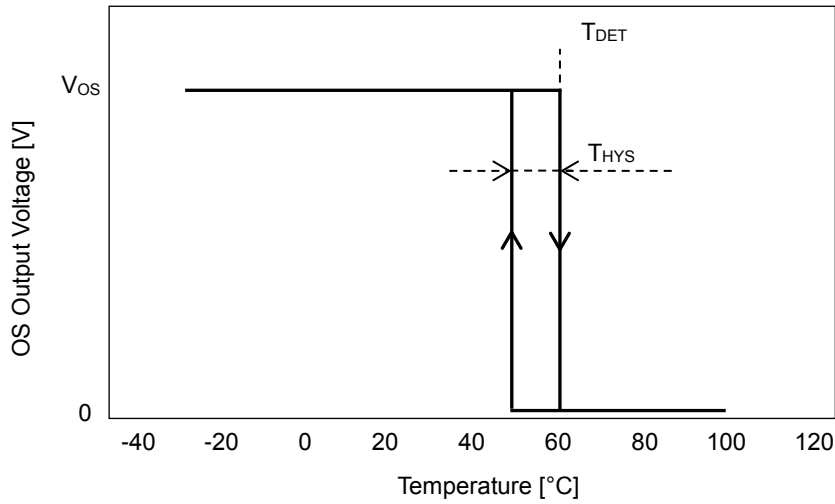


Figure 2. Supply Current vs Temperature

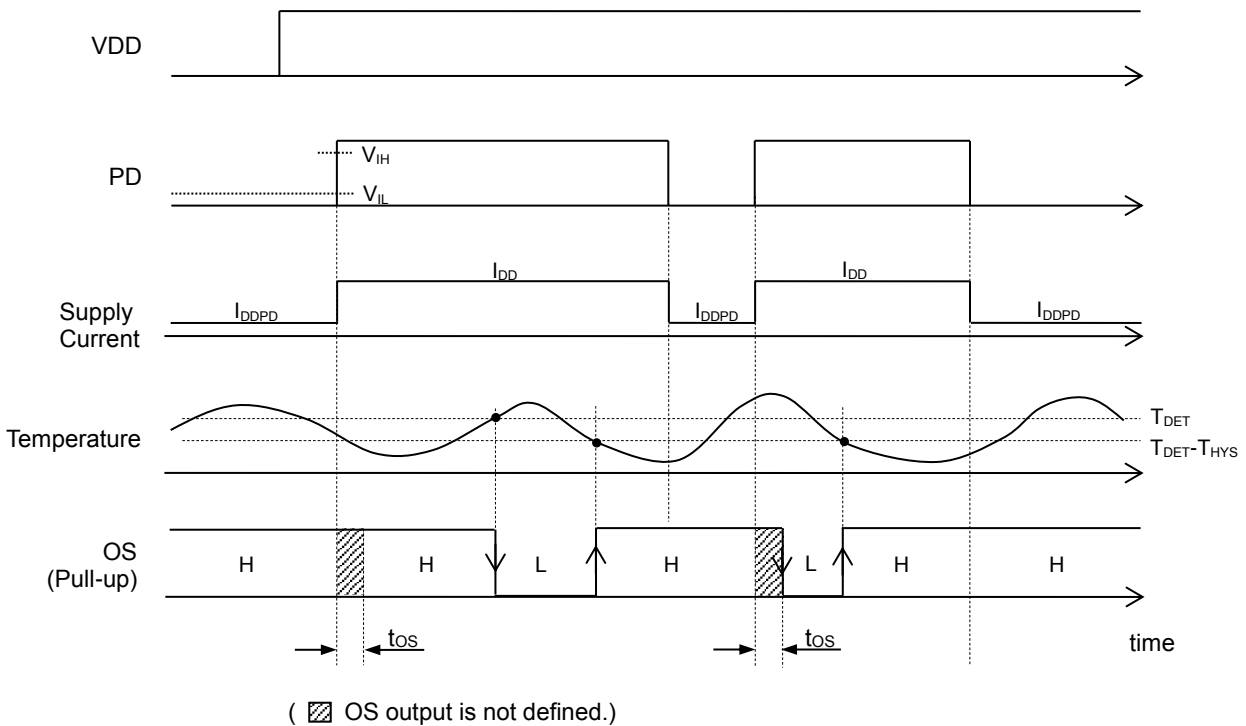
Application Information

1. Function Diagram

If the temperature exceeds the detect point temperature, the internal comparator forces the OS output to change from "H" to "L". OS output returns to "H", when the temperature drops hysteresis temperature( $T_{HYS}$ ) from detection temperature.



2. Operation Sequence



BDJ0600AHFV operation starts after PD "H" Input. Refer to the OS pin signal table below for the wait time after PD "H" Input. A capacitance connected to TEST pin causes to extend output stabilization time. It should not be connected.

Symbol	Wait Time
t <sub>os</sub>	10 ms

I/O Equivalence Circuits

Pin Name	Equivalent Circuit Diagram	Pin Name	Equivalent Circuit Diagram
PD		OS	
TEST			

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.



## Operational Notes – continued

## 11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

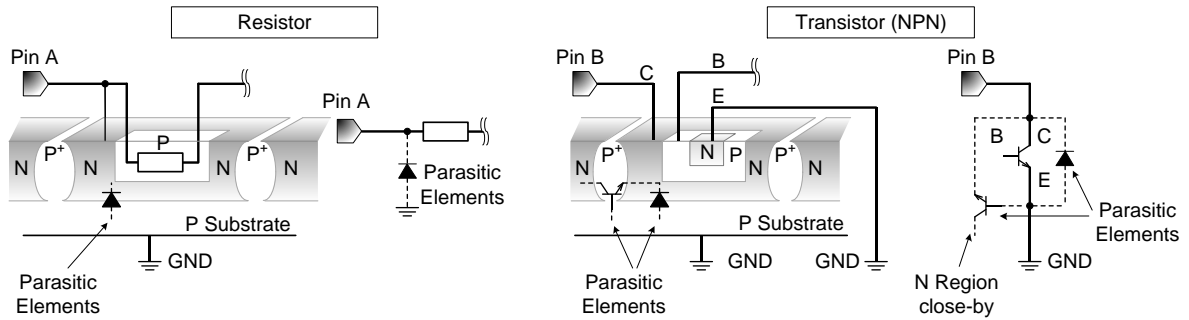


Figure 3. Example of monolithic IC structure

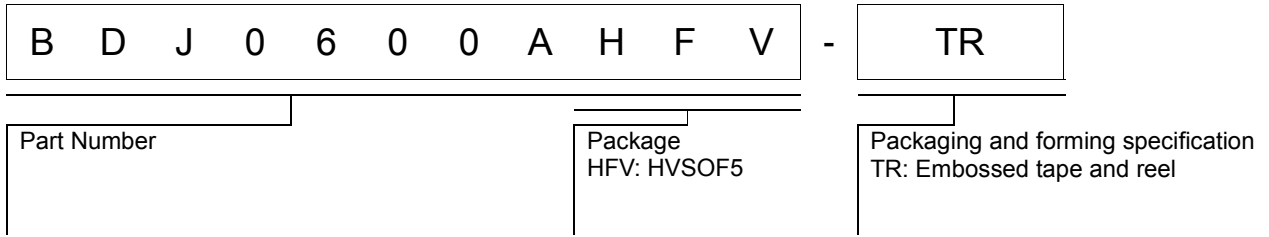
## 12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

## 13. Area of Safe Operation (ASO)

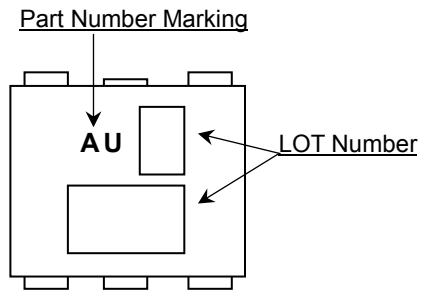
Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

Ordering Information



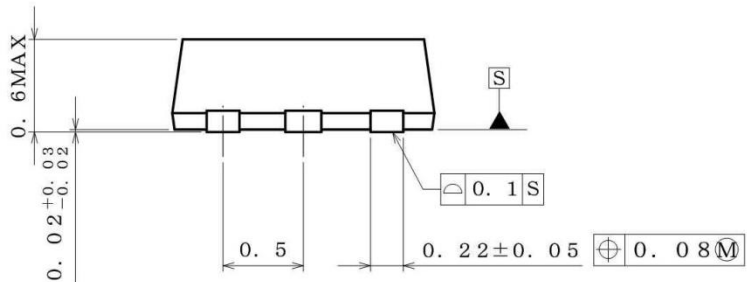
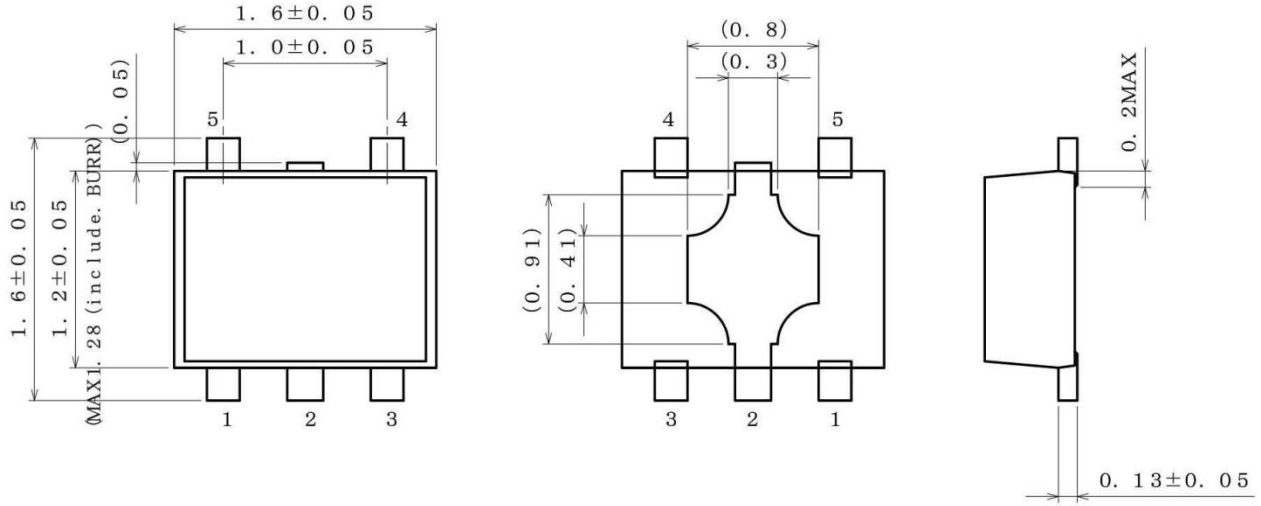
Marking Diagram

HVSO5(TOP VIEW)



Physical Dimension and Packing Information

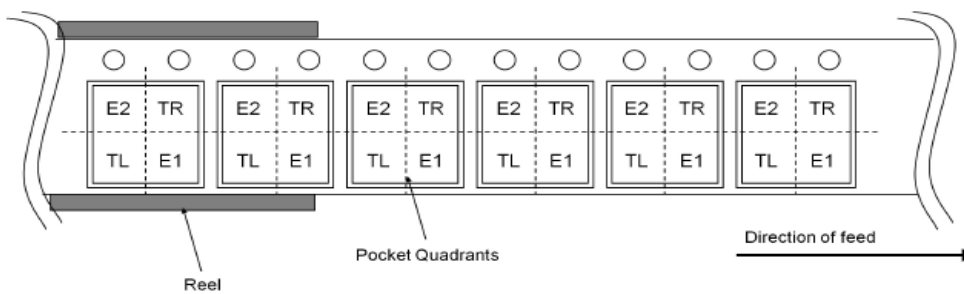
Package Name	HVSO5F5
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(UNIT : mm)  
 PKG : HVSO5F5  
 Drawing No. EX108-5002

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR ( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand )



**Revision History**

Date	Revision	Changes
31.May.2018	001	New Release

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CLASS IV		CLASS III	

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- Confirm that operation temperature is within the specified range described in the product specification.
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