High-performance System Video Drivers

Wide Band 3-output Video Drivers

BH7601FS, BH7602FS

No.11065EBT05

●Description

BH7601FS and BH7602FS are wide band 3-output video drivers for high-definition television system. These video drivers are built in the DC output circuits (LINE1, LINE2, LINE3 output) for D terminal and detector to connect. And they have line-up build in DC shift input, selectable LPF every application.

●Features

1) Built-in the DC output circuits (LINE1, LINE2, LINE3) / detector to connect.
2) Built-in OUTPUT MUTE circuit
3) I^2C BUS control
4) Sync tip clamp input 1ch, bias input 2ch (BH7601FS)
5) Possible to be directly connected with DAC by DC shift circuit (BH7602FS)
6) Built-in power down function (BH7602FS)

●Applications

DVD Player, DVD Recorder, DVC, DSC, STB, TV and so on.

●Line up matrix

Parameter	BH7601FS	BH7602FS
Input form of Py	Sync tip Clamp	DC Shift (Directly connected)
Input form of Pb, Pr	Bias Input	DC Shift (Directly connected)
Voltage Gain	8.45dB	6.0dB
Package	SSOP-A24	SSOP-A20

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply Voltage	Vcc	7	V
Power Dissipation	Pd	800 (SSOP-A24)※ 750 (SSOP-A20)※	mW
Input Voltage Range	Vin	0～Vcc	V
Operating Temperature	Topr	-25～+75 (SSOP-A24) -35～+75 (SSOP-A20)	℃
Storage Temperature	Tstg	-55～+125	℃

※ 70mm × 70mm × 1.6mm mounting on the glass epoxy board.
For operation above Ta=25℃ free-air temperature, power dissipation is decreasing 8.0mW/℃(SSOP-A24), 7.5mW/℃ (SSOP-A20).

●Operating conditions

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Supply Voltage(BH7601FS)	Vcc	4.5	5.0	5.5	V
Supply Voltage(BH7602FS)	Vcc	4.5	5.0	5.25	V

●**Electrical characteristics** (Unless otherwise specified, Ta=25℃,V_{CC}=5V)

○BH7601FS

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
《All Circuit》						
Circuit Current	I_{CC}	13.5	27.0	40.5	mA	No signal
LINEOUT「H」Voltage	V_{LOH}	3.5	4.25	5.0	V	(V_{CC}=5V±5%)
LINEOUT「M」Voltage	V_{LOM}	1.4	1.9	2.4	V	(V_{CC}=5V±5%)
LINEOUT「L」Voltage	V_{LO}	0.0	0.1	0.5	V	(V_{CC}=5V±5%)
LINEOUT Impedance	Z_{LO}	1.3	1.8	2.3	kΩ	
《Video Driver Parts》						
Voltage Gain	G_V	1.65	2.45	3.25	dB	V_{IN}=0.75V_{P-P}, f=1MHz ※1
Frequency Characteristics	V_{F1}	-1	0	1	dB	V_{IN}=0.75V_{P-P}, f=1M/10MHz
MUTE Input Parts Impedance	Z_{MUTE}	75	100	125	kΩ	
MUTE「H」Level Input Voltage	V_{MH}	2.0	-	V_{CC}	V	
MUTE「L」Level Input Voltage	V_{ML}	0	-	1.0	V	
PB, PR Input Impedance	Z_{IN}	14	20	26	kΩ	
《Control Parts》						
「H」Level Input Voltage	V_H	2.0	-	V_{CC}	V	
「L」Level Input Voltage	V_L	0	-	1.0	V	
SDA 「L」Sink Current	I_{SIN}	4.0	-	-	mA	
DET Detection Level「H」	V_{DH}	2.0	-	V_{CC}	V	
DET Detection Level「L」	V_{DL}	0	-	1.0	V	
DET Input Bias Current	I_{DET}	0	-2.0	-20	μA	

※1 Measure at separation of 75Ω+75Ω

○Reference Value

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
《Video Driver Parts》						
Frequency Characteristics2	V_{F2}	-	-1	-	dB	V_{IN}=0.53V_{P-P}, f=1M/30MHz
Mute Attenuation	V_{MT}	-	-40	-	dB	V_{IN}=0.75V_{P-P}, f=20MHz
Channel Crosstalk	C_{TV}	-	-40	-	dB	V_{IN}=0.75V_{P-P}, f=20MHz

○BH7602FS

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
《All Circuits》						
V_{CC} Circuit Current	I_{VCC}	44	56	68	mA	No signal
V_{CC} Circuit Current PD	I_{PD}	-	1.5	3.0	mA	Power down
《Video Driver Parts》						
Y/PB/PR OUT Voltage Gain	G_{20}	5.5	6.0	6.5	dB	Vin=1.0$V_{P-P,}$ f=100kHz
Y/PB/PR OUT Maximum Output Level	V_{OM20}	2.6	2.9	-	V_{P-P}	Vin: THD=1.0% f=10kHz
Y OUT LPF1 Frequency Characteristics 1	F_{1201}	-5.0	-1.5	1.0	dB	Vin=1.0V_{P-P}, f=30M/100kHz, LPF1:ON
Y OUT LPF2 Frequency Characteristics 1	F_{2201}	-1.5	-0.5	0.5	dB	Vin=1.0V_{P-P}, f=13.5M/100kHz, LPF2:ON
PB/PR OUT LPF1 Frequency Characteristics 1	F_{1171}	-5.0	-1.5	1.0	dB	Vin=1.0V_{P-P}, f=15M/100kHz, LPF1:ON
PB/PR OUT LPF2 Frequency Characteristics 1	F_{2171}	-1.5	-0.5	0.5	dB	Vin=1.0V_{P-P}, f=6.75M/100kHz, LPF2:ON
Y OUT LPF1 Frequency Characteristics 2	F_{1202}	-	-45	-28	dB	Vin=1.0V_{P-P}, f=74.25M/100kHz, LPF1:ON
Y OUT LPF2 Frequency Characteristics 2	F_{2202}	-	-40	-28	dB	Vin=1.0V_{P-P}, f=54M/100kHz, LPF2:ON
PB/PR OUT LPF1 Frequency Characteristics 2	F_{1172}	-	-45	-28	dB	Vin=1.0V_{P-P}, f=37.125M/100kHz, LPF1:ON
PB/PR OUT LPF2 Frequency Characteristics 2	F_{2172}	-	-40	-28	dB	Vin=1.0V_{P-P}, f=27M/100kHz, LPF2:ON
MUTE Attenuation	M_{T20}	-	-65	-55	dB	Vin=1.0V_{P-P}, f=4.43MHz
Channel Crosstalk	M_{TCH}	-	-65	-55	dB	Vin=1.0V_{P-P}, f=4.43MHz
《D_DET》						
Input Voltage H	V_{I14H}	4.0	-	V_{CC}	V	
Input Voltage M	V_{I14L}	0.0	-	1.0	V	
Input Impedance	Z_{I14}	100	150	200	kΩ	Pull Up Resistance
《LINE_OUT》						
Output Voltage H	V_{O13H}	4.2	4.5	4.8	V	
Output Voltage M	V_{O13M}	1.7	2.0	2.3	V	
Output Voltage L	V_{O13L}	0.0	0.1	0.5	V	
Input Impedance	Z_{O13}	0.5	0.9	1.3	kΩ	Pull Down Resistance

○BH7601FS, BH7602FS

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
《ADR》						
Input Voltage H	V_{I8H}	2.0	-	Vcc	V	
Input Voltage L	V_{I8L}	0.0	-	1.0	V	
Input Impedance	Z_{I8}	65	100	135	kΩ	Pull Down Resistance
《SCL, SDA》						
Input Voltage H	V_{I9H}	2.0	-	Vcc	V	
Input Voltage L	V_{I9L}	0.0	-	1.0	V	
Input Bias Current	I_{B9}	-10	0	10	μA	

●Block Diagram

○BH7601FS

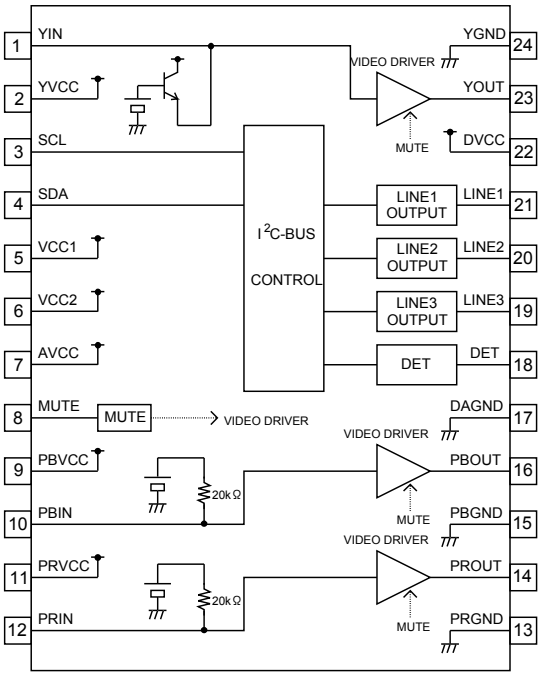


Fig.1

○BH7602FS

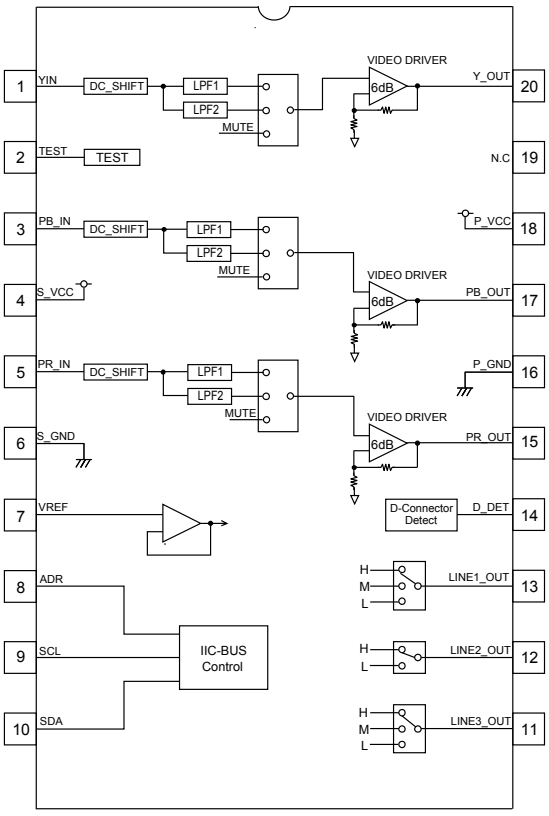
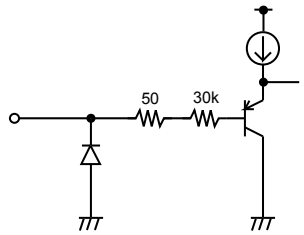
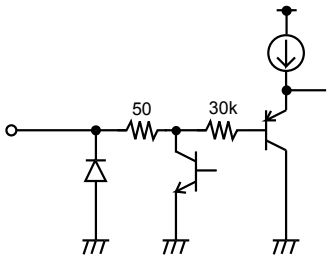
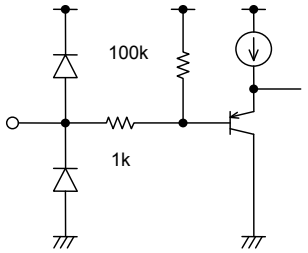
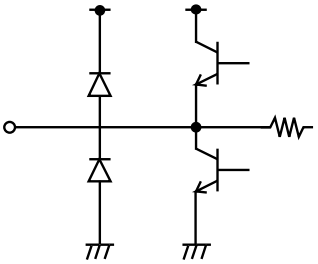
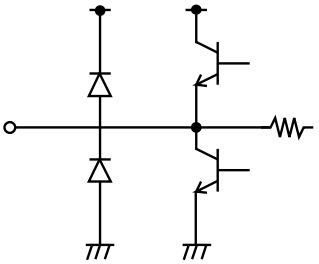
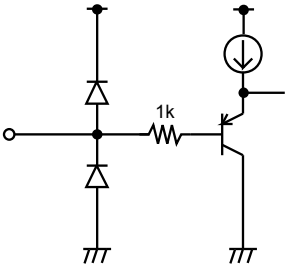


Fig.2

●Terminal Description・Input/Output Equivalent Circuit

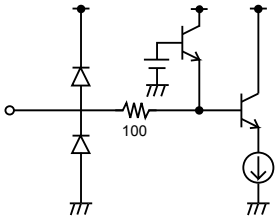
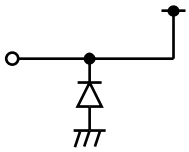
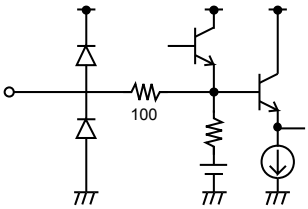
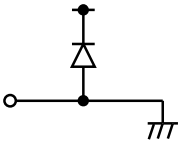
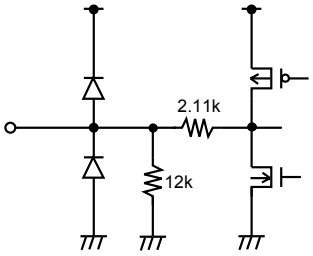
○BH7601FS

Pin.No	Pin Name	IN	OUT	Standard Voltage	Input/Output Equivalent Circuit	Terminal Description
3	SCL	○	—	—		I^2C BUS CLOCK Input Terminal This terminal is serial clock input terminal that is based on I^2C BUS. Usually, it use to pull up by resistor.
4	SDA	○	—	—		I^2C BUS DATA Input Terminal This terminal is serial data input terminal that is based on I^2C BUS. Usually, it use to pull up by resistor.
8	MUTE	○	—	5.0V		Mute Control Terminal This terminal is connected to Vcc with 100kΩ, when the terminal is open or High, mute mode, when Low, normal mode.
14 16	PROUT PBOUT	—	○	2.1V		PB, PR Signal Output Terminal This terminal is the PR, PB output terminal.
23	YOUT	—	○	0.7V		Y Signal Output Terminal This terminal is the Y signal output terminal.
18	DET	○	—	—		DET Terminal This terminal is the detector to connect D terminal. Usually, it use to pull up by resistor.

※ The values in the terminal descriptions and input/output equivalent circuit are for reference only - they are not guaranteed.

●Terminal Description・Input/Output Equivalent Circuit (Continued)

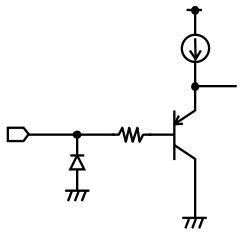
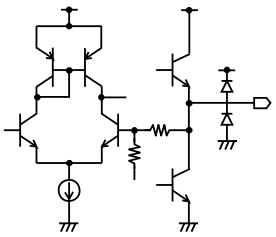
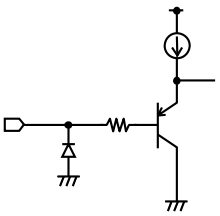
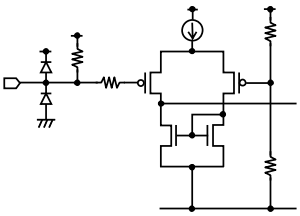
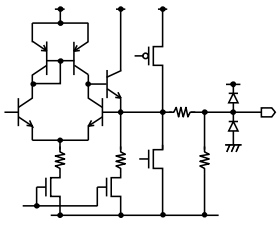
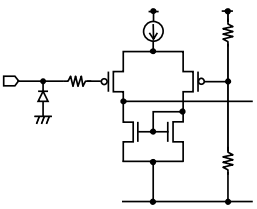
○BH7601FS

Pin.No	Pin Name	IN	OUT	Standard Voltage	Input/Output Equivalent Circuit	Terminal Description
1	YIN	○	—	2.8V		Y Signal Input Terminal This terminal is Y signal input terminal. The input is sync tip clamp.
2 5 6 7 9 11 22	YVcc Vcc1 Vcc2 AVcc PBVcc PRVcc DVcc	—	—	5.0V		Vcc Terminal YVcc, PBVcc, PRVcc are Vcc terminal of video driver. Vcc1, Vcc2, AVcc are the Vcc terminal of the other analog parts (These 3 terminals are connected inside), DVcc is Vcc terminal of the digital parts.
10 12	PBIN PRIN	○	—	2.1V		PB, PR Signal Input Terminal This terminal is the PR, PB input terminal. The input is bias type.
13 15 17 24	PRGND PBGND DAGND YGND	—	—	0.0V		GND Terminal PRGND, PBGND, YGND are GND terminal of video driver. DAGND is the GND terminal of the blocks except video driver.
19 20 21	LINE3 LINE2 LINE1	–	○	–		Line Output Terminal This terminal is the line 3 value output terminal for D terminal. This terminal is controlled by I^2C BUS.

※ The values in the terminal descriptions and input/output equivalent circuit are for reference only - they are not guaranteed.

●Terminal Description・Input/Output Equivalent Circuit (Continued)

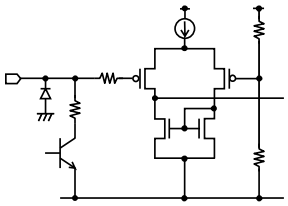
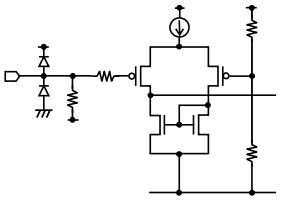
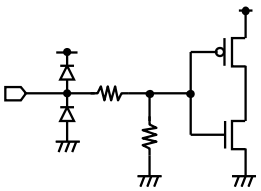
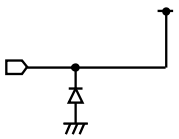
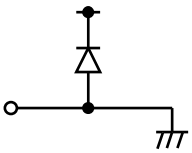
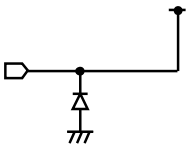
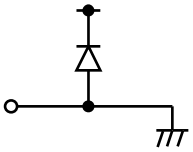
○BH7602FS

Pin.No	Pin Name	IN	OUT	Standard Voltage	Input/Output Equivalent Circuit	Terminal Description
1 3 5	Y_IN PB_IN PR_IN	○	—	(V_{S7}-0.4) ～ (V_{S7}+0.9)		Component signal input terminal Input range is possible to regulate by VREF terminal input voltage (V_{S7}). When Vcc off, this terminal become high impedance.
20 17 15	Y_OUT PB_OUT PR_OUT	—	○	0.7 At input terminal voltage =(V_{S7}-0.4)		Component signal output terminal It is possible to output two drivers.
7	VREF	○	—	0.4～1.4		Reference Terminal This terminal is input terminal of inside reference voltage for DC-shift circuit.
14	D_DET	○	—	5.0V		D Terminal Input Terminal for detector to connect Terminal condition (H/L) is possible to read out by I^2C BUS. When D mode, it is possible to control of power-down into terminal condition (H/L).
13 12 11	LINE1_OUT LINE2_OUT LINE3_OUT	—	○	4.5(H) 2.0(M) 0.1(L)		LINE-OUT Terminal This terminal is the line 3 value output terminal for controlled by I^2C BUS. Each distinction output are correspond with the D terminal standard.
9	SCL	○	—	—		I^2C BUS clock Input Terminal This terminal is possible to operate max 400kHz. When Vcc off, this terminal become high impedance.

※ The values in the terminal descriptions and input/output equivalent circuit are for reference only - they are not guaranteed.

●**Terminal Description・Input/Output Equivalent Circuit (Continued)**

○BH7602FS

Pin.No	Pin Name	IN	OUT	Standard Voltage	Input/Output Equivalent Circuit	Terminal Description
10	SDA	○	○	—		I^2C-BUS Data Input/ Output Terminal This terminal is possible to operate max 400kHz. When VCC off, this terminal become high impedance.
8	ADR	○	—	0V		Slave Address Change Terminal LOW: D8H High: DAH
2	TEST	○	—	0V		LOGIC Test Mode Change Terminal Usually not use. This terminal is 0V input (=GND).
18	P_VCC	—	—	5.0V		VCC terminal for driver output.
19	P_GND	—	—	0V		GND terminal for driver output.
4	S_VCC	—	—	5.0V		VCC terminal for the analog part except driver and digital part.
6	S_GND	—	—	0V		GND terminal for the analog part except driver and digital part.

※ The values in the terminal descriptions and input/output equivalent circuit are for reference only - they are not guaranteed.

●Operation description of each block

■I²C BUS Control Input Specifications 〈 BH7601FS 〉

・I²C BUS Format (WRITE MODE)

S	SLAVE ADDRESS	A	DATA	A	P

S: Start Condition A: Acknowledge P: Stop Condition

	b7	b6	b5	b4	b3	b2	b1	b0
Slave address	1	1	0	1	1	0	0	0
DATA	0	0	LINE1		LINE2		LINE3	

・Select Input Switch

	Explanation		Explanation
LINE1	Setting output of LINE1 OUT 00: LOW ＊(BH7601FS) 01: LOW 10: MIDDLE 11: HIGH	LINE3	Setting output of LINE3 OUT 00: LOW ＊(BH7601FS) 01: LOW 10: MIDDLE 11: HIGH
LINE2	Setting output of LINE2 00: LOW ＊(BH7601FS) 01: LOW 10: MIDDLE 11: HIGH		

・ Setting Mode (When power on, it becomes ＊ condition.)

・I²C BUS Format (READ MODE)

S	SLAVE ADDRESS	A	DATA	NA	P

S: Start Condition A: Acknowledge NA: No Acknowledge P: Stop Condition

	b7	b6	b5	b4	b3	b2	b1	b0
Slave address	1	1	0	1	1	0	0	1
DATA	0	0	0	0	0	0	0	DET

・Select Input Switch・ Setting Mode

	Explanation
DET	Read out the condition of DET (18PIN) pin. 0: LOW 1: HIGH

●Operation description of each block (Continued)

■I²C BUS Control Input Specifications 〈 BH7602FS 〉

・I²C BUS Format (WRITE MODE)

S	SLAVE ADDRESS	A	DATA1	A	DATA2	A	P

S: Start Condition A: Acknowledge P: Stop Condition

	b7	b6	b5	b4	b3	b2	b1	b0
Slave address	1	1	0	1	1	0	ADR	R/W
DATA1	LPF_SW		LINE1		LINE2	0	LINE3	
DATA2	PD	D_MODE	0	0	0	0	0	0

・Select Input Switch

	Explanation		Explanation
ADR	Slave Address (write mode) set by ADR pin. 0: “D8H” when ADR is Low. 1: “DAH” when ADR is High.	R/W	READ/WRITE Setting Mode 0: WRITE 1: READ
LPF_SW	LPF_SW Setting output 00: LPF1 01: LPF2 10: － 11: MUTE ＊ (NOTE)“10” is No use	LINE1	Setting output of LINE1_OUT for D terminal 00: L ＊ 01: L 10: M 11: H
LINE2	Setting output of LINE2_OUT for D terminal 0: L ＊ 1: H	LINE3	Setting of output of LINE3_OUT for D terminal 00: L ＊ 01: L 10: M 11: H
PD	Power down control 0: Normal ＊ 1: PD(Power down)	D_MODE	D terminal detect mode change 0: OFF ＊ 1: ON(D terminal detect mode)

・ Setting Mode (When power on, it becomes ＊ condition.)

・D_MODE (D terminal detect mode)

When I²C BUS sets D_MODE=ON, POWER DOWN is controlled by D_DET pin input level and the PD pin input is ignore.

D_MODE	PD	D_DET	Output
OFF	0	L	Normal
	0	H	Normal
	1	L	Power down
	1	H	Power down
ON	0	L	Normal
	0	H	Power down
	1	L	Normal
	1	H	Power down

●Operation description of each block (Continued)

・I^2C BUS Format (READ MODE)

S	SLAVE ADDRESS	A	DATA1	NA	P

S: Start Condition A: Acknowledge NA: No Acknowledge P: Stop Condition

	b7	b6	b5	b4	b3	b2	b1	b0
Slave address	1	1	0	1	1	0	ADR	R/W
DATA	0	0	0	0	0	0	0	D_DET

・Select Input Switch

	Explanation		Explanation
ADR	Slave Address (read mode) set by ADR 0: “D9H”, when ADR is LOW. 1: “DBH”, when ADR is High.	D_DET	Read out D_DET condition 0: LOW 1: HI
R/W	READ/WRITE setting mode 0: WRITE 1: READ		

●Operation description of each block (Continued)

■BH7602FS How to set video input level in DC_SHFT circuit

BH7602FS is build in DC_Shift block and it operate without input coupling capacitor. It is necessary to set input voltage of VREF (7pin) terminal to VIDEO signal input level because of enough output dynamic range.

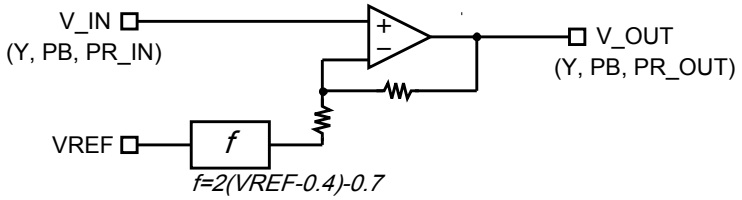


Fig. 3 DC_Shift block equivalent circuit

The relation of V_IN, VREF, V_OUT in this place

V_OUT=0.7+2(V_IN-VREF+0.4) (eq.1)

and the input possible range of VREF is

0.4≦VREF≦1.4 [V] (eq.2)

It shows the relation of V_IN-V_OUT at each VREF value on Fig.5.
On the other hand, the operation range of V_OUT (VIDEO OUTPUT) becomes 0.7V～3.3V (2.6Vp-p) of the circuit composition, and needs to adjust VREF terminal voltage to be kept this range for inputted VIDEO signal.
VREF terminal voltage and V_IN input possible range are shown in Fig.4. Caution on use, after confirming Fig.4, adjust VREF terminal voltage.

VREF [V]	V_IN input possible range [V]
0.4	0.0～1.3
0.5	0.1～1.4
0.6	0.2～1.5
0.7	0.3～1.6
0.8	0.4～1.7
0.9	0.5～1.8
1.0	0.6～1.9
1.1	0.7～2.0
1.2	0.8～2.1
1.3	0.9～2.2
1.4	1.0～2.3

Fig. 4 The relation of VREF terminal voltage and input possible range

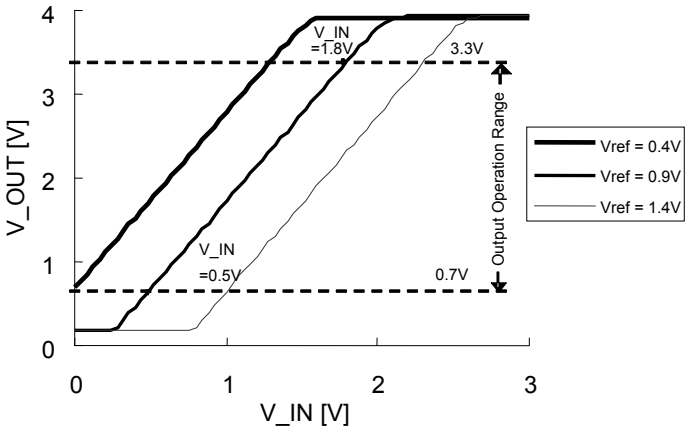


Fig. 5 The relation of V_IN-V_OUT at each VREF value (measurement value)

●Application circuit

○BH7602FS

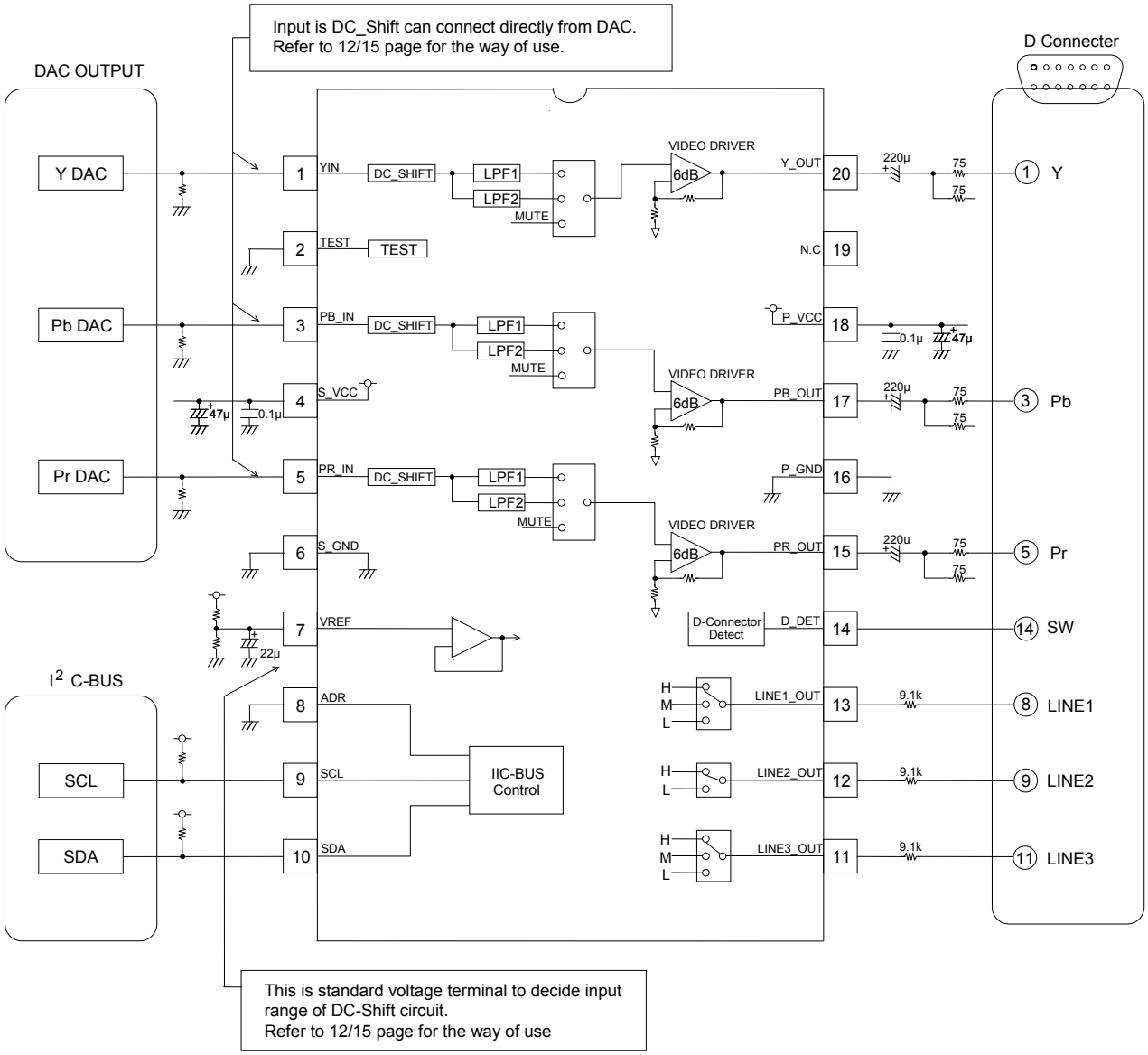


Fig. 6

●Reference Data

○BH7601FS

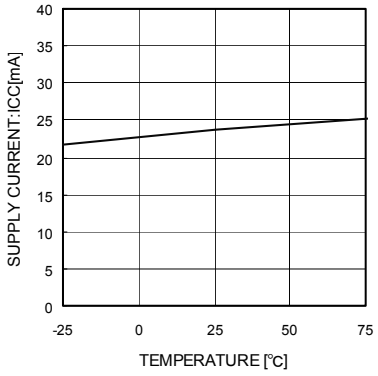


Fig.7 Circuit Current

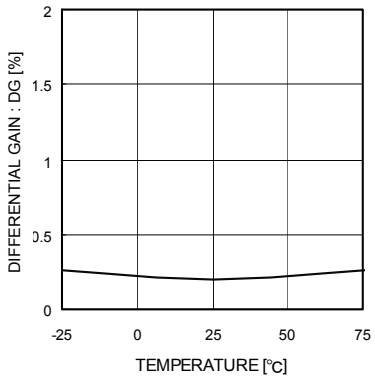


Fig.8 Differential Gain

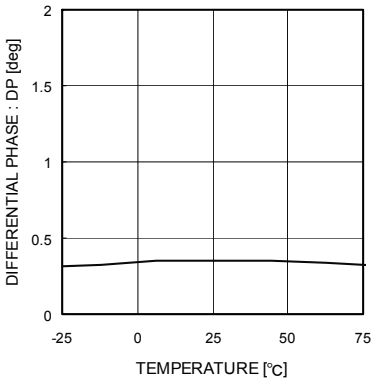


Fig.9 Differential Phase

○BH7602FS

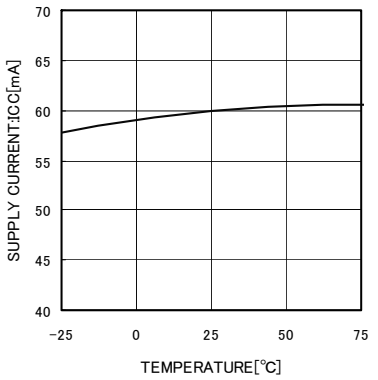


Fig.10 Circuit Current

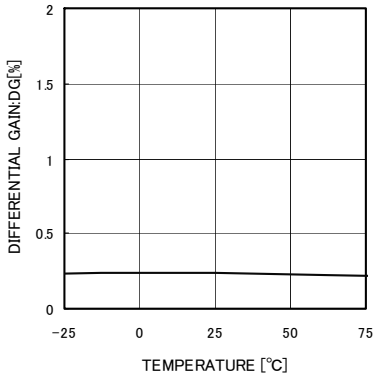


Fig.11 Differential Gain

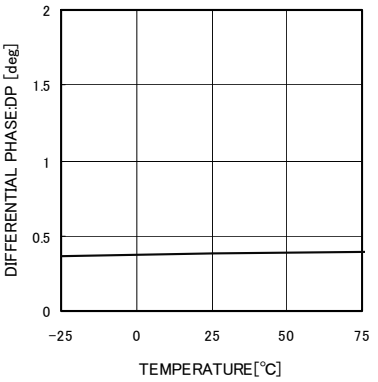


Fig.12 Differential Phase

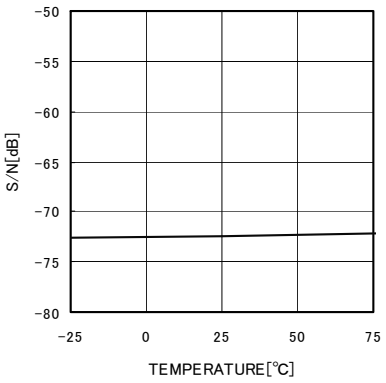


Fig.13 S/N

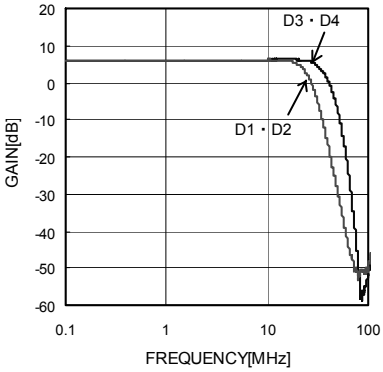


Fig.14 YLPF Characteristics

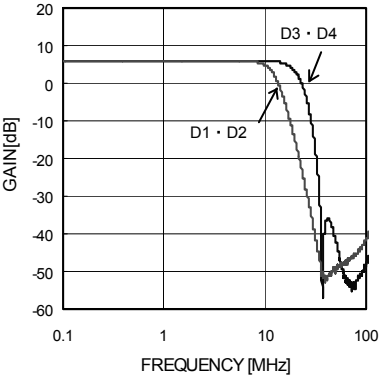


Fig.15 PBLPF Characteristics

●Ordering part number

B	H	7	6	0	1	F	S	-	E	2

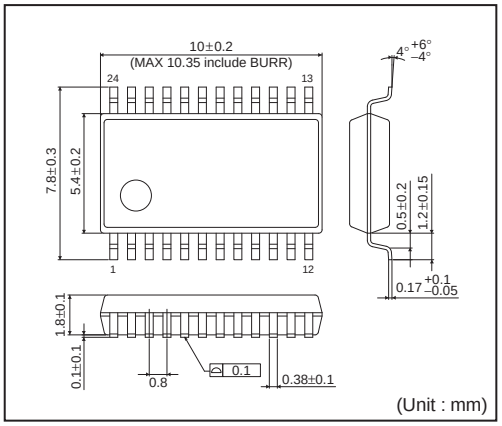
Part No.

Part No.
7601
7602

Package
FS: SSOP-A24
SSOP-A20

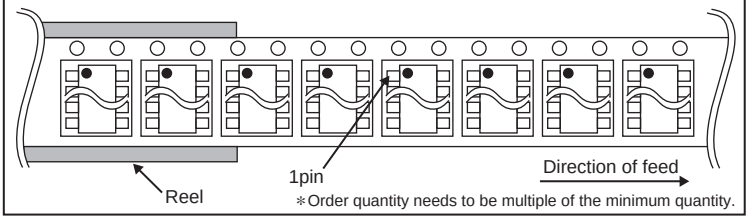
Packaging and forming specification
E2: Embossed tape and reel

SSOP-A24



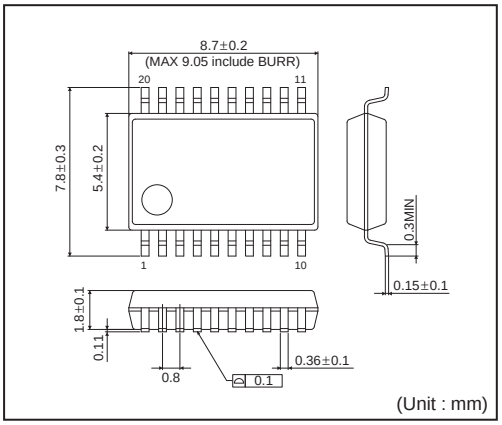
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



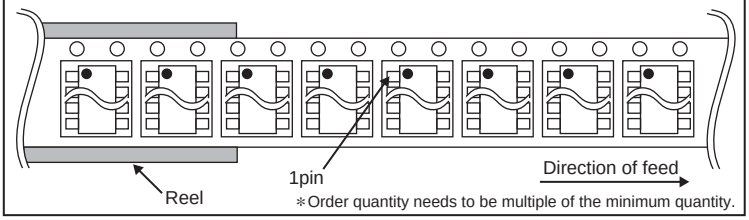
＊Order quantity needs to be multiple of the minimum quantity.

SSOP-A20



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

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