Structure Silicon Monolithic Integrated Circuit

Product name Low voltage operation wide band 3-outputs video driver with LPF

Type **BH7606GU**

Function
- Built in 3-output video drivers for Y, PB and PR signal
- Built in 6dB AMP
- Built in standby function (0μA TYP)
- Built in LPF (Y : fc=27MHz, PB/PR : fc=15MHz)
- No output coupling capacitor required
- Small package 15-Bump WL-CSP(2.26x2.26x1.0[mm])

※ Radiation resistance is not included in the design.

■Absolute Maximum Ratings （Ta=25℃）

Parameter	Symbol	Limits	Unit	Condition
CP_VCC Supply voltage	Vcp	3.55	V	CP_VCC - (CP_GND or V_GND)
V_VCC Supply voltage	Vv	3.55	V	V_VCC - (CP_GND or V_GND)
V_VCC to CP_VCC voltage	Vcc	-0.3～+0.3	V	V_VCC - CP_VCC
V_GND to CP_GND voltage	Vgg	0	V	V_GND - CP_GND
Input voltage 1	Vin1	-0.3~(V_VCC+0.3)	V	STBY
Input voltage 2	Vin2	(VEE_IN)-0.3 ~(V_VCC+0.3)	V	Y_IN, PB_IN, PR_IN
Power dissipation	Pd	920	mW	*
Storage temperature	Tstg	-55～+125	℃	

* In case mounting on a (110mm × 100mm × 1.6mm) grass-epoxy PCB.
* Reduced by 9.2 mW/°C at 25°C or higher.

■Operating range（Ta=25℃）

Parameter	Symbol	Rating.	Unit
CP_VCC Supply voltage	Vcpo	2.85 ~ 3.45	V
V_VCC Supply voltage	Vvo	2.85 ~ 3.45	V
Operating temperature	Topr	-40 ~ +85	℃

■Electrical characteristics 【Unless otherwise noted, Ta=25℃, CP_VCC=V_VCC=3V】

Parameter		Symbol	Limits			Unit	conditions
			Min.	Typ.	Max.		
Circuit current	ACTIVE	Icc_1	50	70	90	mA	No signal
	STANDBY	Icc_2	—	0	2	μA	Standby mode
Y/PB/PR_OUT Voltage gain		G_V	5.5	6.0	6.5	dB	Vin=1.0Vpp , f=100kHz
Y/PB/PR_OUT Maximum output level		V_{omv}	3.2	4.0	—	Vp-p	THD=1%, f=10kHz
Y_OUT Frequency characteristics 1		G_{f1Y}	-4.5	-1.5	1.0	dB	Vin=1.0Vpp , f=27M/100kHz
PB_OUT Frequency characteristics 1		G_{f1PB}	-3.0	-1.0	1.0	dB	Vin=1.0Vpp , f=15M/100kHz
PR_OUT Frequency characteristics 1		G_{f1PR}	-3.0	-1.0	1.0	dB	Vin=1.0Vpp , f=15M/100kHz
Y_OUT Frequency characteristics 2		G_{f2Y}	—	-26	-15	dB	Vin=1.0Vpp , f=54M/100kHz
PB_OUT Frequency characteristics 2		G_{f2PB}	—	-35	-28	dB	Vin=1.0Vpp , f=54M/100kHz
PR_OUT Frequency characteristics 2		G_{f2PR}	—	-35	-28	dB	Vin=1.0Vpp , f=54M/100kHz
Cross talk		C_T	—	-70	-50	dB	Vin=1.0Vpp , f=4.43MHz
Y/PB/PR_IN Input impedance		R_{inV}	100	150	200	kΩ	Y/PB/PR_IN－V_GND
Y/PB/PR_OUT Output DC offset		V_{off}	-100	0	100	mV	Terminated 75Ω
STBY Input voltage H		V_{thH}	V_VCC -1.2	—	V_VCC	V	ACTIVE mode
STBY Input voltage L		V_{thL}	0.0	—	0.45	V	STANDBY mode
STBY Input impedance		R_{inST}	100	150	200	kΩ	STBY－V_GND

■Control pin settings

Parameter	Status	Operational mode
STANDBY (B3)	H	ACTIVE
	L	STANDBY
	OPEN	

■Physical dimensions ・ Block diagram

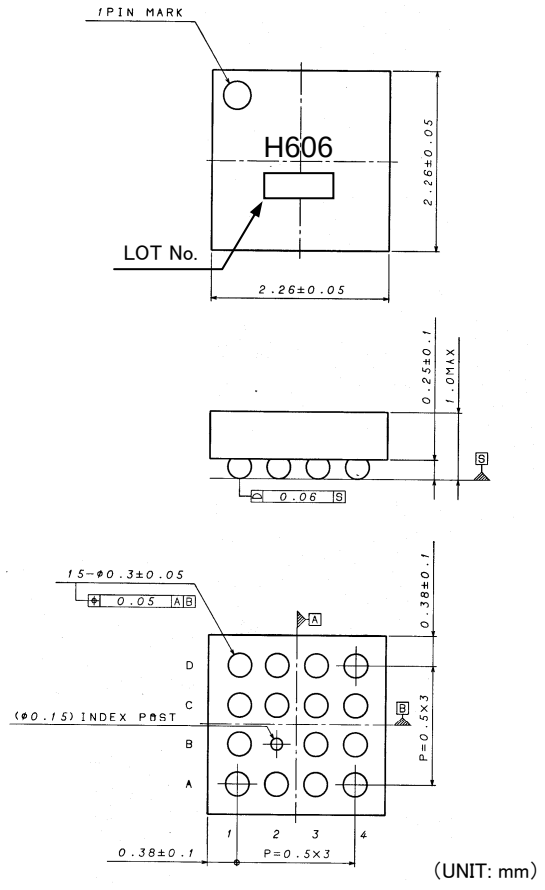

Fig.1. Physical dimensions (VCSP85H2)

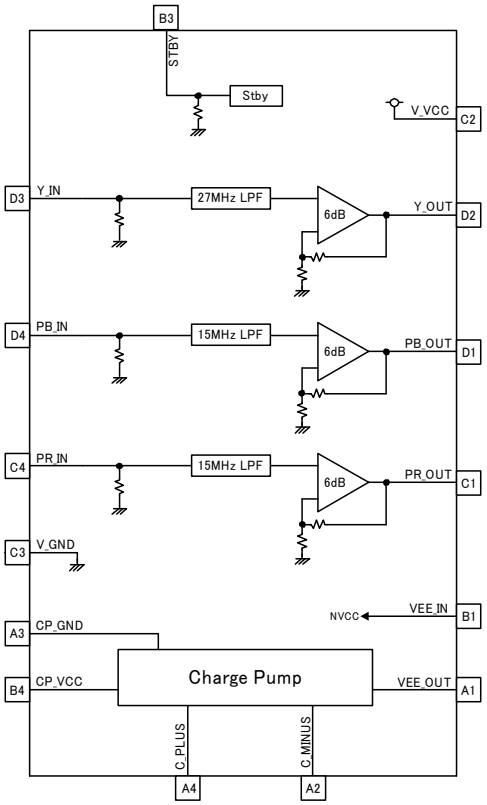

Fig.2. Block diagram

■Pin assignment

Symbol	Pin name	Symbol	Pin name
A1	VEE_OUT	C1	PR_OUT
A2	C_MINUS	C2	V_VCC
A3	CP_GND	C3	V_GND
A4	C_PLUS	C4	PR_IN
B1	VEE_IN	D1	PB_OUT
–	–	D2	Y_OUT
B3	STBY	D3	Y_IN
B4	CP_VCC	D4	PB_IN

Table. 1. Pin assignment

■Cautions on use

(1) Absolute maximum ratings
If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you think of a case in which absolute maximum ratings are exceeded, enforce fuses or other physical safety measures and investigate how not to apply the conditions under which absolute maximum ratings are exceeded to LSI.

(2) VEE line
Connect VEE_IN(B1) and VEE_OUT(A1) as shortly as possible on a board.

(3) GND line
Connect CP_GND(A3) and V_GND(C3) to board's GND layer with thick line as shortly as possible. When every GND line's common impedance becomes large, the noise characteristic sometimes deteriorates.

(4) VCC line
Short CP_VCC(B4) and V_VCC(C2) on the board, and supply voltage from the identical power. At the same time, place decoupling capacitor near the VCC pins.

(5) Cross talk
Board layout affects the cross talk. Draw low impedance line such as the GND line in-between so the line will minimize interference among the video signals.

(6) The noise characteristic of video signal
Board layout affects the noise characteristic of video signal. Draw low impedance line such as the GND line in-between so the line will minimize interference among the video signals.

(7) Thermal design
Perform thermal design in which there are adequate margins by taking into account the allowable power dissipation in actual states of use.

(8) Shorts between pins and miss-installation
When mounting the LSI on a board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is miss-installed and the power is turned on, the LSI may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the LSI or between a pin and a power supply or a pin and GND.

(9) Operation in strong magnetic fields
Adequately evaluate use in a strong magnetic field, since there is a possibility of malfunction.

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