High-Performance Video System Drivers

4-output DVD System Video Driver

Pb Free ROHM Electronic Components RoHS Directive Compliance

BH76071FJ

No.11065EAT09

●Description

The BH76071FJ is a system video driver that integrated three output wideband video drivers with built-in LPF corresponding to the high-definition television and one output video driver with built-in LPF corresponding to the composite video signal in 1chip. It is suitable for the set not equipped with type S terminal.

●Features

1) Built-in 4-output video driver, supporting PY, PB, PR, and CVBS
2) Supports D4 broadband standard
3) Built-in 6 dB amp
4) Built-in LPF for noise elimination (component: f = 30 MHz(8^{th})/13.5 MHz(6^{th}), composite: f = 6.75 MHz(6^{th}))
5) Built-in mute function
6) Enables two load drivers per driver channel
7) Usable for output capacitor less drivers (only 1 channel at same time)

●Applications

DVD/BD players, DVD/BD recorders, and other video devices such as DSC, DVC, STB, TV

●Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VCCmax	7.0	V
Power dissipation	Pd	820 *1	mW
Input voltage	VIN	-0.3 to (VCC+0.3)	V
Storage temperature	Tstg	-55 to +125	℃

*1 When mounted on a 70 mm × 70 mm × 1.6 mm glass epoxy substrate(1layer).
Reduced by 8.2 mW per 1℃ when Ta =25℃ or higher.

●Operation Range

Parameter	Symbol	Ratings	Unit
Supply voltage	VCC	4.5 to 5.5	V
Operating temperature	Topr	-40 to +85	℃

●Electrical Characteristics (unless otherwise noted, Ta = 25℃,VCC = 5V)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
VCC current 1	ICC1	32	45	58	mA	No signal, 30 MHz LPF is selected during 4ch ACT
VCC current 2 *2	ICC2	—	45	—	mA	No signal, 30 MHz LPF is selected during CVBS_OUT MUTE
VCC current 3 *2	ICC3	—	45	—	mA	No signal, 30 MHz LPF is selected during component MUTE
VCC current 4 *2	ICC4	—	45	—	mA	No signal, 13.5 MHz LPF is selected during 4ch ACT
CVBS_OUT voltage gain	G_{V1}	5.5	6.0	6.5	dB	Vin=1.0Vp-p, f=100kHz
PY/PB/PR_OUT voltage gain	G_{V2}	5.5	6.0	6.5	dB	Vin=0.7Vp-p, f=100kHz
Maximum output level	V_{omV}	2.6	2.9	—	Vp-p	THD=1 % f=10kHz
6.75 MHz LPF frequency characteristics 1	G_{f1675}	-1.5	-0.5	0.5	dB	Vin=1.0Vp-p, f=6.75MHz/100kHz
13.5MHz LPF frequency characteristics 1	G_{f1135}	-1.5	-0.5	0.5	dB	Vin=0.7Vp-p, f=13.5M/Hz100kHz
30MHz LPF frequency characteristics 1	G_{f1300}	-3.0	-1.0	1.0	dB	Vin=0.7Vp-p, f=30MHz/100kHz
6.75MHz LPF frequency characteristics 2	G_{f2675}	—	-48	-30	dB	Vin=1.0Vp-p, f=27MHz/100kHz
13.5MHz LPF frequency characteristics 2	G_{f2135}	—	-48	-30	dB	Vin=0.7Vp-p, f=54MHz/100kHz
30MHz LPF frequency characteristics 2	G_{f2300}	—	-35	-20	dB	Vin=0.7Vp-p, f=74.25MHz/100kHz
MUTE attenuation	M_T	—	-65	-55	dB	Vin=1.0Vp-p, f=4.43MHz
Cross talk between channels	C_T	—	-65	-55	dB	Vin=1.0Vp-p, f=4.43MHz
PB/PR_IN input impedance	Zin	100	150	200	kΩ	
Control pin input voltage = H	V_{thH}	2.0	—	VCC	V	
Control pin input voltage = L	V_{thL}	0.0	—	0.8	V	
Control pin input impedance	Rin	100	150	200	kΩ	
Differential gain *2	D_G	—	0.5	—	%	Vin = 1.0 Vp-p, Standard stair-step signal input
Differential phase *2	D_P	—	0.5	—	deg	Vin=1.0 Vp-p, Standard stair-step signal input
S/N *2	S_N	—	75	—	dB	Vin = 1.0 Vp-p, band:100 kHz to 6 MHz 100% white video signal input

*2 Indicates items with design certification (shipment inspections are not performed for these items.)

●Reference Data (1/10)

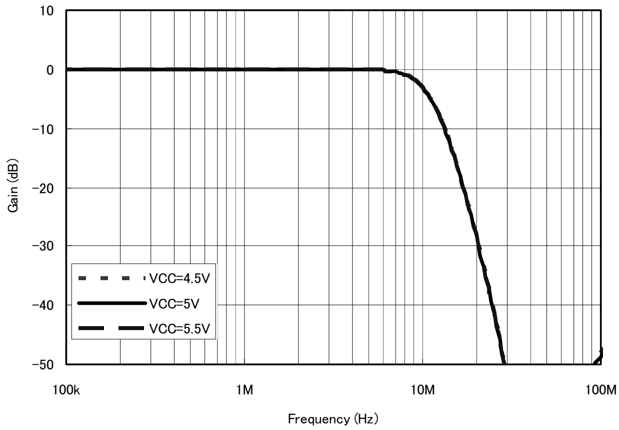


Fig.1 6.75MHzLPF Vcc - Freq. Characteristics

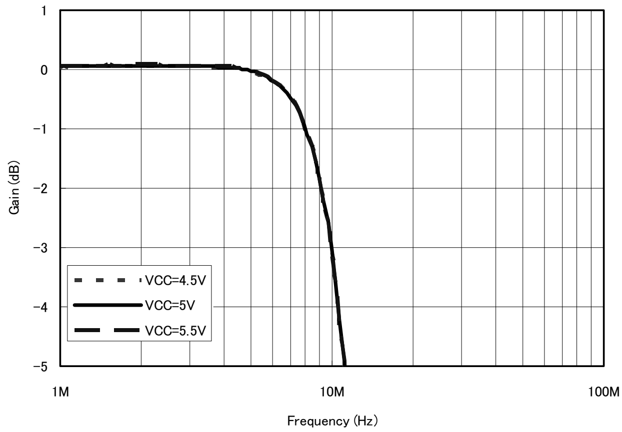


Fig.2 6.75MHzLPF Vcc - Freq. Characteristics
Magnification pass-band

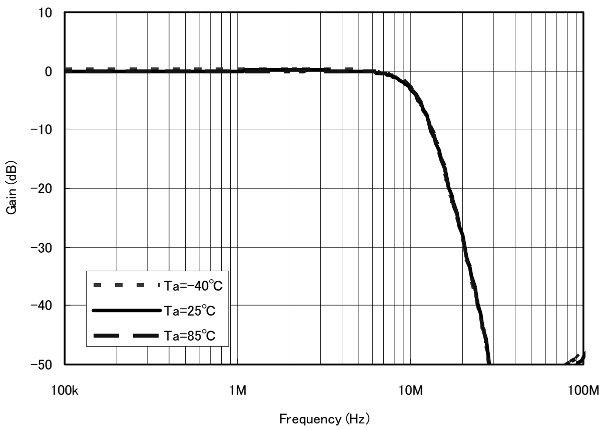


Fig.3 6.75MHz LPF Temp. - Freq. Characteristics

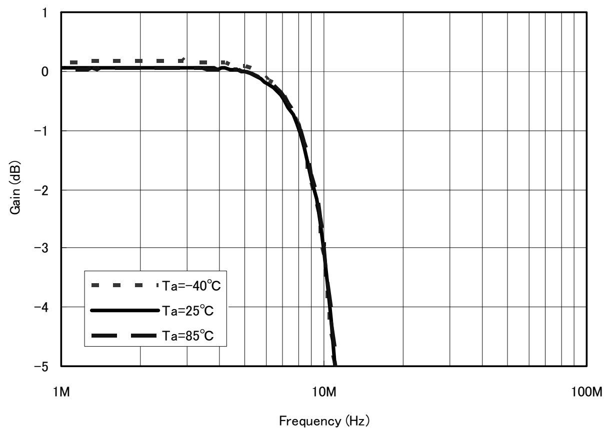


Fig.4 6.75MHz LPF Temp. - Freq. Characteristics
Magnification pass-band

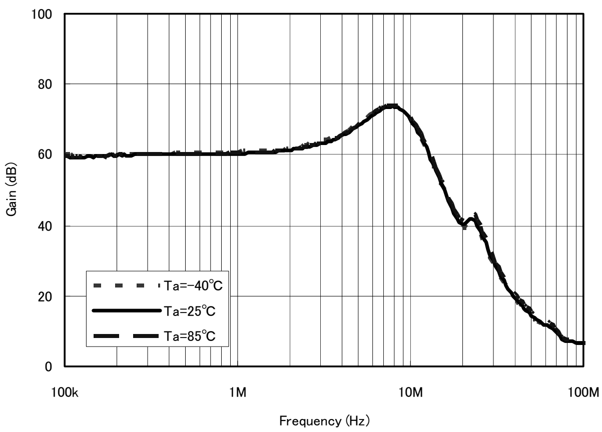


Fig.5 6.75MHzLPF Vcc - Group Delay

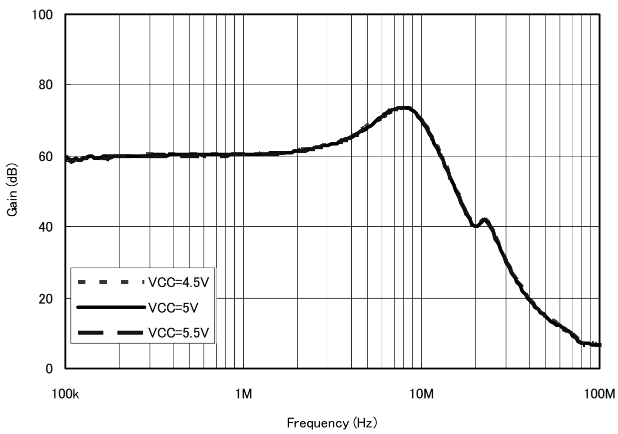


Fig.6 6.75MHzLPF Temp. - Group Delay

●Reference Data (2/10)

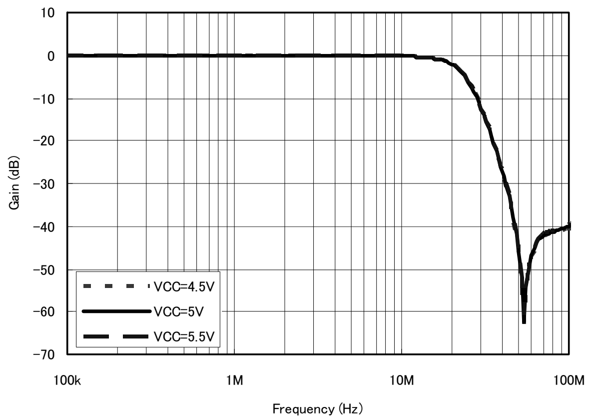


Fig.7 13.5MHzLPF Vcc - Freq. Characteristics

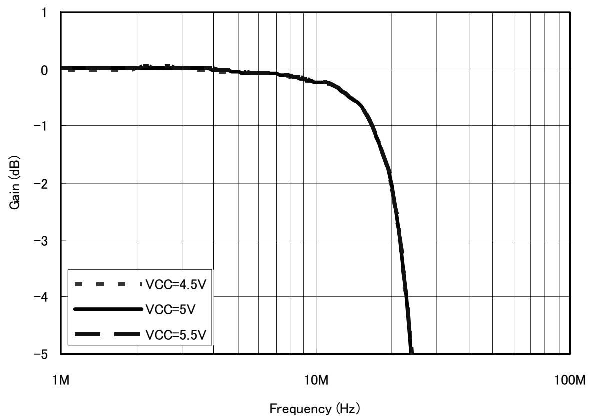


Fig.8 13.5MHzLPF Vcc - Freq. Characteristics
Magnification pass-band

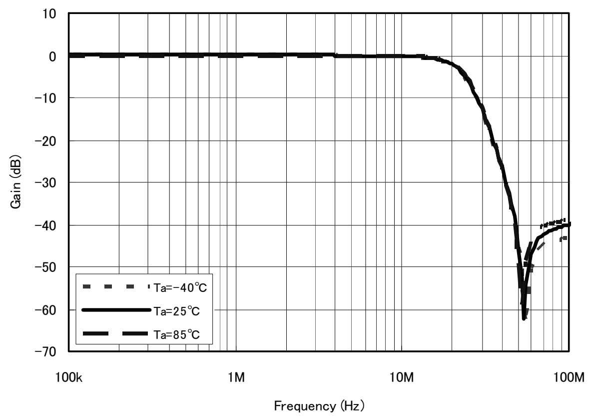


Fig.9 13.5MHzLPF Temp. - Freq. Characteristics

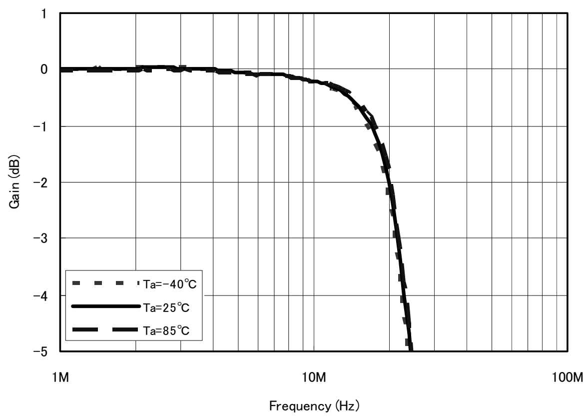


Fig.10 13.5MHzLPF Temp. - Freq. Characteristics
Magnification pass-band

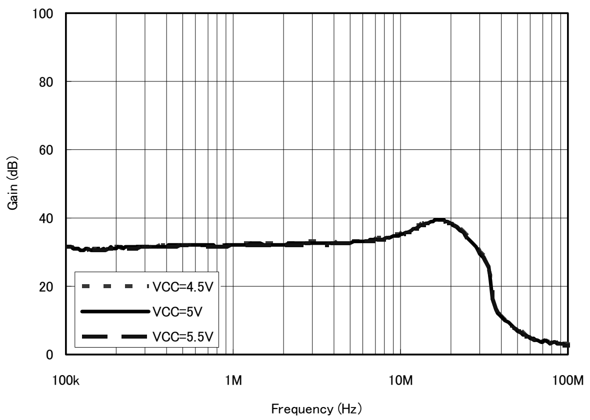


Fig.11 13.5MHzLPF Vcc - Group Delay

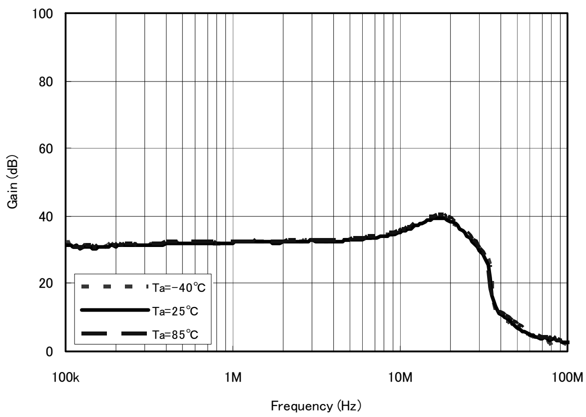


Fig.12 13.5MHzLPF Temp. - Group Delay

●Reference Data (3/10)

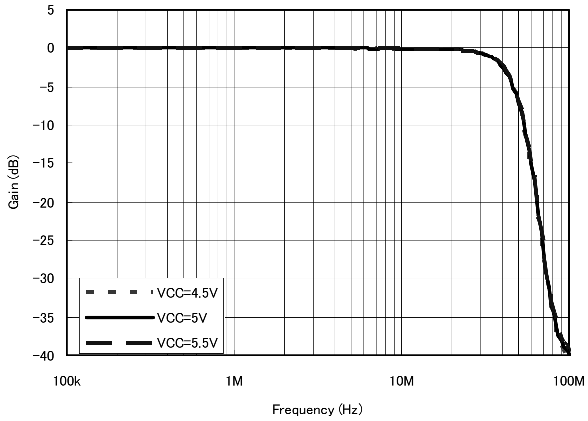


Fig.13 30MHzLPF Vcc - Freq. Characteristics

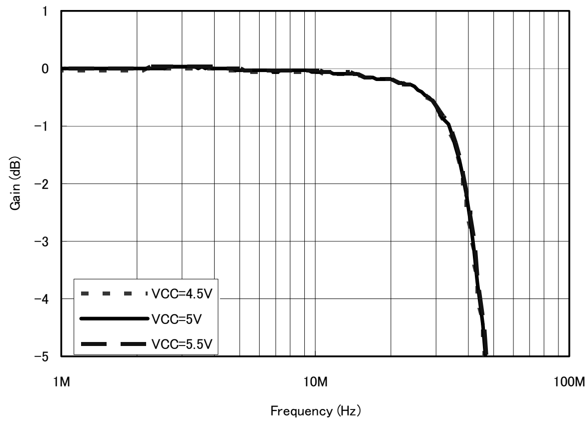


Fig.14 30MHzLPF Vcc - Freq. Characteristics
Magnification pass-band

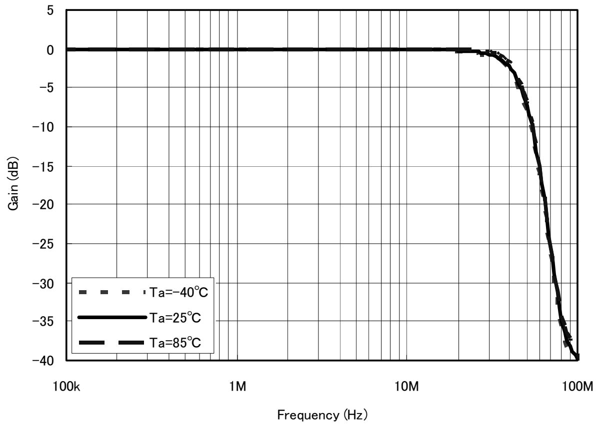


Fig.15 30MHzLPF Temp. Freq. Characteristics

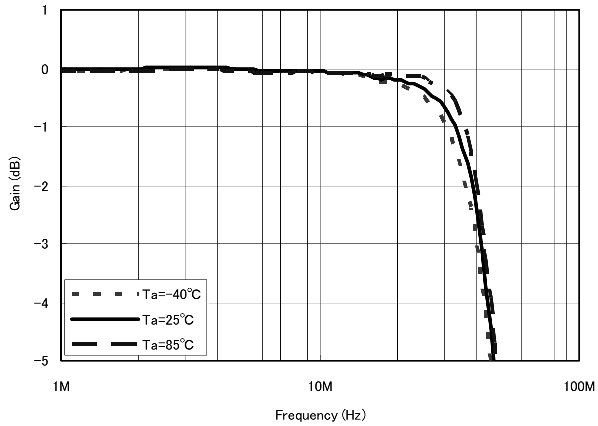


Fig.16 30MHzLPF Temp. - Freq. Characteristics
Magnification pass-band

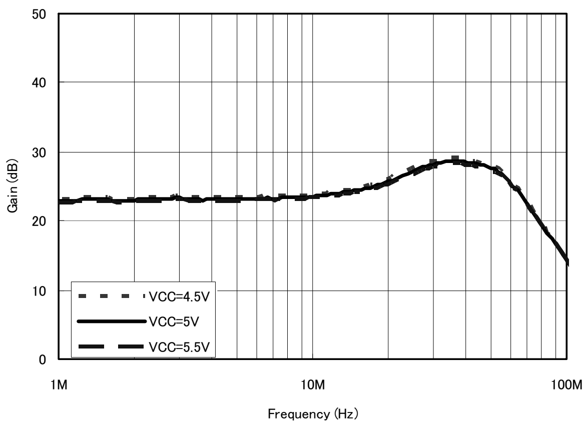


Fig.17 30MHzLPF Vcc - Group Delay

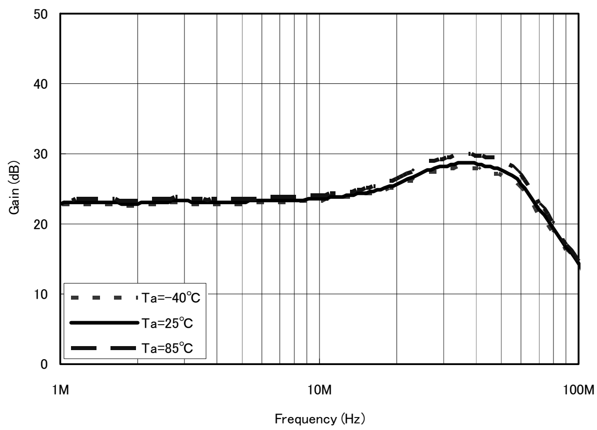


Fig.18 30MHzLPF Temp. - Group Delay

●Reference Data (4/10)

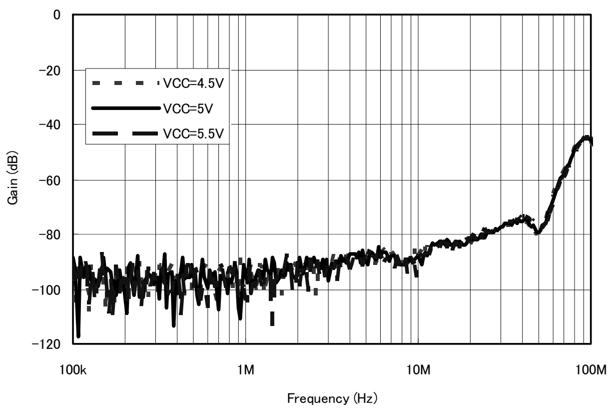


Fig.19 6.75MHzLPF Vcc - MUTE attenuation

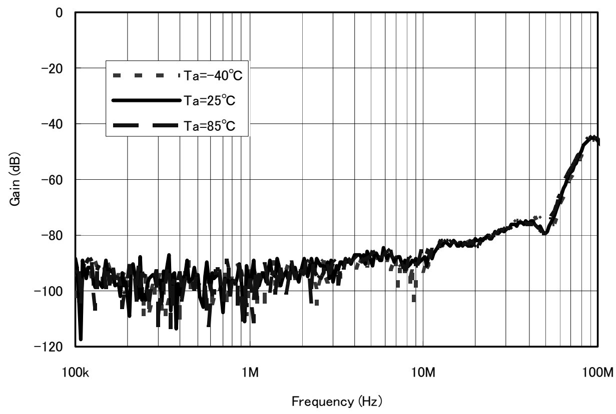


Fig.20 6.75MHzLPF Temp. - MUTE attenuation

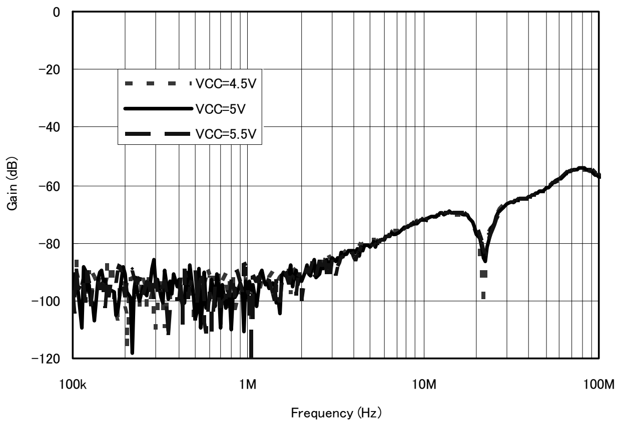


Fig.21 13.5MHzLPF Vcc - MUTE attenuation

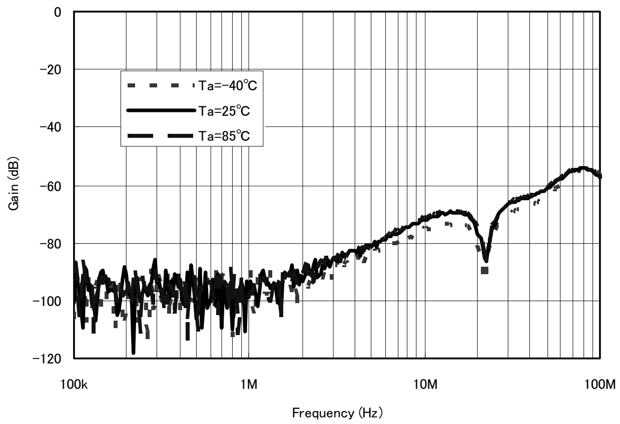


Fig.22 13.5MHzLPF Temp. - MUTE attenuation

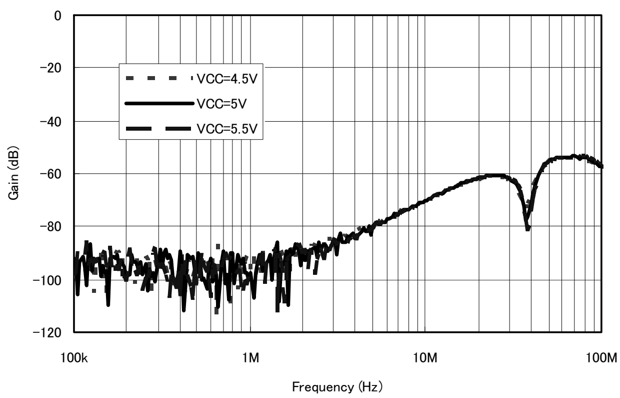


Fig.23 30MHzLPF vcc - MUTE attenuation

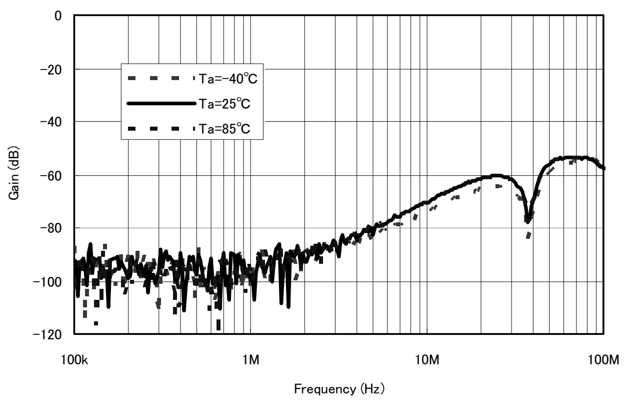


Fig.24 30MHzLPF Temp. - MUTE attenuation

●Reference Data (5/10)

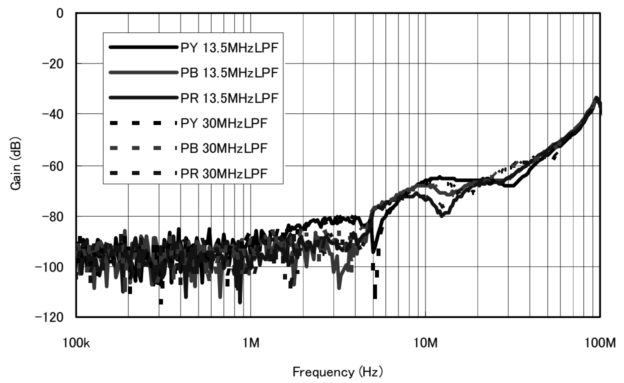


Fig.25 Crosstalk CVBS_IN

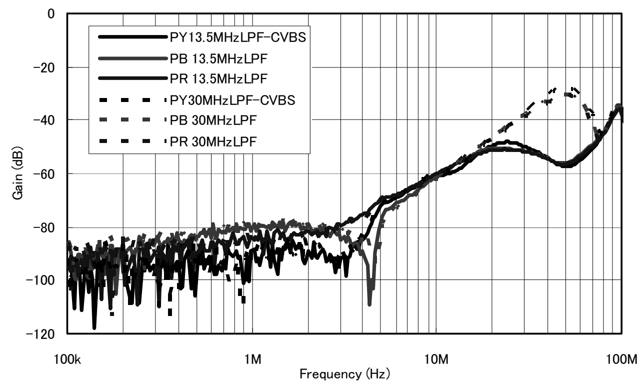


Fig.26 Crosstalk PY_IN

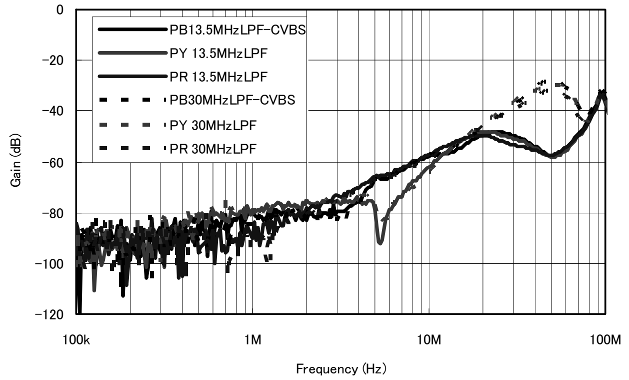


Fig.27 Crosstalk PB_IN

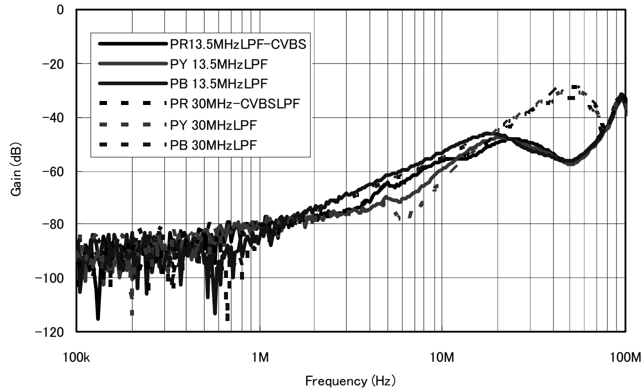


Fig.28 Crosstalk PR_IN

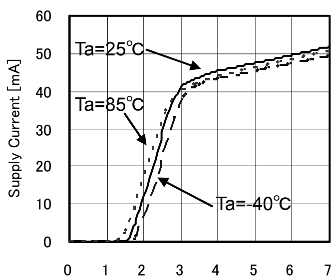


Fig.29 ICC30MHz LPF

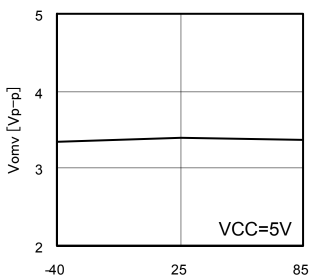


Fig.30 Vomv(CVBS)

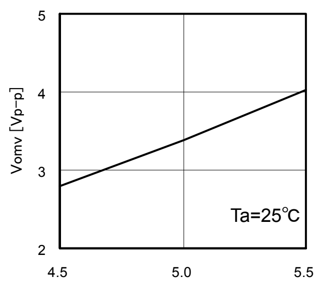


Fig.31Vomv(CVBS)

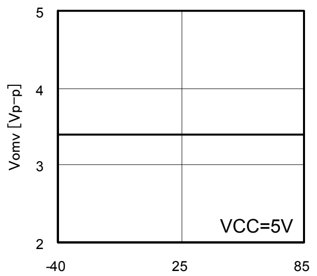


Fig.32 Vomv(PY-13.5MHz)

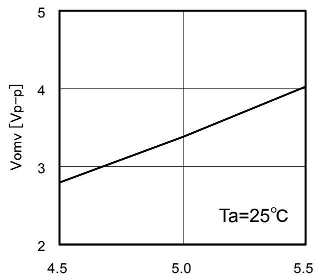


Fig.33 Vomv (PY-13.5MHz)

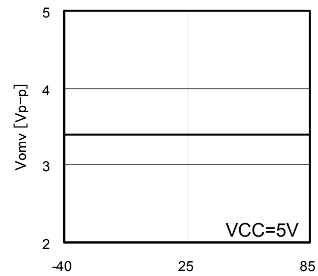


Fig.34 Vomv (PY-30MHz)

●Reference Data (6/10)

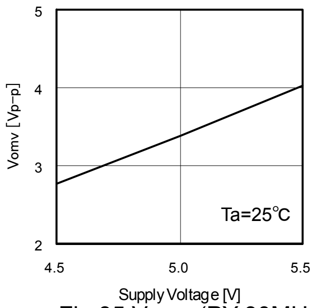


Fig.35 Vomv (PY-30MHz)

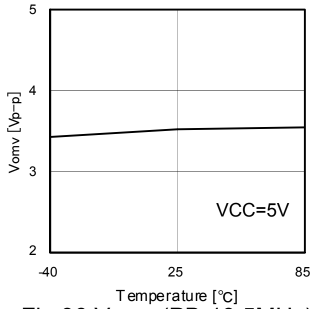


Fig.36 Vomv (PB-13.5MHz)

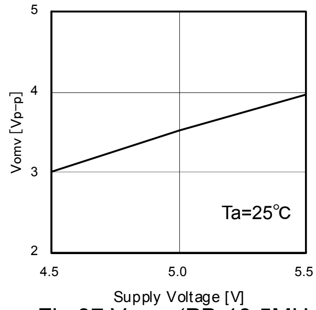


Fig.37 Vomv (PB-13.5MHz)

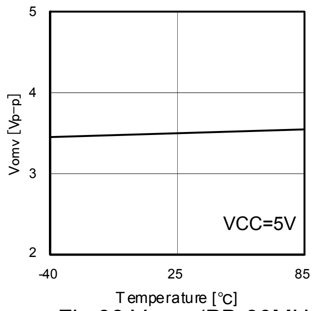


Fig.38 Vomv (PB-30MHz)

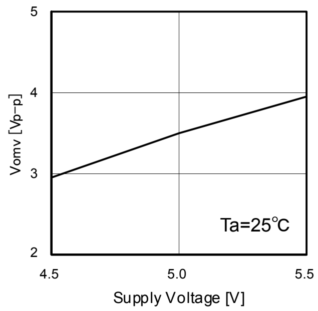


Fig.39 Vomv (PB-30MHz)

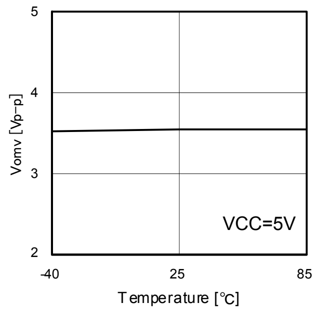


Fig.40 Vomv (PR-13.5MHz)

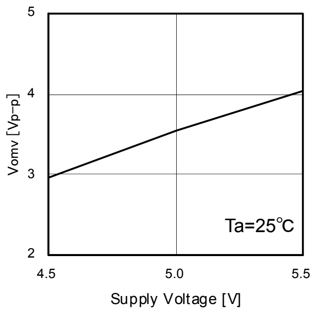


Fig.41 Vomv (PR-13.5MHz)

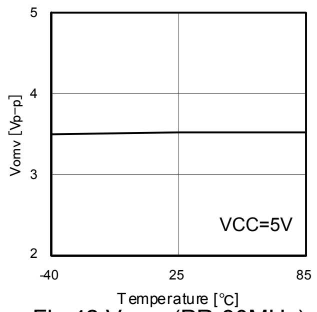


Fig.42 Vomv (PR-30MHz)

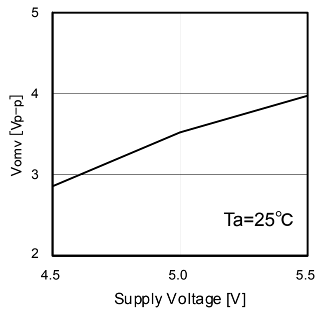


Fig.43 Vomv (PR-30MHz)

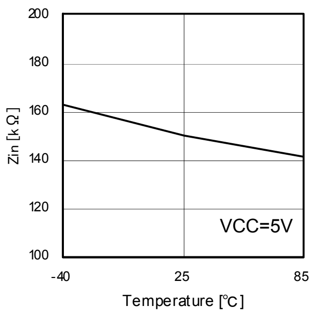


Fig.44 PB/PR_IN input impedance

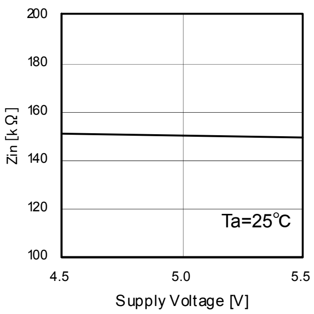


Fig.45 PB/PR_IN input impedance

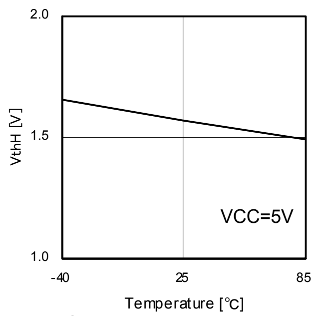


Fig.46 Control pin input voltage=H

● Reference Data (7/10)

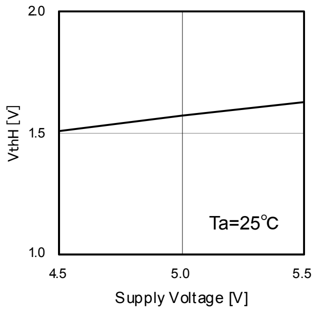


Fig.47 Control pin input voltage=H

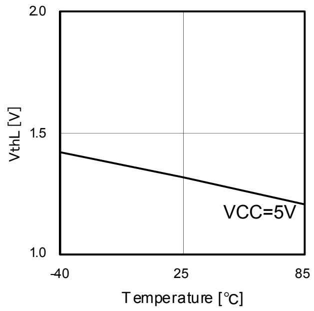


Fig.48 Control pin input voltage=L

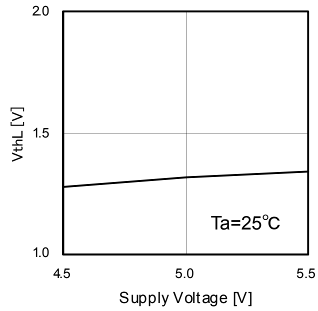


Fig.49 Control pin input voltage=L

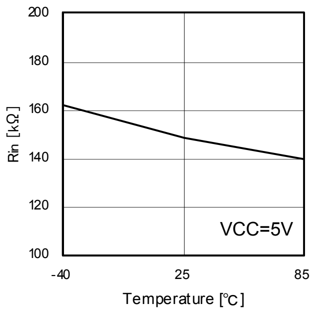


Fig.50 Control pin input impedance

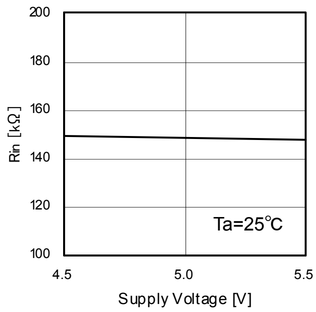


Fig.51 Control pin input impedance

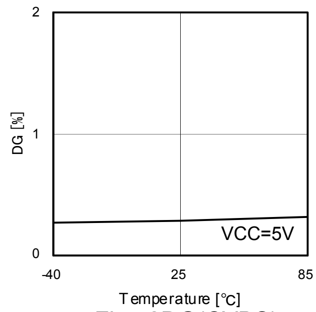


Fig.52DG(CVBS)

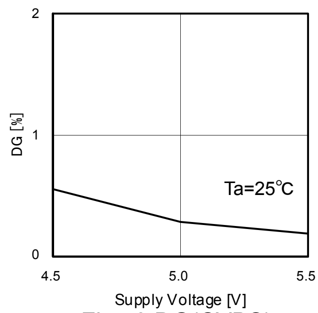


Fig.53 DG(CVBS)

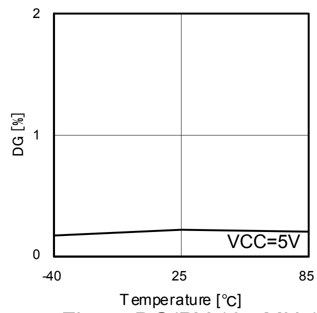


Fig.54 DG(PY-13.5MHz)

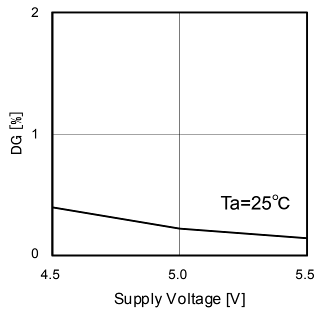


Fig.55 DG(PY-13.5MHz)

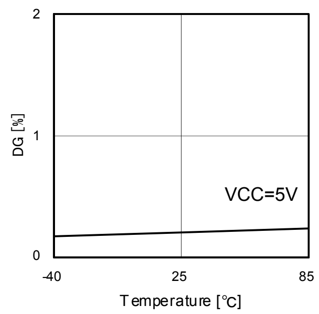


Fig.56 DG(PY-30MHz)

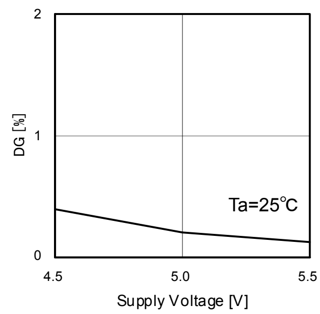


Fig.57 DG(PY-30MHz)

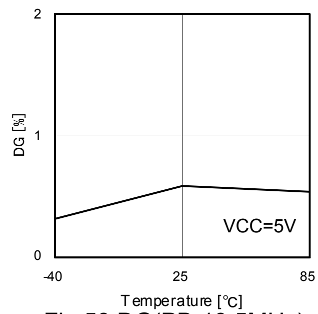


Fig.58 DG(PB-13.5MHz)

●Reference Data (8/10)

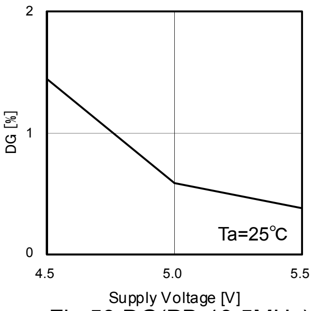


Fig.59 DG(PB-13.5MHz)

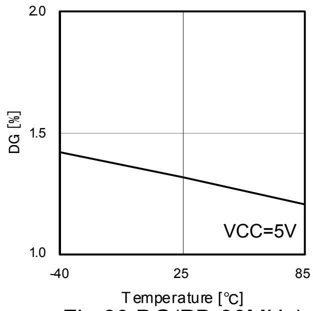


Fig.60 DG(PB-30MHz)

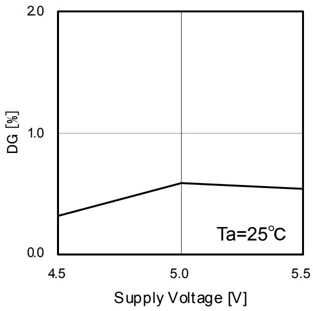


Fig.61 DG(PB-30MHz)

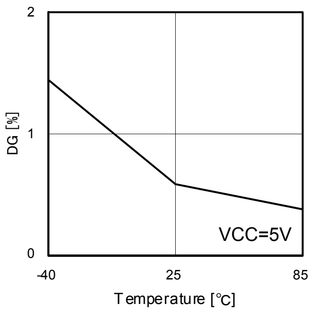


Fig.62 DG(PR-13.5MHz)

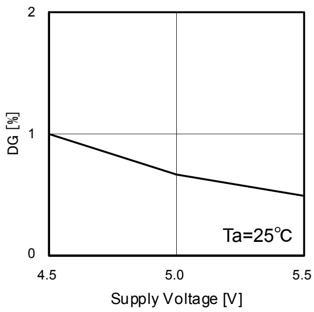


Fig.63 DG(PR-13.5MHz)

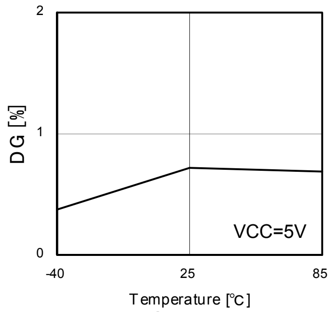


Fig.64 DG(PR-30MHz)

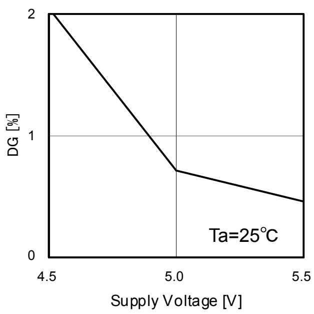


Fig.65 DG(PR-30MHz)

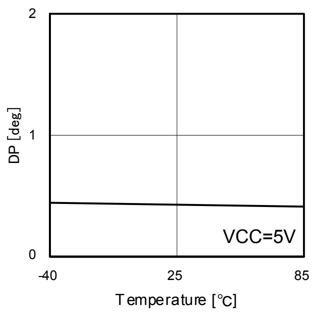


Fig.66 DP(CVBS)

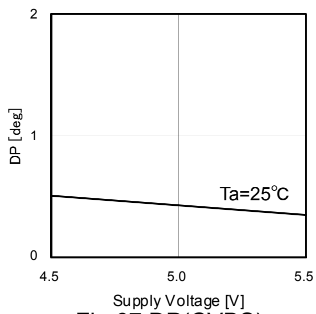


Fig.67 DP(CVBS)

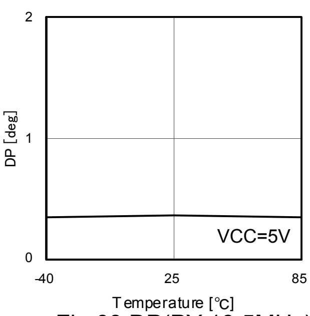


Fig.68 DP(PY-13.5MHz)

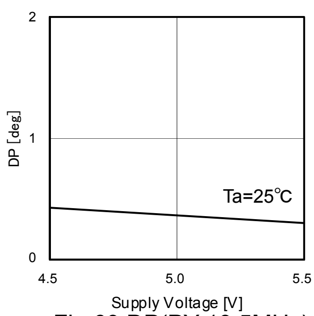


Fig.69 DP(PY-13.5MHz)

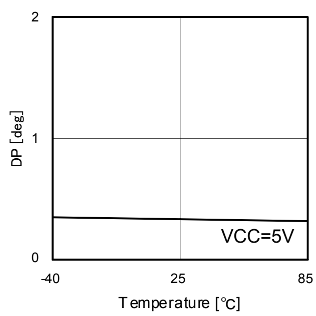


Fig.70 DP(PY-30MHz)

●Reference Data (9/10)

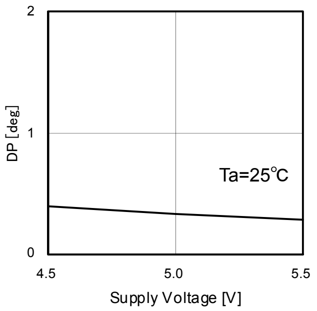


Fig.71 DP(PY-30MHz)

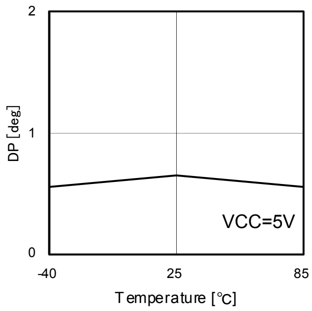


Fig.72 DP(PB-13.5MHz)

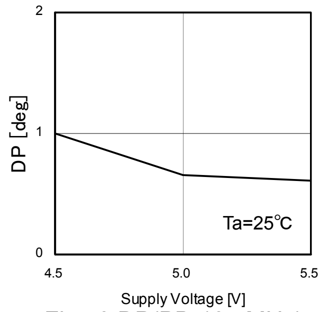


Fig.73 DP(PB-13.5MHz)

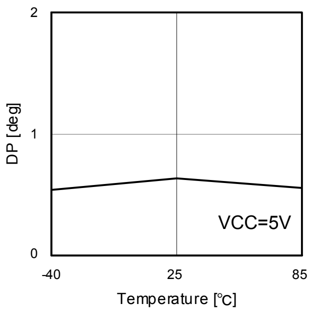


Fig.74 DP(PB-30MHz)

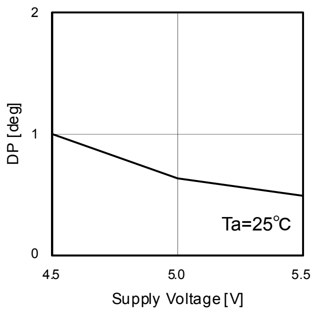


Fig.75 DP(PB-30MHz)

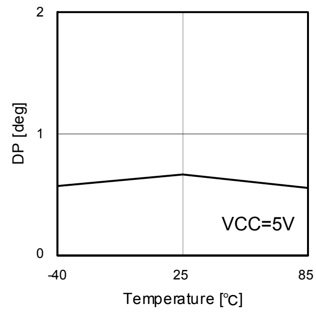


Fig.76 DP(PR-13.5MHz)

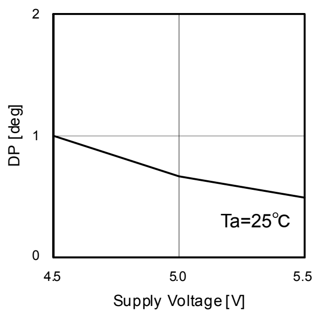


Fig.77 DP(PR-13.5MHz)

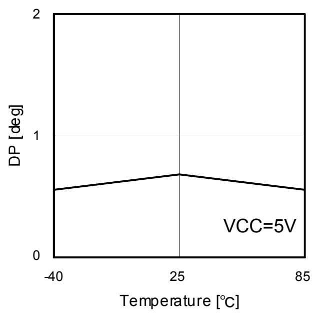


Fig.78 DP(PR-30MHz)

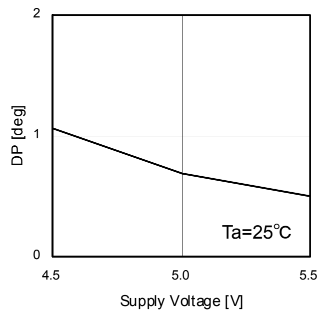


Fig.79 DP(PR-30MHz)

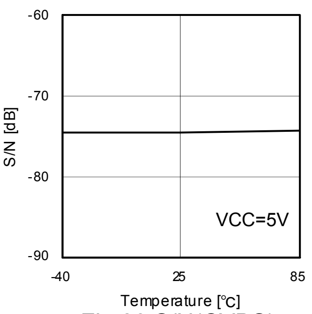


Fig.80 S/N(CVBS)

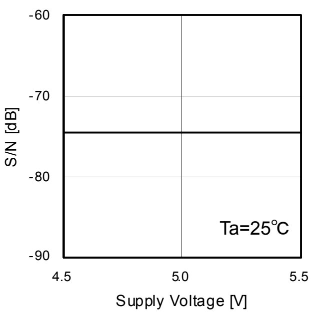


Fig.81 S/N(CVBS)

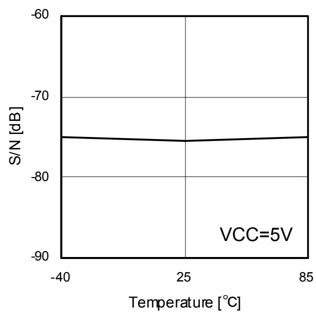


Fig.82 S/N(PY-13.5MHz)

●Reference Data (10/10)

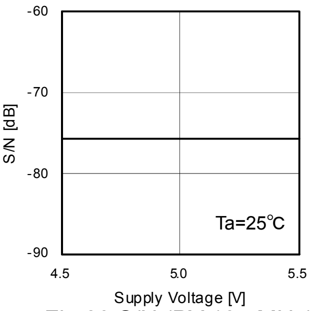


Fig.83 S/N (PY-13.5MHz)

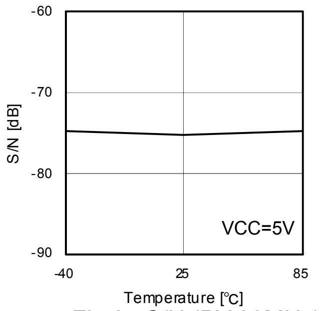


Fig.84 S/N (PY-30MHz)

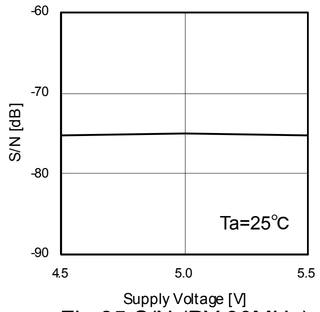


Fig.85 S/N (PY-30MHz)

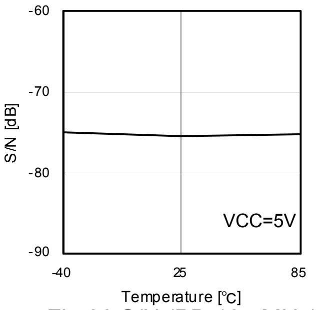


Fig.86 S/N (PB-13.5MHz)

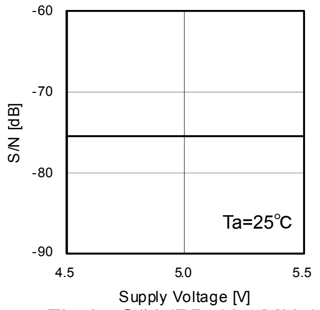


Fig.87 S/N (PB-13.5MHz)

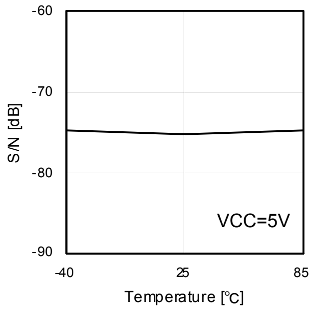


Fig.88 S/N (PB-30MHz)

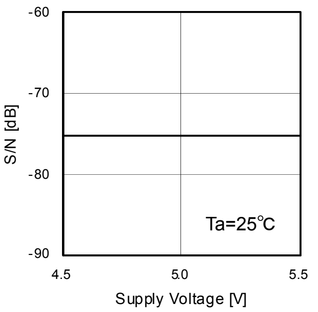


Fig.89 S/N (PB-30MHz)

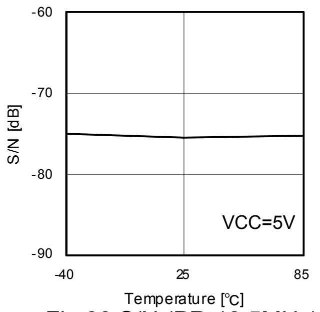


Fig.90 S/N (PR-13.5MHz)

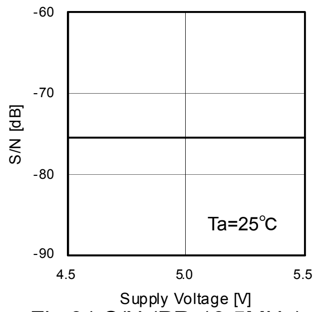


Fig.91 S/N (PR-13.5MHz)

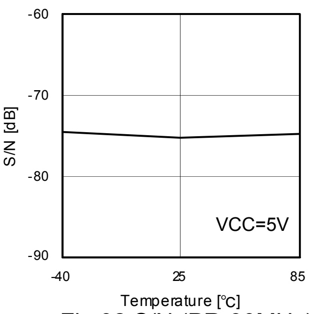


Fig.92 S/N (PR-30MHz)

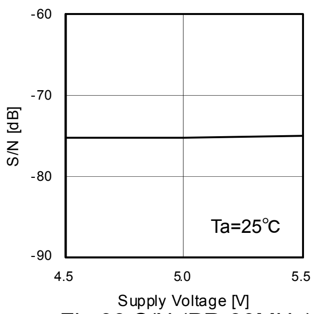


Fig.93 S/N (PR-30MHz)

●Block Diagram

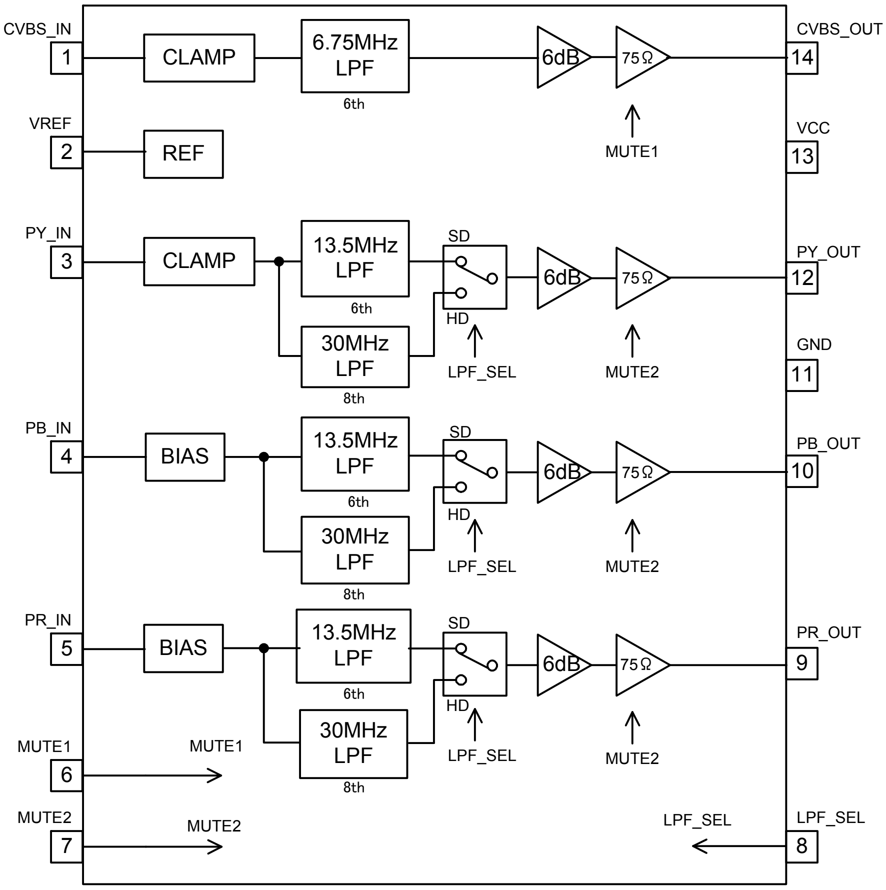


Fig.94 Block Diagram

●Control Specifications

Pin	Function
6pin (MUTE1)	Mute control of composite output (CVBS_OUT) *3 L : MUTE H : Normal operation
7pin (MUTE2)	Mute control of component outputs (PY/PB/PR_OUT) *3 L : MUTE H : Normal operation
8pin (LPF_SEL)	LPF selector for component L : 13.5 MHz LPF H : 30 MHz LPF

*3 When operating in mute mode, each output pin normally outputs the bias voltage when there is no signal.

●Pin Number / Pin Name

No.	Pin Name	I/O	DESCRIPTION
1	CVBS_IN	I	Video signal input pin Sync tip clamp input LPF=6.75 MHz
2	VREF	I	Bias capacitor connection pin
3	PY_IN	I	Video signal input pin Sync tip clamp input LPF=13.5 MHz/30 MHz
4	PB_IN	I	Video signal input pin Bias input LPF=13.5 MHz/30 MHz
5	PR_IN	I	Video signal input pin Bias input LPF=13.5 MHz/30 MHz
6	MUTE1	I	Mute control of CVBS_OUT L : MUTE H : Normal operation
7	MUTE2	I	Mute control of PY/PB/PR_OUT L : MUTE H : Normal operation
8	LPF_SEL	I	LPF selector for component output L : 13.5 MHz LPF H : 30 MHz LPF
9	PR_OUT	O	Video signal output pin Enable load driving up to 75 Ω (2 drives)
10	PB_OUT	O	Video signal output pin Enable load driving up to 75 Ω (2 drives)
11	GND	I	GND pin
12	PY_OUT	O	Video signal output pin Enable load driving up to 75 Ω (2 drives)
13	VCC	I	Power supply pin
14	CVBS_OUT	O	Video signal output pin Enable load driving up to 75 Ω (2 drives)

●Selection of Application Parts

Method for determining capacity of input coupling capacitor

Input pin	Input impedance Zin	Capacity of input coupling capacitor (recommended value)	Capacity of output coupling capacitor (recommended value)
CVBS/PY_IN	Approximately 10 MΩ	0.1 μF	470 μF to 1000 μF
PB/PR_IN	150 kΩ	1.0 μF	

The HPF includes an input coupling capacitor and an Internal input impedance Zin of the IC. Since the fc value of the HPF is calculated using the following equation (a), above recommended value of capacity for the input capacitor is derived. Usually, the cutoff frequency fc is set several Hz.

$fc = 1 / (2\pi \times C \times Zin)$ ・・・・(a)

A horizontal stripe signal called an "H bar signal" (shown in Fig. 95) is suitable when evaluating sag characteristics and determining the capacity of the capacitor during video signal input, and this type of signal is used instead of a color bar signal to evaluate characteristics and determine capacity.

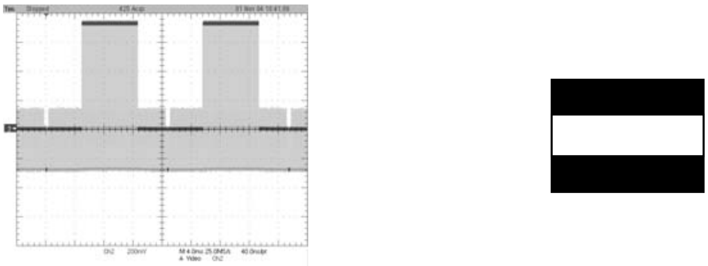


Fig.95 Example of Screen with Obvious Sag (H-bar Signal)

Method for determining capacity of output coupling capacitor

The output pins have an HPF that includes an output coupling capacitor and load resistance R_L (= 150 Ω). When fc is set within the range of 1 Hz to 2 Hz, the capacity of the output coupling capacitor must be within the range of 470 μF to 1000 μF.
With this model, up to two monitors (loads) can be connected (see the connection example in Fig. 96). When there are multiple loads, the number of output coupling capacitors must be increased, or a larger capacitance must be set, According to the table shown below.

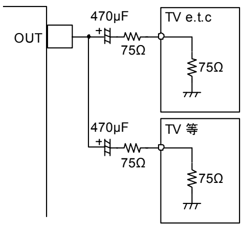


Fig.96(a) Application Circuit 1 (2 Drives)

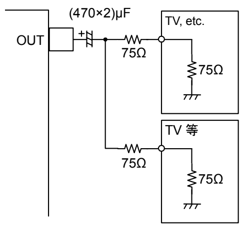


Fig.96(b) Application Circuit 2 (2 Drives)

Application circuit	Number of output capacitors	Capacitance per output capacitor (recommended values)
Fig.96(a)	2	470 μF to 1000 μF (Same as with 1 drive)
Fig.96(b)	1	(2 × 470 to 1000) μF

●Evaluation Board Layout (2 layers)

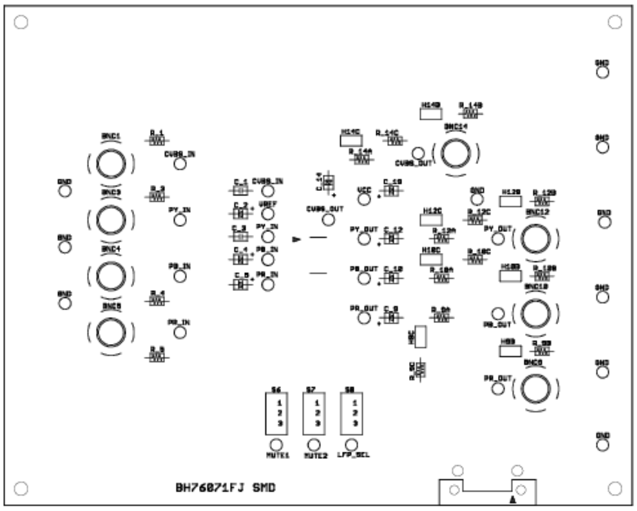


Fig.97 Top Surface Silk

Fig.98 Bottom Surface Silk

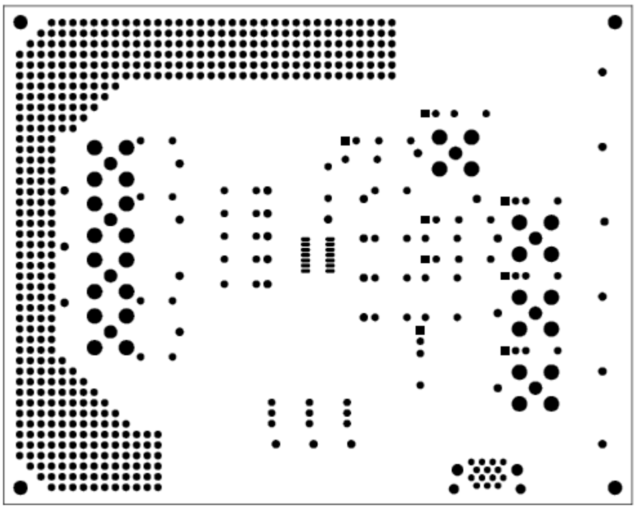


Fig.99 Top Surface Resist

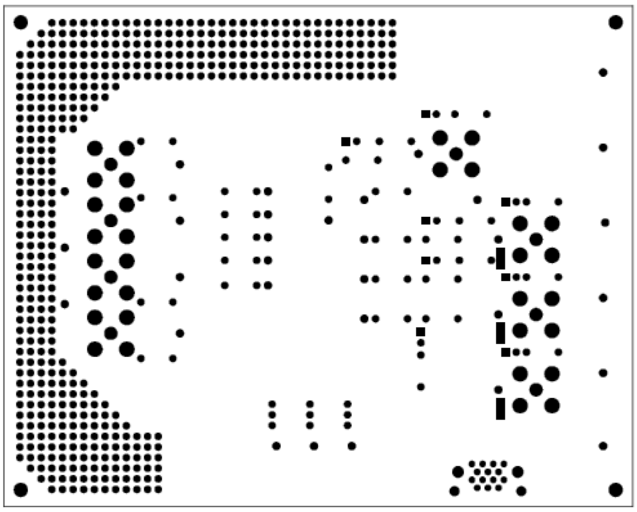


Fig.100 Bottom Surface Resist

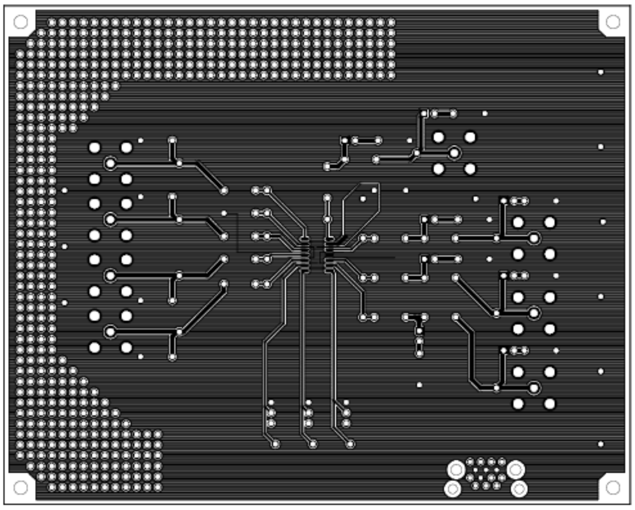


Fig.101 Top Surface Pattern

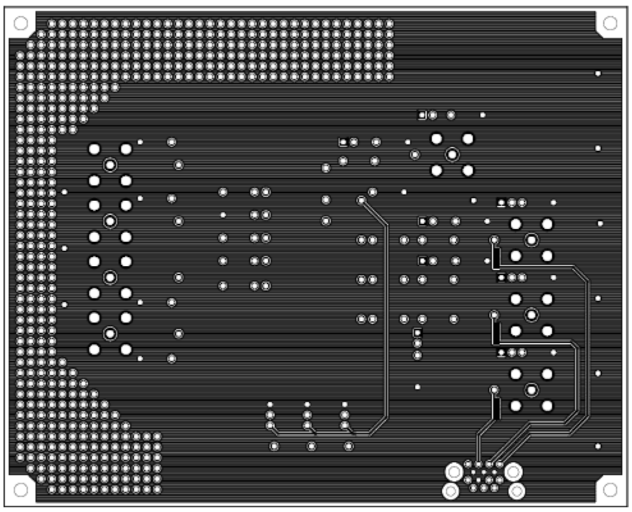


Fig.102 Bottom Surface Pattern

●Evaluation Board Circuit Diagram

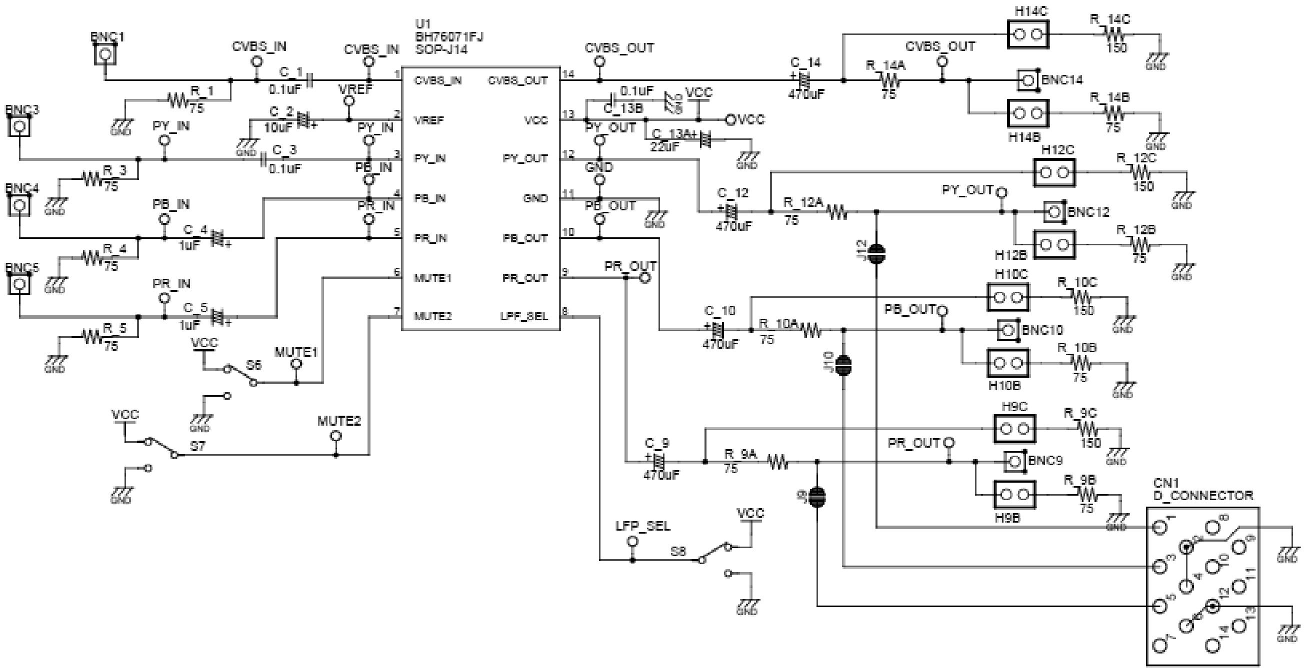


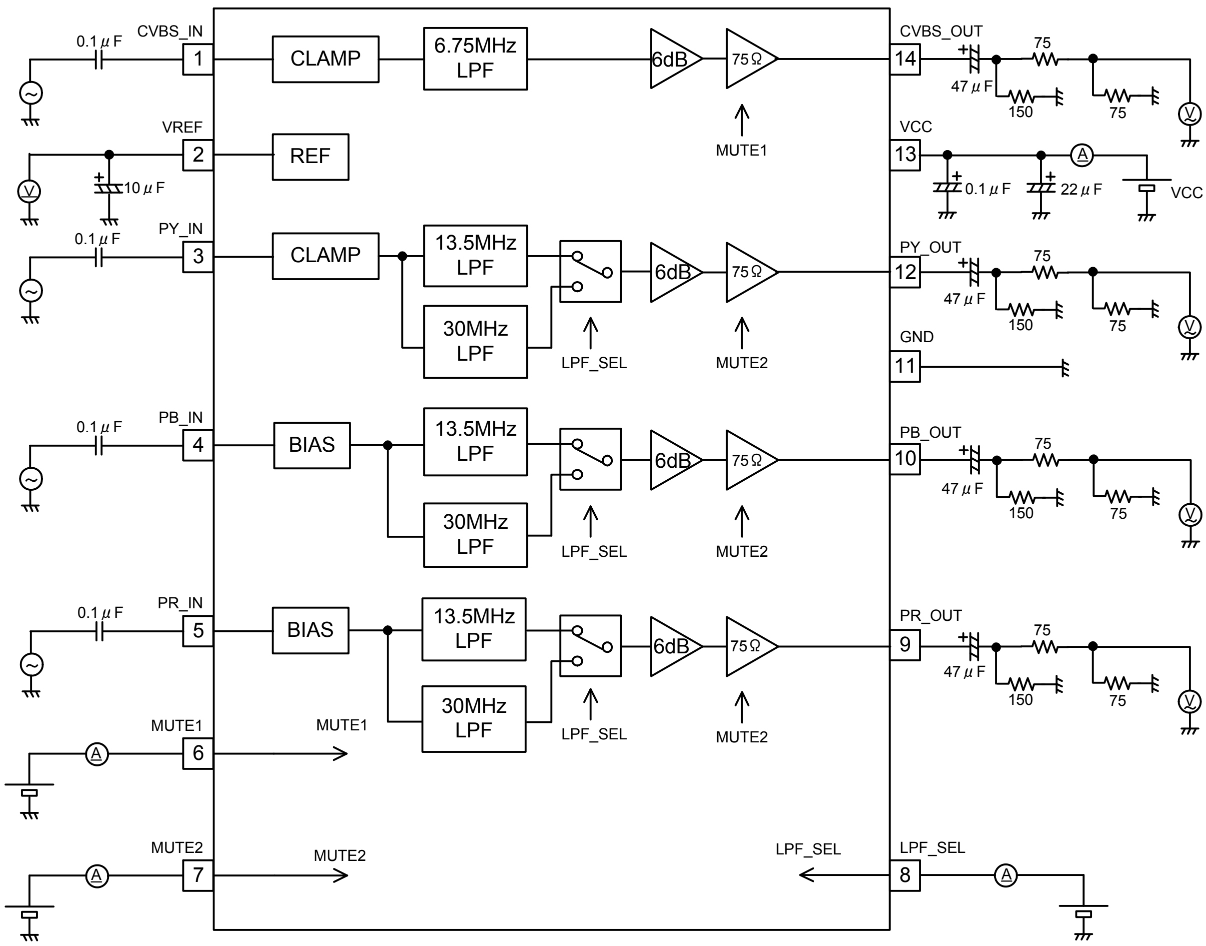
Fig.103 Evaluation Board Circuit Diagram

●Description of External Parts

Symbol	Function	Recommended value	Comments
C_1, C_3	Input coupling capacitor	0.1 µF	Refer to *1
C_2	Bias capacitor	10 µF	Refer to *1
C_4, C_5	Input coupling capacitor	1 µF	Refer to *1
C_9, C_10, C_12, C_14	Output coupling capacitor	470 µF	Recommended Electrolytic Capacitor
C_13A	Decoupling capacitor	22 µF	Refer to *1
C_13B	Decoupling capacitor	0.1 µF	Refer to *1
R1, R3, R4, R5	Input terminating resistor	75 Ω	
R9_A, R10_A, R12_A, R13_A R9_B, R10_B, R12_B, R13_B	Output terminating resistor	75 Ω	
R9_C, R10_C, R12_C, R13_C	Output terminating resistor	150 Ω	For comparing number of drives (for 2 drives)
BNC1, BNC3, BNC4, BNC5	BNC connector for video signal input		
BNC9, BNC10, BNC12, BNC14	BNC connector for video signal output		
D-CONNECTOR	Type D-connector for video signal output		

*1 : Recommended Capacitance Tolerance code B type Ceramic Capacitor

●Test Circuit Diagram



※ Test circuits are used for shipment inspections, and differ from application circuits.

Fig.104 Test Circuit Diagram

●Application Circuit

(1) Use output coupling capacitor (Enable load driving up to 75 Ω (2 drives))

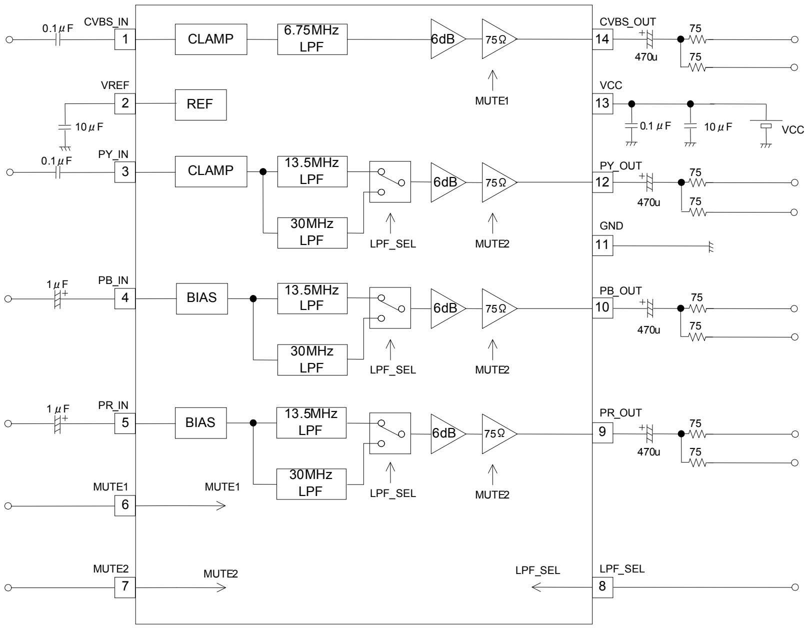


Fig.105 Application Circuit 1

See page 15/22 for description of how to determine the capacitance of an input/output coupling capacitor.
Use when the terminating impedance of the clamp input pins (1 and 3pin) is 1 kΩ or less.

(2) Without output coupling capacitors (Enable load driving up to 150 Ω (1 drive only))

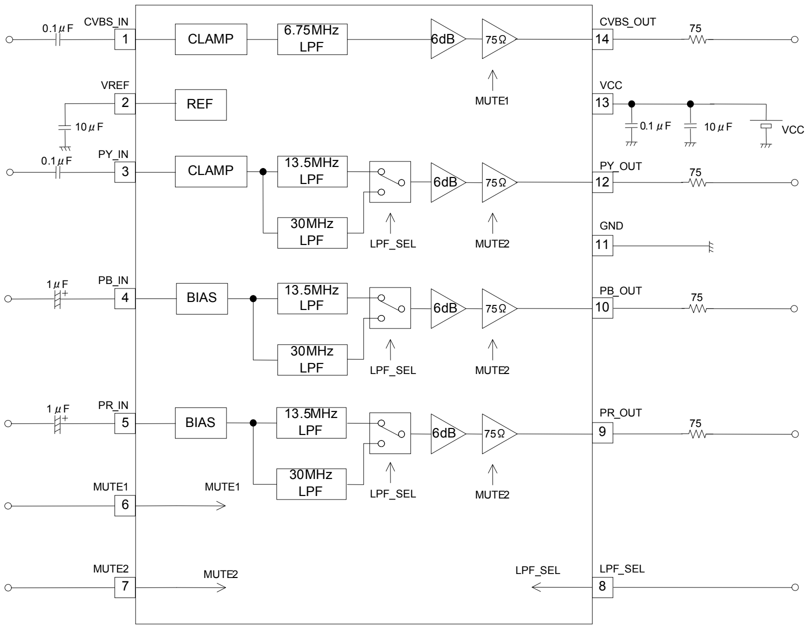


Fig.106 Application Circuit 2

See page 15/22 for description of how to determine the capacitance of an input/output coupling capacitor.

Use when the terminating impedance of the clamp input pins (1 and 3pin) is 1 kΩ or less.
The frequency characteristic of the low area can realize the improvement of the SAG characteristic, the substrate space's and part cost's being able to be reduced without output coupling capacitors.
However, because the DC current flows to the set connected this IC without output coupling Capacitors, be careful of the specification of the connection set and so on sufficiently.
Use a substrate in equal to or more than 4 layers when mounts of the IC without output coupling capacitors from the viewpoint of the permission loss.

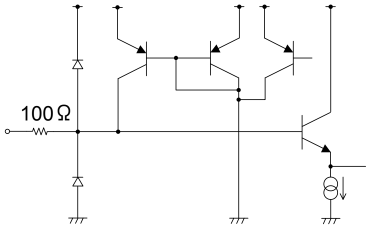
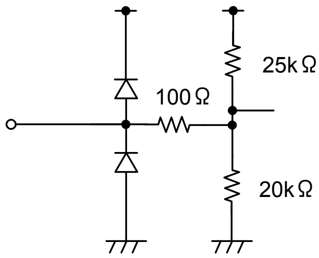
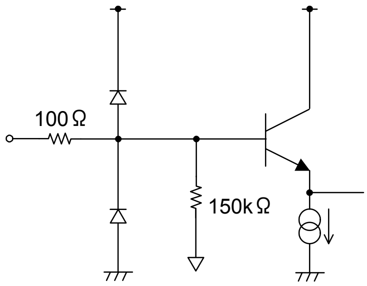
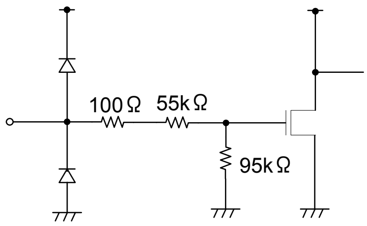
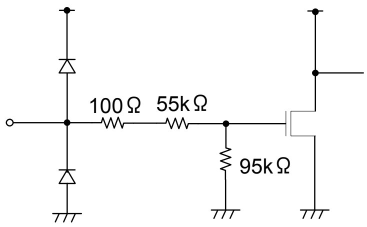
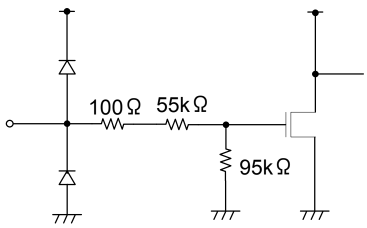
●Application Circuit (Cont.)

Reference data

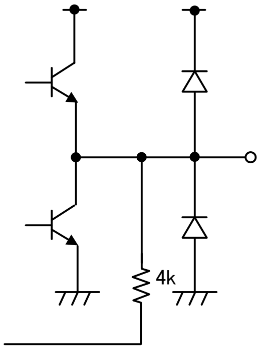
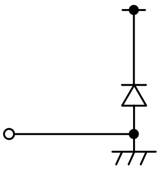
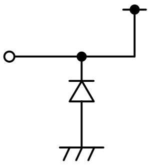
		With output capacitors	Without output capacitors	Conditions
ICC		45mA	70mA	
CVBS	DG	0.24%	0.26%	Vin = 1.0 Vp-p, Standard stair-step signal input
	DP	0.36deg	0.31deg	Vin=1.0 Vp-p, Standard stair-step signal input
	S/N	-74.5dB	-74.7dB	Vin = 1.0 Vp-p, band:100 kHz to 6 MHz 100% white video signal input
PY	DG	0.23%	0.26%	Vin = 1.0 Vp-p, Standard stair-step signal input
	DP	0.33deg	0.26deg	Vin=1.0 Vp-p, Standard stair-step signal input
	S/N	-75.2dB	-75.2dB	Vin = 1.0 Vp-p, band:100 kHz to 6 MHz 100% white video signal input
PB	DG	0.56%	0.81%	Vin = 1.0 Vp-p, Standard stair-step signal input
	DP	0.54deg	0.59deg	Vin=1.0 Vp-p, Standard stair-step signal input
	S/N	-75.0dB	-75.1dB	Vin = 1.0 Vp-p, band:100 kHz to 6 MHz 100% white video signal input
PR	DG	0.65%	0.62%	Vin = 1.0 Vp-p, Standard stair-step signal input
	DP	0.60deg	0.50deg	Vin=1.0 Vp-p, Standard stair-step signal input
	S/N	-74.5dB	-75.3dB	Vin = 1.0 Vp-p, band:100 kHz to 6 MHz 100% white video signal input

* When mounted on a 70 mm × 70 mm × 1.6 mm glass epoxy substrate (4layer). Pd=1.45W
  Reduced by 14.5 mW per 1℃ when Ta =25℃ or higher.
* When mounted on a 70 mm × 70 mm × 1.6 mm glass epoxy substrate (1layer). Pd=0.82W
  Reduced by 8.2 mW per 1℃ when Ta =25℃ or higher.

●I/O Equivalent Circuit Diagrams (page 1 of 2)

Pin No.	Pin name	Standard potential	I/O equivalent circuit diagram	Description of pins
1	CVBS_IN	1.5V		Video signal input pin Sync tip clamp input
3	PY_IN			
2	VREF	2.2V		Bias capacitor connection pin
4	PB_IN	2.9V		Video signal input pin Bias input
5	PR_IN			
6	MUTE1	0V		Mute control of CVBS_OUT L : MUTE H : Normal operation
7	MUTE2	0V		Mute control of PY/PB/PR_OUT L : MUTE H : Normal operation
8	LPF_SEL	0V		Composite output LPF select L : 13.5 MHz LPF H : 30 MHz LPF

●I/O Equivalent Circuit Diagrams (page 2 of 2)

Pin No.	Pin name	Standard potential	I/O equivalent circuit diagram	Description of pins
9	PR_OUT	1.9V		Video signal output pin Enable load driving up to 75 Ω (2 drives)
10	PB_OUT			
12	PY_OUT	0.7V		
14	CVBS_OUT			
11	GND	0V		GND pin
13	VCC	5V		Power supply pin

Note 1) The above DC potential is only for when VCC = 5 V. This is a reference value, and it is not guaranteed.
Note 2) Numerical values in the figures are design values, and standards compliance is not guaranteed.

●Notes for use

1. Numerical values and data that are cited are representative design values and their values are not guaranteed.

2. We are confident in recommending the above application circuit example, but we ask that you carefully check the characteristics before using it. When using it with different external part constants, differences between the external part and this IC, including not just the static characteristics but also transient characteristics, should be carefully checked to determine adequate margins.

3. Absolute maximum ratings
   If absolute maximum ratings such as applied voltage and operating temperature range are exceeded, the IC may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you are considering circumstances in which an absolute maximum rating may be exceeded, try using a physical safety measure such as a fuse so that conditions that exceed the absolute maximum ratings are not applied to the IC.

4. GND potential
   Even if the voltage of the GND pin is left in an operating state, make it the minimum voltage. Actually confirm that the voltage of each pin does not become a lower voltage than the GND pin, including for transient phenomena.

5. Thermal design
   Thermal design should be done using an ample margin that takes into consideration the allowable dissipation under actual use conditions.

6. Shorts between pins and mounting errors
   When mounting the IC on a board, be careful of the direction of the IC and of misalignment. If the IC is mounted badly and current is passed through it, it may be damaged. The IC also may be damaged if shorted by a foreign substance getting in between IC pins, or between an IC pin and the power supply or GND.

7. Operation in a strong electromagnetic field
   When used within a strong electromagnetic field, evaluate carefully to avoid the risk of operation faults.

8. Place the power supply's decoupling capacitor as close as possible to the VCC pin (PIN 13).

9. Be careful to avoid inserting the IC upside down. When upside down, the electrostatic damage preventing diode may be set to operation mode, depending on the input condition of the CONTROL pin, and the IC may become damaged.

10. If any input pins that use the clamp input method are left OPEN they will oscillate, so unused input pins should instead be connected to GND via a capacitor or else directly connected to VCC.

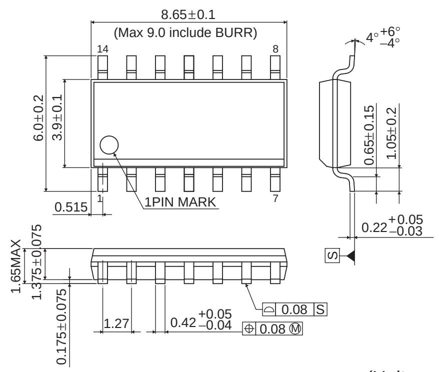
11. Problems such as sync contraction or oscillation may occur if the terminating impedance of the clamp input pins (pins 1 and 3) is high. Fully evaluate the temperature characteristics as well, to keep this value to 1 kΩ or less.

●Ordering part number

B	H		7	6	0	7	1		F	J	-	E	2

- B H — Part No.
- 7 6 0 7 1 — Part No.
- F J — Package, FJ : SOP-J14
- E 2 — Packaging and forming specification, E2: Embossed tape and reel

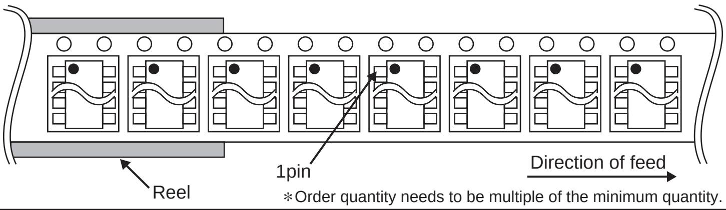
SOP-J14



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Notes

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