AC/DC Drivers

PWM Control IC

BM1P067FJ

● General

The PWM control IC for AC/DC "BM1P067FJ" provides an optimum system for all products that include an electrical outlet.

A built-in start circuit that withstands 650 V helps to keep power consumption low. Both isolated and non-isolated versions are supported, making for simpler design of various types of low-power converters. Switching MOSFET and current detection resistors are external devices, thus achieving a higher degree of freedom in power supply design. The switching frequency is set as fixed. Since current mode control is used, a current limit is imposed in each cycle, and excellent performance is demonstrated in bandwidth and transient response. With a light load, frequency is reduced and higher efficiency is realized. A frequency hopping function is also built in, contributing to low EMI.

Also on chip are soft start and burst functions, a per-cycle overcurrent limiter, VCC overvoltage protection, overload protection, and other protection functions.

● Basic Specifications

- Operating power supply voltage range: VCC 8.9 V to 26.0 V; VH: to 600 V
- Operating current: Normal: 0.60 mA (Typ.); Burst mode: 0.35 mA (Typ.)
- Oscillation frequency: BM1P067FJ: 65 kHz (Typ.)
- Operating temperature range: -40°C to +85°C

● Features

- PWM frequency: 65 kHz, 100 kHz
- PWM current mode method
- Frequency hopping function
- Burst operation during light load / Frequency reduction function
- 650 V start circuit
- VCC pin undervoltage protection
- VCC pin overvoltage protection
- CS pin open protection
- CS pin Leading-Edge-Blanking function
- Per-cycle overcurrent limiter function
- Overcurrent limiter with AC voltage compensation function
- Soft start function
- Secondary overcurrent protection circuit

● Package

SOP-J8 4.90 mm × 6.00 mm × 1.65 mm pitch 1.27 mm
(Typ.) (Typ.) (Typ.) (Typ.)

● Applications

AC adapters, TVs, and household appliances (vacuum cleaners, humidifiers, air cleaners, air conditioners, IH cooking heaters, rice cookers, etc.)

● Application circuit

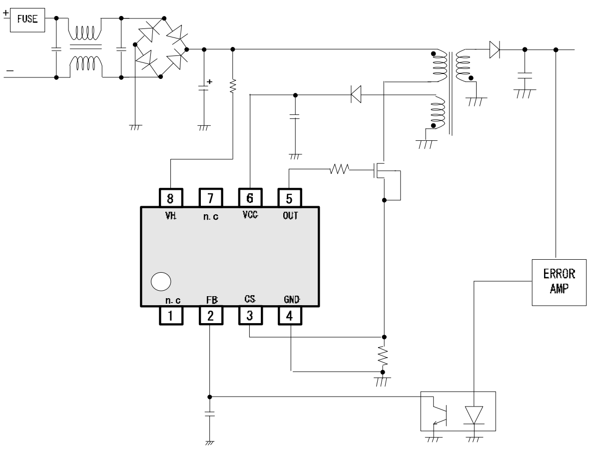


Figure 1. Application Circuit

● Line-up

	Frequency	VCCOVP	VCC recharge	X-cap discharge	Brown-out
BM1P061FJ	65kHz	Auto-restart	○	○	○
BM1P062FJ	65kHz	Latch	○	○	○
BM1P063FJ	65kHz	Auto-restart	○	×	×
BM1P064FJ	65kHz	Latch	○	×	×
BM1P065FJ	65kHz	Auto-restart	×	×	○
BM1P066FJ	65kHz	Latch	×	×	○
BM1P067FJ	65kHz	Auto-restart	×	×	×
BM1P068FJ	65kHz	Latch	×	×	×
BM1P101FJ	100kHz	Auto-restart	○	○	○
BM1P102FJ	100kHz	Latch	○	○	○
BM1P103FJ	100kHz	Auto-restart	○	×	×
BM1P104FJ	100kHz	Latch	○	×	×
BM1P105FJ	100kHz	Auto-restart	×	×	○
BM1P106FJ	100kHz	Latch	×	×	○
BM1P107FJ	100kHz	Auto-restart	×	×	×
BM1P108FJ	100kHz	Latch	×	×	×

○ Product structure：Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays

● **Absolute Maximum Ratings (Ta = 25°C)**

Parameter	Symbol	Rating	Unit	Conditions
Maximum voltage 1	Vmax1	-0.3 ~ 30.0	V	VCC
Maximum voltage 2	Vmax2	-0.3 ~ 6.5	V	CS, FB, ACMONI
Maximum voltage 3	Vmax3	-0.3 ~ 15.0	V	OUT
Maximum voltage 4	Vmax4	-0.3 ~ 650	V	VH
OUT pin peak current	I_{OUT}	±1.0	A	
Allowable dissipation	Pd	674.9 (Note1)	mW	When mounted
Operating temperature range	Topr	-40 ~ +85	°C	
Storage temperature range	Tstr	-55 ~ +150	°C	

(Note1) SOP-J8: When mounted, 70 × 70 × 1.6 mm (glass epoxy on single-layer substrate). Reduce to 5.40 mW/°C when used at Ta = 25°C or above.

● **Recommended Operating Conditions (Ta = 25°C)**

Parameter	Symbol	Rating	Unit	Conditions
Supply voltage range 1	VCC	8.9 ~ 26.0	V	VCC pin voltage
Supply voltage range 2	VH	80 ~ 600	V	VH pin voltage

● **Electrical Characteristics (Unless otherwise noted, Ta = 25°C, VCC = 15 V)**

Parameter	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
［Circuit current］						
Circuit current (ON) 1	I_{ON1}	-	600	1000	μA	FB = 2.0 V (during pulse operation)
Circuit current (ON) 2	I_{ON2}	-	350	450	μA	FB = 0.0 V (during burst operation)
［VCC pin (5 pin) protection function ］						
VCC UVLO voltage 1	V_{UVLO1}	12.50	13.50	14.50	V	VCC rise
VCC UVLO voltage 2	V_{UVLO2}	7.50	8.20	8.90	V	VCC drop
VCC UVLO hysteresis	V_{UVLO3}	-	5.30	-	V	$V_{UVLO3} = V_{UVLO1} - V_{UVLO2}$
VCC OVP voltage 1	V_{OVP1}	26.00	27.50	29.00	V	VCC rise
VCC OVP voltage 2	V_{OVP2}	-	23.50	-	V	VCC drop
VCC OVP hysteresis	V_{OVP3}	-	4.00	-	V	
[Output driver block]						
OUT pin H voltage	V_{OUTH}	10.5	12.5	14.5	V	IO = -20 mA
OUT pin L voltage	V_{OUTL}	-	-	1.00	V	IO = +20 mA
OUT pin pull-down resistance	R_{PDOUT}	75	100	125	kΩ	
[Start circuit block]						
Start current 1	I_{START1}	0.400	0.700	1.000	mA	VCC = 0 V
Start current 2	I_{START2}	1.000	3.000	5.000	mA	VCC = 10 V
OFF current	I_{START3}	-	10	20	uA	Inflow current from VH pin after release of UVLO
Start current switching voltage	V_{SC}	0.400	0.800	1.400	V	

● **Electrical characteristics of control IC block (Unless otherwise noted, Ta = 25°C, VCC = 15 V)**

Parameter	Symbol	Rating Min.	Rating Typ.	Rating Max.	Unit	Conditions
[PWM type DC/DC driver block]						
Oscillation frequency 1a	F_{SW1a}	60	65	70	kHz	FB = 2.00 V average frequency
Oscillation frequency 2	F_{SW2}	-	25	-	kHz	FB = 0.40 V average frequency
Frequency hopping range	F_{DEL1}	-	4.0	-	kHz	FB = 2.00 V average frequency
Hopping fluctuation frequency	F_{CH}	75	125	175	Hz	
Minimum pulse width	T_{min}	-	400	-	ns	
Soft start time 1	T_{SS1}	0.30	0.50	0.70	ms	
Soft start time 2	T_{SS2}	0.60	1.00	1.40	ms	
Soft start time 3	T_{SS3}	1.20	2.00	2.80	ms	
Soft start time 4	T_{SS4}	2.40	4.00	5.60	ms	
Maximum duty	D_{max}	68.0	75.0	82.0	%	
FB pin pull-up resistance	R_{FB}	22	30	38	kΩ	
FB / CS gain	Gain	-	4.00	-	V/V	
FB burst voltage 1	V_{BST1}	0.300	0.400	0.500	V	FB drop
FB burst voltage 2	V_{BST2}	0.350	0.450	0.550	V	FB rise
FBOLP voltage 1a	V_{FOLP1A}	2.60	2.80	3.00	V	When overload is detected (FB rise)
FBOLP voltage 1b	V_{FOLP1B}	-	V_{FOLP2A}-0.2	-	V	When overload is detected (FB drop)
FBOLP detection timer	T_{FOLP}	44	64	84	ms	
[Overcurrent detection block]						
Overcurrent detection voltage	V_{CS}	0.380	0.400	0.420	V	Ton = 0 us
Overcurrent detection voltage SS1	V_{CS_SS1}	-	0.100	-	V	0 [ms] ~ Tss1 [ms]
Overcurrent detection voltage SS2	V_{CS_SS2}	-	0.150	-	V	TSS1 [ms] ~ TSS2 [ms]
Overcurrent detection voltage SS3	V_{CS_SS3}	-	0.200	-	V	TSS2 [ms] ~ TSS3[ms]
Overcurrent detection voltage SS4	V_{CS_SS4}	-	0.300	-	V	TSS3 [ms] ~ TSS4 [ms]
Leading edge blanking time	T_{LEB}	-	250	-	ns	
Overcurrent detection AC compensation factor	K_{CS}	12	20	28	mV/us	

● Pin Descriptions

Table1. I/O Pin Functions

No.	Pin Name	I/O	Function	ESD Diode	
				VCC	GND
1	N.C	-	Non Connection	-	-
2	FB	I	Feedback signal input pin	○	○
3	CS	I	Primary current sense pin	○	○
4	GND	I/O	GND pin	○	-
5	OUT	O	External MOS drive pin	○	○
6	VCC	I/O	Power supply input pin	-	○
7	N.C.	-	Non Connection	-	-
8	VH	I	Start circuit pin	-	○

● I/O Equivalent Circuit Diagram

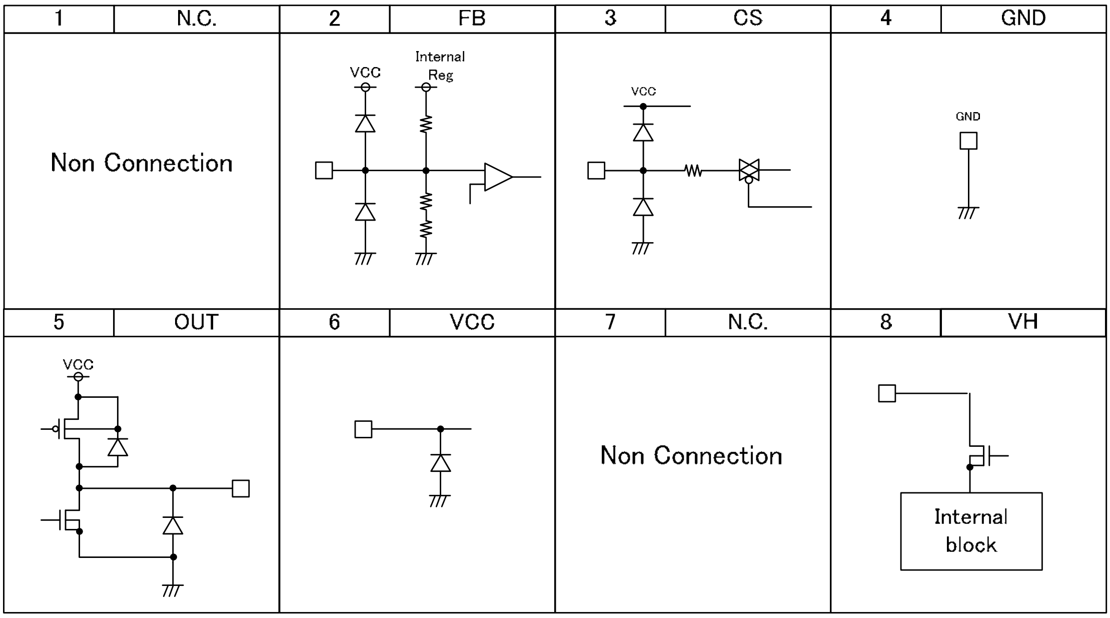


Figure 2. I/O Equivalent Circuit Diagram

● **Block Diagram**

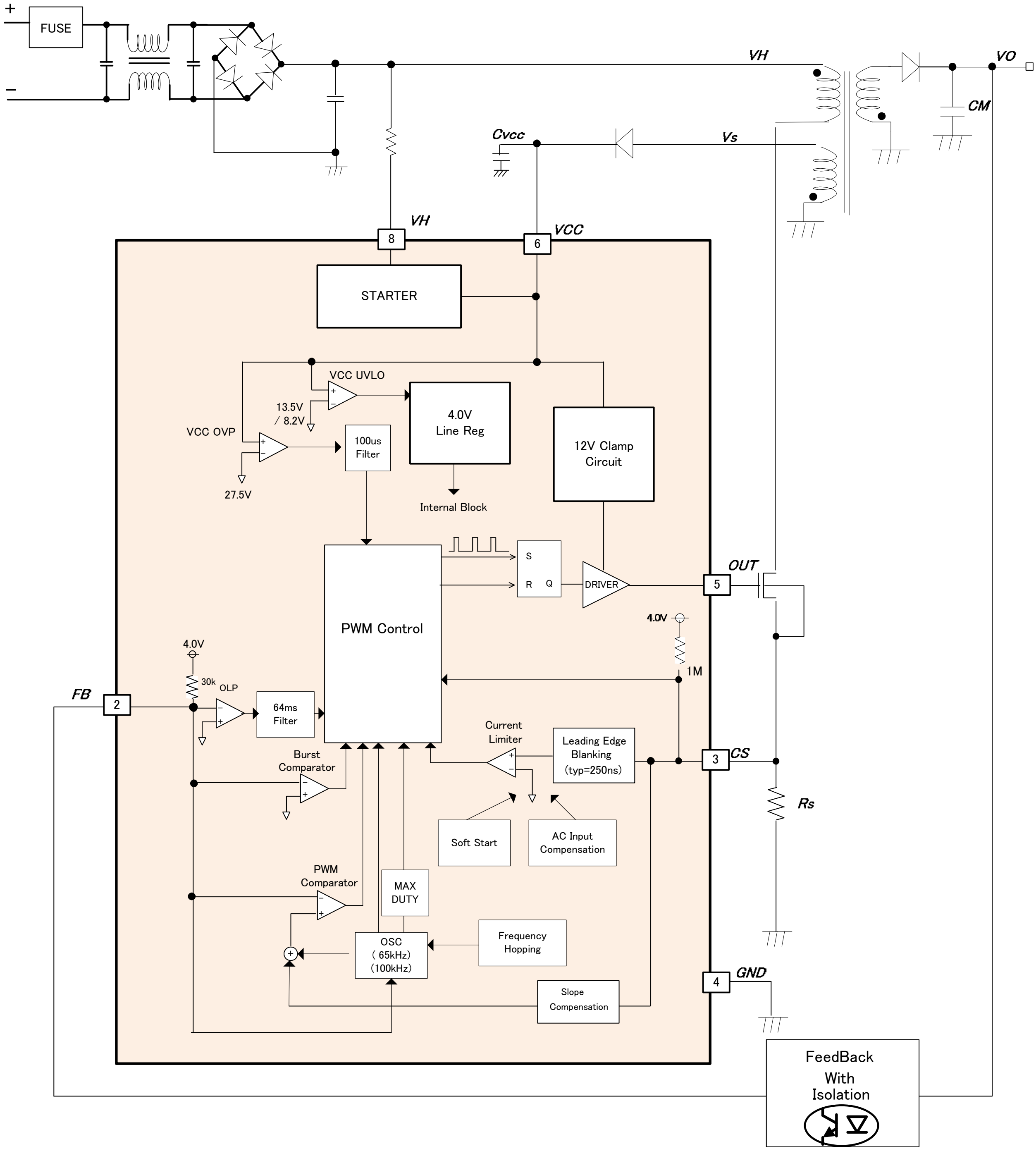


Figure 3. Block Diagram

- **Description of application operations in blocks**

(1) Start circuit (VH pin: 8 pin)

This IC has a built-in start circuit (withstands 650 V). This enables both low standby mode power and high-speed startup.

This start circuit operates only at startup. The current flow when operating is shown in Figure 5.

After startup, the power consumed is only for the idling current I_{START3} (typ = 10 uA).

ex) When Vac = 100 V, power consumption is from start circuit only
PVH = 100 V*√2*10 uA = 1.41 mW

ex) When Vac = 240 V, power consumption is from start circuit only
PVH = 240 V*√2*10 uA = 3.38 mW

Startup time is determined based on the inflow current for the VH pin and the capacitance for the VCC pin.
Startup time reference values are shown in Figure 6. For example, when C_{VCC} = 10 uF, startup takes about 0.07 seconds.
When the VCC pin has been shorted by GND, the ISTART1 current in Figure 5 flows.
When the VH pin has been shorted by GND, a large current flows to GND from the VH line. To prevent this, insert resistor R_{VH} (5 kΩ ~ 60 kΩ) to limit the current between the VH line and the VH pin of the IC.
When the VH pin is shorted, the power of VH^2/R_{VH} is applied to the resistor. Therefore, select a resistor size that is able to tolerate this amount of power.
If one resistor is not enough for the allowable power, connect two or more resistors in series.

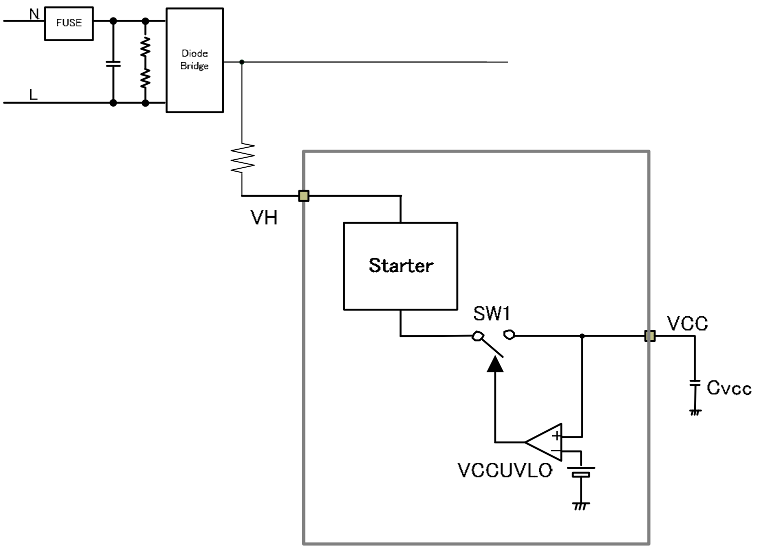


Figure 4. Block Diagram of Start Circuit

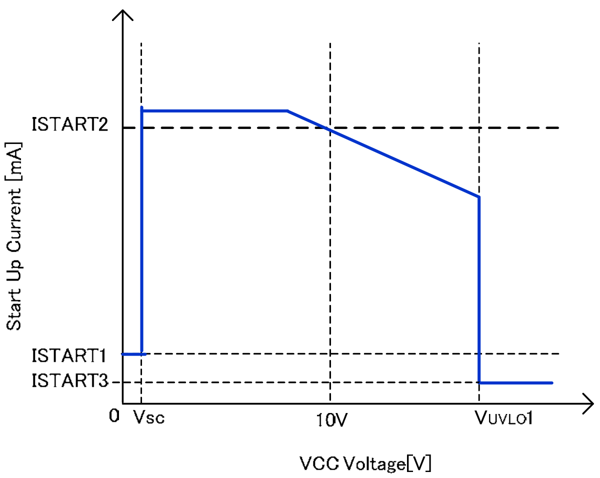


Figure 5. Start Current vs VCC Voltage
(* Start current flows from the VH pin.)
The operating waveform at startup is as follows.

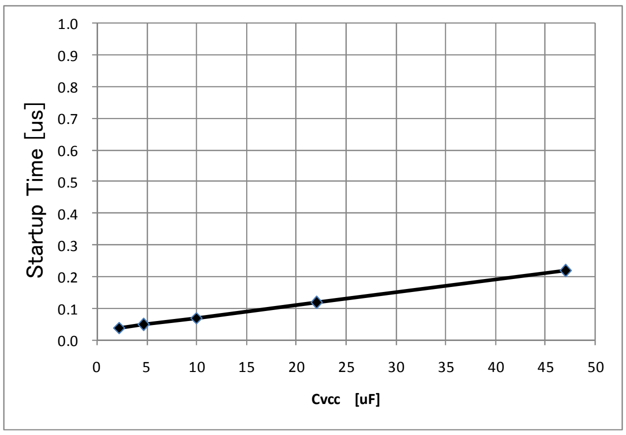


Figure 6. Startup Time (Reference Value)
(C_{VCC} is capacitance for the VCC pin.)

The operating waveform at startup is shown in Figure 7.

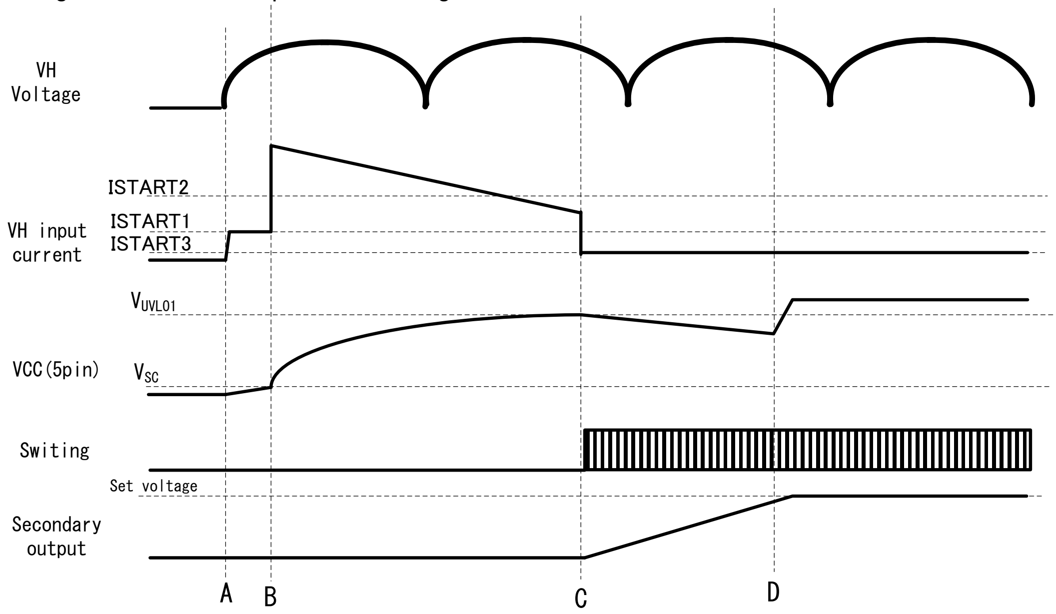


Figure 7. Operating Waveform at Startup

A: VH voltage is applied when plugged into the outlet. At that time, charging starts from the VH pin via the start circuit to the VCC pin.
At that time, VCC < V_{SC} (typ = 0.8 V), so the VH input current is limited to ISTART1 by the VCC pin short protection function.
B: Since VCC voltage > V_{SC} (typ = 0.8 V), VCC short protection is cancelled and current flow is from the VH input current.
C: Since VCC voltage > V_{UVLO1} (typ = 13.5 V), the start circuit is stopped and the VH input current flow is only ISTART3 (typ = 10 uA).
When switching starts, secondary output begins to increase, but since secondary output is low, the VCC pin voltage is reduced. The drop rate of VCC is determined by the consumption current between the VCC pin capacitor and the IC and by the load current connected to the VCC pin. (V/t = Cvcc/Icc)
D: Since secondary output has risen to a constant voltage, voltage is applied from the auxiliary winding to the VCC pin, and VCC voltage is stabilized.

(2) Startup sequences (soft start operation, light load operation, auto recovery operation during overload protection)
Startup sequences are shown in Figure 8.
See the sections below for detailed descriptions.

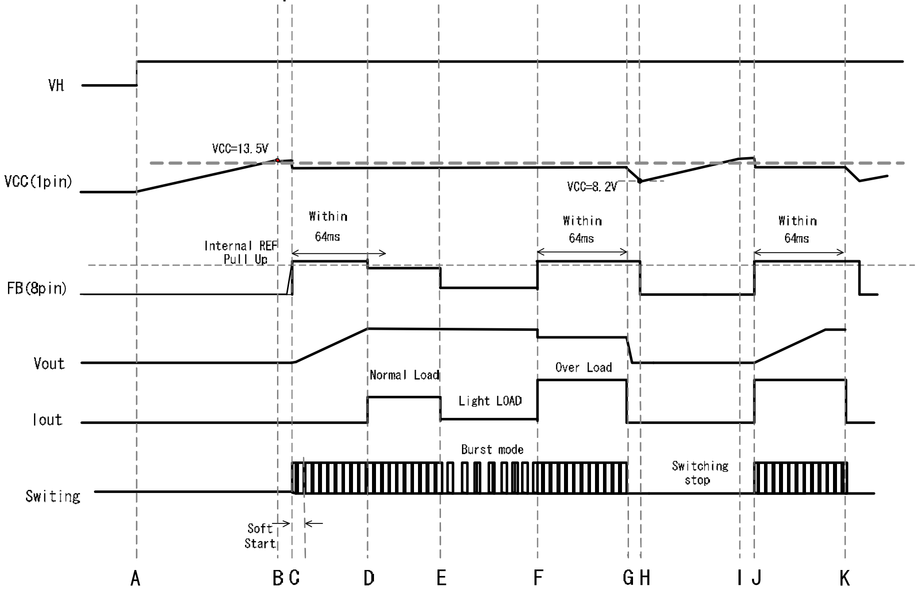


Figure 8. Startup Sequence Time Chart

A: Voltage is applied to the input voltage (VH) pin (pin 8).
B: The VCC pin (pin 6) voltage rises, and when VCC ＞ V_{UVLO1} (13.5 V typ) this IC starts to operate.
When protection functions (VCC, CS, FB pin, temperature) are judged as normal, switching operation begins.
At this time, the VCC pin (pin 6) consumption current necessarily causes the VCC pin voltage to drop. When VCC < V_{UVLO2} (8.2 V typ), switching operation stops by VCC UVLO function. For that, set VCC capacitor to finish start-up before VCC<V_{UVLO2}(8.2V.typ)
C: With the soft start function, excessive rises in voltage and current are prevented by adjusting the voltage level of the CS pin (pin 3). During a soft start, the IC changes the overcurrent detection voltage from V_{CC_SS1} to V_{CC_SS4} to prevent overshoot of the output voltage. VCC_SS1 is described in Table 2 below.

Table 2 Overcurrent Detection Voltage at Startup

Soft start	Vlim1
Start ~ 0.5 ms	0.10 V (12%)
0.5 ms ~1 ms	0.15 V (25%)
1 ms ~2 ms	0.20 V (50%)
2 ms ~4 ms	0.30 V (75%)
4 ms ~	0.500 V (100%)

D: When the switching operation starts, the secondary output voltage VOUT rises.
After switching has started, set the output voltage to within T_{FOLP} (64 ms typ) to become the rated voltage.
E: When there is a light load, burst operation suppresses power consumption.
F: When there is an overload, the FB pin (pin 2) voltage becomes greater than V_{FOLP1A} to reduce the output voltage.
G: If the FB pin (pin 2) voltage exceeds V_{FOLP1A} for T_{FOLP} (64 ms typ) or longer, the overload protection circuit stops the switching operation. For that, set to finish the start-up time within T_{FOLP} (64 ms typ).
When the FB pin (pin 2) voltage exceeds V_{FOLP1B}, the IC's internal timer T_{FOLP} (64 ms typ) is reset.
H: When VCC voltage becomes VCC < V_{UVLO2} (8.2 V typ), the start circuit operates and VCC charging is started.

I: When VCC voltage becomes VCC> V_{UVLO1} (13.5 V typ), the start circuit stops charging VCC.
J: Same as F
K: Same as G
Startup waveforms are shown as reference examples in Figure 9 and Figure 10.

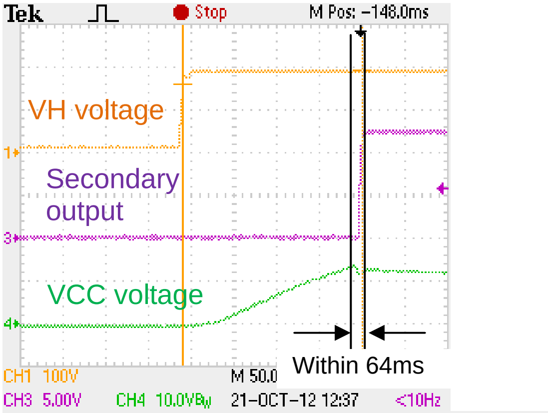


Figure 9. Waveform of No-load Startup

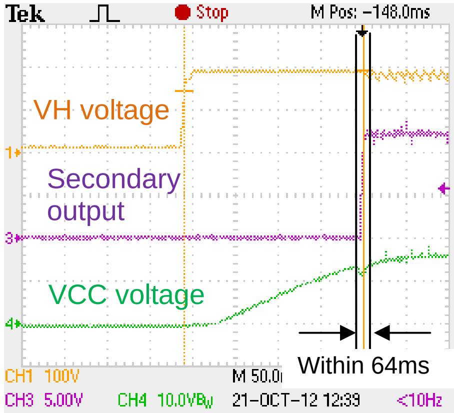


Figure 10. Waveform of High-load Startup

(3) VCC pin protection function

This IC includes a VCC pin under voltage protection function VCC UVLO (Under Voltage Protection) and overvoltage protection function VCC OVP (Over Voltage Protection).

The VCC UVLO function and VCC OVP function prevent damage to the switching MOSFET that can occur when the VCC voltage drops or becomes excessive.

(3-1) VCC UVLO and VCC OVP functions

VCC UVLO is an auto recovery type comparator with voltage hysteresis. For VCC OVP, the BM1P067FJ has an auto recovery type comparator.

After VCCOVP operation detects, switching operation re-start when VCC<V_{OVP2} (typ=23.5V).

The operation is shown in Figure 11.

A mask time T_{LATCH} (typ = 100 us) is built in for VCC OVP to prevent miss-detection. The detection is performed when the VCC pin (pin 6) voltage continues to exceed V_{OVP1} (typ = 27.5 V) for T_{LATCH} (typ = 100 us).

This function masks surges or the like that occur at the pin. (See section (7) below.)

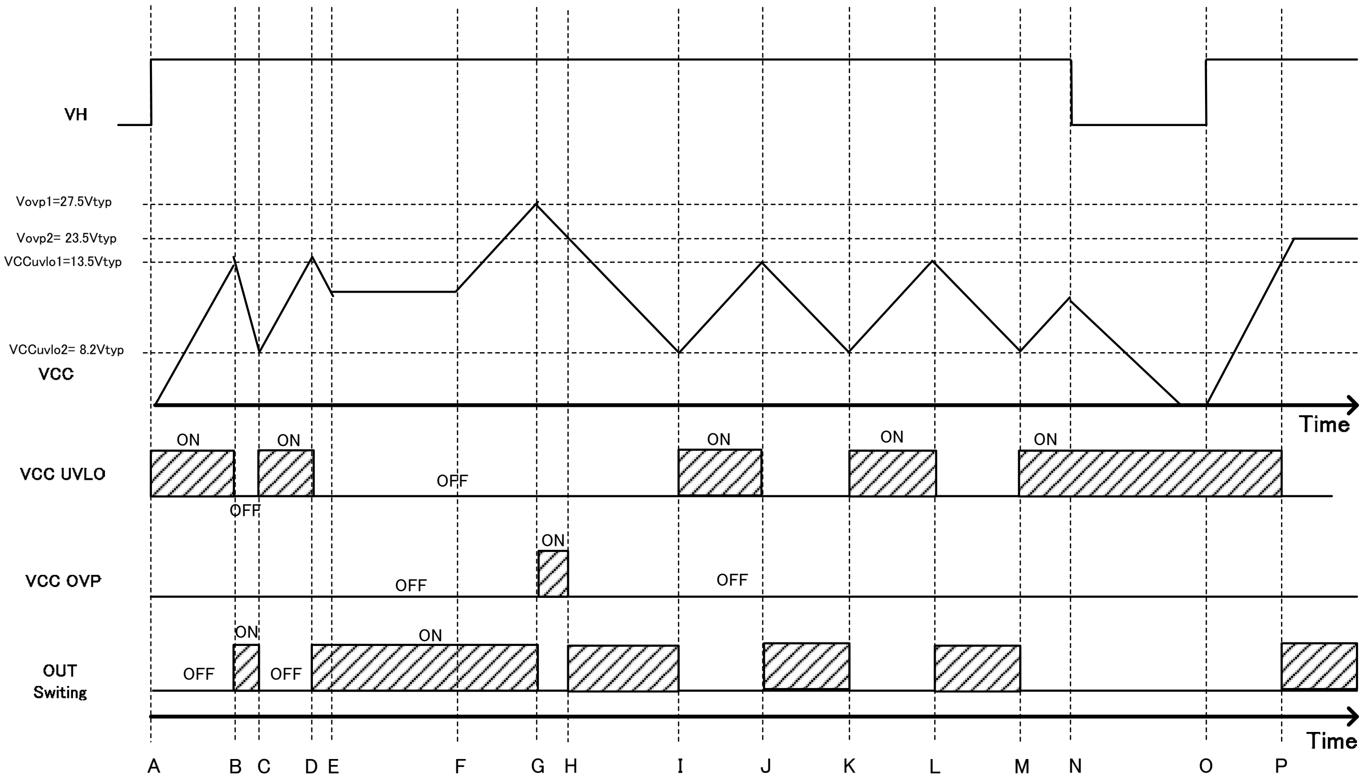


Figure 11. VCC UVLO / OVP Time Chart

A: Voltage is applied to the VH pin (pin 8) and voltage at the VCC pin (pin 6) starts to rise.
B: When VCC pin (pin 6) voltage > V_{UVLO1}, the VCC UVLO function is canceled and the DC/DC operation starts. Then VCC start-up circuit stops charging.
C: When VCC pin (pin 6) voltage < V_{UVLO2}, the VCC UVLO function is operated and the DC/DC operation stops. Then VCC start-up circuit starts charging.
D: When VCC pin (pin 6) voltage > V_{UVLO1}, the VCC UVLO function is canceled and the DC/DC operation starts. Then VCC start-up circuit stops charging.
E: After finishing start-up, VCC pin voltage is stable as secondary output voltage is stable.
F: VCC pin voltage rises
G: When VCC pin (pin 6) voltage > V_{OCP} status continues for T_{LATCH} (typ = 100us), switching operation is stopped by the VCC OVP function.
H: When VCC pin voltage < V_{OVP2}, VCCOVP function is released, and the switching operation re-starts.
I: When VCC pin voltage < V_{UVLO2}, VCCUVLO function operates, and switching operation stops.
J: When VCC pin (pin 6) voltage > V_{UVLO1}, the VCC UVLO function is canceled and the DC/DC operation starts.
K: The same as I.
L: The same as J.
M: The same as K.
N: High voltage line VH is reduced. Then VCC pin voltage drops because IC cannot charge the power to VCC pin.
O: When VCC < V_{UVLO2}, the VCC UVLO function operates.
P: When VCC ＞ V_{UVLO}, start-up circuit stops, and the switching operation re-starts.

・Capacitance value of VCC pin

To ensure stable operation of the IC, set the VCC pin capacitance value to 10 uF or above.

If the capacitor for the VCC pin is too large, it will delay the response of the VCC pin to secondary output. In cases where the transformer has a low degree of coupling, a large surge can be generated at the VCC pin, which may damage the IC. In such cases, insert a resistance of 10 Ω to 100 Ω on a bus between the diode and capacitor after the auxiliary winding. As for constants, perform a waveform evaluation of the VCC pin and enter settings that will prevent any surge at the VCC pin from exceeding the absolute maximum rating for the VCC pin.

・VCC OVP voltage protection settings for increased secondary output

The VCC pin voltage is determined by the secondary output and the transformer ratio (Np:Ns).
Accordingly, when secondary output has become large, it can be protected by VCC OVP.
The VCC OVP protection settings are as follows.

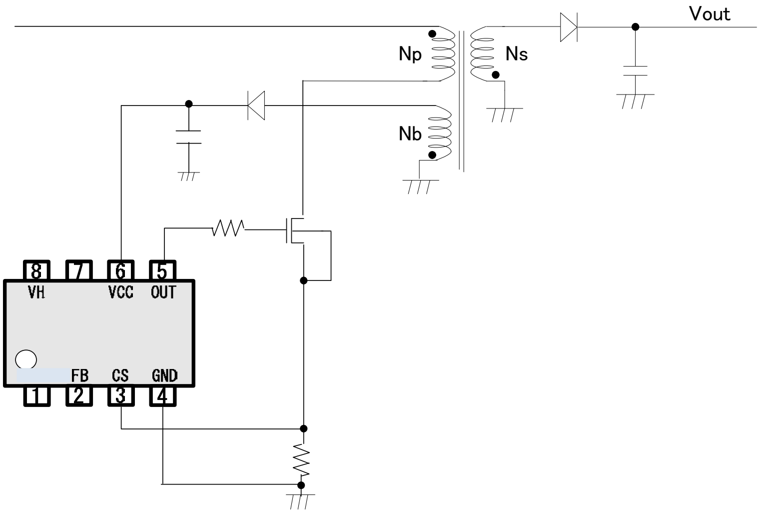


Figure 12　VCC OVP Settings

This is determined by VCC voltage = Vout x Nb/Ns.
(Vout: Secondary output, Nb: auxiliary winding turns, Ns: secondary winding turns).

When secondary output voltage rises 30% high, and protection is desired, set the number of winding turns so that 1.3 x Vout x (Nb/Ns) ＞ V_{OVP1}.
For VCC OVP protection, since there is the T_{LATCH} (typ = 100 us) blanking time, VCC OVP protection cannot be detected for instantaneous surges at the VCC pin.
However, VCC OVP is detected when the VCC pin voltage has become higher than V_{OVP1} for at least the T_{LATCH} period, such as due to the impact of a low degree of transformer couplings, so an application evaluation should be done to check this before setting VCC OVP.

(4) DC/DC driver (PWM comparator, frequency hopping, slope compensation, OSC, burst)

(4-1) PWM basic operations

Figure 13 shows a PWM basic block diagram and Figure 14 illustrates PWM basic operations.

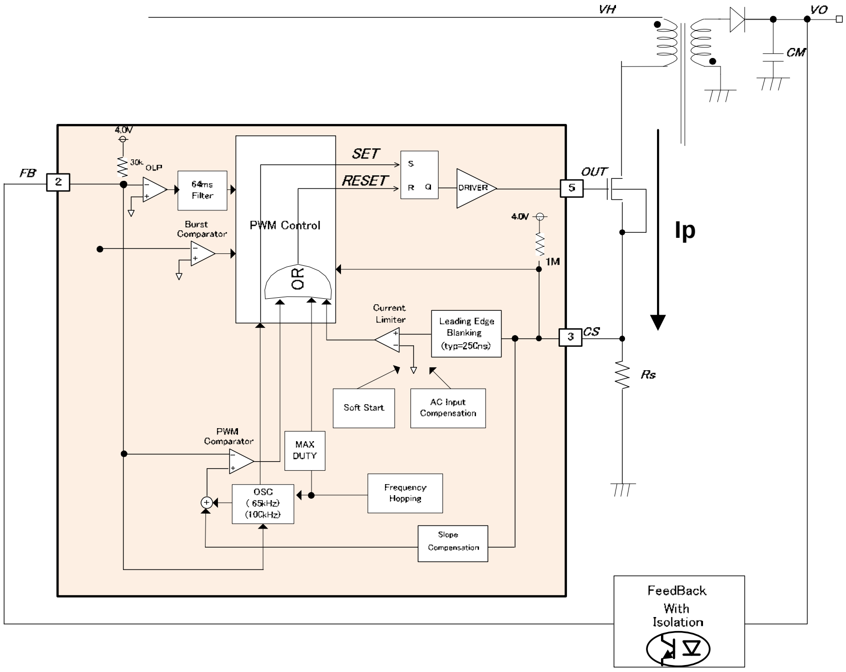


Figure 13. Block Diagram of IC Internal PWM Operations

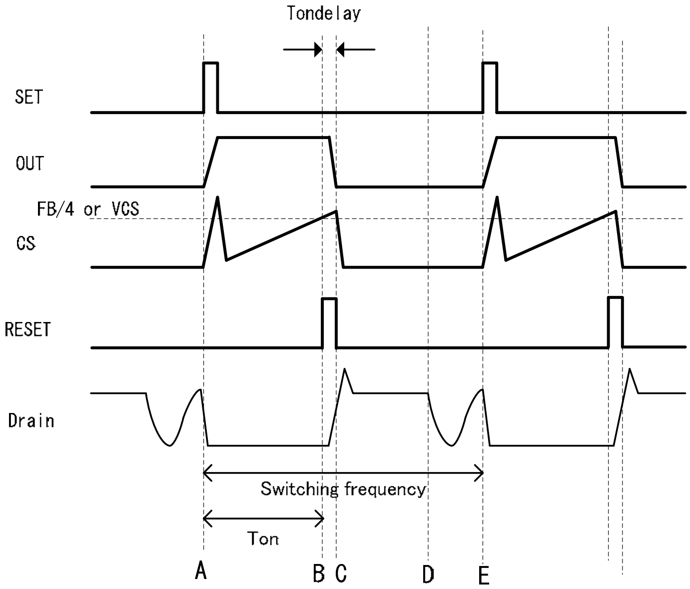


Figure 14. PWM Basic Operations

A: A SET signal is output from the oscillator in the IC, and the MOSFET is turned ON.
At that time, the capacitance between the MOSFET drain and source becomes discharged, and noise is generated at the CS pin.
This noise is called the leading edge.
This IC has a built-in filter for this noise. (See (5).)
As a result of this filter and delay time, the minimum pulse width of the IC is 400 ns (typ).
Afterward, current flow to the MOSFET and the Vcs = Rs * Ip voltage is applied to the CS pin.

B: When CS pin voltage rises to become greater than the FB pin voltage/Gain (typ = 4) or the overcurrent detection voltage Vcs, the RESET signal is output and OUT is turned off.

C: There is a delay time Tondelay between time point B and actual turn-off. This time is the result of differences in maximum power that occur based on the AC voltage. This IC includes a function that suppresses these differences. (See (4-4).)

D: The energy that accumulates in the transformer during Ton status is discharged to the secondary side, and the drain voltage starts to oscillate freely based on the transformer Lp value and the MOSFET Cds (drain-source capacitance).

E: Since the switching frequency within the IC is predetermined, SET signal output from the internal oscillator occurs for a set period starting from point A, and the MOSFET is turned on.

(4-2) Frequency operations

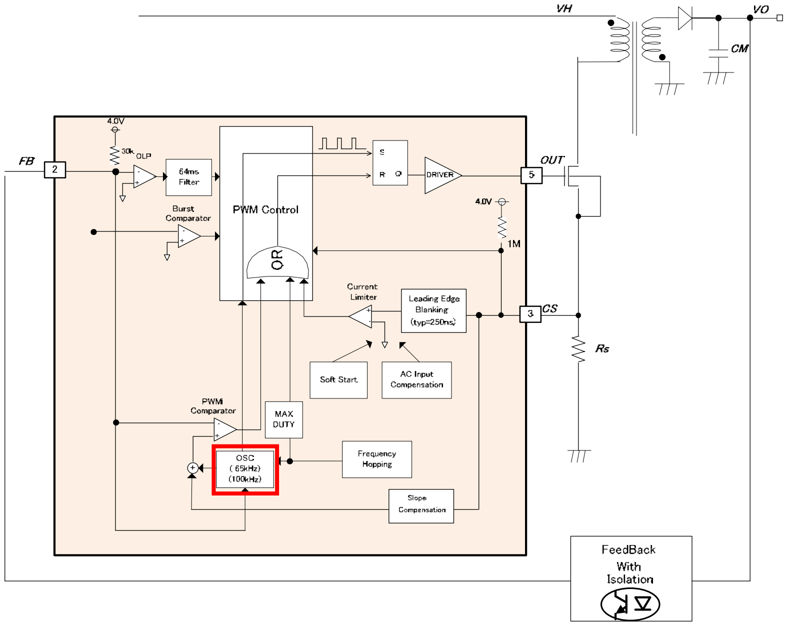


Figure 15. PWM Operations in IC

The PWM frequency is generated by the OSC block (internal oscillator) in Figure 15.
This oscillator has a switching frequency hopping function and the switching frequency fluctuates such as is shown in Figure 16.
The fluctuation cycle is 125 Hz. Due to this frequency hopping function, the frequency spectrum is dispersed and the frequency spectrum peak is lowered. This increases the margin for EMI testing.

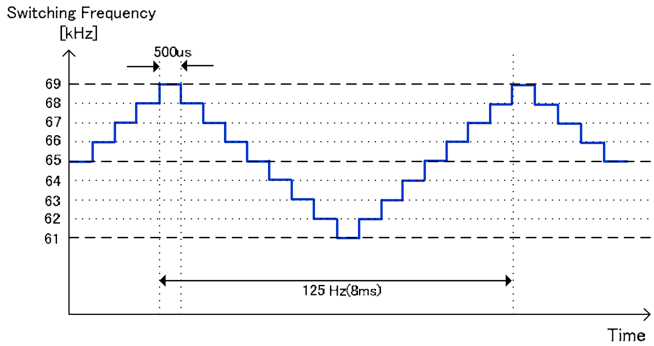


Figure 16. Frequency Hopping Function

In Figure 16, the duty is calculated as Ton * Switching frequency * 100. The maximum duty value is Dmax (typ = 75%).
Since the PWM current mode method is being used, if the duty exceeds 50% sub harmonic oscillation may occur. 22 mV/us slope compensation is built in as a countermeasure to this.
To reduce power consumption when there is a light load, a burst mode circuit and frequency reduction circuit are built in. These operations are illustrated in Figure17. As shown in this figure, frequency fluctuates according to the FB voltage. If the FB voltage is in the range shown for mode2, switching loss is reduced by reducing internal oscillations based on the FB voltage.

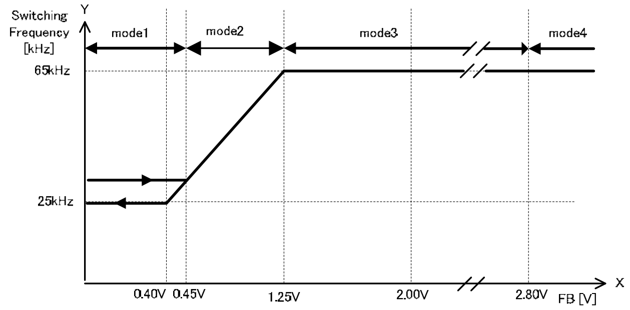


Figure 17. Operation with FB pin voltage

・mode1: Burst operation
・mode2: Frequency reduction operation (reduces maximum frequency.)
・mode3: Fixed frequency operation (operates at maximum frequency.)
・mode4: Overload operation (overload status is detected and pulse operation is stopped.)

(4-3) Overcurrent detection operation

R_{FB} (30 kΩ.typ) is used as pull-up resistance for the FB pin with regard to the internal power supply (4.0 V).
When the load of the secondary output voltage (secondary load power) changes, the photo-coupler current changes, and so the FB pin voltage also changes.
FB voltage VFB is determined by the equation FB voltage = 4 V - IFB. (IFB: photo coupler current)
For example, when the load becomes heavier, the FB current is reduced, so the FB voltage rises.
When the load becomes lighter, the FB current is increased, so the FB voltage drops.
In this way, secondary voltage is monitored by the FB pin.

As the FB pin voltage is monitored, if the load becomes lighter (if FB voltage drops), a burst mode operation or frequency reduction operation is executed.
Figure 18 shows the CS detection voltage with regard to FB voltage.

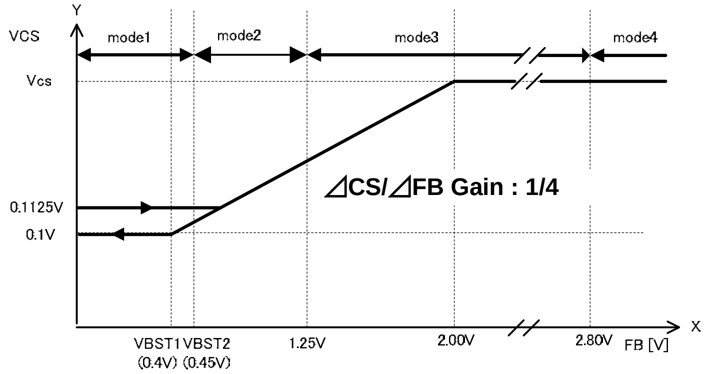


Figure 18 FB Voltage and CS Voltage Characteristics

When FB voltage is less than 2.0 V or when the CS voltage exceeds the FB voltage / Gain (typ = 4), the MOSFET is turned off.
(See time point C in Figure 14.)
When the FB voltage exceeds 2.0 V, the CS voltage = Vcs + Kcs * Ton. Kcs * Ton depends on AC voltage compensation. (See 4-4.)
Therefore, peak current Ip is determined as Ip = Vcs1 / Rs.
The current value for the MOSFET should be set with a margin with regard to the Ip value obtained from this formula.

Maximum power is determined as Pmax = 1/2 x Lp x Ip^2 x Fsw. (Lp: primary inductance value, Ip: primary peak current, Fsw: switching frequency)

Vcs1 is determined as Vcs1 = Vcs (typ = 0.4 V) + Kcs (typ = 20) * Ton + Vdelay.
Vdelay is the amount of CS voltage increase during the delay time Rondelay between B and C in Figure 14.
This is calculated as Vdelay = Vin / Lp * Tondelay * Rs.

(4-4) AC voltage dependent compensation of overcurrent limiter

This IC has an AC voltage compensation function on chip. This function performs compensation for AC voltage by increasing the level of the overcurrent limiter over time. In the equation below, (A) and (B) are assigned values similar to those for AC 100 V and AC 200 V to perform compensation.

$$V_{cs1} = V_{cs}\,(typ = 0.4\,V) + \underbrace{K_{cs}\,(typ = 20) * T_{on}}_{(A)} + \underbrace{V_{delay}}_{(B)}$$

These operations are shown in Figures 19, 20, and 21.

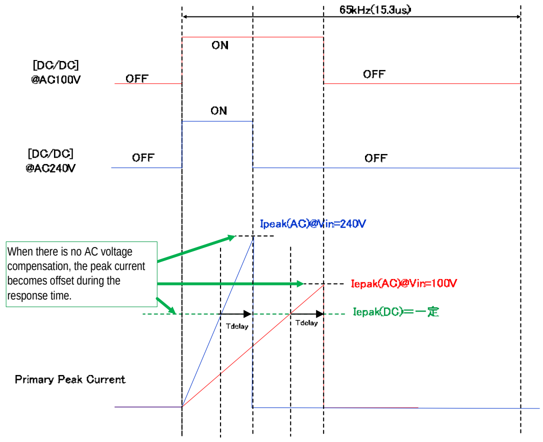


Figure 19. Without AC Voltage Compensation Function

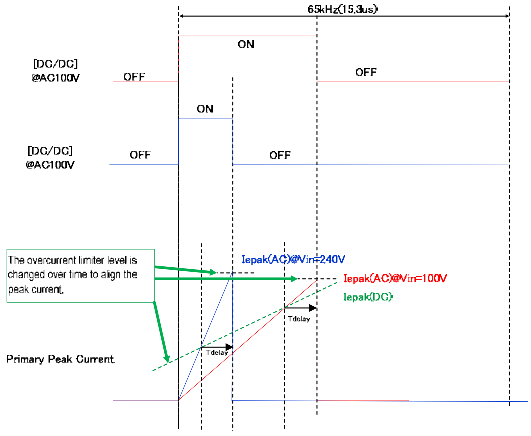


Figure 20. With AC Voltage Compensation Function

Primary peak current that flows during overload mode is defined as follows.

Primary peak current $I_{peak} = V_{cs}/R_s + K_{cs} * T_{on}/R_s + V_{in}/L_p * T_{ondelay}$

V_{cs}: Overcurrent limiter voltage in IC
R_s: Current detection resistor
V_{in}: Input DC voltage
L_p: Primary peak current
$T_{ondelay}$: Delay time after overcurrent limiter detection

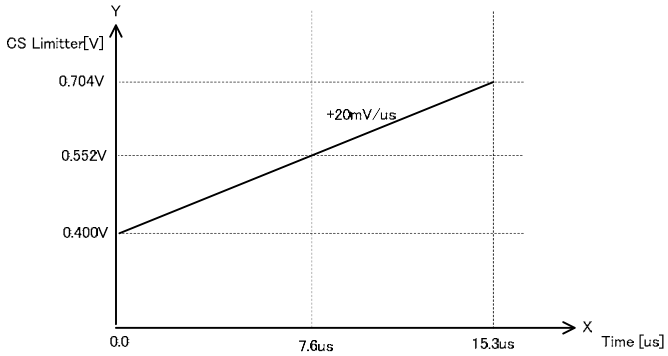


Figure 21. Overcurrent Limiter Voltage

(6) L.E.B period

When the driver MOSFET is turned on, a surge current is generated at time point A in Figure 14.
At that time, the CS voltage (pin 4) rises, which may cause detection errors in the overcurrent limiter circuit.
To prevent these detection errors, the OUT pin in this IC is switched from low to high and the CS voltage (pin 4) is masked for 250 ns by the built-in L.E.B. function (Leading Edge Blanking function).
This blanking function can reduce the CS pin noise filter for the noise that is generated when switching the OUT pin from low to high.
However, if the CS pin noise does not stay within this 250 ns period, an RC filter should be applied to this pin, such as is shown in Figure 22. At this time, a delay time occurs due to the RC filter when the CS pin is detected.
Even if there is no filter, attachment of R_{CS} as a surge countermeasure is recommended.
The recommended resistance for Rcs is 1 kΩ. When a filter ring is desired, use Ccs to adjust for this resistance.

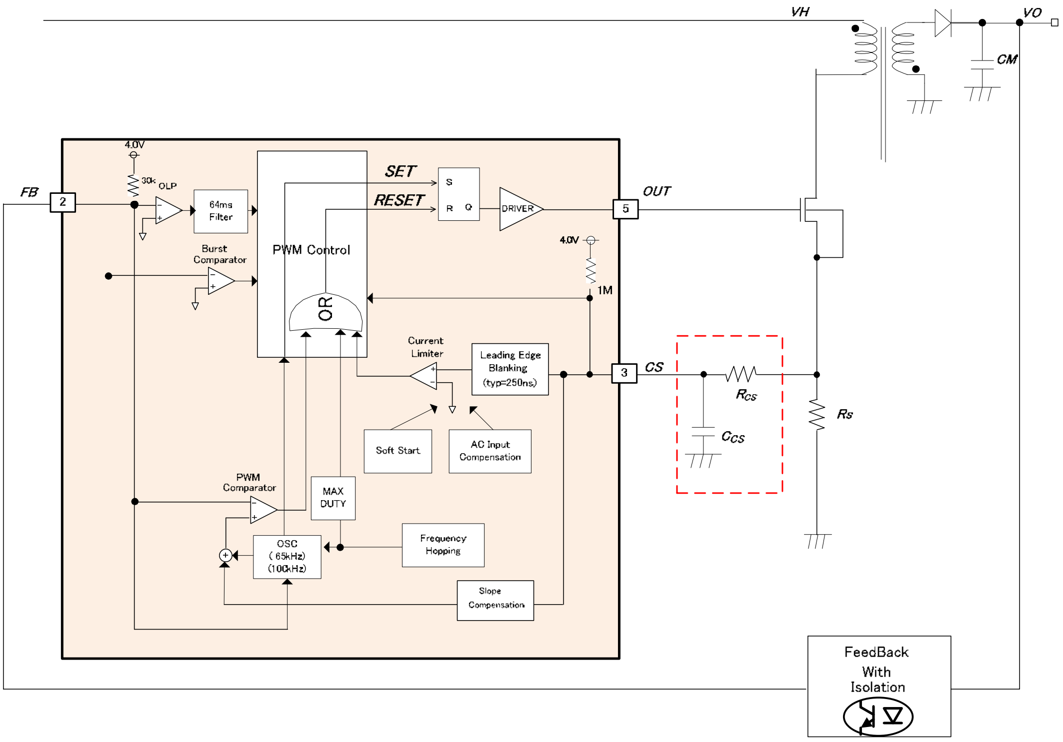


Figure22. Circuits Peripheral to the CS Pin

(6) CS pin open protection

When the CS pin (pin 4) has become an open pin, transient heat (due to noise, etc.) occurs in the IC, which may become damaged.
An open protection circuit has been built in to prevent such damage. (Auto recovery protection)

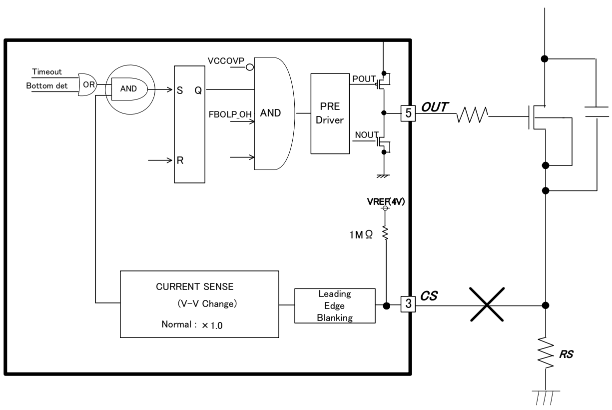


Figure 23. CS Pin Peripheral Circuit

(7) Output overload protection function (FB OLP comparator)

As is shown in mode4 of Figure 17, when the FB pin voltage rises to above a certain value, it is called an overload condition.

The output overload protection function stops switching operations when mode4 has an overload condition.

During an overload condition, the output voltage drops and so current no longer flows to the photo coupler while the FB voltage (pin 2) rises.

When the FB voltage (pin 2) exceeds V_{FOLP1A} (2.8 V typ) continuously for T_{FOLP2} (64 ms typ), it is judged as an overload condition and switching is stopped.

While the FB pin (pin 2) exceeds V_{FOLP1A} (2.8 V typ), if the FB pin (pin 2) voltage drops below V_{FOLP1B} (2.6 V typ) during the T_{FOLP} (64 ms typ) period, the overload protection timer is reset. Switching operation are performed during the T_{FOLP} (64 ms typ) period. At startup, the FB pin (pin 2) voltage is pulled up by a resistance to the IC internal voltage, and operations start when the voltage reaches V_{FOLP1A} (2.8 V typ) or above. Therefore, at startup the start time of secondary output voltage must be set so that the FB voltage (pin 2) drops to V_{FOLP1B} (2.6 V typ) or below within the T_{FOLP} (64 ms typ) period. Once FBOLP is detected, the switching operation stops, and VCC voltage falls down because secondary output voltage falls down. When VCC voltage is lower than Vuvlo2(8.2V.typ), IC is reset, and IC starts by starter circuit shown in (1).

The switching stop time is calculated by VCC pin voltage and VCC capacitor and Icc current

Stop time : Tstop Tstop=Cvcc*(VCC － Vuvlo2) / Icc

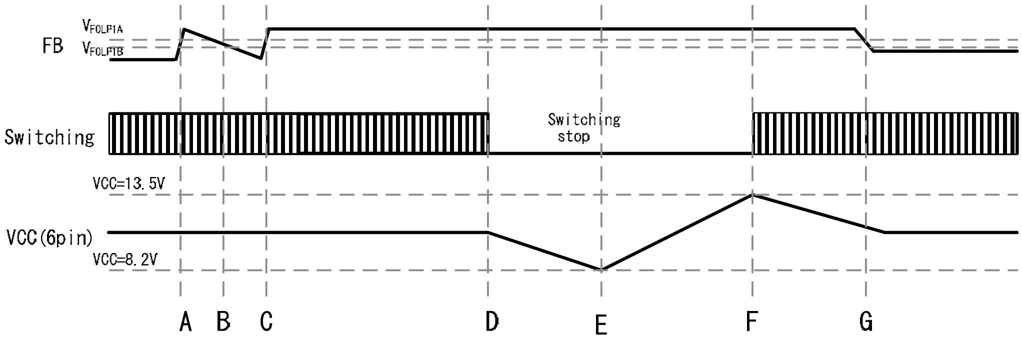


Figure 24. Overload Protection (Auto Recovery)

A: Since FB > V_{FOLP1A}, the FBOLP comparator detects an overload.
B: When FB<V_{FOLP1B} within T_{FOLP}（typ=64ms） period, FB overload detection is released, and FBOLP timer is reset.
C: Since FB > V_{FOLP1A}, the FBOLP comparator detects an overload.
D: When the condition at C continues for T_{FOLP} (typ = 64 ms), switching is stopped by the overload protection function. As switching operation stops, VCC pin voltage falls down because output voltage falls down.
E: When VCC pin voltage < V_{UVLO2}, IC is reset by VCC UVLO function, and start-up circuit operates.
F: When VCC pin voltage > V_{UVLO1}, VCC UVLO is released, and switching operation starts.
G: Because secondary output voltage is stable, VCC pin voltage is also stable.

(8-1) OUT pin clamp function

To protect the external MOSFET, the high voltage level of the OUT pin (pin 5) is clamped to V_{OUTH} (typ = 12.5 V). The VCC pin (pin 6) voltage is raised to prevent MOSFET gate damage. (Shown in Figure25.)

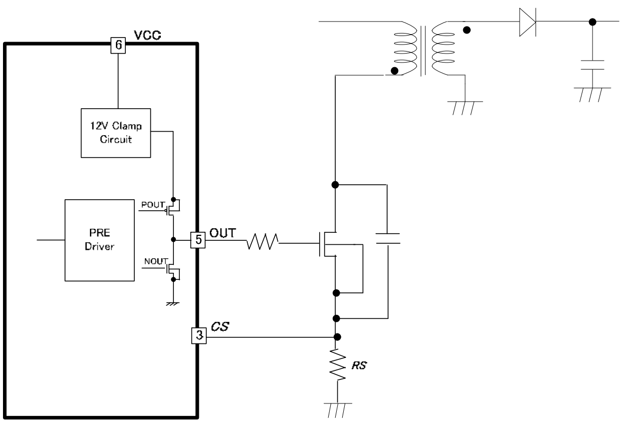


Figure 25. OUT Pin (Pin 5) Schematic

(8-2) OUT pin driver circuit

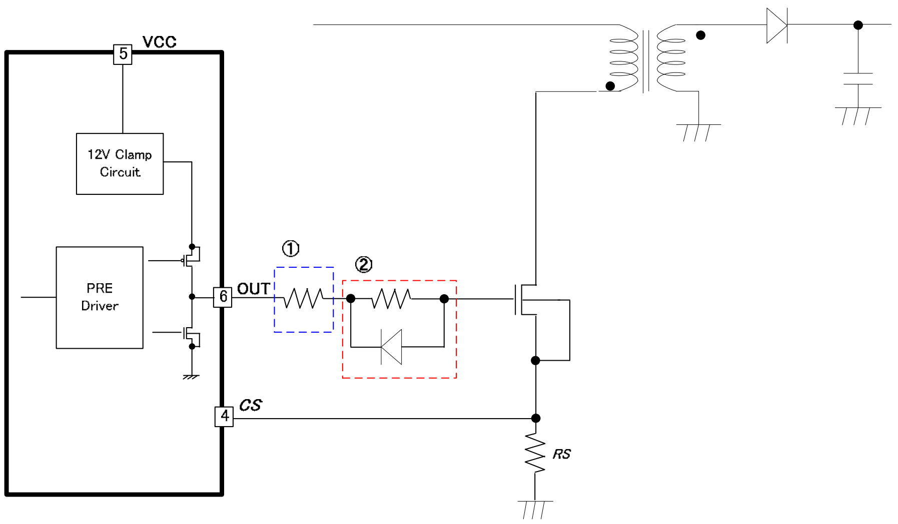


Figure 26. OUT Pin (Pin 5) Driver Circuit

Switching noise that occurs when OUT is turned on or off may cause EMI-related problems.
In such cases, the MOSFET turn-on time and turn-off time must be delayed.
However, when the turn off time is delayed, switching loss increases.
Figure 26 shows a delay circuit for the OUT pin. In Figure 26, ① is valid during both turn-on and turn-off operations.
② shows a delay in the turn-on only, while turn-off is accelerated.

(9) Caution points for board layout pattern

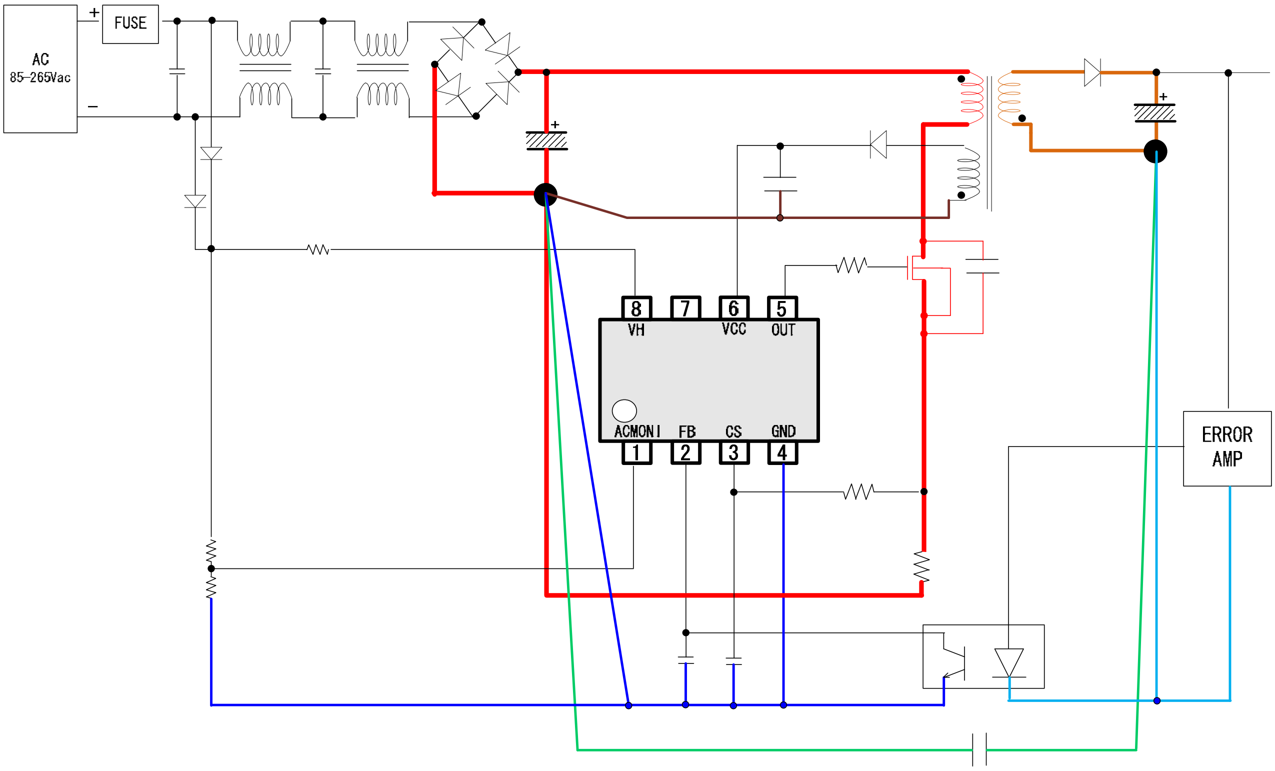


Figure 27. Board Layout Pattern

・Caution points

① The red lines shown in Figure 27 are large current pathways. In the layout, these should be as short as possible since they can cause ringing, dissipation, etc.
Also, any loops that occur in the red line should be made as small as possible in this layout.

② The orange lines in the secondary side of Figure 27 should also be made short and thick like the red lines and should be made with small loops in this layout.

③ Be sure to implement grounding for the red lines, brown lines, blue lines, and green lines.

④ The green lines are pathways for surges on the secondary side to escape to the primary side, and since a large current may flow instantaneously, they should be laid out independently of the red lines and blue lines.

⑤ The blue lines are GND lines for IC control. They do not have any large current flow, but they are susceptible to noise effects, so they should be laid out independently of the red lines, green lines, and brown lines.

⑥ The brown lines are current pathways for the VCC pin. A current flows on these lines during switching, so they should also be laid out independently.

⑦ Do not route any IC control lines directly under the transformer, since they may be affected by magnetic flux.

(Application circuit example)

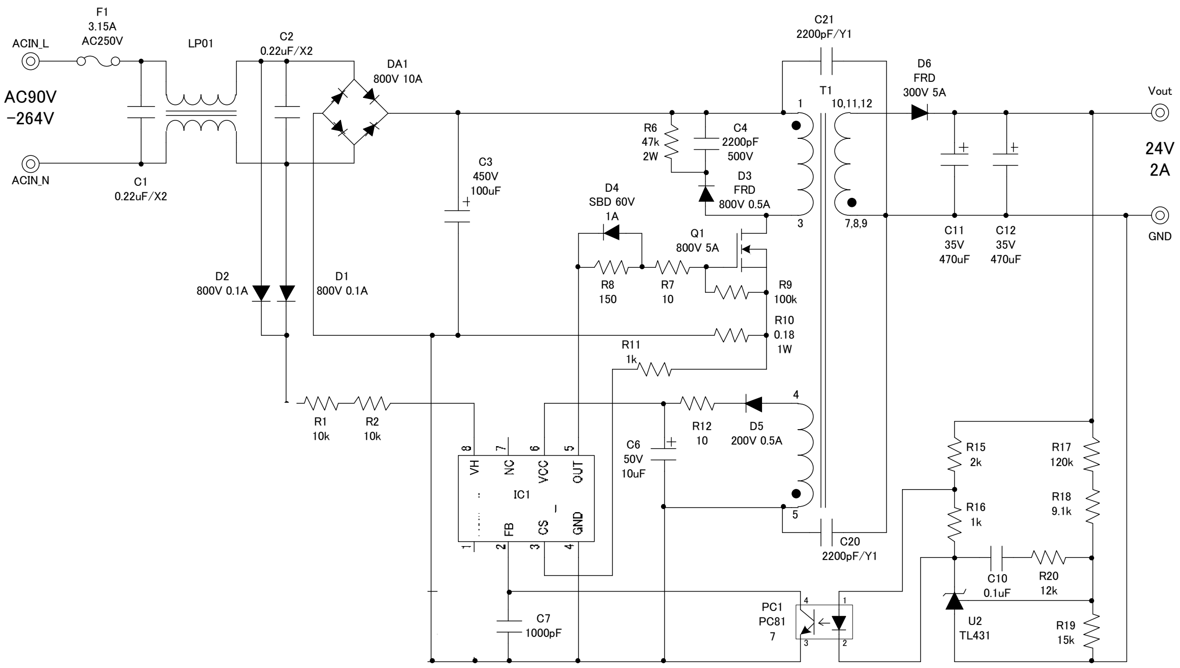


Figure 28. Application Circuit Example

● Operation modes of protection circuit

Table 3 lists the operation mode of each protection function.

Table 3. Operation Modes of Protection Circuit

Function	Operation mode
VCC Undervoltage Locked Out	Auto recovery
VCC Overvoltage Protection	Auto recovery (with 100-us timer)
FB Over Limited Protection	Auto recovery (with 64-us timer)
CS OPEN Protection	Auto recovery (with 100-us timer)

● Sequence

The sequence for this IC is shown in Figure 29.
A transition to OFF mode occurs under all conditions when VCC exceeds 8.2 V.

Figure 29. Sequence Diagram

● **Thermal loss**

In the thermal design, set operations for the following conditions.
(The temperature shown below is the guaranteed temperature, so be sure that a margin is taken into account.)

1. Ambient temperature Ta must be 85°C or less.
2. IC loss must be within the allowable dissipation Pd.

The thermal abatement characteristics are follows. (PCB: 70 mm x 70 mm x 1.6 mm, when mounted on glass epoxy substrate)

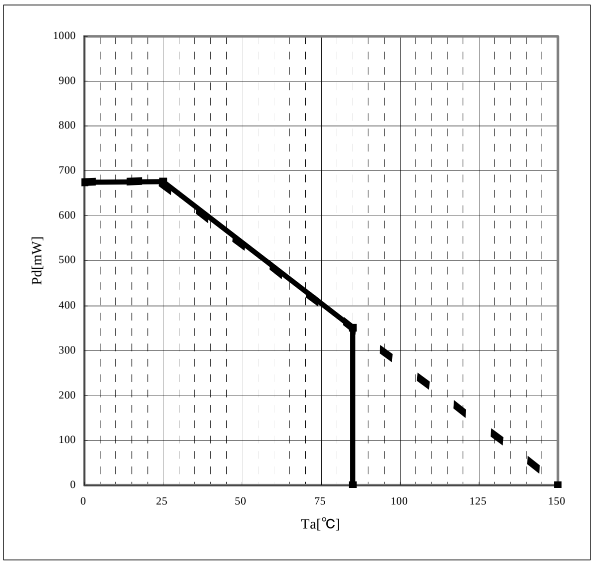


Figure 30. Thermal Abatement Characteristics

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

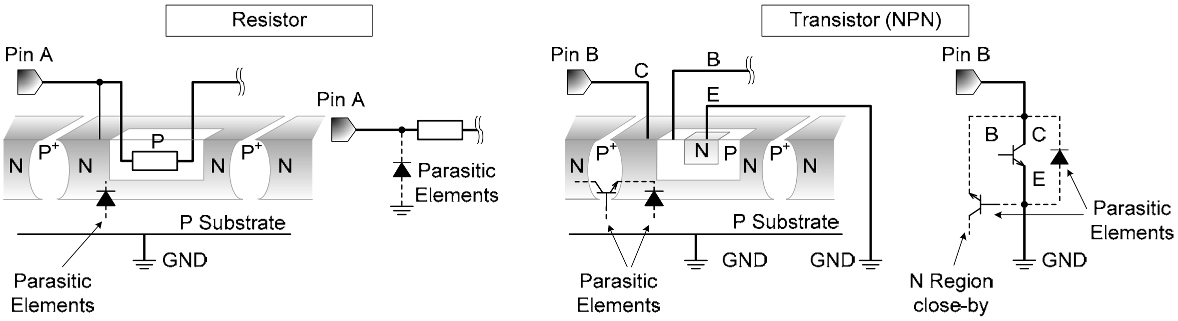


Figure 31. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

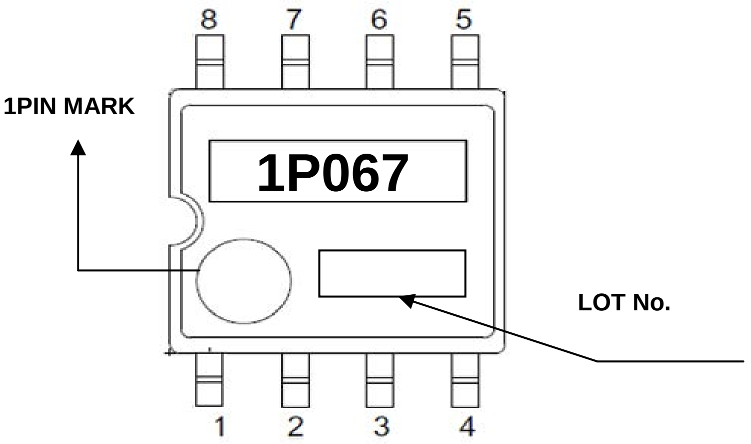
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

● Part Number selection

B M 1 P 0 6 7 F J - E 2

- Part name
- Package
  FJ: **SOP-J8**
- Packaging and forming specifications
  E2: Reel type embossed tape

● Marking diagram

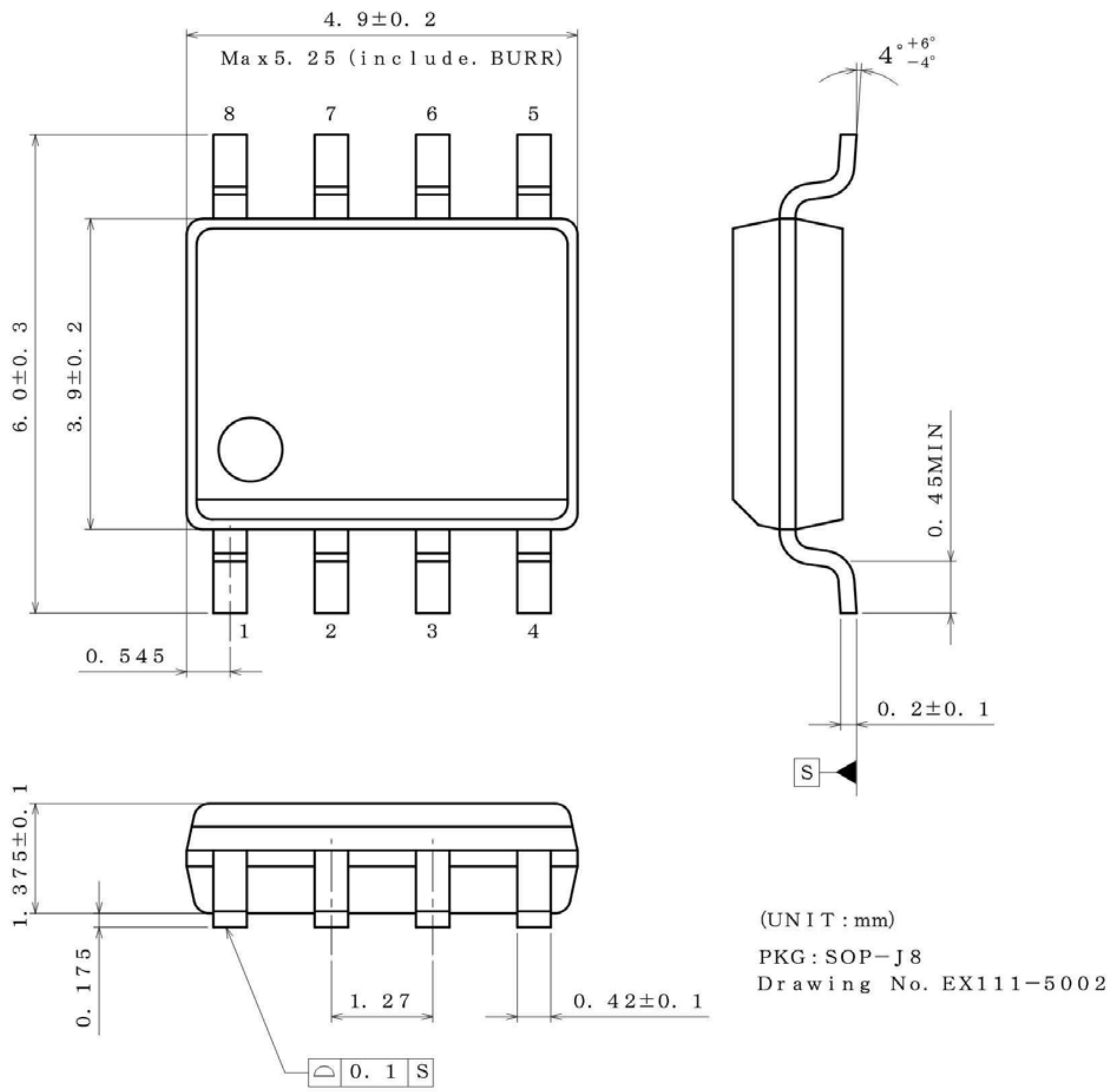


● Line-up

Model name (BM1PXXXFJ)
BM1P061FJ
BM1P062FJ
BM1P063FJ
BM1P064FJ
BM1P065FJ
BM1P066FJ
BM1P067FJ
BM1P068FJ
BM1P101FJ
BM1P102FJ
BM1P103FJ
BM1P104FJ
BM1P105FJ
BM1P106FJ
BM1P107FJ
BM1P108FJ

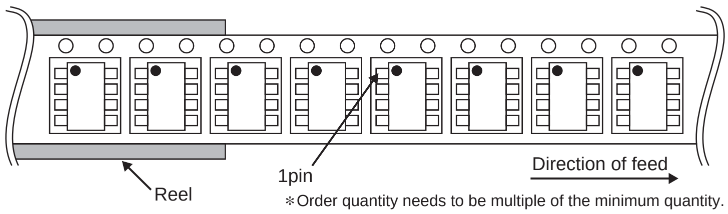
Physical Dimension, Tape and Reel Information

Package Name	SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
02.Oct.2013	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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