

Automotive IPD Series

1ch/2ch Low Side Switch IC

BV1LC105FJ-C / BM2LC105FJ-C

Features

- AEC-Q100 Qualified (Note1)
- Built-in overcurrent limiting circuit(OCP)
- Built-in thermal shutdown circuit(TSD)
- Built-in active clamp circuit
- Built-in Open load detection circuit(OLD) at output off
- Direct control enabled from CMOS logic IC, etc.
- Built-in diagnostic(ST) output function
- On-state resistance $R_{DS(ON)}=105m\Omega$ (Typ)
(when $V_{IN}=5V$, $I_{out}=0.8A$, $T_j=25^\circ C$)
- Monolithic power management IC with the control block (CMOS) and power MOS FET mounted on a single chip
- Surface mount package SOP-J8
(Note 1) Grade1

Product Summary

On-state resistance ($T_j=25^\circ C$, Typ)	105m Ω
Overcurrent limit ($T_j=25^\circ C$, Typ)	6A
Output clamp voltage (Min)	42V
Active clamp energy ($T_j=25^\circ C$)	150mJ

Package
SOP-J8

W(Typ) x D(Typ) x H(Max)
4.90mm x 6.00mm x 1.65mm

General Description

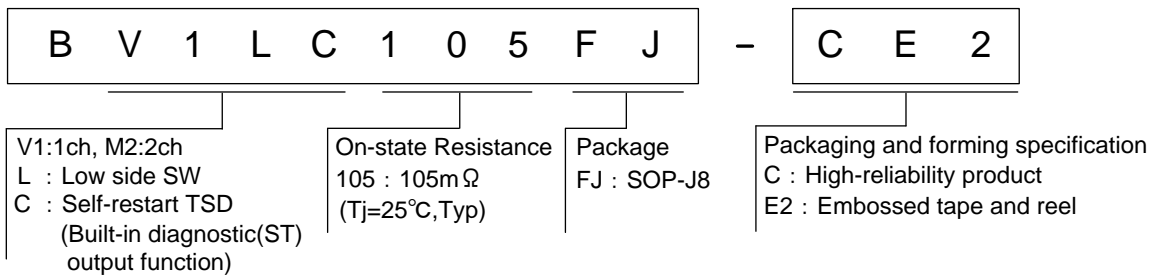
BV1LC105FJ-C is 1ch, BM2LC105FJ-C is 2ch automotive low side switch IC, which has built-in overcurrent limiting circuit, thermal shutdown circuit, overvoltage (active clamp) protection circuit and open load detection circuit.



Applications

Low side switch for driving resistive, Inductive load, Capacitive load

Ordering Information



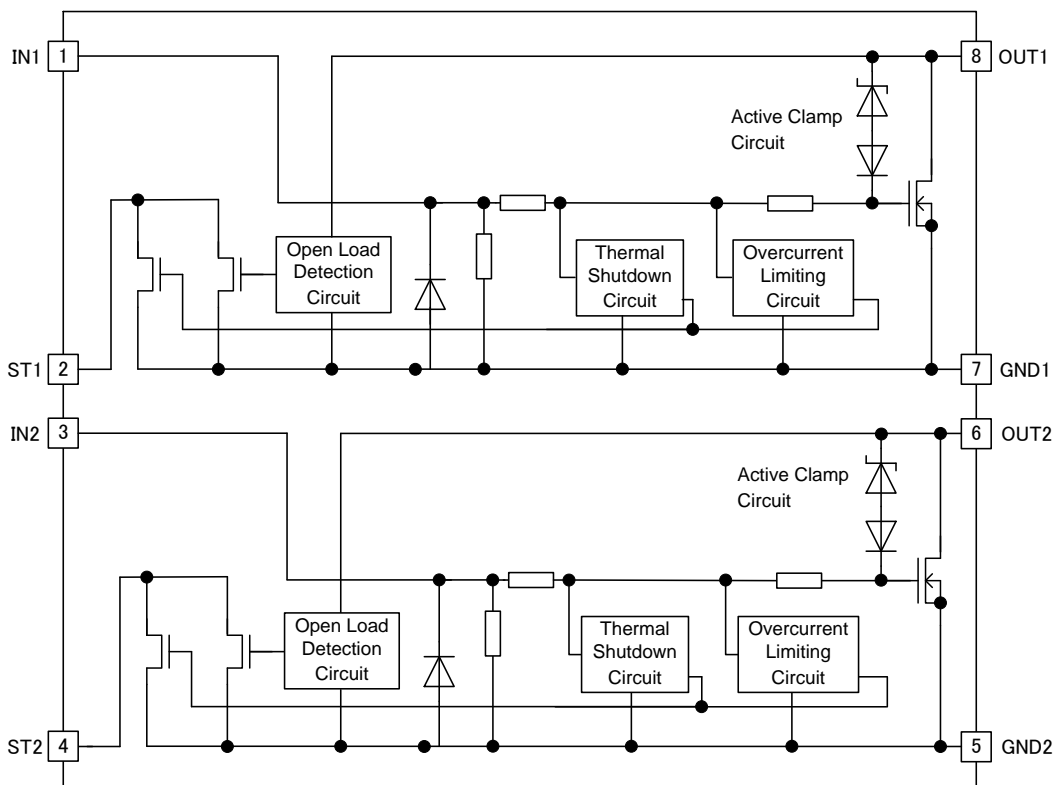
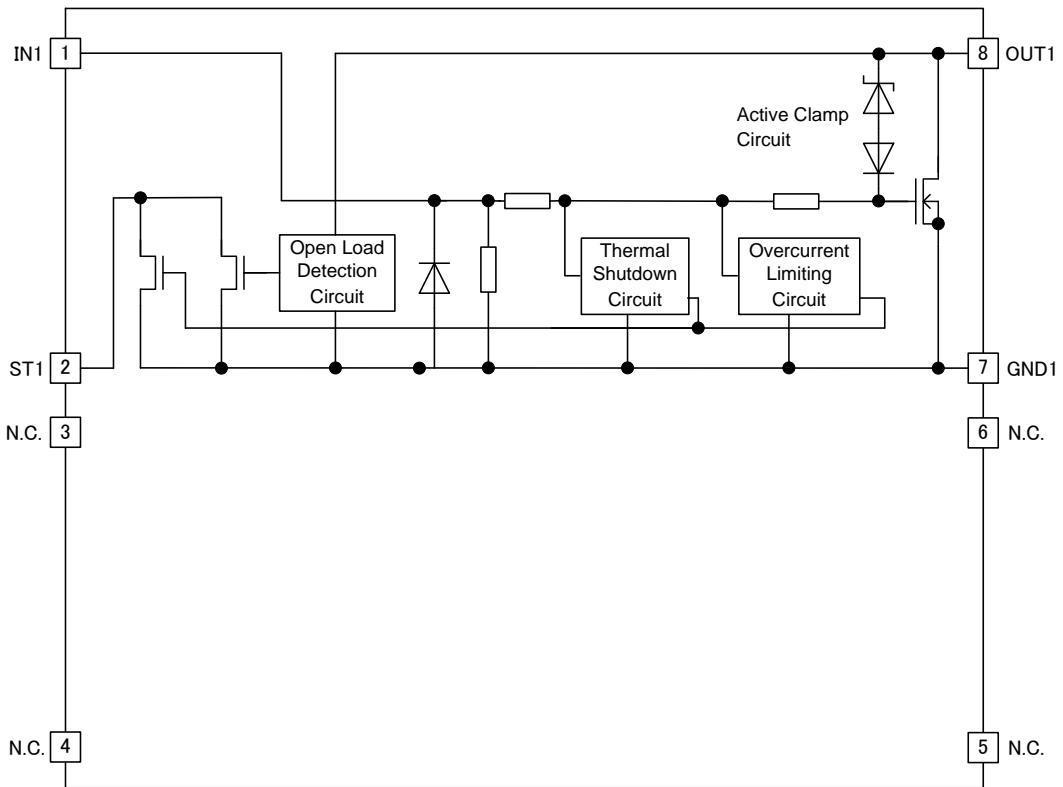
Line up

On-state resistance (Typ)	Ordering Information (Typ)	Total channel number	Package	Ordering Information
105m Ω	6A	1	SOP-J8	BV1LC105FJ-CE2
		2		BM2LC105FJ-CE2

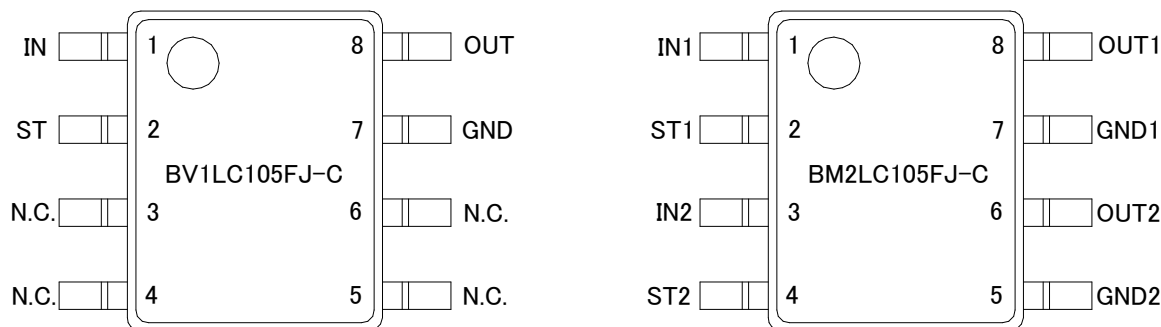
○Product structure: Silicon monolithic integrated circuit

○This product is not designed to protect it from radiation.

Block Diagrams



Pin Configurations



Pin Descriptions

■ BV1LC105FJ-C

Pin No.	Symbol	Function
1	IN	Input pin. Input pin is used to internally connect a pull-down resistor.
2	ST	Self-diagnostic output pin
3	N.C.	N.C pin ^(Note 1)
4	N.C.	N.C pin ^(Note 1)
5	N.C.	N.C pin ^(Note 1)
6	N.C.	N.C pin ^(Note 1)
7	GND	GND pin
8	OUT	Output pin

(Note 1) N.C.Pin is recommended to short with GND. N.C.Pin can be open because it isn't connect it inside of IC.

■ BM2LC105FJ-C

Pin No.	Symbol	Function
1	IN1	Input pin 1. Input pin is used to internally connect a pull-down resistor.
2	ST1	Self-diagnostic output pin 1
3	IN2	Input pin 2. Input pin is used to internally connect a pull-down resistor.
4	ST2	Self-diagnostic output pin 2
5	GND2	GND pin 2
6	OUT2	Output pin 2
7	GND1	GND pin 1
8	OUT1	Output pin 1

Definition

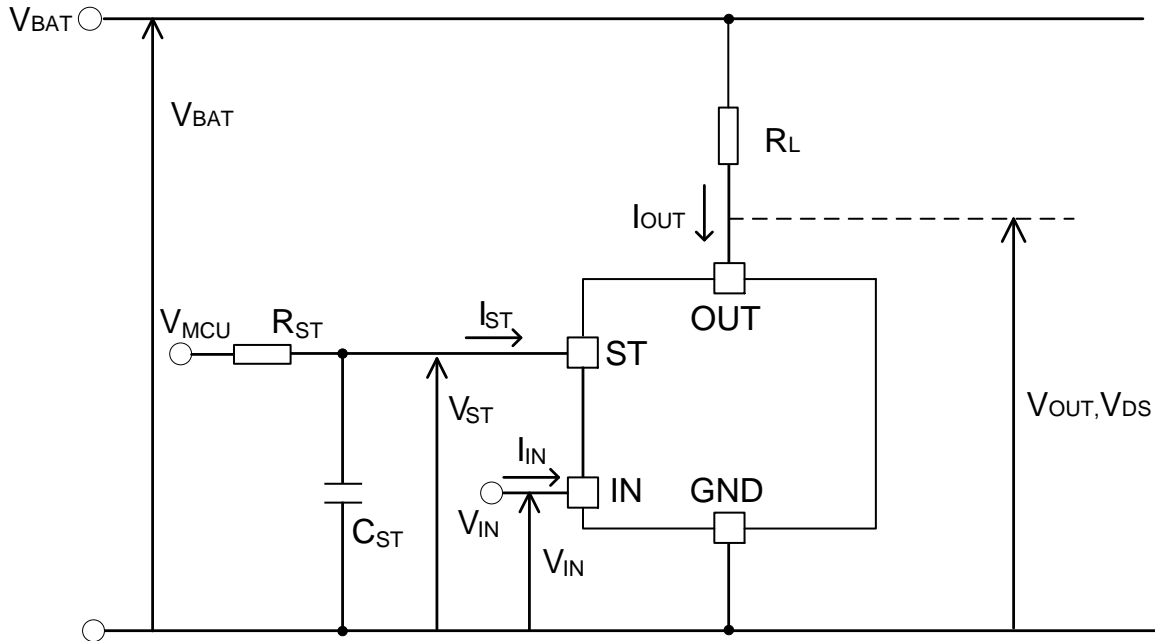


Figure 1. Definition

Absolute Maximum Ratings (T_j = 25°C)

Parameter	Symbol	Ratings	Unit
Drain-Source voltage in output block	V _{DS}	-0.3 to +42 (Note 1)	V
Input voltage	V _{IN}	-0.3 to +7.0	V
Output current (DC)	I _{OUT(OCF)}	3.0(Internally limited) (Note 2)	A
Diagnostic output voltage	V _{ST}	-0.3 to +7.0	V
Diagnostic output current	I _{ST}	10	mA
Active clamp energy (Single pulse) T _{j(start)} = 25°C (Note 3)	E _{AS(25°C)}	150	mJ
Active clamp energy (Single pulse) T _{j(start)} = 150°C (Note 3) (Note 4)	E _{AS(150°C)}	50	
Operating temperature range	T _j	-40 to +150	°C
Storage temperature range	T _{stg}	-55 to +150	°C
Maximum junction temperature	T _{jmax}	150	°C

(Note 1) Please refer to P.21 "Operation Notes", when is used at less than -0.3V.

(Note 2) Internally limited by the overcurrent limiting circuit.

(Note 3) Maximum Active clamp energy, using single non-repetitive pulse of I_{AR} = 1.9A, V_{BAT} = 16V .

$$E_{AS} = \frac{1}{2} I_{AR}^2 \cdot \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CL)}} \right)$$

(Note 4) Not 100% tested.

Thermal Characteristics (Note 1)

Parameter	Symbol	Ratings	Unit	Conditions
SOP-J8(1ch ON)				
Thermal Resistance between channel and ambient temperature	θ_{JA}	167.9	°C / W	1s (Note 2)
		105.8	°C / W	2s (Note 3)
		85.6	°C / W	2s2p (Note 4)

Parameter	Symbol	Ratings	Unit	Conditions
SOP-J8(All ch ON)				
Thermal Resistance between channel and ambient temperature	θ_{JA}	141.5	°C / W	1s (Note 2)
		84.1	°C / W	2s (Note 3)
		67.1	°C / W	2s2p (Note 4)

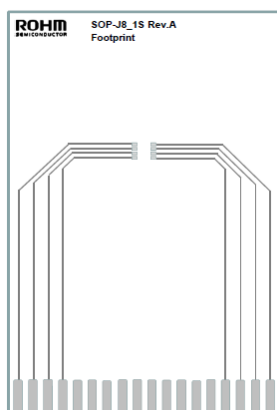
(Note 1) The thermal impedance is based on JESD51 - 2A (Still - Air) standard . It is used the chip of BM2LC105FJ-C

(Note 2) JESD51 - 3 compliance FR4 114.3 mm x 76.2 mm x 1.57 mm 1 layer (1s)
(top layer copper : Rohm recommend land pattern + measurement wiring, copper thickness 2oz)

(Note 3) JESD51 -5 compliance FR4 114.3 mm x 76.2 mm x 1.60 mm 2 layer (2s)
(top layer copper : Rohm recommend land pattern + measurement wiring, bottom layer copper area : 74.2 mm x 74.2 mm,
Copper thickness (top and bottom layers) 2 oz)

(Note 4) JESD51 -5 / -7 compliance FR4 114.3 mm x 76.2 mm x 1.60 mm 4 layer (2s2p)
(top layer copper : Rohm recommend land pattern + measurement wiring / 2 layer, 3 layer, bottom layer copper area: 74.2 mm x 74.2 mm,
Copper thickness (top and bottom layers / inner layer) 2 oz / 1oz)

■ PCB layout 1 layer (1s)



Footprint Only

Figure 2. PCB layout 1 layer (1s)

Dimension	Value
Board finish thickness	1.57 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top layer)	0.070mm (Cu:2oz)

■ PCB layout 2layers (2s)

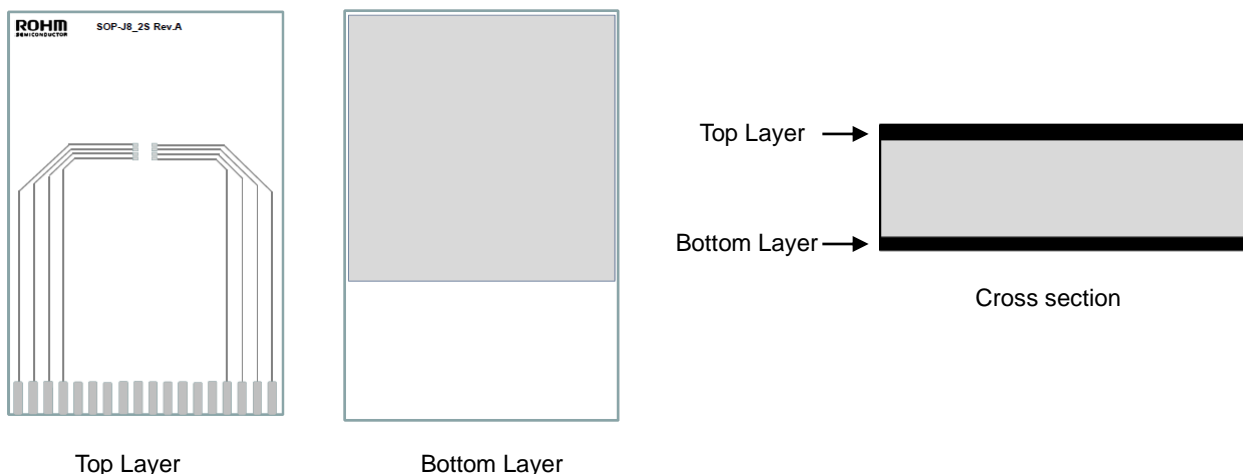


Figure 3. PCB layout 2layer (2s)

Dimension	Value
Board finish thickness	1.60 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu + Plating)

■ PCB layout 4layers (2s2p)

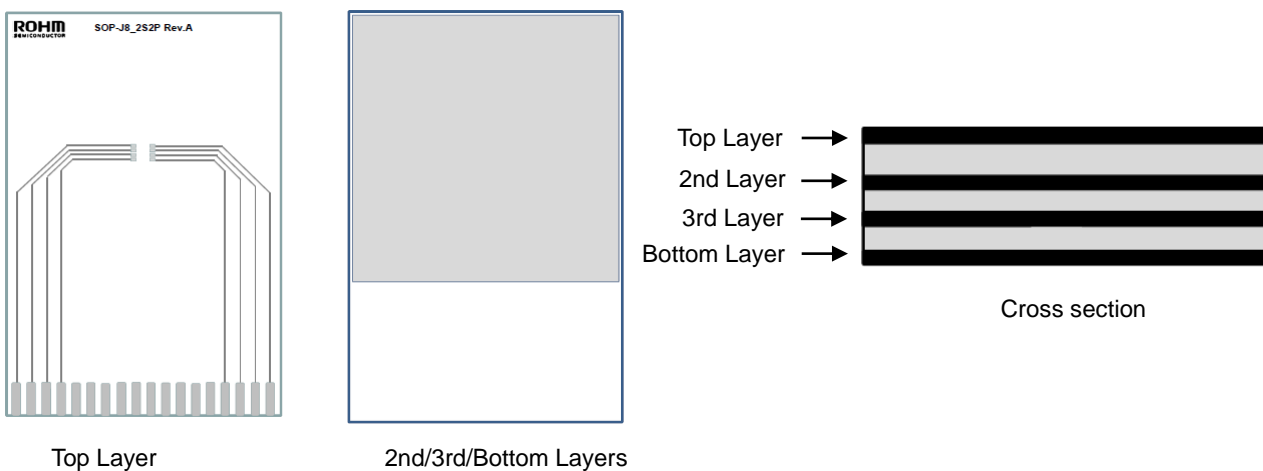


Figure 4. PCB layout 4layer (2s2p)

Dimension	Value
Board finish thickness	1.60 mm ± 10%
Board dimension	76.2 mm x 114.3 mm
Board material	FR4
Copper thickness (Top/Bottom layers)	0.070mm (Cu + Plating)
Copper thickness (Inner layers)	0.035mm

■ Transient Thermal Resistance (Single Pulse) 1ch ON

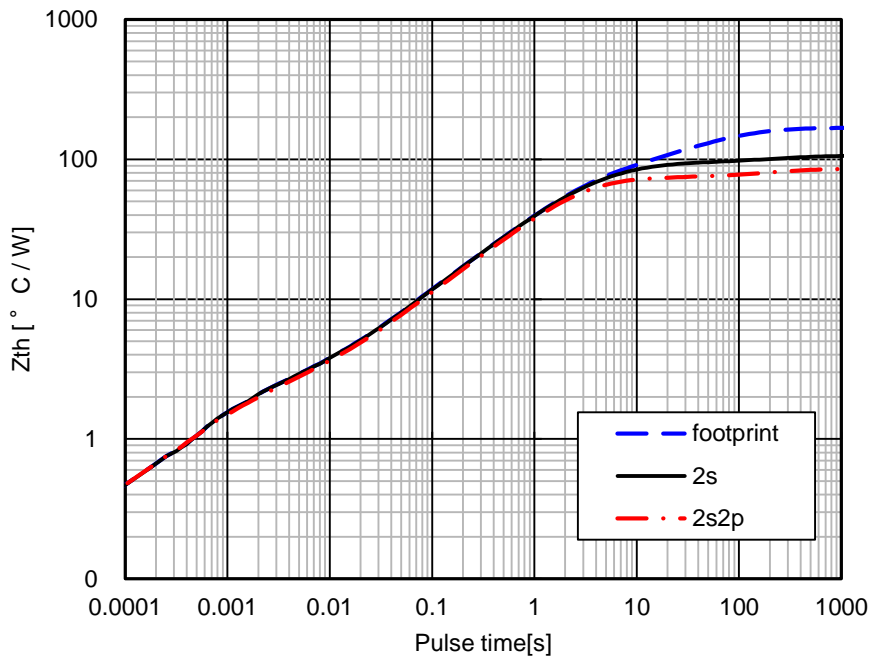


Figure 5. Transient Thermal Resistance

■ Transient Thermal Resistance (Single Pulse) All ch ON

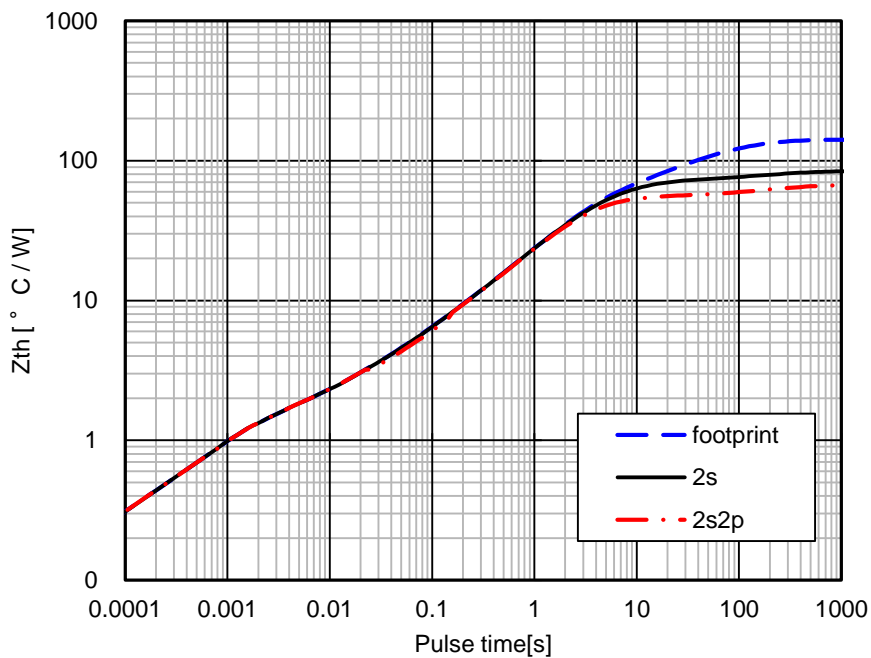


Figure 6. Transient Thermal Resistance

Electrical Characteristics1 (Unless otherwise specified, $-40^{\circ}\text{C} \leq T_j \leq +150^{\circ}\text{C}$ and $V_{\text{IN}}=3.0\text{V}$ to 5.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Output Clamp Voltage	$V_{\text{OUT(CL)}}$	42	48	54	V	$V_{\text{IN}}=0\text{V}, I_{\text{OUT}}=1\text{mA}$
On-state Resistance1 (at 25 °C)	$R_{\text{DS(ON)1}}$	-	105	130	m Ω	$V_{\text{IN}}=5\text{V}, I_{\text{OUT}}=0.8\text{A}, T_j=25^{\circ}\text{C}$
On-state Resistance1 (at 150 °C)	$R_{\text{DS(ON)1}}$	-	200	250	m Ω	$V_{\text{IN}}=5\text{V}, I_{\text{OUT}}=0.8\text{A}, T_j=150^{\circ}\text{C}$
On-state Resistance2 (at 25 °C)	$R_{\text{DS(ON)2}}$	-	135	175	m Ω	$V_{\text{IN}}=3\text{V}, I_{\text{OUT}}=0.8\text{A}, T_j=25^{\circ}\text{C}$
On-state Resistance2 (at 150 °C)	$R_{\text{DS(ON)2}}$	-	245	315	m Ω	$V_{\text{IN}}=3\text{V}, I_{\text{OUT}}=0.8\text{A}, T_j=150^{\circ}\text{C}$
Leak Current (at 25 °C)	$I_{\text{OUT(L)}}$	40	60	80	μA	$V_{\text{IN}}=0\text{V}, V_{\text{OUT}}=18\text{V}, T_j=25^{\circ}\text{C}$
Leak Current (at 150 °C)	$I_{\text{OUT(L)}}$	50	85	200	μA	$V_{\text{IN}}=0\text{V}, V_{\text{OUT}}=18\text{V}, T_j=150^{\circ}\text{C}$
Turn-ON TIME1	t_{ON1}	-	-	80	μs	$V_{\text{IN}}=0\text{V}$ to 5V , $R_{\text{L}}=15\Omega$, $V_{\text{BAT}}=12\text{V}$, $T_j=25^{\circ}\text{C}$
Turn-OFF TIME1	t_{OFF1}	-	-	80	μs	$V_{\text{IN}}=5\text{V}$ to 0V , $R_{\text{L}}=15\Omega$, $V_{\text{BAT}}=12\text{V}$, $T_j=25^{\circ}\text{C}$
Turn-ON TIME2	t_{ON2}	-	-	80	μs	$V_{\text{IN}}=\text{OPEN}$ to 5V , $R_{\text{L}}=15\Omega$, $V_{\text{BAT}}=12\text{V}$, $T_j=25^{\circ}\text{C}$
Turn-OFF TIME2	t_{OFF2}	-	-	100	μs	$V_{\text{IN}}=5\text{V}$ to OPEN , $R_{\text{L}}=15\Omega$, $V_{\text{BAT}}=12\text{V}$, $T_j=25^{\circ}\text{C}$
Slew rate on1	SR_{ON1}	-	0.7	1.2	V/ μs	$V_{\text{IN}}=0\text{V}$ to 5V , $R_{\text{L}}=15\Omega$, $V_{\text{BAT}}=12\text{V}$, $T_j=25^{\circ}\text{C}$
Slew rate off1	SR_{OFF1}	-	1.0	1.5	V/ μs	$V_{\text{IN}}=5\text{V}$ to 0V , $R_{\text{L}}=15\Omega$, $V_{\text{BAT}}=12\text{V}$, $T_j=25^{\circ}\text{C}$
Slew rate on2	SR_{ON2}	-	0.7	1.2	V/ μs	$V_{\text{IN}}=\text{OPEN}$ to 5V , $R_{\text{L}}=15\Omega$, $V_{\text{BAT}}=12\text{V}$, $T_j=25^{\circ}\text{C}$
Slew rate off2	SR_{OFF2}	-	1.0	1.5	V/ μs	$V_{\text{IN}}=5\text{V}$ to OPEN , $R_{\text{L}}=15\Omega$, $V_{\text{BAT}}=12\text{V}$, $T_j=25^{\circ}\text{C}$
Input Threshold Voltage	$V_{\text{IN(TH)}}$	1.5	-	2.7	V	$I_{\text{OUT}}=1\text{mA}$
High-level Input Current1 (in normal operation)	$I_{\text{IN(H)1}}$	-	125	250	μA	$V_{\text{IN}}=5\text{V}$
High-level Input Current2 (in abnormal operation) ^(Note1)	$I_{\text{IN(H)2}}$	-	-	500	μA	$V_{\text{IN}}=5\text{V}$
Low-level Input Current	$I_{\text{IN(L)}}$	-10	0	10	μA	$V_{\text{IN}}=0\text{V}$

(Note1) When Thermal Shutdown circuit or Overcurrent Limiting circuit is ON.

Electrical Characteristics2 (Unless otherwise specified, $-40^{\circ}\text{C} \leq T_j \leq +150^{\circ}\text{C}$ and $V_{\text{IN}}=3.0\text{V}$ to 5.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Overcurrent Detection Current	I_{OCP}	3	6	9	A	$V_{\text{IN}}=5\text{V}$, $V_{\text{BAT}}=12\text{V}$, $T_j=25^{\circ}\text{C}$
Open Load Detection Voltage	V_{OPEN}	1.5	-	4.5	V	$V_{\text{IN}}=0\text{V}$
ST Output On Voltage1	$V_{\text{ST(ON1)}}$	-	0.2	0.5	V	$V_{\text{IN}}=5\text{V}$, $I_{\text{ST}}=1\text{mA}$
ST Output On Voltage2	$V_{\text{ST(ON2)}}$	-	0.2	0.5	V	$V_{\text{IN}}=0\text{V}$, $V_{\text{OUT}}=4.5\text{V}$, $I_{\text{ST}}=0.5\text{mA}$
ST Output Leak Current1	$I_{\text{ST(L1)}}$	-	-	20	μA	$V_{\text{IN}}=5\text{V}$, $V_{\text{ST}}=5\text{V}$
ST Output Leak Current2	$I_{\text{ST(L2)}}$	-	-	20	μA	$V_{\text{IN}}=0\text{V}$, $V_{\text{OUT}}=1.5\text{V}$, $V_{\text{ST}}=5\text{V}$
ST Output Delay Time Detect	T_{STDET}	-	3	30	μs	$V_{\text{IN}}=0\text{V}$, $V_{\text{OUT}}=5\text{V}$ to 1V , $V_{\text{MCU}}=5\text{V}$, $R_{\text{ST}}=10\text{k}\Omega$, $C_{\text{ST}}=10\text{pF}$
ST Output Delay Time Release	T_{STREL}	-	3	30	μs	$V_{\text{IN}}=0\text{V}$, $V_{\text{OUT}}=1\text{V}$ to 5V , $V_{\text{MCU}}=5\text{V}$, $R_{\text{ST}}=10\text{k}\Omega$, $C_{\text{ST}}=10\text{pF}$
TSD Detection Temperature (Note 2)	$T_{j\text{d}}$	150	175	-	$^{\circ}\text{C}$	$V_{\text{IN}}=5\text{V}$
TSD Release Temperature (Note 2)	$T_{j\text{r}}$	135	-	-	$^{\circ}\text{C}$	$V_{\text{IN}}=5\text{V}$
TSD Hysteresis (Note 2)	$T_{j\Delta\text{HYS}}$	-	15	-	$^{\circ}\text{C}$	$V_{\text{IN}}=5\text{V}$

(Note 2) Not 100% tested.

Typical Performance Curves (Unless otherwise specified, $T_j=25^\circ\text{C}, V_{IN}=5.0\text{V}$)

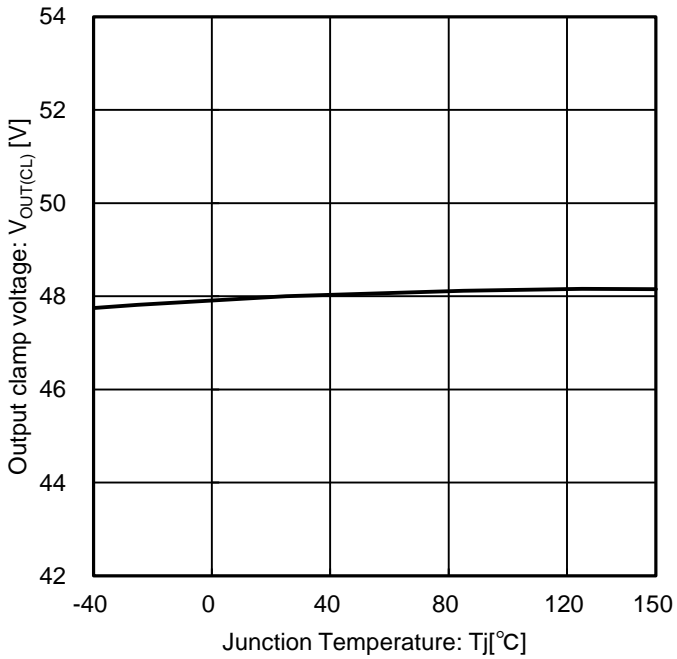


Figure 7. Output clamp voltage vs. Junction Temperature

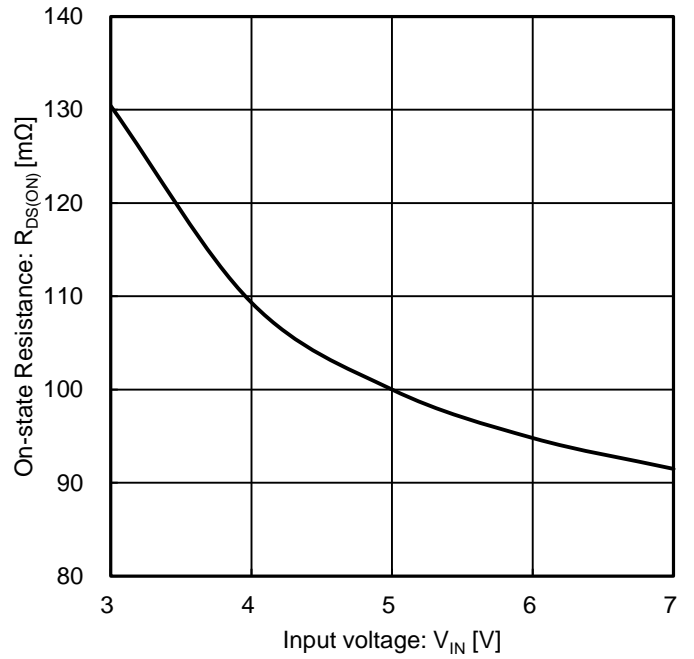


Figure 8. On-state Resistance vs. Input voltage

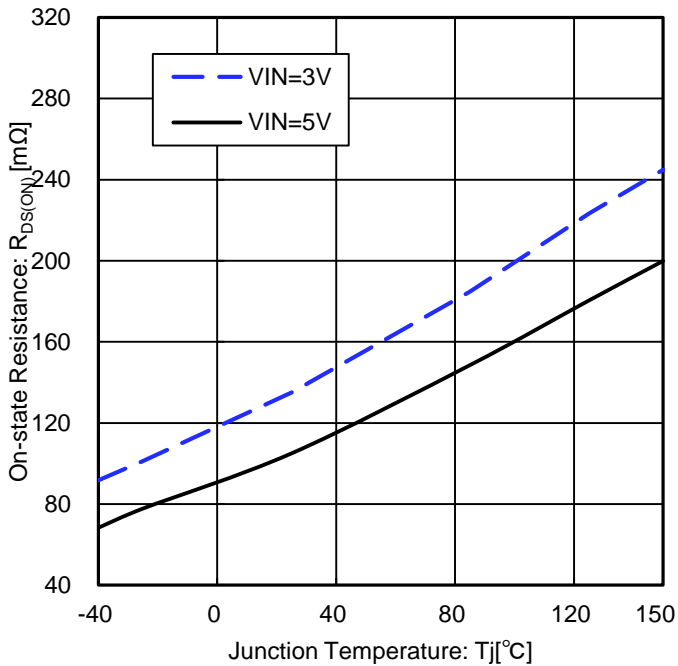


Figure 9. On-state Resistance vs. Junction Temperature

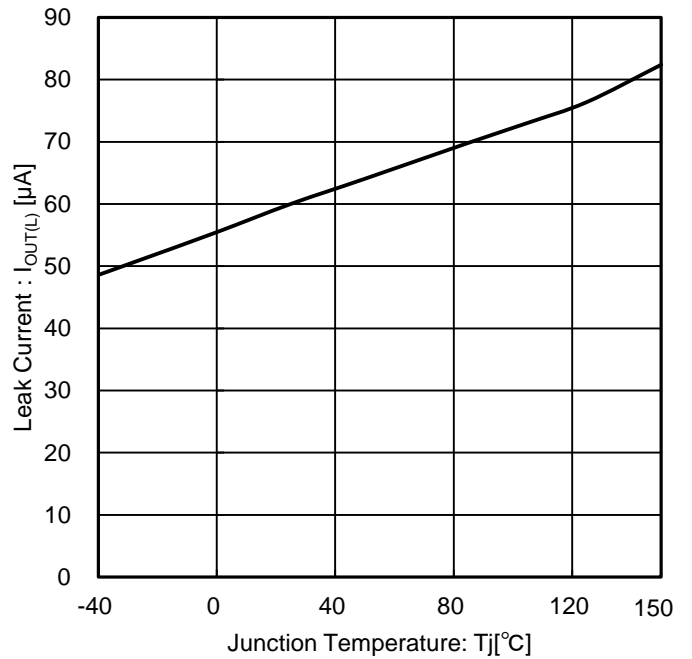


Figure 10. Leak Current vs. Junction Temperature

Typical Performance Curves (Unless otherwise specified, $T_j=25^{\circ}\text{C}, V_{\text{IN}}=5.0\text{V}$) – continued

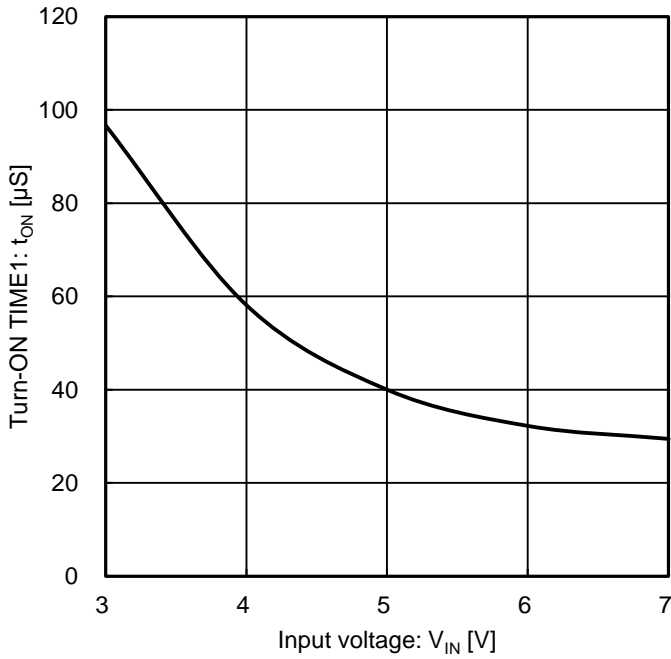


Figure 11. Turn-ON TIME1 vs. Input voltage

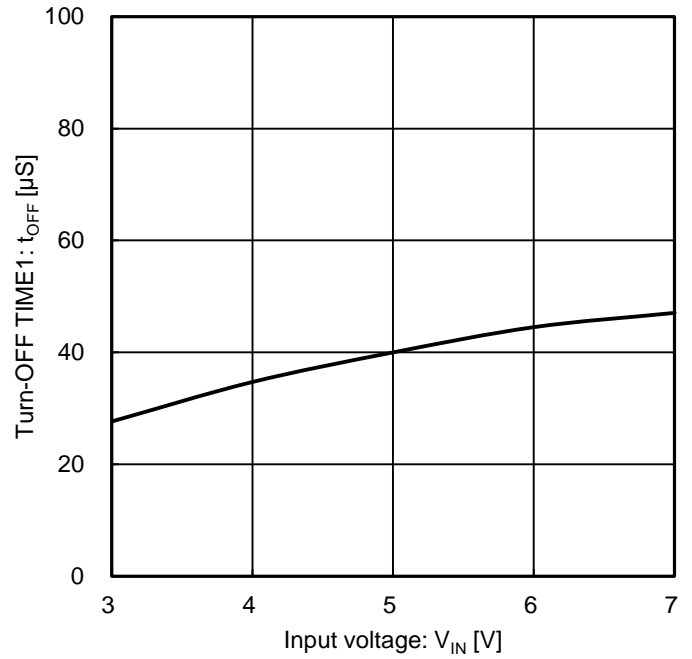


Figure 12. Turn-OFF TIME1 vs. Input voltage

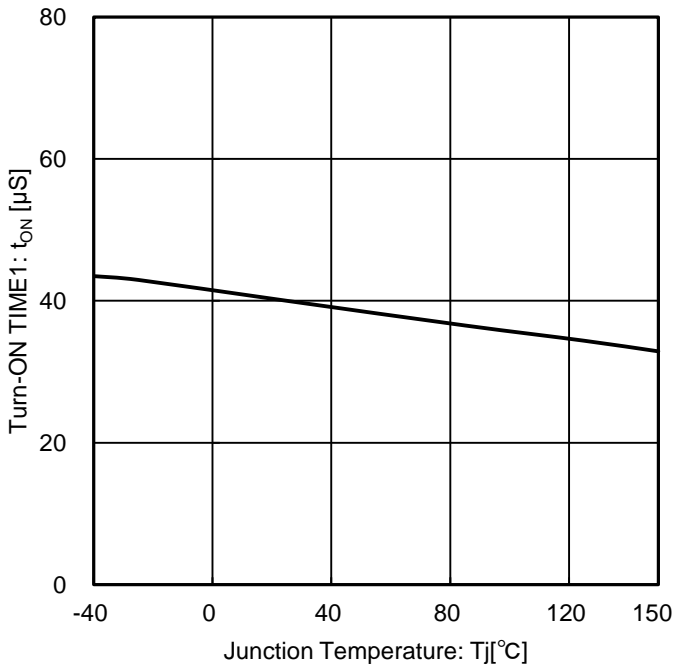


Figure 13. Turn-ON TIME1 vs. Junction Temperature

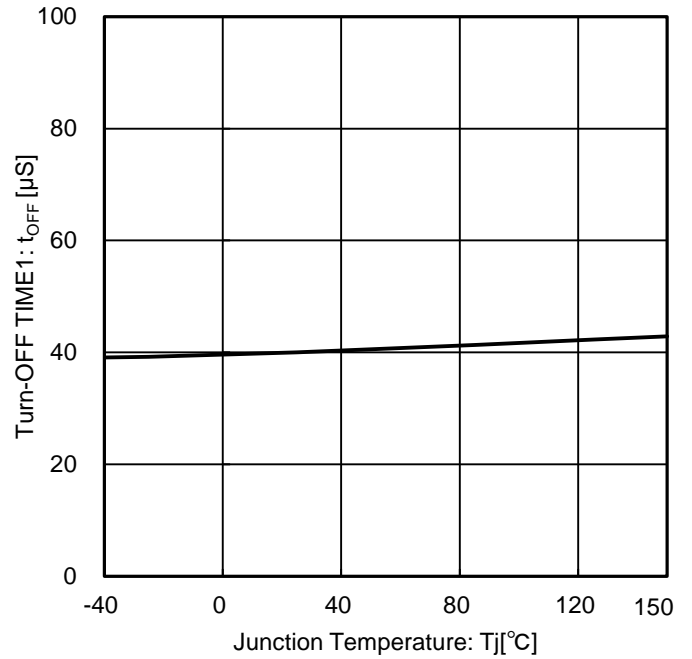


Figure 14. Turn-OFF TIME1 vs. Junction Temperature

Typical Performance Curves (Unless otherwise specified, $T_j=25^{\circ}\text{C}$, $V_{\text{IN}}=5.0\text{V}$) – continued

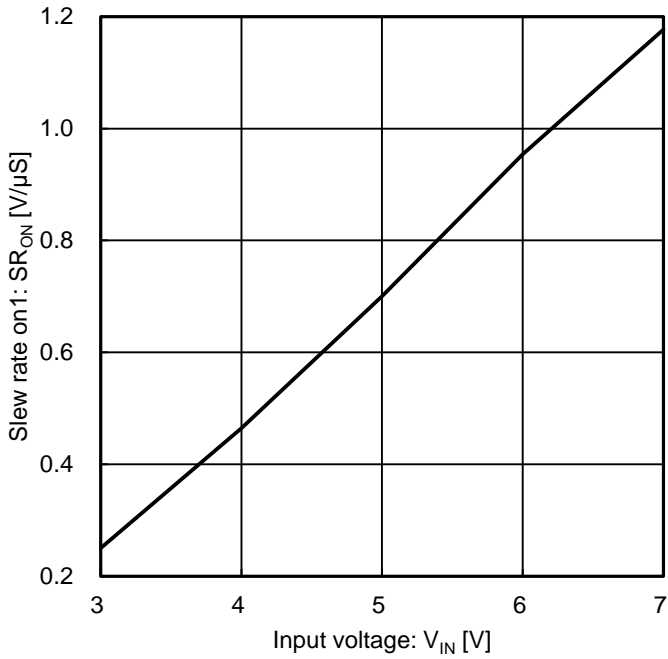


Figure 15. Slew rate on1 vs. Input voltage

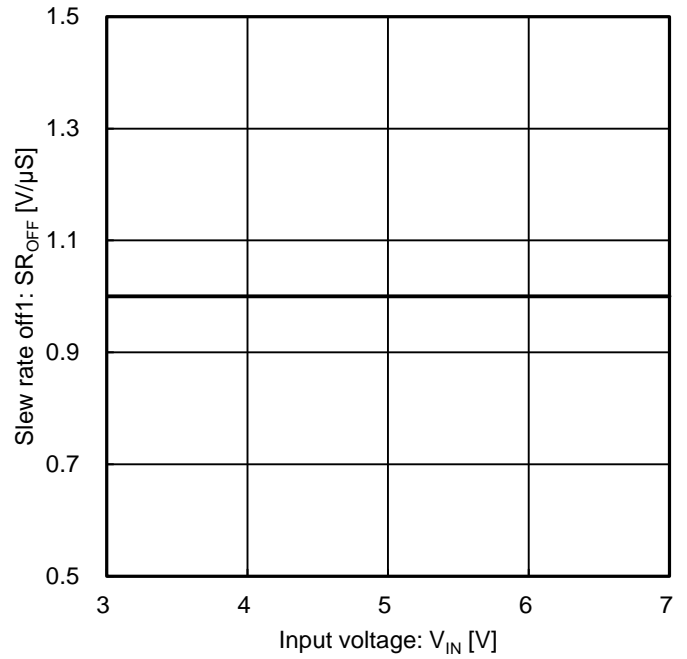


Figure 16. Slew rate off1 vs. Input voltage

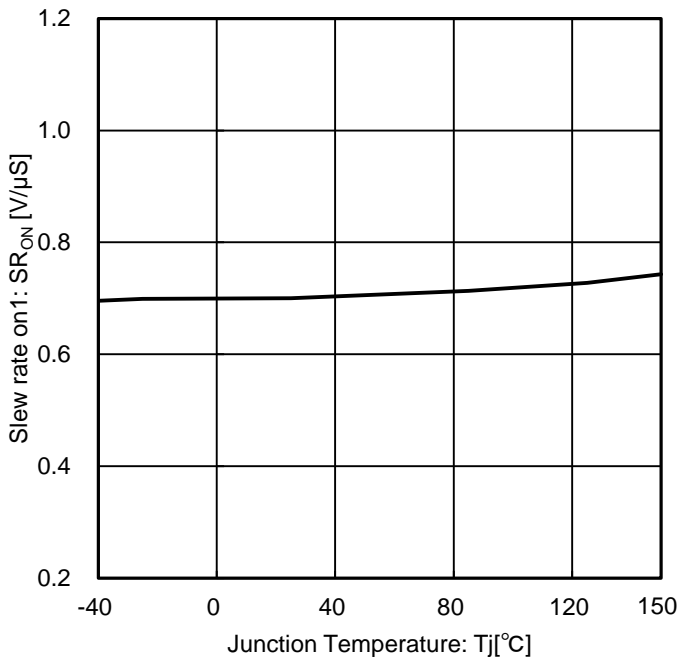


Figure 17. Slew rate on1 vs. Junction Temperature

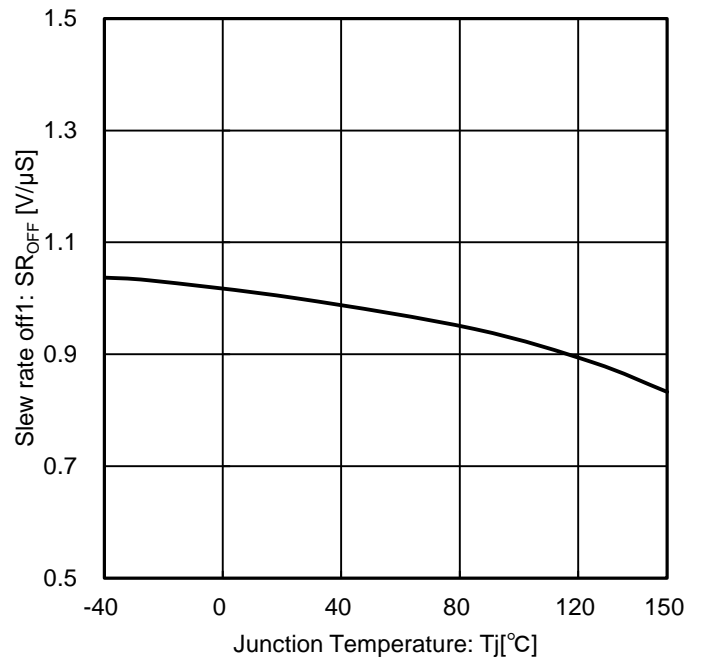


Figure 18. Slew rate off1 vs. Junction Temperature

Typical Performance Curves (Unless otherwise specified, $T_j=25^\circ\text{C}, V_{IN}=5.0\text{V}$) – continued

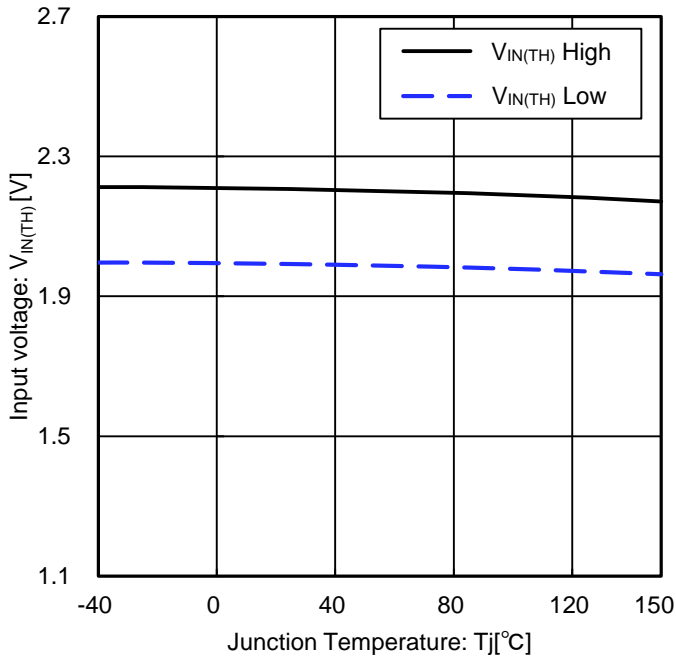


Figure 19. Input voltage vs. Junction Temperature

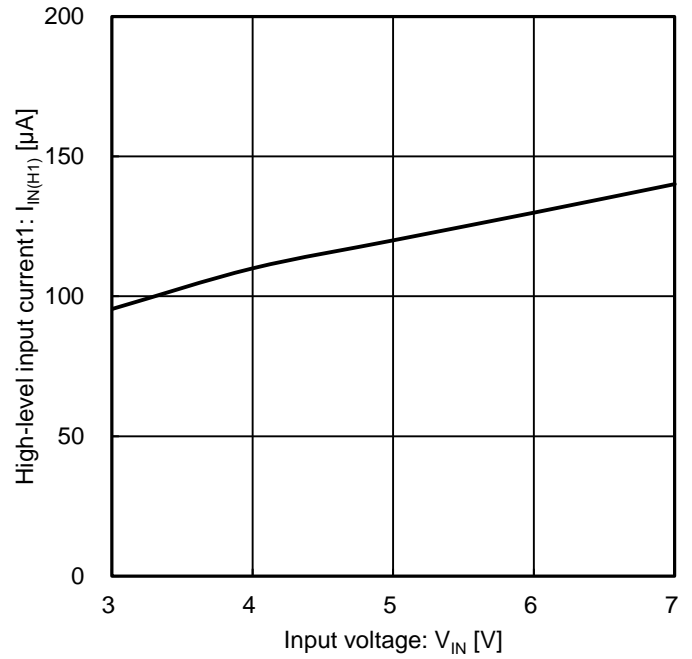


Figure 20. High-level input current1 (in normal operation) vs. Input voltage

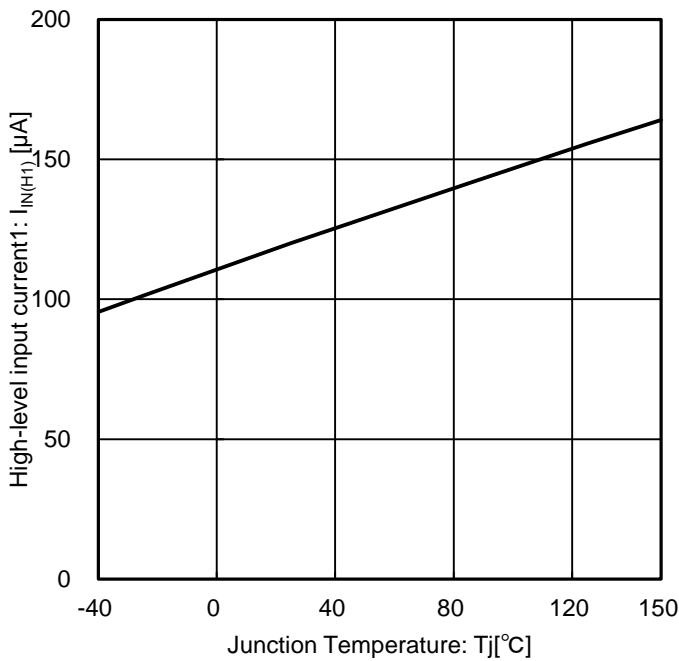


Figure 21. High-level input current1 (in normal operation) vs. Junction Temperature

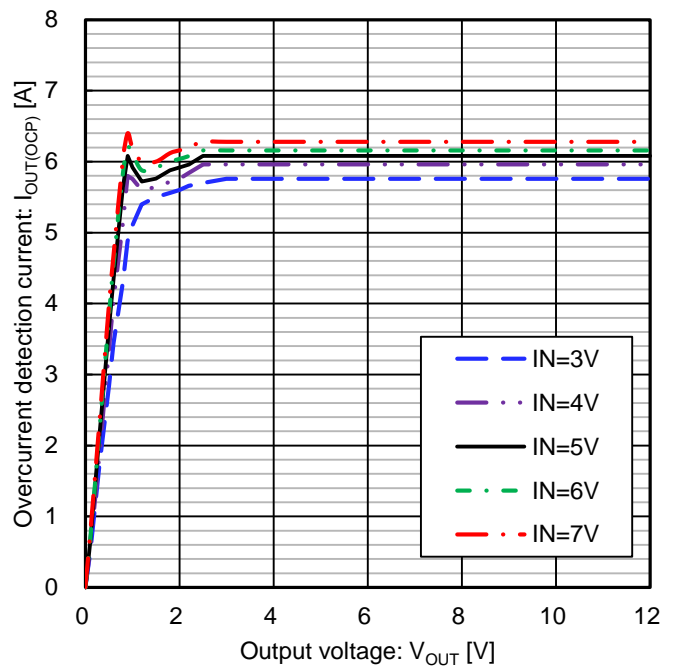


Figure 22. Overcurrent detection current vs. Output voltage

Typical Performance Curves (Unless otherwise specified, $T_j=25^\circ\text{C}$, $V_{IN}=5.0\text{V}$) – continued

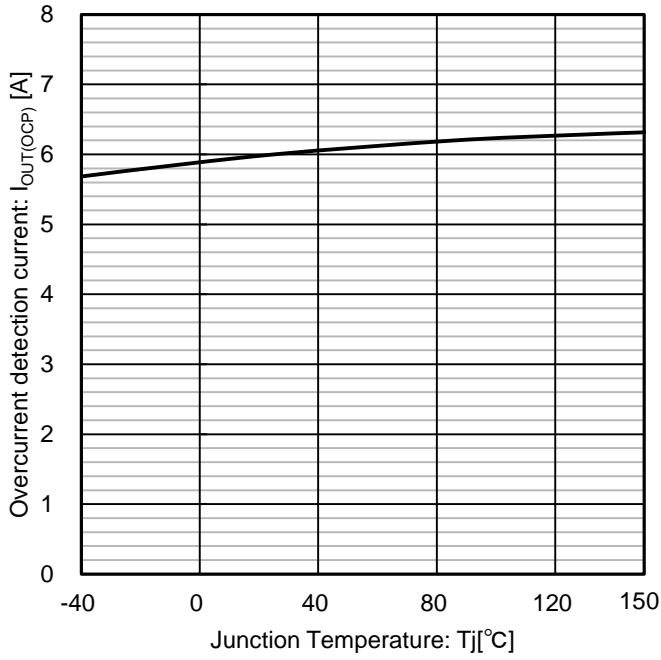


Figure 23. Overcurrent detection current vs. Junction Temperature

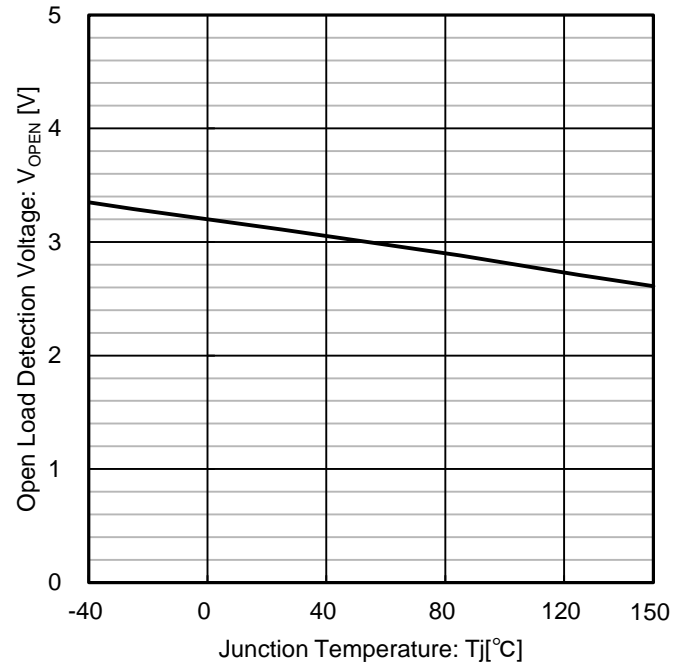


Figure 24. Open Load Detection Voltage vs. junction temperature

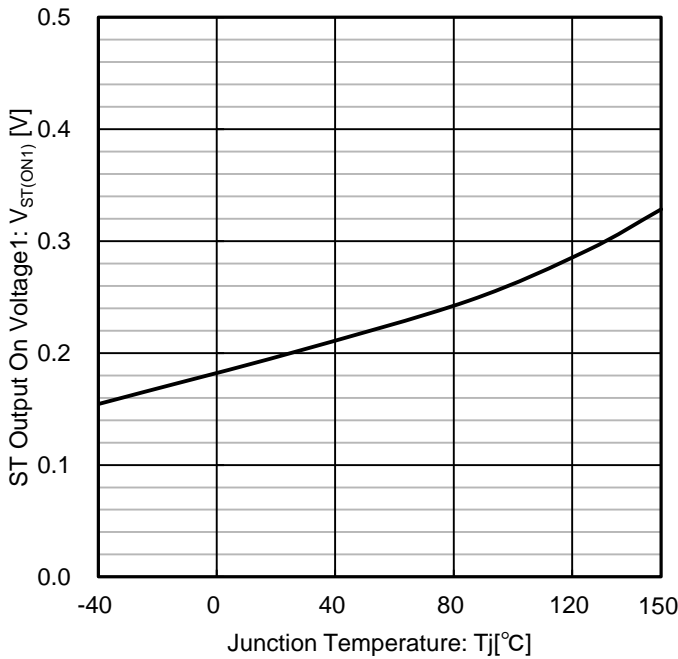


Figure 25. ST Output On Voltage1 vs. junction temperature

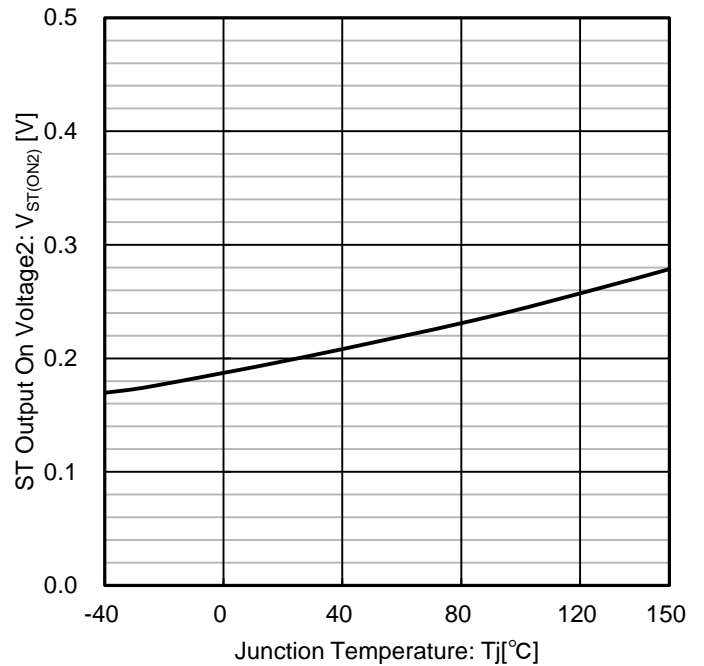


Figure 26. ST Output On Voltage2 vs. junction temperature

Typical Performance Curves (Unless otherwise specified, $T_j=25^\circ\text{C}$, $V_{IN}=5.0\text{V}$) – continued

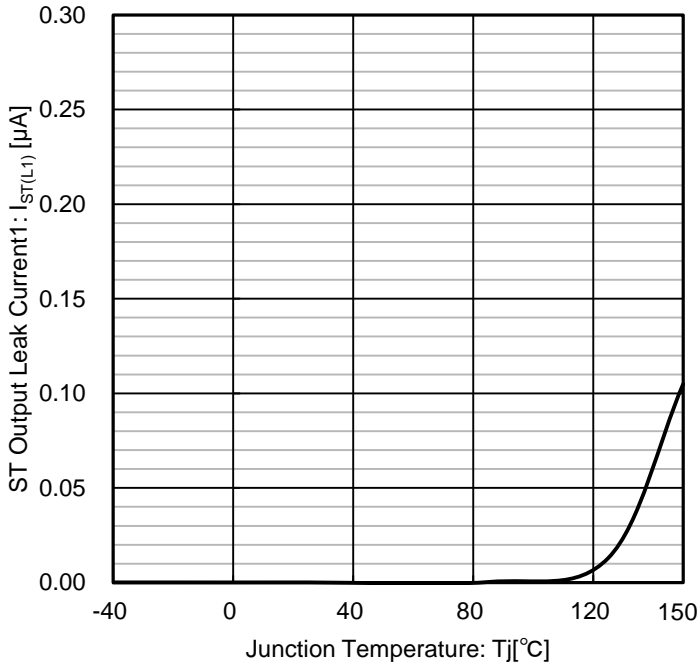


Figure 27. ST Output Leak Current1 vs. junction temperature

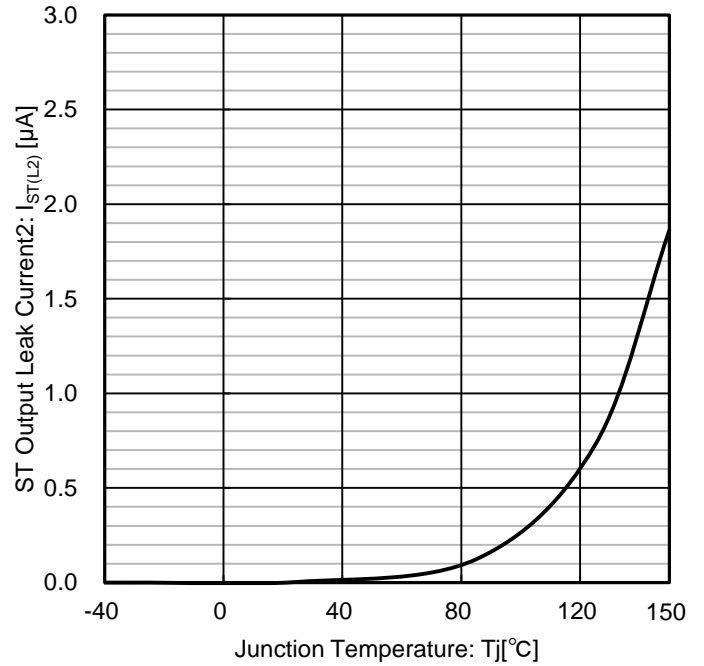


Figure 28. ST Output Leak Current2 vs. junction temperature

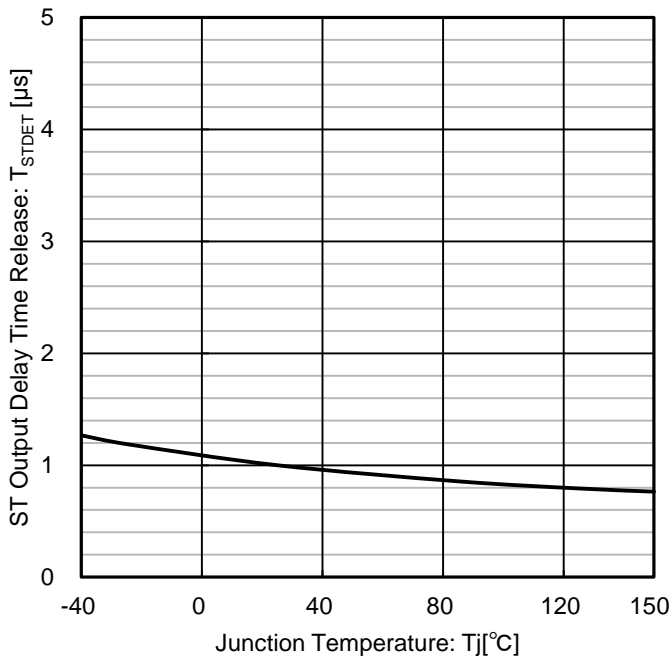


Figure 29. ST Output Delay Time Release vs. junction temperature

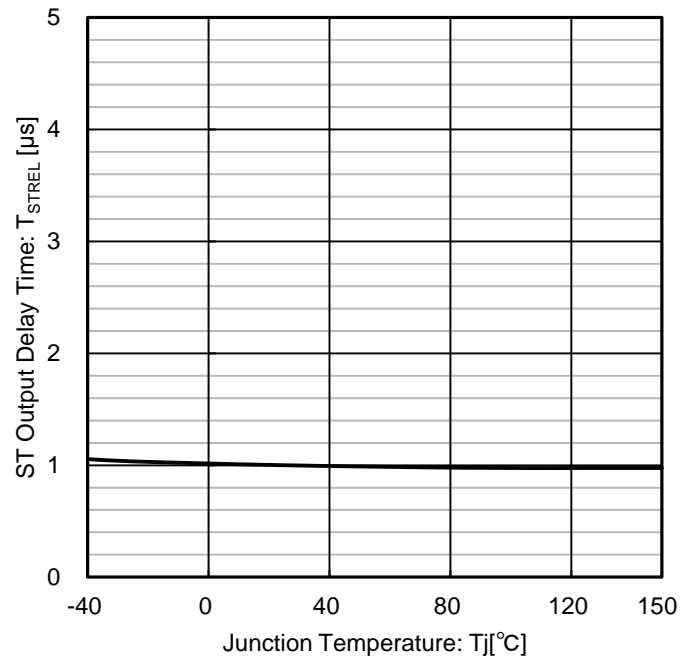
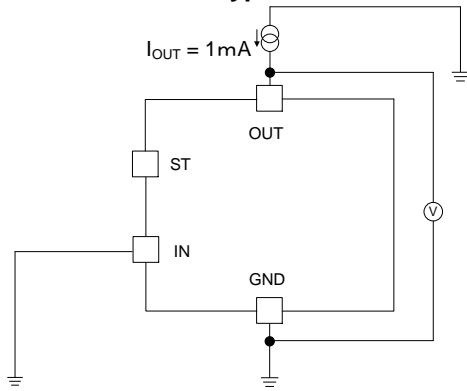
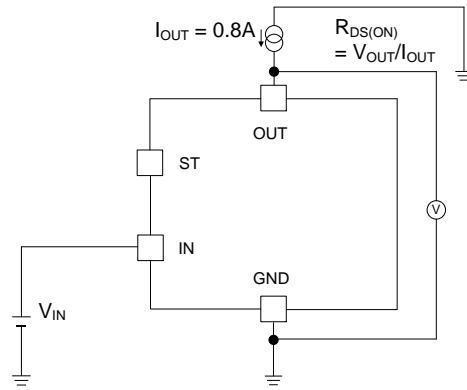


Figure 30. ST Output Delay Time vs. junction temperature

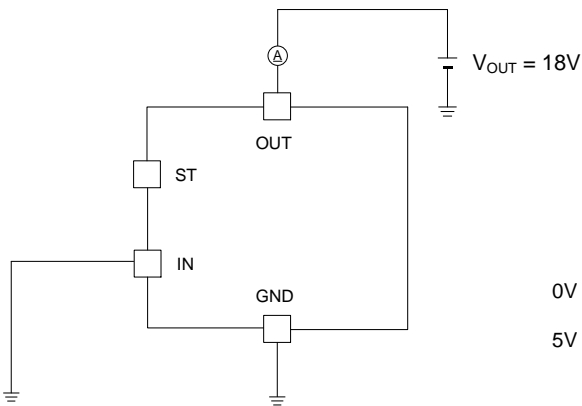
Measurement circuit for Typical Performance Curves



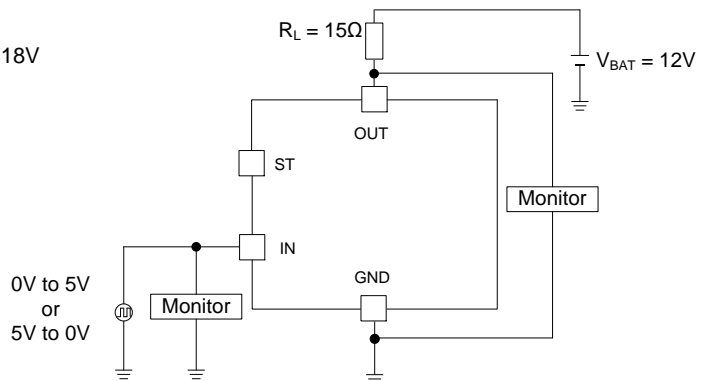
Measurement Circuit for Figure 7



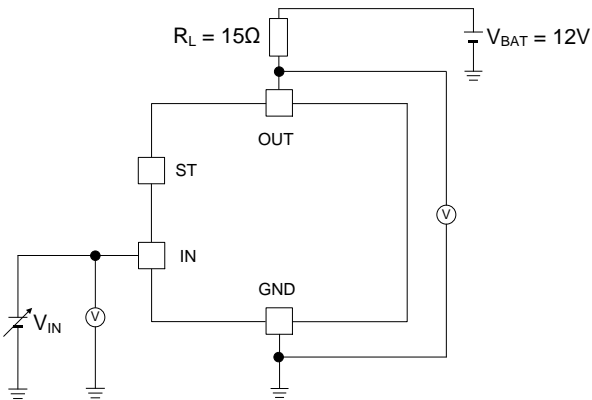
Measurement Circuit for Figure 8,9



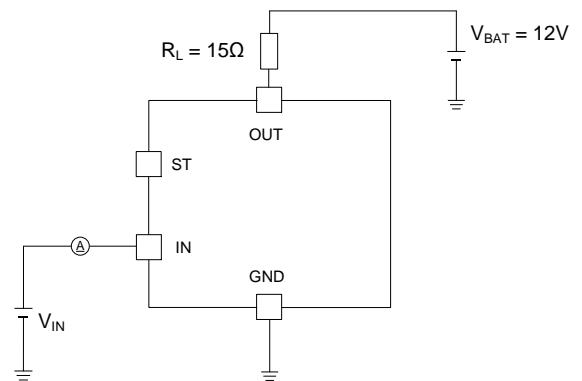
Measurement Circuit for Figure 10



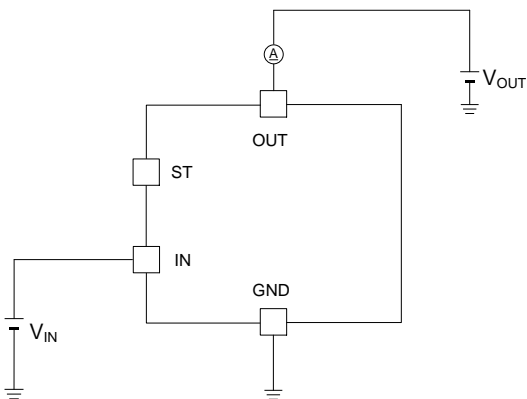
Measurement Circuit for Figure 11, 12, 13, 14, 15, 16, 17, 18



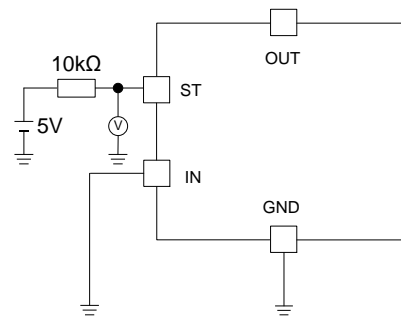
Measurement Circuit for Figure 19



Measurement Circuit for Figure 20, 21

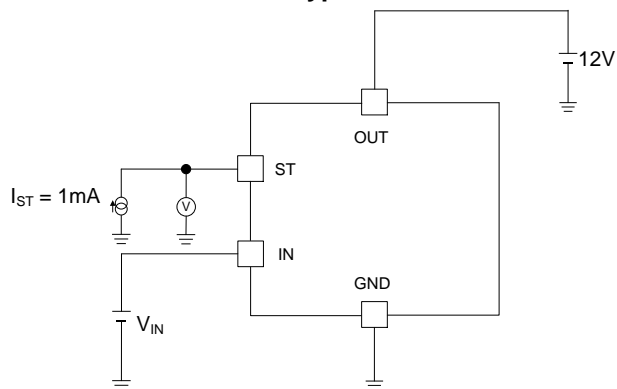


Measurement Circuit for Figure 22, 23

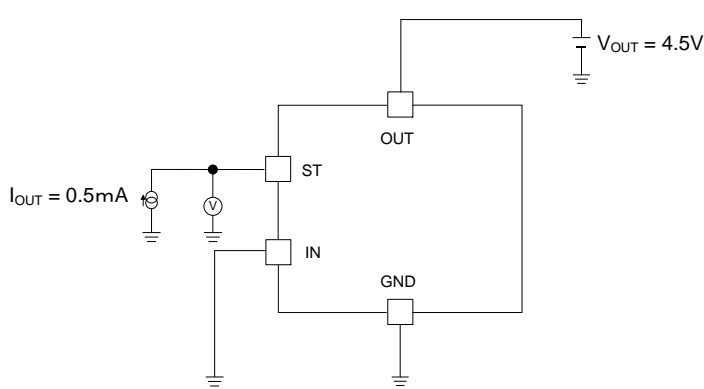


Measurement Circuit for Figure 24

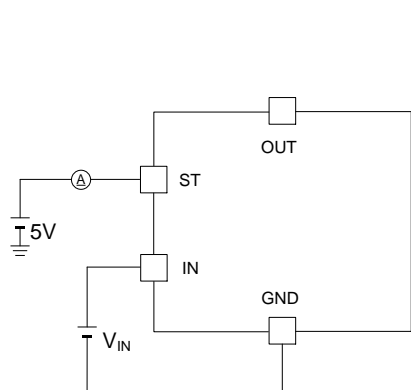
Measurement circuit for Typical Performance Curves – continued



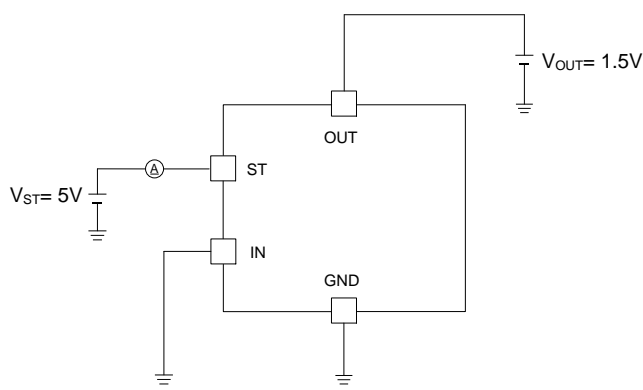
Measurement Circuit for Figure 25



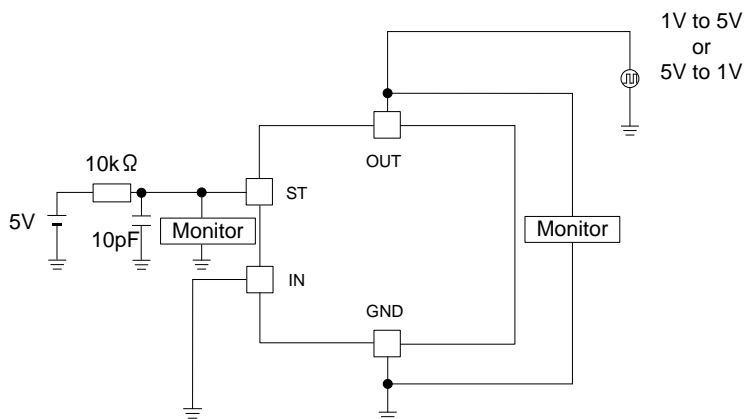
Measurement Circuit for Figure 26



Measurement Circuit for Figure 27



Measurement Circuit for Figure 28



Measurement Circuit for Figure 29, 30

I/O Pin Truth Table

Operating Status	Input Signal	Output Level	ST Level
Normal	L	H	L
	H	L	H
Overcurrent	L	H	L
	H	Clamp	L
Load open	L	L	H
	H	L	H
Over Temperature	L	H	L
	H	H	L

Timing Chart

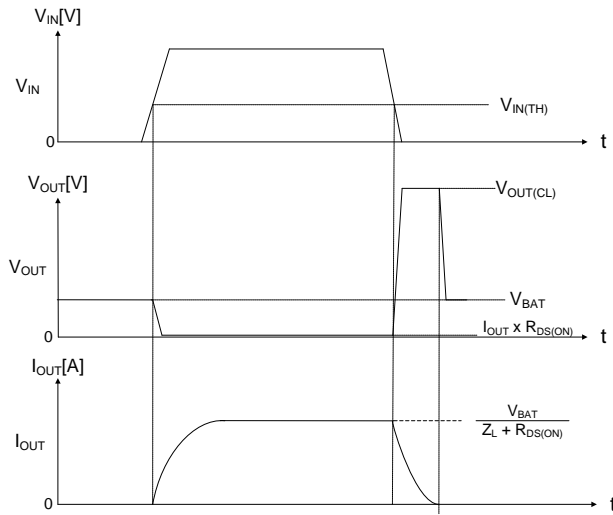


Figure 31. Inductive Load Operation

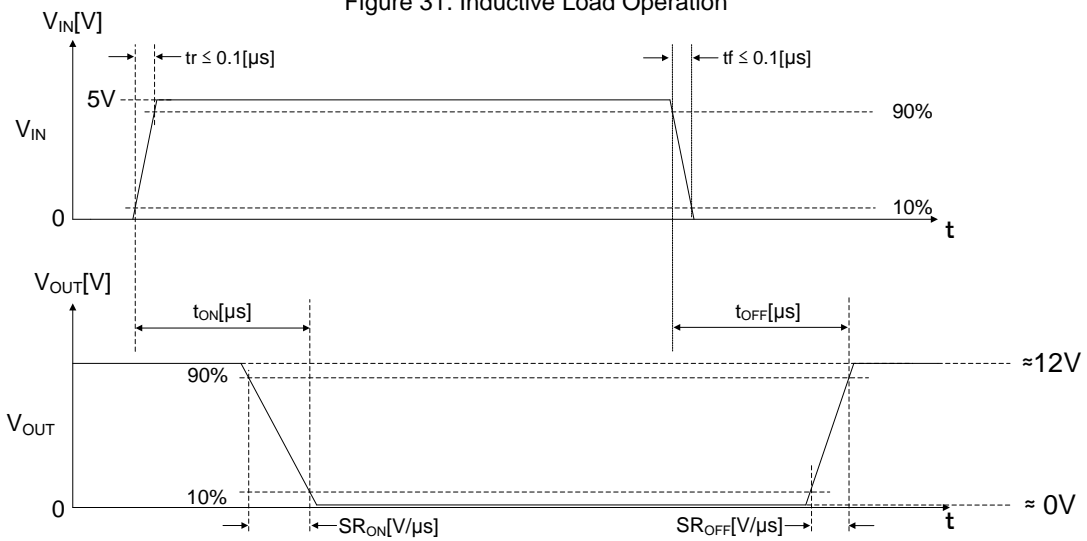


Figure 32. Switching Time

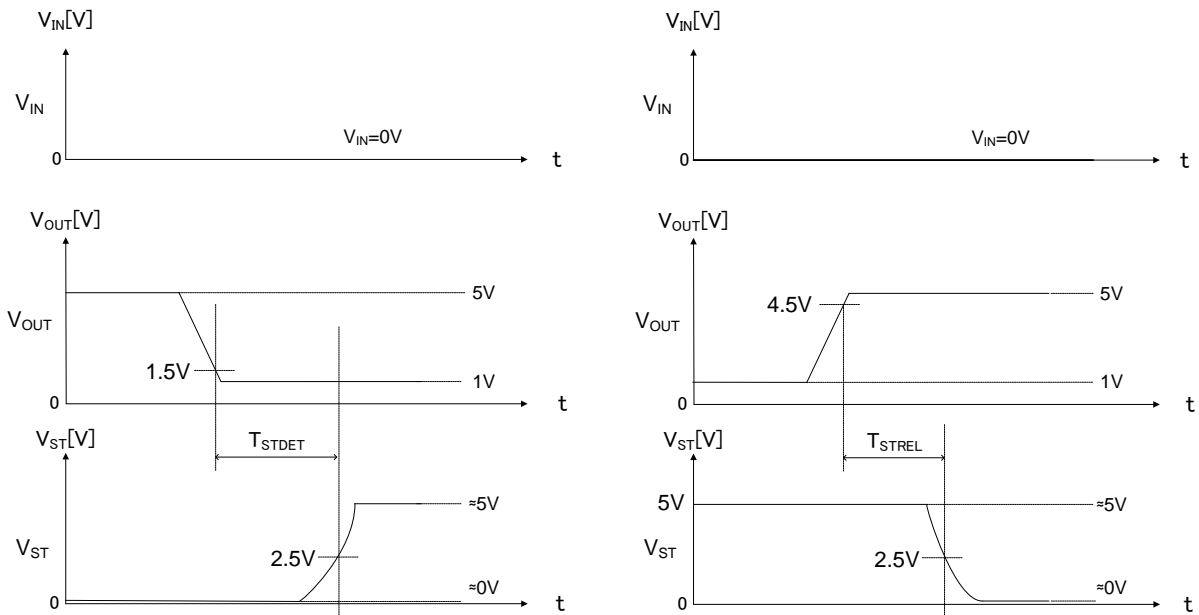
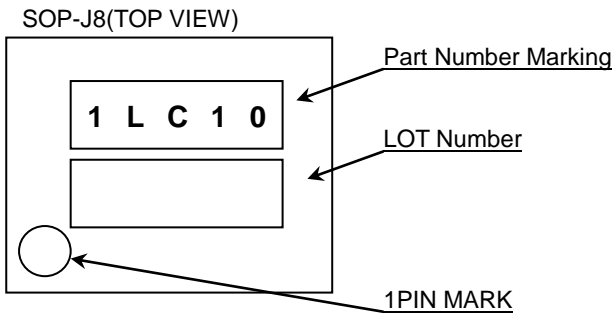


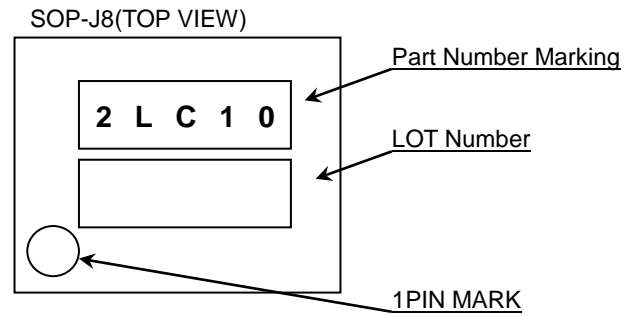
Figure 33. ST Output Delay Time

Marking Diagram

■ BV1LC105FJ-C

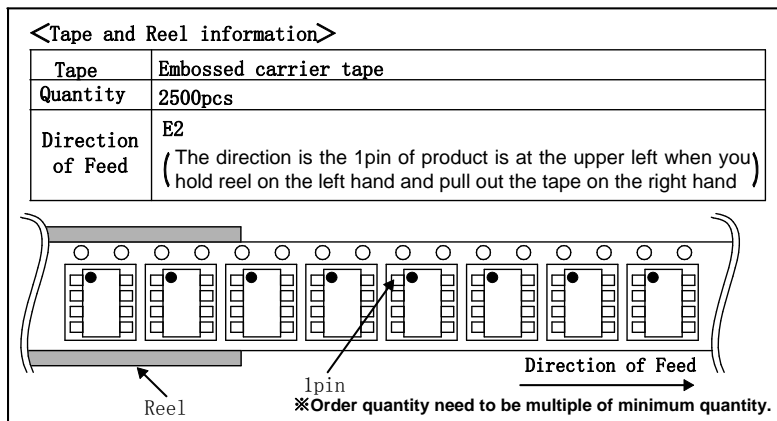
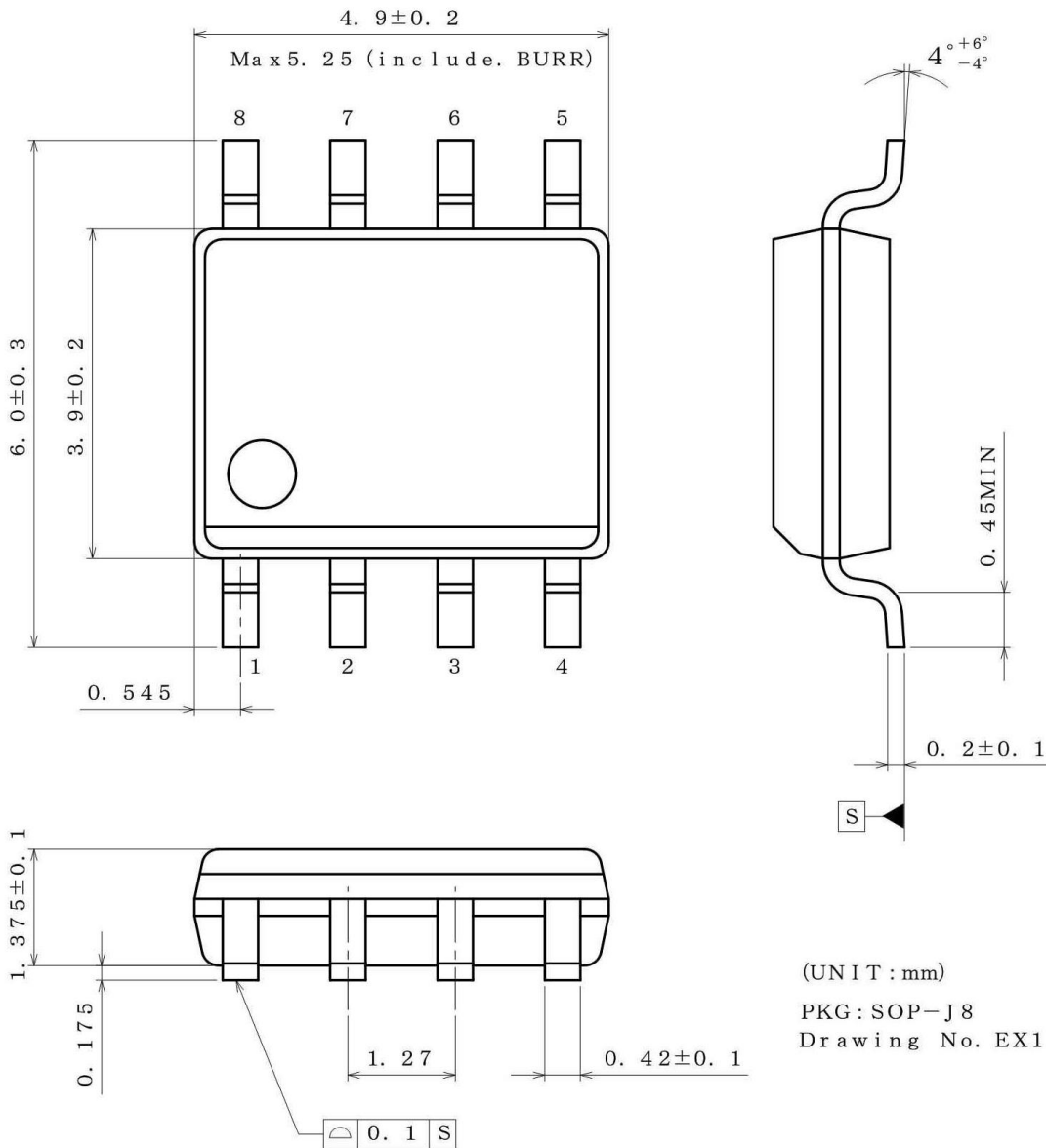


■ BM2LC105FJ-C



Physical Dimension, Tape and Reel Information

Package Name	SOP-J8
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Operational Notes

1. Grounding Interconnection Pattern

When a small-signal ground and a high-current ground are used, it is recommended to isolate the high-current grounding interconnection pattern and the small-signal grounding interconnection pattern and establish a single ground at the reference point of a set so that voltage changes due to the resistance and high current of patterned interconnects will not cause any changes in the small-signal ground voltage. Pay careful attention to prevent changes in the interconnection pattern of ground for external components.

The ground lines must be as short and thick as possible to reduce line impedance.

2. Thermal Consideration

The amount of heat generated depends on the On-state resistance and Output current.

Should by any condition the maximum junction temperature $T_{jmax} = 150\text{ }^{\circ}\text{C}$ rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design.

3. Absolute Maximum Ratings

Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

4. Inspections on Set Board

If a capacitor is connected to a low-impedance pin in order to conduct inspections of the IC on a set board, stress may apply to the IC. To avoid that, be sure to discharge the capacitor in each process. In addition, to connect or disconnect the IC to or from a jig in the testing process, be sure to turn OFF the power supply prior to connecting the IC, and disconnect it from the jig only after turning OFF the power supply. Furthermore, in order to protect the IC from static electricity, establish a ground for the IC assembly process and pay utmost attention to transport and store the IC.

5. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

6. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

7. Thermal Shutdown Circuit

IC has a built-in thermal shutdown circuit as an overheat-protection measure. The circuit is designed to turn OFF output when the temperature of the IC chip exceeds $175\text{ }^{\circ}\text{C}$ (Typ) and return the IC to the normal operation when the temperature falls below $160\text{ }^{\circ}\text{C}$ (Typ).

The thermal shutdown circuit is a circuit absolutely intended to protect the IC from thermal runaway, not intended to protect or guarantee the IC. Consequently, do not operate the IC based on the subsequent continuous use or operation of the circuit.

8. Overcurrent Limiting Circuit

IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

9. Overvoltage (Active Clamp) Protection Function

IC has a built-in overvoltage protection function in order for the IC to absorb counter-electromotive force energy generated when inductive load is turned OFF. Since the input voltage is clamped at 0V. When the active clamp circuit is activated, the thermal shutdown circuit is disabled.

10. Counter-electromotive Force

Fully ensure that the counter-electromotive force presents no problems in the operation of the IC.

Operational Notes – continued

11. Negative Current of Output

When supply a negative current from OUT(DRAIN) terminal in the state that supplied the voltage to IN terminal. The current pass from IN terminal to OUT(DRAIN) terminal through a parasitic transistor and voltage of IN terminal descend as shown in Figure 34 and Figure 35.

As shown in Figure 34 power MOS is turned on, set the OUT(DRAIN) terminal is more than -0.3V. Because a negative current may be passed to OUT(DRAIN) terminal from a power supply of the connection of the IN terminal (MCU, and so on).

As shown in Figure 35 power MOS is turned off, add a restriction resistance higher than 330 Ω to IN terminal. Because a negative current may be passed to DRAIN terminal from GND of the connection of the IN terminal.

The restriction resistance value, set up in consideration of the voltage descent caused by the IN terminal current.

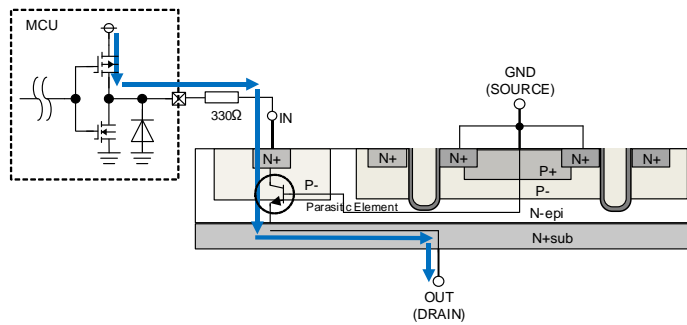


Figure 34. Negative current path (when power MOS is turned on)

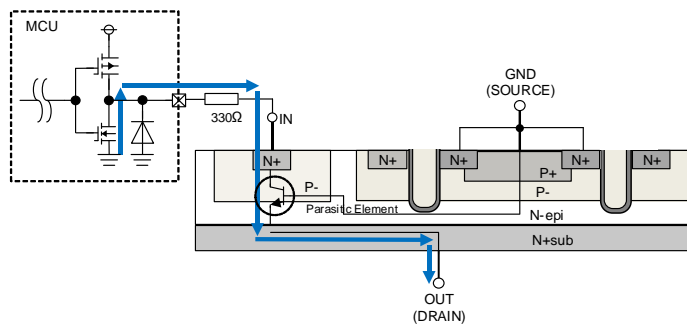


Figure 35. Negative current path (when power MOS is turned off)

Revision History

Date	Revision	Changes
23.Mar.2017	001	New Release
22.Sep.2017	002	P1 Line up was corrected. P1 General Description was corrected. P2 Block Diagrams was corrected. P9 Electrical Characteristics ST Output Delay Time Detect and ST Output Delay Time Release conditions were corrected. P17 Measurement Circuit for Figre 29, 30 was corrected.

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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