

Serial EEPROM Series Standard EEPROM I²C BUS EEPROM (2-Wire) BR24G08-3

General Description

BR24G08-3 is an 8Kbit serial EEPROM of I²C BUS interface.

Features

- Completely conforming to the world standard I²C BUS.
All controls available by 2 ports of serial clock (SCL) and serial data (SDA)
- Other devices than EEPROM can be connected to the same port, saving microcontroller port
- 1.6V to 5.5V Single Power Source Operation most suitable for battery use
- 1.6V to 5.5V wide limit of operating voltage, possible FAST MODE 400KHz operation
- Up to 16Byte in Page Write Mode
- Bit Format 1K x 8
- Self-timed Programming Cycle
- Low Current Consumption
- Prevention of Write Mistake
 - Write (Write Protect) Function Added
 - Prevention of Write Mistake at Low Voltage
- More than 1 million write cycles
- More than 40 years data retention
- Noise Filter Built in SCL / SDA Terminal
- Initial delivery state FFh

Packages W (Typ) x D(Typ) x H(Max)

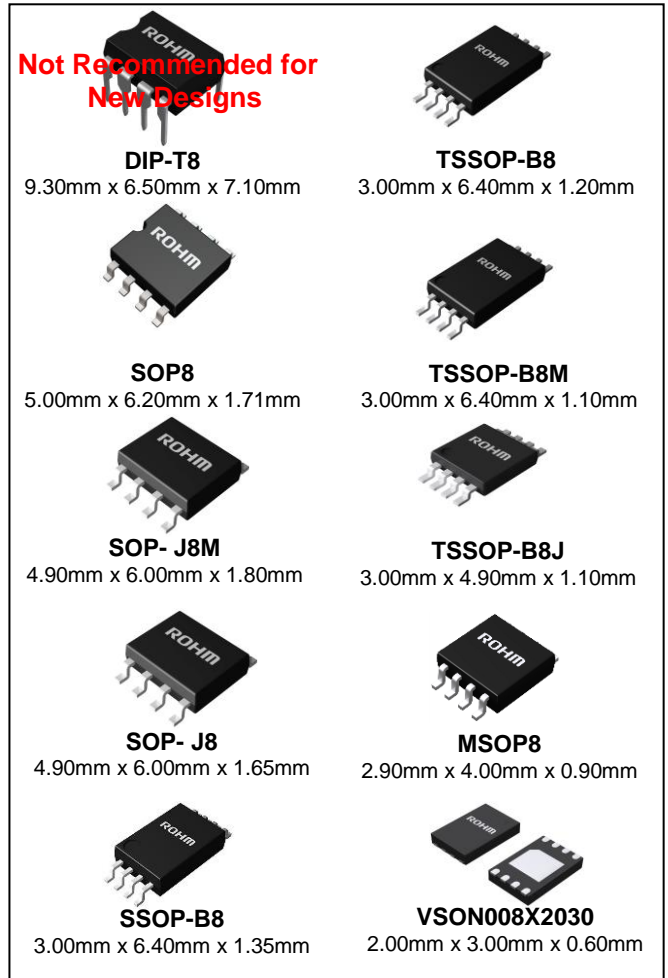


Figure 1.

Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Rating | Unit | Remark |
|--|---|------------------------------|------|---|
| Supply Voltage | V _{CC} | -0.3 to +6.5 | V | |
| Power Dissipation | Pd | 0.45 (SOP8) | W | Derate by 4.5mW/°C when operating above Ta=25°C |
| | | 0.45 (SOP-J8M) | | Derate by 4.5mW/°C when operating above Ta=25°C |
| | | 0.45 (SOP-J8) | | Derate by 4.5mW/°C when operating above Ta=25°C |
| | | 0.30 (SSOP-B8) | | Derate by 3.0mW/°C when operating above Ta=25°C |
| | | 0.33 (TSSOP-B8) | | Derate by 3.3mW/°C when operating above Ta=25°C |
| | | 0.33 (TSSOP-B8M) | | Derate by 3.3mW/°C when operating above Ta=25°C |
| | | 0.31 (TSSOP-B8J) | | Derate by 3.1mW/°C when operating above Ta=25°C |
| | | 0.31 (MSOP8) | | Derate by 3.1mW/°C when operating above Ta=25°C |
| | | 0.30 (VSON008X2030) | | Derate by 3.0mW/°C when operating above Ta=25°C |
| 0.80 (DIP-T8 ⁽¹⁾) | Derate by 8.0mW/°C when operating above Ta=25°C | | | |
| Storage Temperature | T _{stg} | -65 to +150 | °C | |
| Operating Temperature | T _{opr} | -40 to +85 | °C | |
| Input Voltage / Output Voltage | - | -0.3 to V _{CC} +1.0 | V | The Max value of Input voltage/ Output voltage is not over 6.5V. When the pulse width is 50ns or less the Min value of Input voltage/Output voltage is not below -0.8V. |
| Junction Temperature | T _{jmax} | 150 | °C | Junction temperature at the storage condition |
| Electrostatic discharge voltage (human body model) | V _{ESD} | -4000 to +4000 | V | |

(1) Not Recommended for New Designs.

Memory Cell Characteristics (Ta=25°C, V_{CC}=1.6V to 5.5V)

| Parameter | Limit | | | Unit |
|-------------------------------|-----------|-----|-----|-------|
| | Min | Typ | Max | |
| Write Cycles ⁽²⁾ | 1,000,000 | - | - | Times |
| Data Retention ⁽²⁾ | 40 | - | - | Years |

(2)Not 100% TESTED

Recommended Operating Ratings

| Parameter | Symbol | Rating | Unit |
|----------------------|-----------------|----------------------|------|
| Power Source Voltage | V _{CC} | 1.6 to 5.5 | V |
| Input Voltage | V _{IN} | 0 to V _{CC} | |

DC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, V_{CC}=1.6V to 5.5V)

| Parameter | Symbol | Limit | | | Unit | Conditions |
|------------------------|------------------|---------------------|-----|----------------------|------|---|
| | | Min | Typ | Max | | |
| Input High Voltage1 | V _{IH1} | 0.7V _{CC} | - | V _{CC} +1.0 | V | 1.7V≤V _{CC} ≤5.5V |
| Input Low Voltage1 | V _{IL1} | -0.3 ⁽³⁾ | - | +0.3V _{CC} | V | 1.7V≤V _{CC} ≤5.5V |
| Input High Voltage2 | V _{IH2} | 0.8V _{CC} | - | V _{CC} +1.0 | V | 1.6V≤V _{CC} <1.7V |
| Input Low Voltage2 | V _{IL2} | -0.3 ⁽³⁾ | - | 0.2V _{CC} | V | 1.6V≤V _{CC} <1.7V |
| Output Low Voltage1 | V _{OL1} | - | - | 0.4 | V | I _{OL} =3.0mA, 2.5V≤V _{CC} ≤5.5V (SDA) |
| Output Low Voltage2 | V _{OL2} | - | - | 0.2 | V | I _{OL} =0.7mA, 1.6V≤V _{CC} <2.5V (SDA) |
| Input Leakage Current | I _{LI} | -1 | - | 1 | μA | V _{IN} =0 to V _{CC} |
| Output Leakage Current | I _{LO} | -1 | - | 1 | μA | V _{OUT} =0 to V _{CC} (SDA) |
| Supply Current (Write) | I _{CC1} | - | - | 2.0 | mA | V _{CC} =5.5V, f _{SCL} =400kHz, t _{WR} =5ms, Byte write, Page write |
| Supply Current (Read) | I _{CC2} | - | - | 0.5 | mA | V _{CC} =5.5V, f _{SCL} =400kHz Random read, current read, sequential read |
| Standby Current | I _{SB} | - | - | 2.0 | μA | V _{CC} =5.5V, SDA· SCL=V _{CC} A0,A1,A2=GND,WP=GND |

(3) When the pulse width is 50ns or less, it is -0.8V.

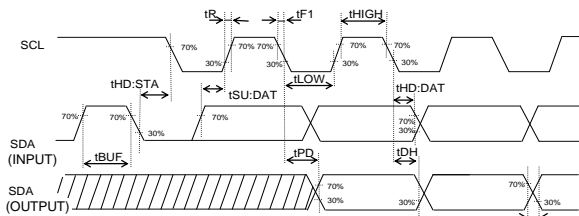
AC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, Vcc=1.6V to 5.5V)

| Parameter | Symbol | Limit | | | Unit |
|---|----------------------|-------|-----|-----|------|
| | | Min | Typ | Max | |
| Clock Frequency | f _{SCL} | - | - | 400 | kHz |
| Data Clock High Period | t _{HIGH} | 0.6 | - | - | μs |
| Data Clock Low Period | t _{LOW} | 1.2 | - | - | μs |
| SDA, SCL (INPUT) Rise Time ⁽¹⁾ | t _R | - | - | 1.0 | μs |
| SDA, SCL (INPUT) Fall Time ⁽¹⁾ | t _{F1} | - | - | 1.0 | μs |
| SDA (OUTPUT) Fall Time ⁽¹⁾ | t _{F2} | - | - | 0.3 | μs |
| Start Condition Hold Time | t _{HD:STA} | 0.6 | - | - | μs |
| Start Condition Setup Time | t _{SU:STA} | 0.6 | - | - | μs |
| Input Data Hold Time | t _{HD:DAT} | 0 | - | - | ns |
| Input Data Setup Time | t _{SU:DAT} | 100 | - | - | ns |
| Output Data Delay Time | t _{PD} | 0.1 | - | 0.9 | μs |
| Output Data Hold Time | t _{DH} | 0.1 | - | - | μs |
| Stop Condition Setup Time | t _{SU:STO} | 0.6 | - | - | μs |
| Bus Free Time | t _{BUF} | 1.2 | - | - | μs |
| Write Cycle Time | t _{WR} | - | - | 5 | ms |
| Noise Spike Width (SDA and SCL) | t _i | - | - | 0.1 | μs |
| WP Hold Time | t _{HD:WP} | 1.0 | - | - | μs |
| WP Setup Time | t _{SU:WP} | 0.1 | - | - | μs |
| WP High Period | t _{HIGH:WP} | 1.0 | - | - | μs |

(1) Not 100% TESTED.

Condition Input data level: V_{IL}=0.2×V_{cc} V_{IH}=0.8×V_{cc}Input data timing reference level: 0.3×V_{cc}/0.7×V_{cc}Output data timing reference level: 0.3×V_{cc}/0.7×V_{cc}

Rise/Fall time : ≤20ns

Serial Input / Output Timing

- Input read at the rise edge of SCL
- Data output in sync with the fall of SCL

Figure 2-(a). Serial Input / Output Timing

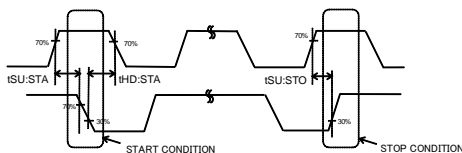


Figure 2-(b). Start-Stop Bit Timing

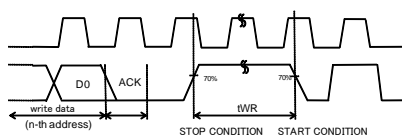


Figure 2-(c). Write Cycle Timing

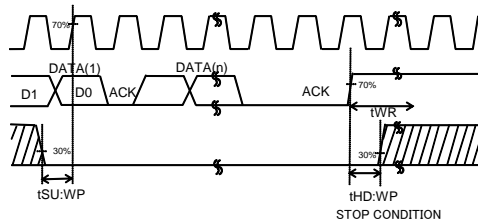


Figure 2-(d). WP Timing at Write Execution

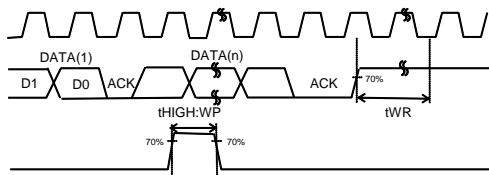


Figure 2-(e). WP Timing at Write Cancel

Block Diagram

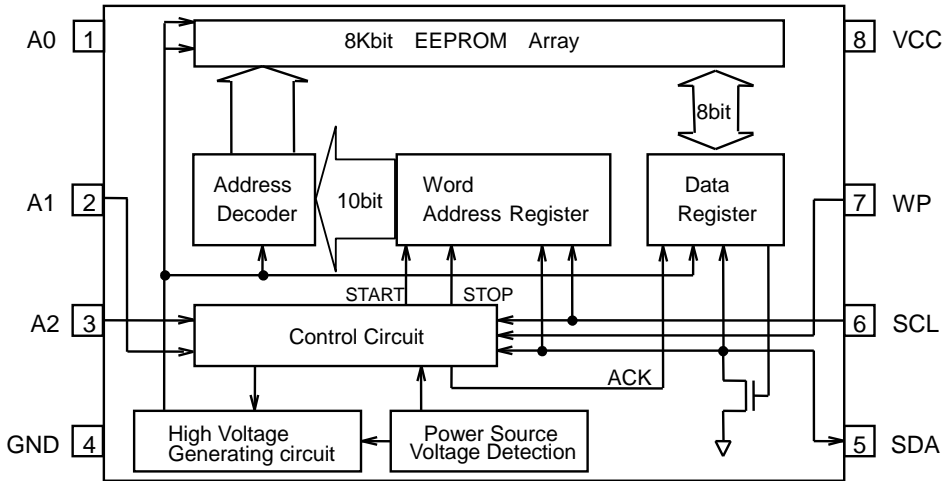
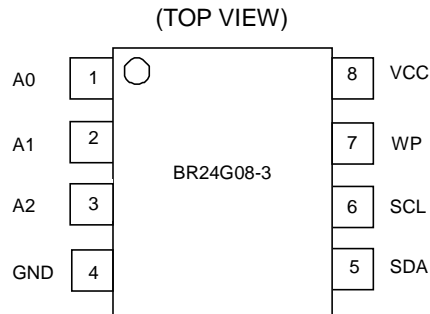


Figure 3. Block Diagram

Pin Configuration



Pin Descriptions

| Terminal Name | Input/Output | Descriptions |
|---------------|--------------|---|
| A0 | - | Don't use ⁽¹⁾ |
| A1 | - | Don't use ⁽¹⁾ |
| A2 | Input | Slave address setting ⁽²⁾ |
| GND | - | Reference voltage of all input / output, 0V |
| SDA | Input/Output | Serial data input serial data output |
| SCL | Input | Serial clock input |
| WP | Input | Write protect terminal |
| VCC | - | Connect the power source. |

(1) Pins not used as device address may be set to any of High, Low, and High-Z states
 (2) A2 is not allowed to use as open.

Typical Performance Curves

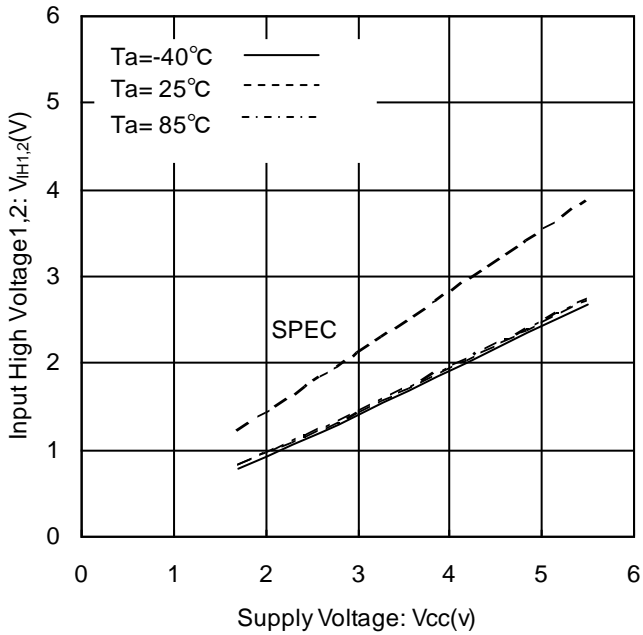


Figure 4. Input High Voltage1,2 vs. Supply Voltage (A2, SCL, SDA, WP)

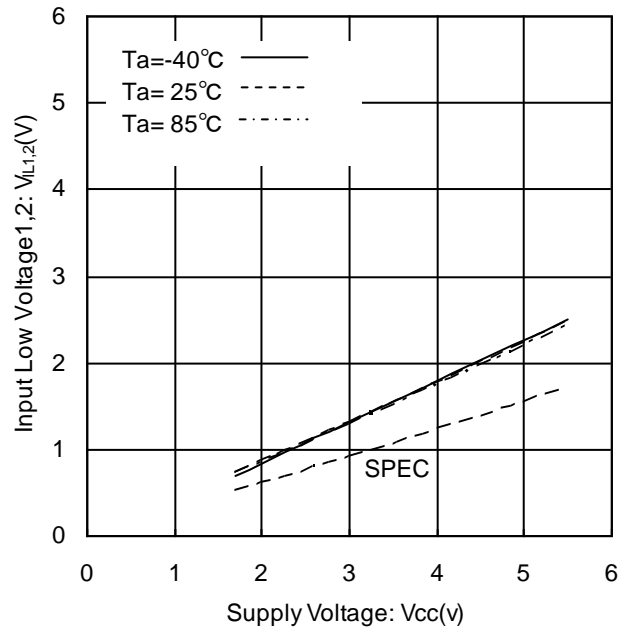


Figure 5. Input Low Voltage1,2 vs. Supply Voltage (A2, SCL, SDA, WP)

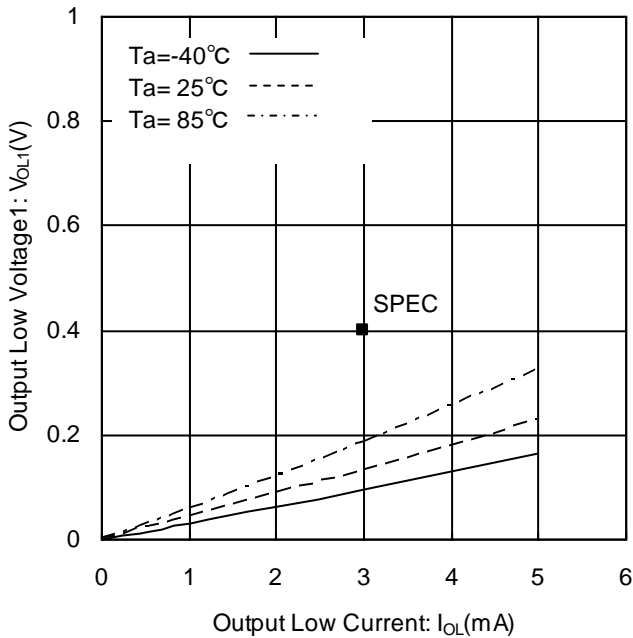


Figure 6. Output Low Voltage1 vs. Output Low Current (V_{CC}=2.5V)

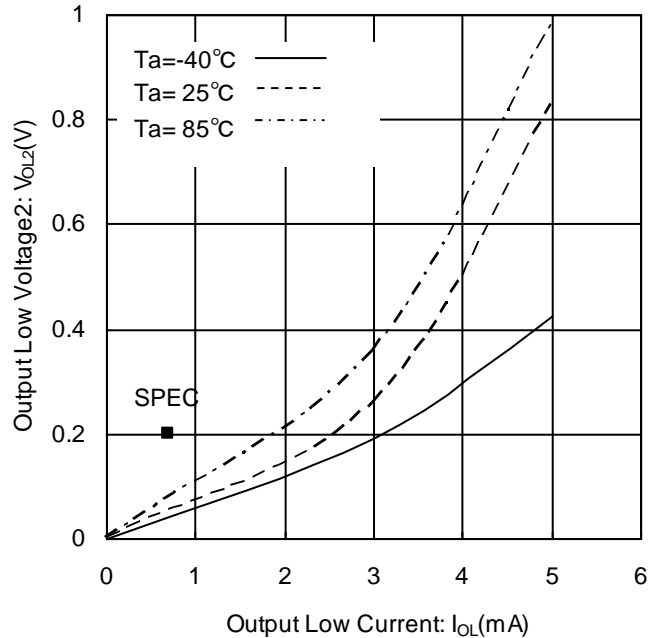


Figure 7. Output Low Voltage2 vs. Output Low Current (V_{CC}=1.6V)

Typical Performance Curves - Continued

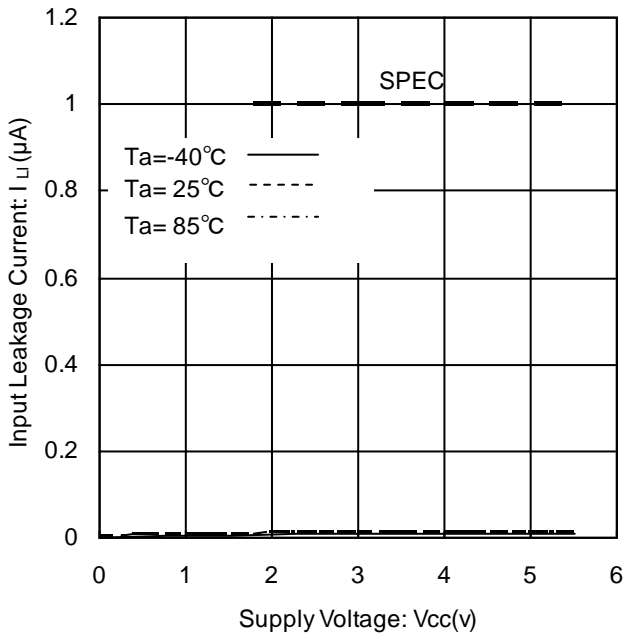


Figure 8. Input Leakage Current vs. Supply Voltage (A2, SCL, WP)

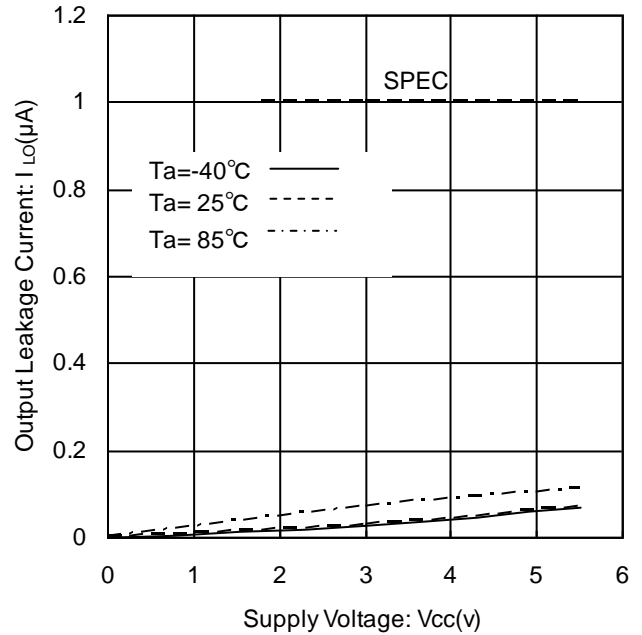


Figure 9. Output Leakage Current vs. Supply Voltage (SDA)

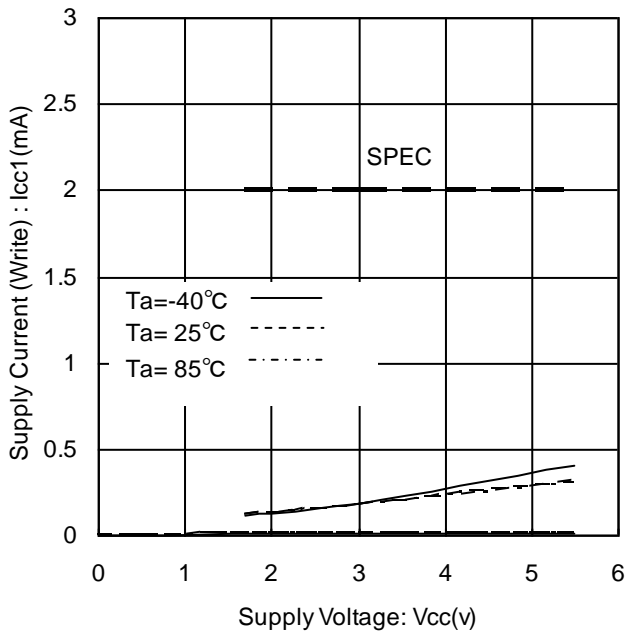


Figure 10. Supply Current (Write) vs. Supply Voltage (f_{scl}=400kHz)

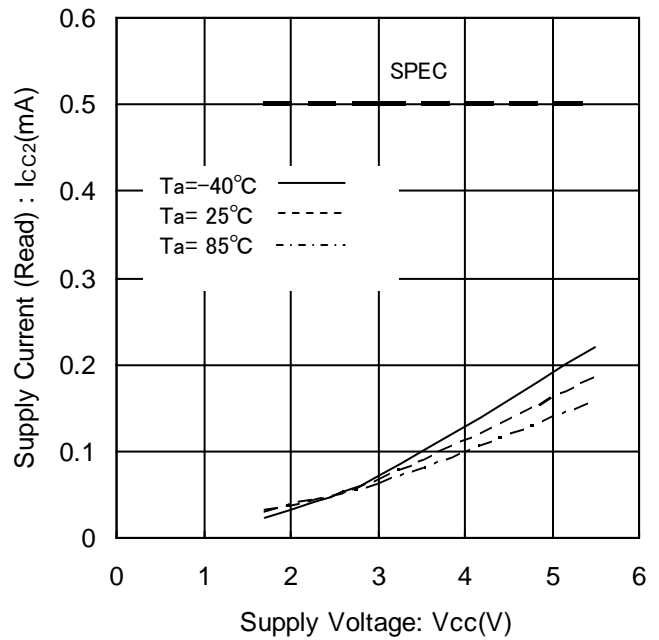


Figure 11. Supply Current (Read) vs. Supply Voltage (f_{scl}=400kHz)

Typical Performance Curves - Continued

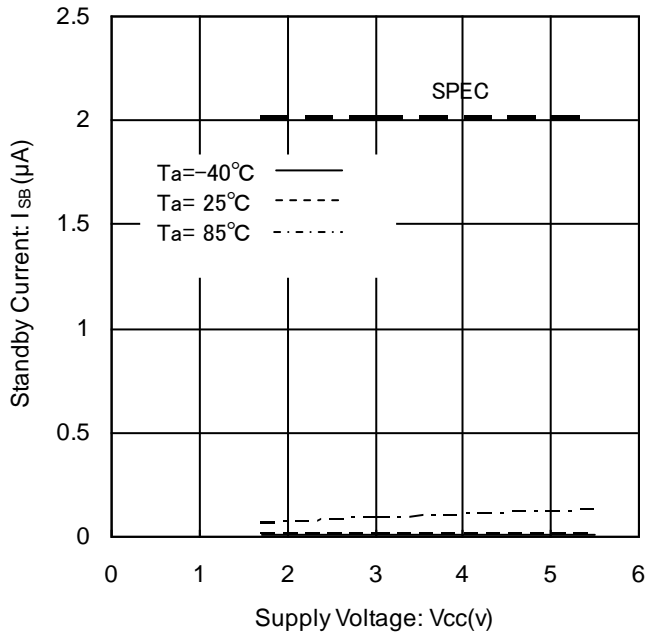


Figure 12. Standby Current vs. Supply Voltage

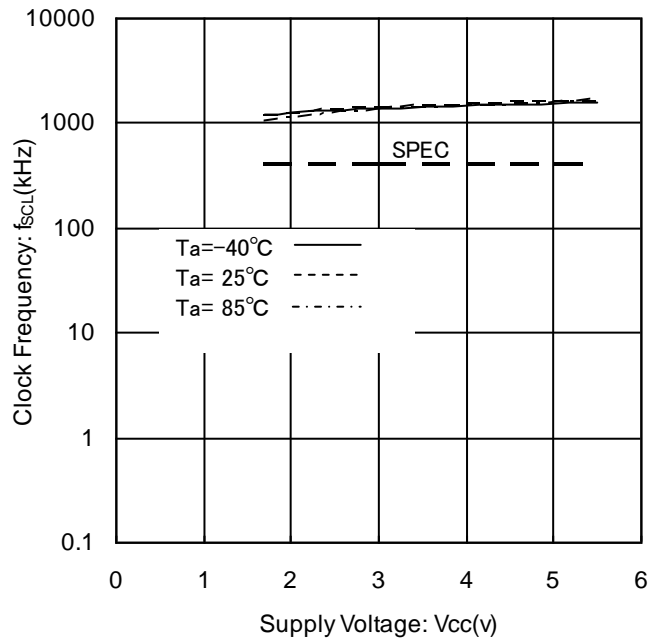


Figure 13. Clock Frequency vs. Supply Voltage

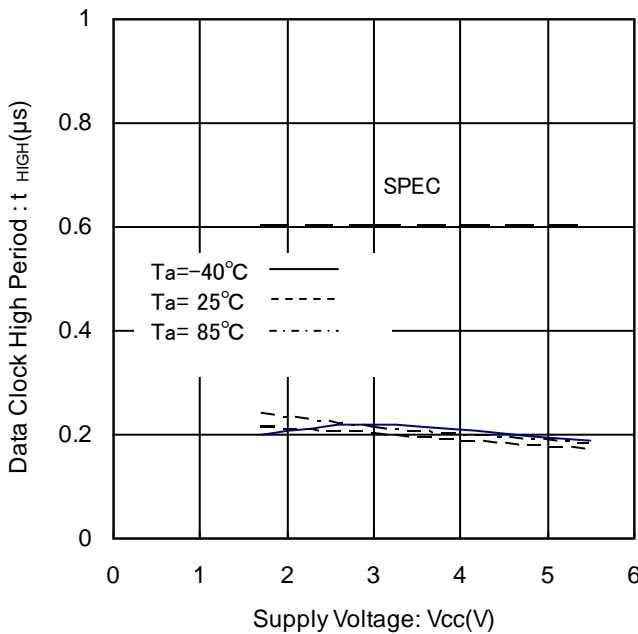


Figure 14. Data Clock High Period vs Supply Voltage

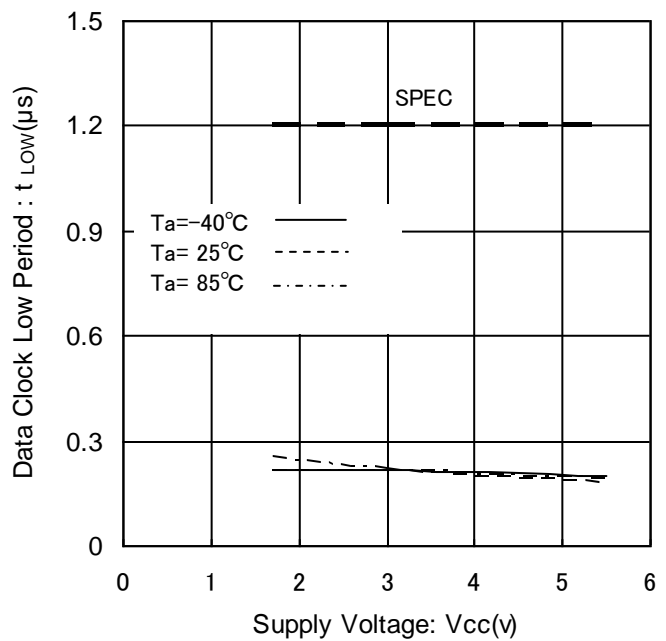


Figure 15. Data Clock Low Period vs. Supply Voltage

Typical Performance Curves - Continued

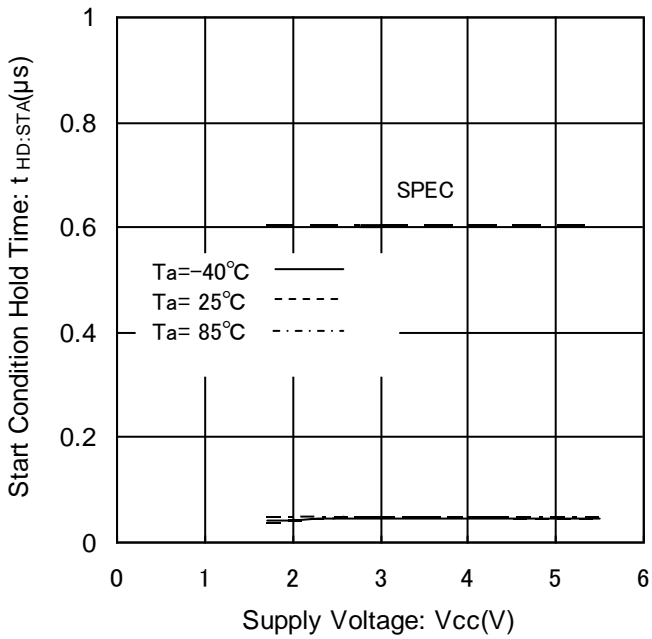


Figure 16. Start Condition Hold Time vs. Supply Voltage

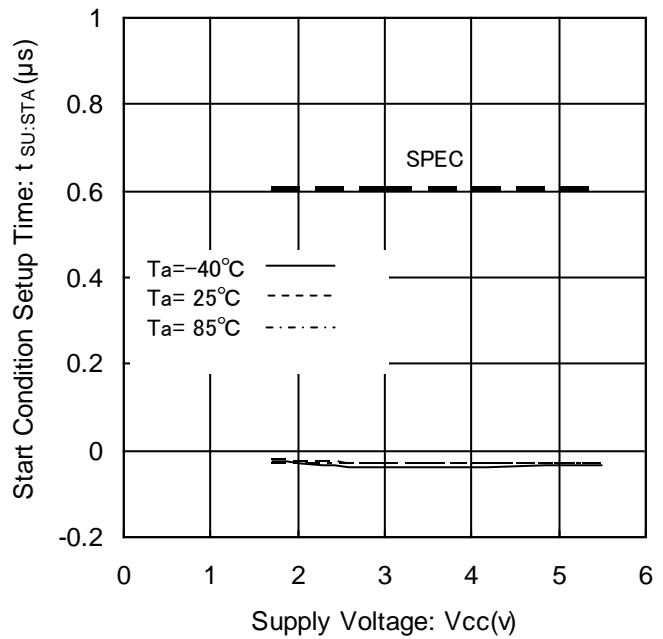


Figure 17. Start Condition Setup Time vs. Supply Voltage

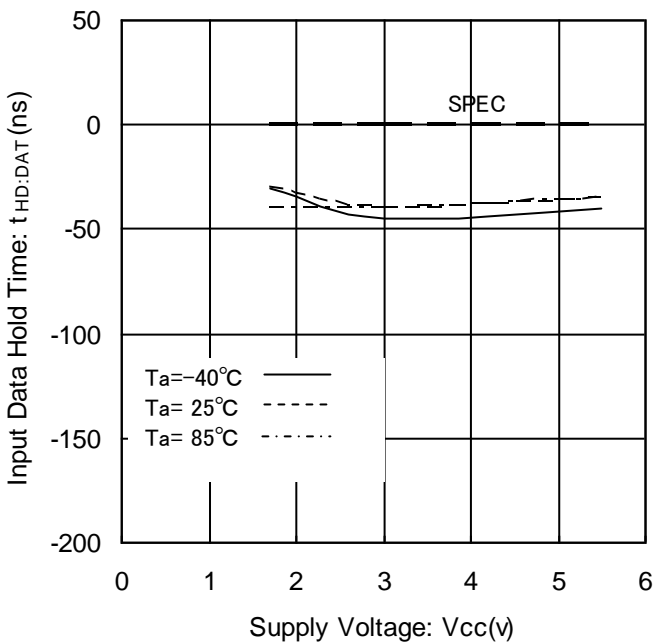


Figure 18. Input Data Hold Time vs. Supply Voltage (HIGH)

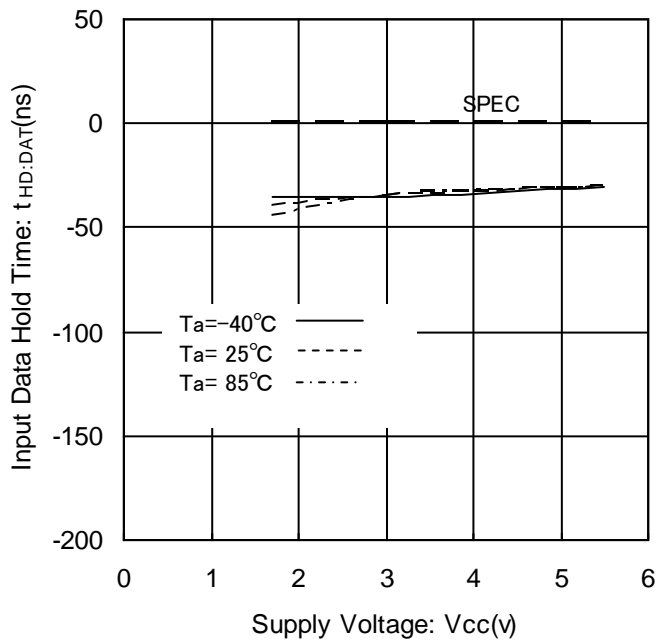


Figure 19. Input Data Hold Time vs. Supply Voltage (LOW)

Typical Performance Curves - Continued

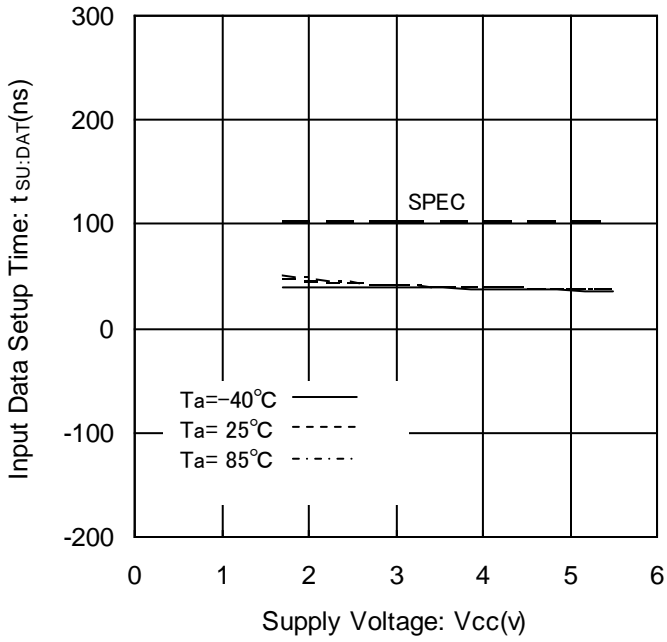


Figure 20. Input Data Setup Time vs. Supply Voltage (HIGH)

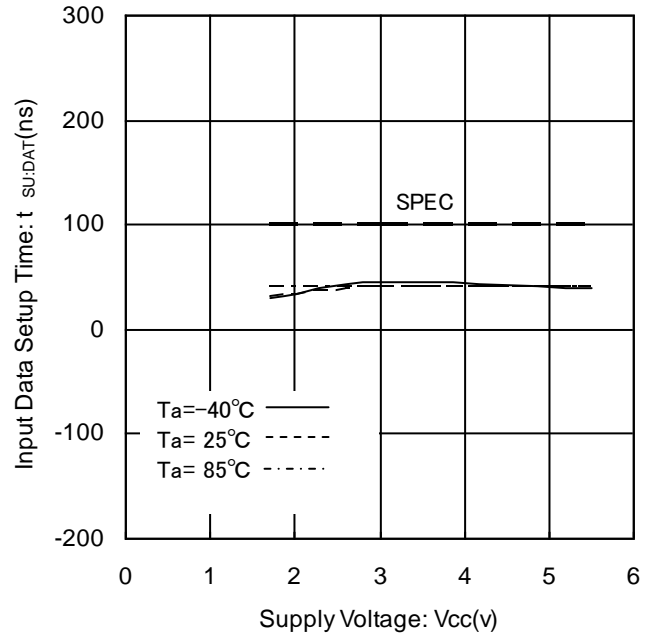


Figure 21. Input Data Setup Time vs. Supply Voltage (LOW)

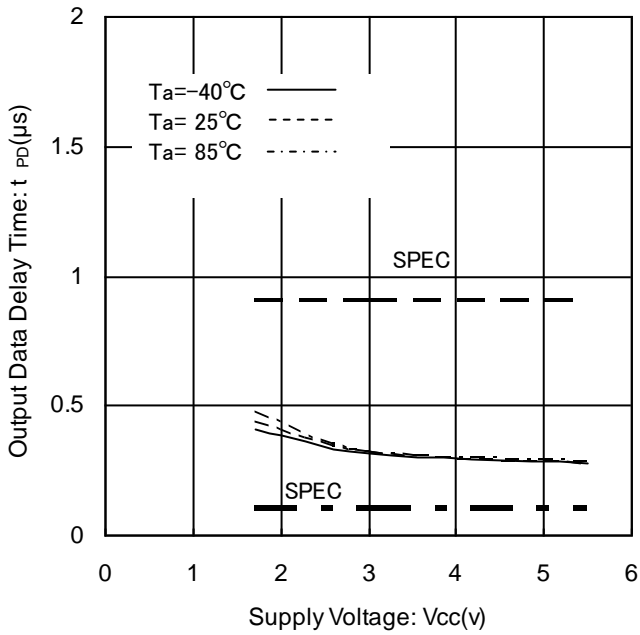


Figure 22. Output Data Delay Time vs. Supply Voltage (LOW)

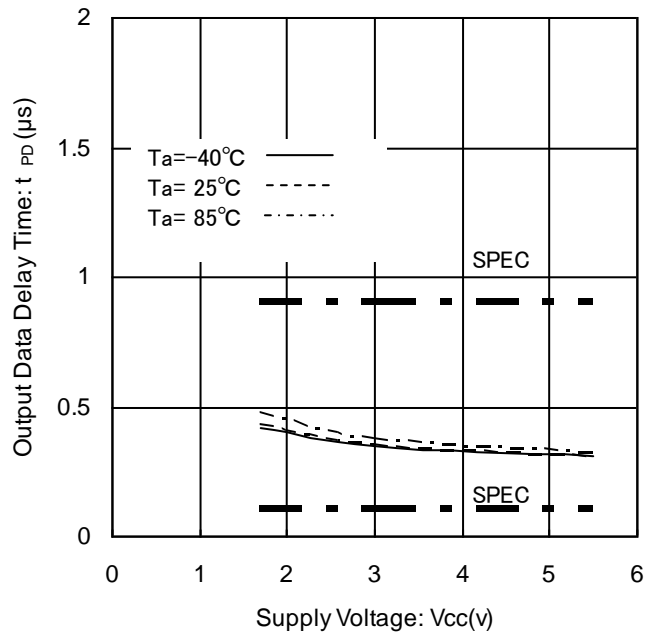


Figure 23. Output Data Delay Time vs. Supply Voltage (HIGH)

Typical Performance Curves - Continued

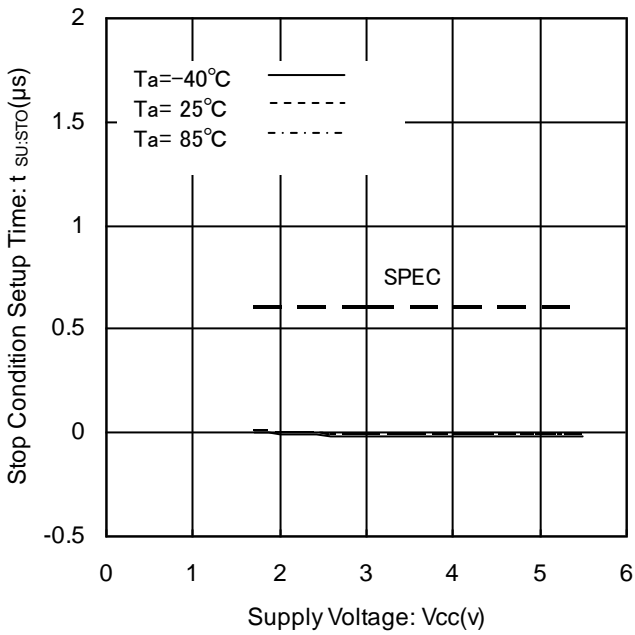


Figure 24. Stop Condition Setup Time vs. Supply Voltage

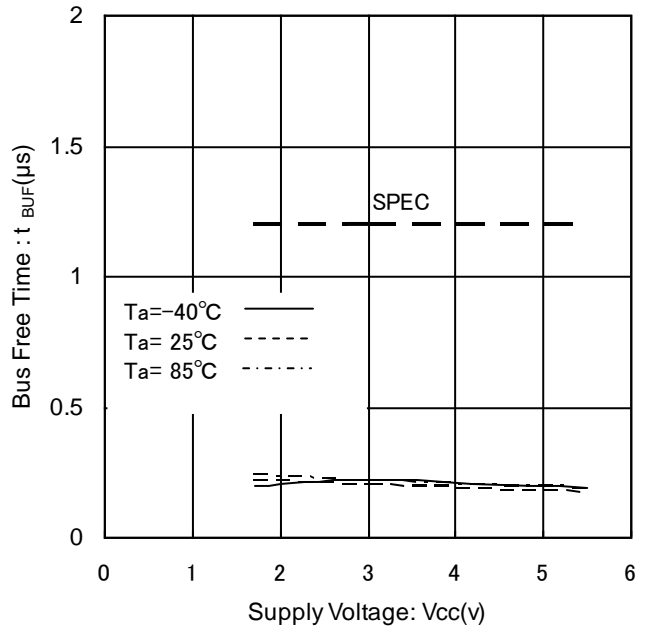


Figure 25. Bus Free Time vs. Supply Voltage

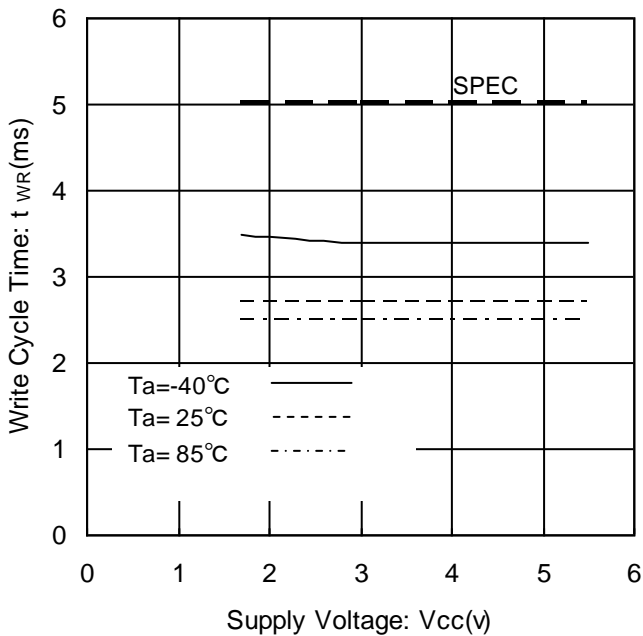


Figure 26. Write Cycle Time vs. Supply Voltage

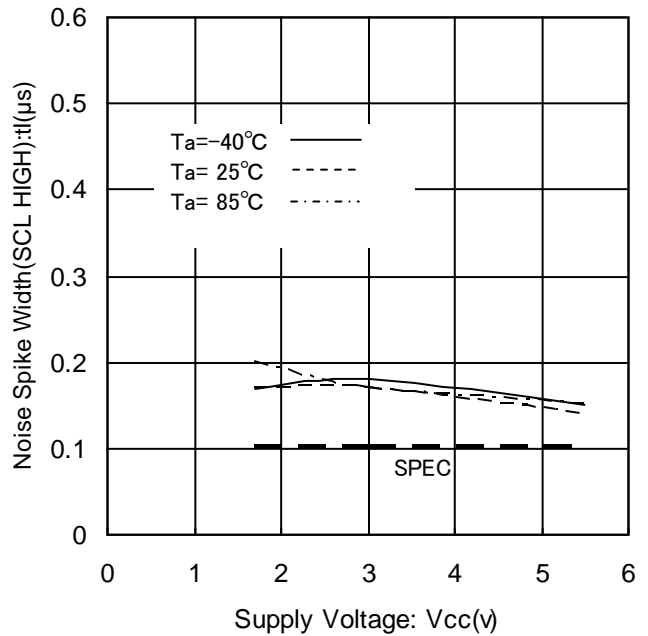


Figure 27. Noise Spike Width vs. Supply Voltage (SCL HIGH)

Typical Performance Curves - Continued

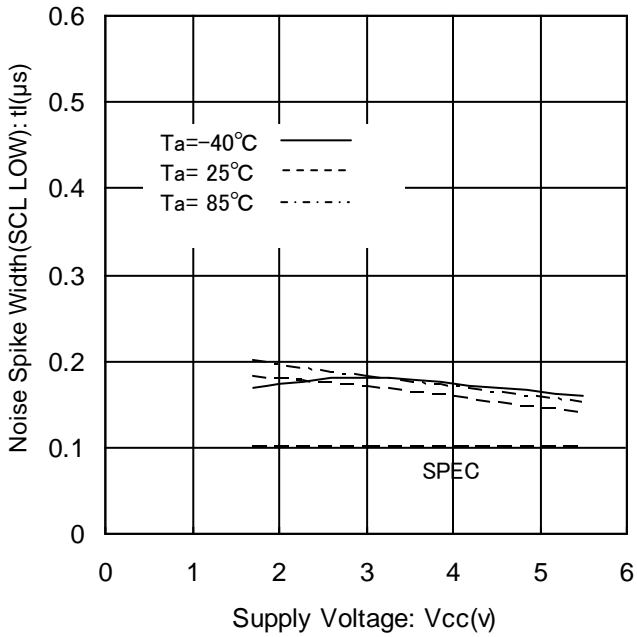


Figure 28. Noise Spike Width vs. Supply Voltage (SCL LOW)

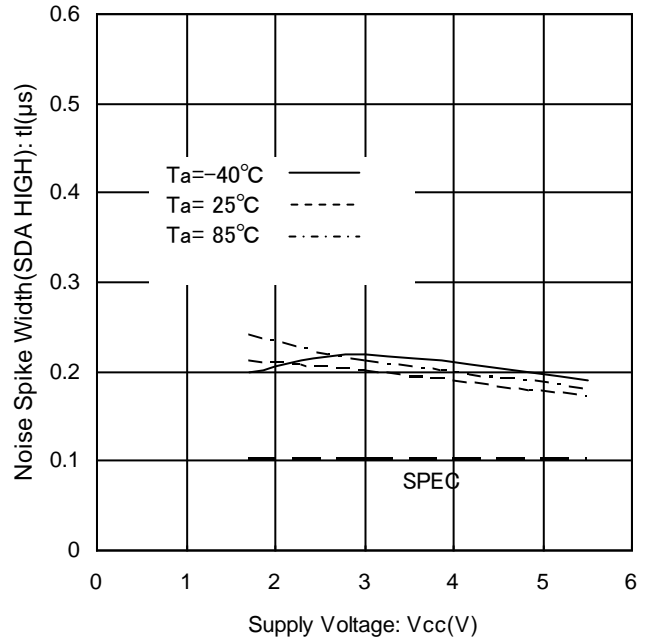


Figure 29. Noise Spike Width vs. Supply Voltage (SDA HIGH)

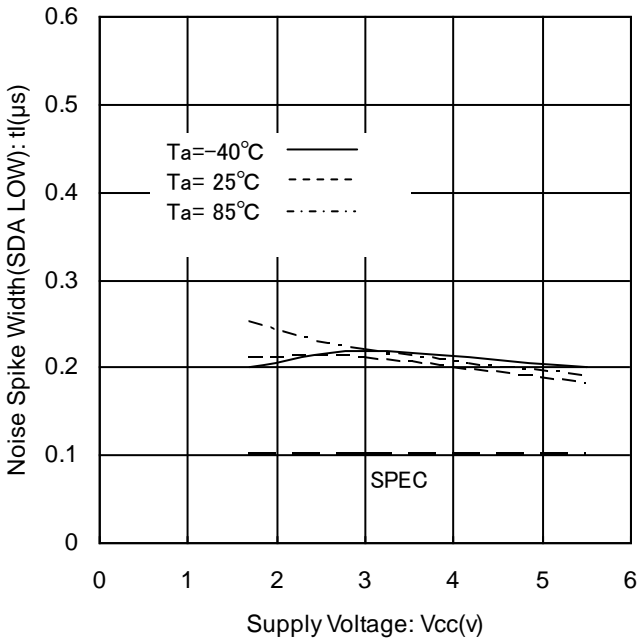


Figure 30. Noise Spike Width vs. Supply Voltage (SDA LOW)

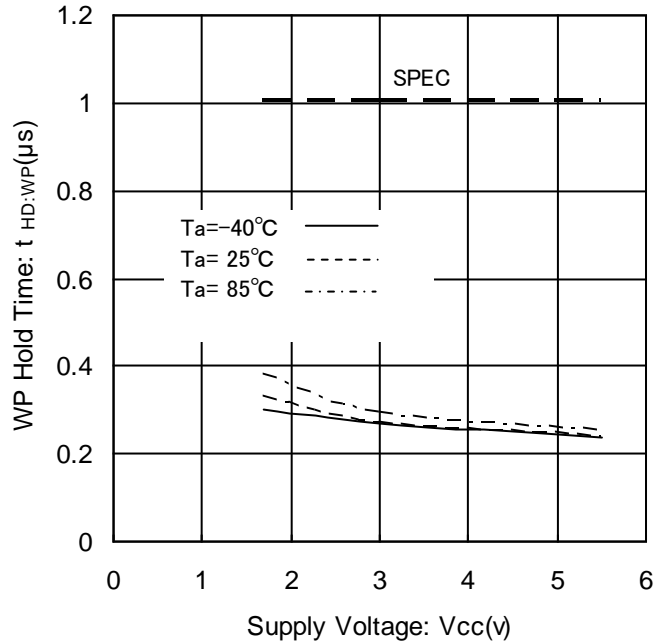


Figure 31. WP Hold Time vs. Supply Voltage

Typical Performance Curves - Continued

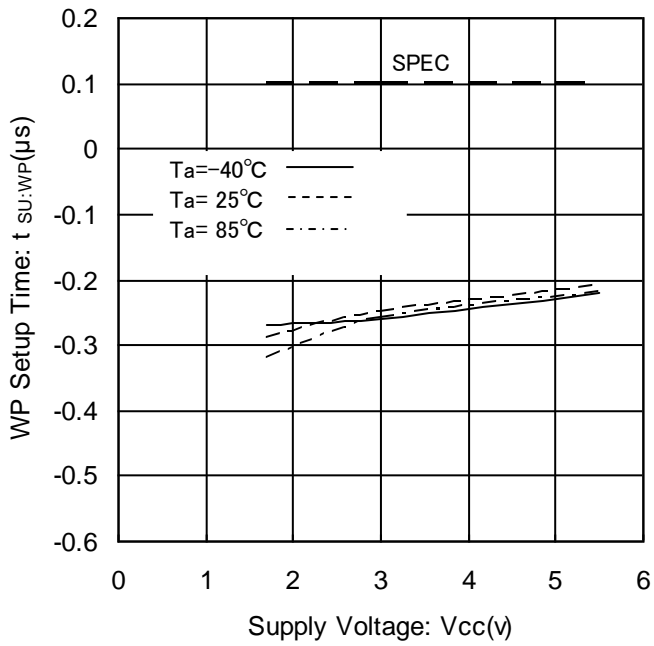


Figure 32. WP Setup Time vs. Supply Voltage

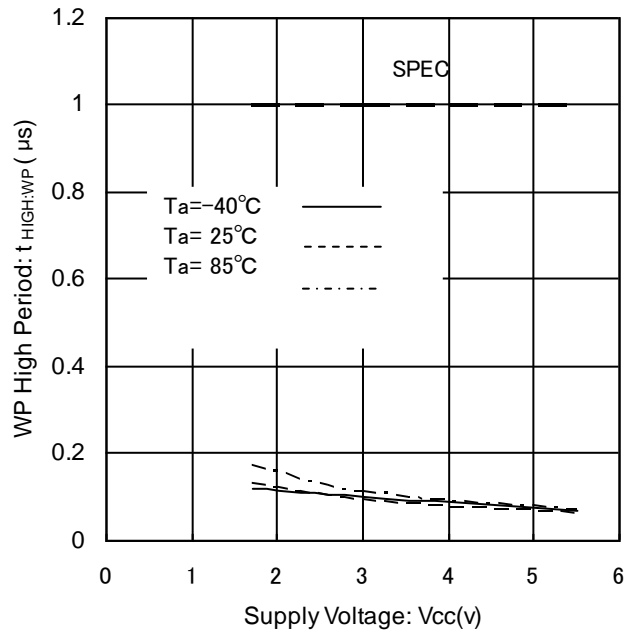


Figure 33. WP High Period vs. Supply Voltage

Timing Chart

1. I²C BUS Data Communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS carries out data transmission with several devices is possible by connecting with 2 communication lines: serial data (SDA) and serial clock (SCL).

Among the devices, there should be a "master" that generates clock and control communication start and end. The rest become "slave" which are controlled by an address peculiar to each device like this EEPROM. The device that outputs data to the bus during data communication is called "transmitter", and the device that receives data is called "receiver".

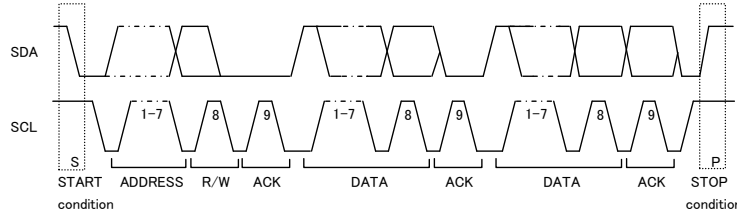


Figure 34. Data Transfer Timing

2. Start Condition (Start Bit Recognition)

- (1) Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
- (2) This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command cannot be executed.

3. Stop Condition (Stop Bit Recognition)

- (1) Each command can be ended by a stop condition (stop bit) where SDA goes from Low to High while SCL is High.

4. Acknowledge (ACK) Signal

- (1) The acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master-slave communication, the device (Ex. μ -COM sends slave address input for write or read command to this IC) at the transmitter (sending) side releases the bus after output of 8bit data.
- (2) The device (Ex. This IC receives the slave address input of write or read command from the μ -COM) at the receiver (receiving) side sets SDA 'LOW' during the 9th clock cycle, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- (3) This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
- (4) After receiving 8bit data (word address and write data) during each write operation, this IC outputs acknowledge signal (ACK signal) 'LOW'.
- (5) During read operation, this IC outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'. When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (μ -COM) side, this IC continues to output data. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, recognizes stop condition (stop bit), and ends read operation. Then this IC becomes ready for another transmission.

5. Device Addressing

- (1) Slave address comes after start condition from master.
- (2) The significant 4 bits of slave address are used for recognizing a device type. The device code of this IC is fixed to '1010'.
- (3) Next slave addresses (A2 --- device address) are for selecting devices, and multiple devices can be used on a same bus according to the number of device addresses.
- (4) The most insignificant bit (R/\bar{W} --- READ / WRITE) of slave address is used for designating write or read operation, and is as shown below.

Setting R/\bar{W} to 0 ----- write (setting 0 to word address setting of random read)

Setting R/\bar{W} to 1 ----- read

| Slave address | Maximum number of Connected buses |
|------------------------------|-----------------------------------|
| 1 0 1 0 A2 P1 P0 R/\bar{W} | 2 |

P0 and P1 are page select bits.

Write Command

1. Write Cycle

(1) Arbitrary data can be written to this EEPROM. When writing only 1 byte. Byte Write is normally used, and when writing continuous data of 2 bytes or more, simultaneous write is possible by Page Write cycle. The maximum number of bytes is specified per device of each capacity. Up to 16 arbitrary bytes can be written.

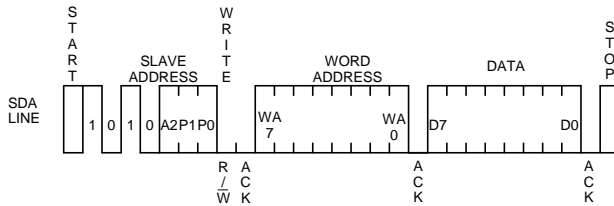


Figure 35. Byte Write Cycle

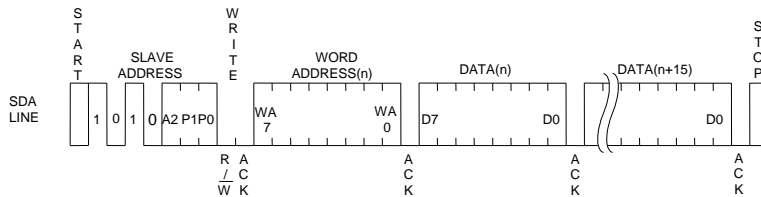


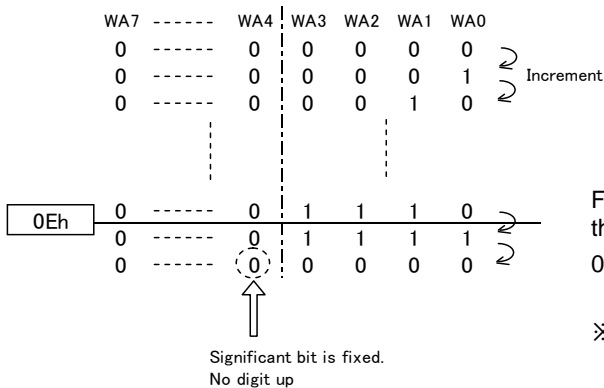
Figure 36. Page Write Cycle

- (2) During internal write execution, all input commands are ignored, therefore ACK is not returned.
- (3) Data is written to the address designated by word address (n-th address)
- (4) By issuing stop bit after 8bit data input, internal write to memory cell starts.
- (5) When internal write is started, command is not accepted for t_{WR} (5ms at maximum).
- (6) Using page write cycle, writing in bulk is done as follows: When data or more than 16Byte is sent, the bytes in excess overwrites the data already sent first. (Refer to "Internal address increment")
- (7) As for page write cycle of BR24G08-3 where 2 or more bytes of data are intended to be written, after page select bit 'P0,P1' of slave address are designated arbitrarily, only the 4 least significant bits in the address are incremented internally, so that data up to 16 bytes of memory only can be written.

In the case BR24G08-3, 1 page=16bytes, but the page write cycle time is 5ms at maximum for 16byte bulk write. It does not stand 5ms at maximum \times 16byte=80ms(Max)

2. Internal Address Increment

Page write mode (in the case of BR24G08-3)



For example, when it is started from address 0Eh, then, increment is made as below,
0Eh→0Fh→00h→01h··· please take note.

※0Eh···0E in hexadecimal, therefore,
00001110 becomes a binary number.

3. Write Protect (WP) Terminal

Write Protect (WP) Function

When WP terminal is set at V_{CC} (H level), data rewrite of all addresses is prohibited. When it is set at GND (L level), data rewrite of all addresses is enabled. Be sure to connect this terminal to V_{CC} or GND, or control it to H level or L level. Do not leave it open.

In case using of it as ROM, it is recommended to connect it to pull up or V_{CC} .

At extremely low voltage at power ON / OFF, by setting the WP terminal 'H', write error can be prevented.

Read Command

1. Read Cycle

Read cycle is when data of EEPROM is read. Read cycle could be random read cycle or current read cycle. Random read cycle is a command to read data by designating a specific address, and is used generally. Current read cycle is a command to read data of internal address register without designating an address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available where the next address data can be read in succession.

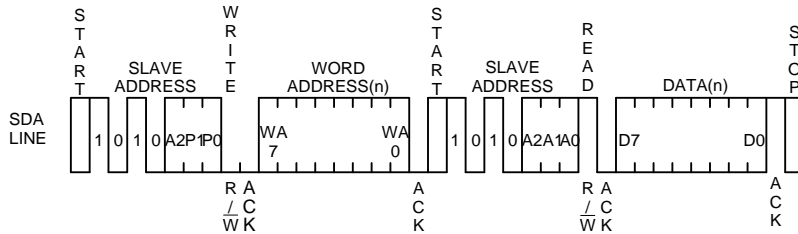


Figure 37. Random Read Cycle

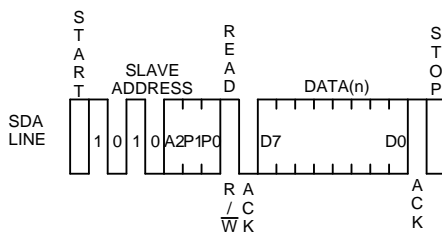


Figure 38. Current Read Cycle

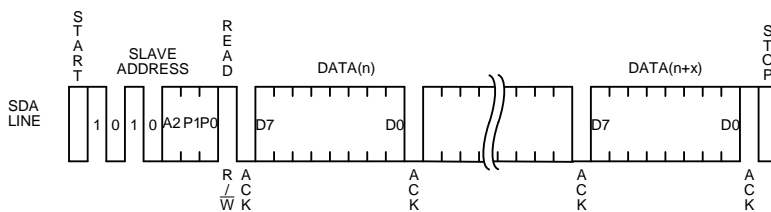


Figure 39. Sequential Read Cycle (in the case of current read cycle)

- (1) In random read cycle, data of designated word address can be read.
- (2) When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th address, i.e., data of the (n+1)-th address is output.
- (3) When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (μ -COM) side, the next address data can be read in succession.
- (4) Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal goes from 'L' to 'H' while SCL signal is 'H'.
- (5) When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output. Therefore, read command cycle cannot be ended. To end read command cycle, be sure to input 'H' to ACK signal after D0, and the stop condition where SDA goes from 'L' to 'H' while SCL signal is 'H'.
- (6) Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is asserted from 'L' to 'H' while SCL signal is 'H'.

Software Reset

Software reset is executed to avoid malfunction after power on, and during command input. Software reset has several kinds and 3 kinds of them are shown in the figure below. (Refer to Figure 40-(a), Figure 40-(b), Figure 40-(c).) Within dummy clock input area, the SDA bus is released ('H' by pull up) and ACK output and read data '0' (both 'L' level) may be output from EEPROM. Therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

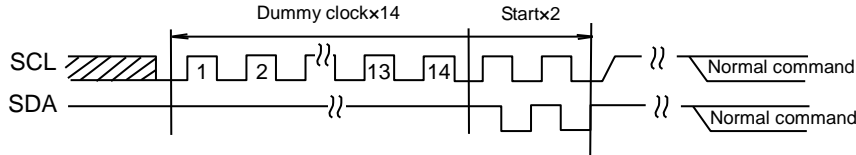


Figure 40-(a). The Case of Dummy Clockx14 + START+START+ Command Input

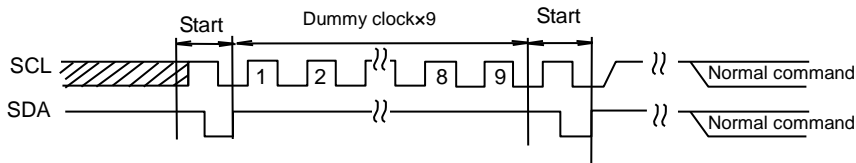


Figure 40-(b). The Case of START + Dummy clockx9 + START + Command Input

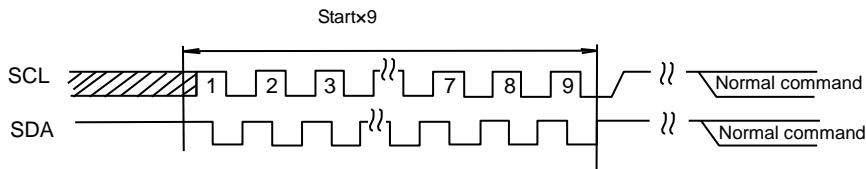


Figure 40-(c). STARTx9 + Command Input

※Start command from START input.

Acknowledge Polling

During internal write execution, all input commands are ignored, therefore ACK is not returned. During internal automatic write execution after write cycle input, next command (slave address) is sent. If the first ACK signal sends back 'L', then it means end of write operation, else 'H' is returned, which means writing is still in progress. By the use of acknowledge polling, next command can be executed without waiting for $t_{WR} = 5ms$.

To write continuously, $R/\overline{W} = 0$, then to carry out current read cycle after write, slave address $R/\overline{W} = 1$ is sent. If ACK signal sends back 'L', and then execute word address input and data output and so forth.

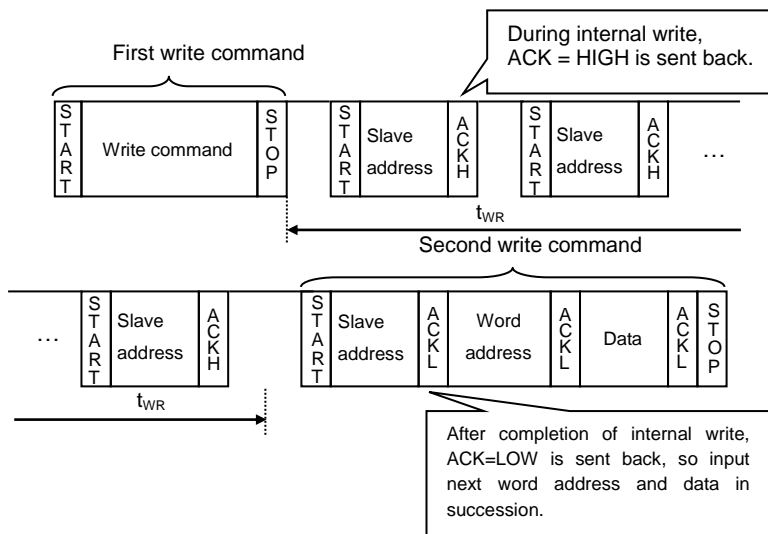


Figure 41. Case of Continuously Write by Acknowledge Polling

WP Valid Timing (Write Cancel)

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so on, pay attention to the following WP valid timing. During write cycle execution, inside cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to take in D0 of data (in page write cycle, the first byte data) is the cancel invalid area.

WP input in this area becomes Don't care. The area from the rise of SCL to take in D0 to the stop condition input is the cancel valid area. Furthermore, after the execution of forced end by WP, the IC enters standby status.

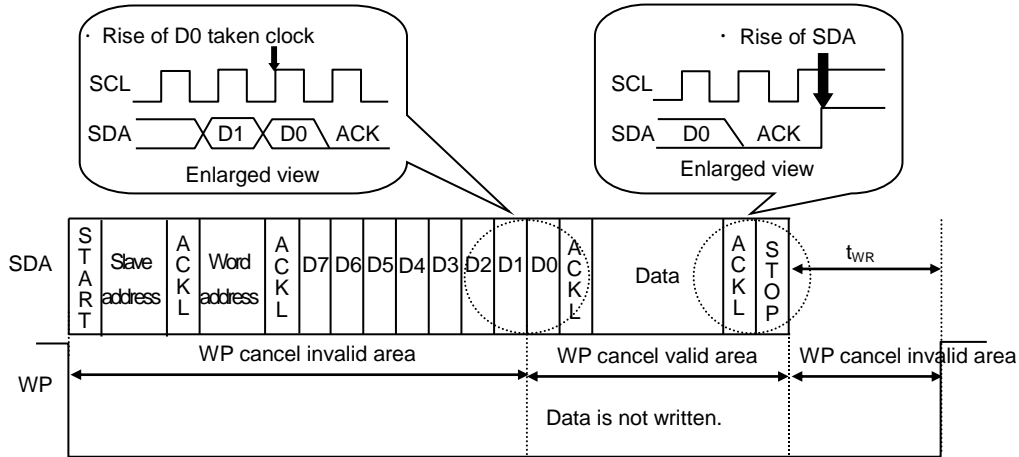


Figure 42. WP Valid Timing

Command Cancel by Start Condition and Stop Condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Figure 43.) However, within ACK output area and during data read, SDA bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. When command is cancelled by start-stop condition during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined. Therefore, it is not possible to carry out current read cycle in succession. To carry out read cycle in succession, carry out random read cycle.

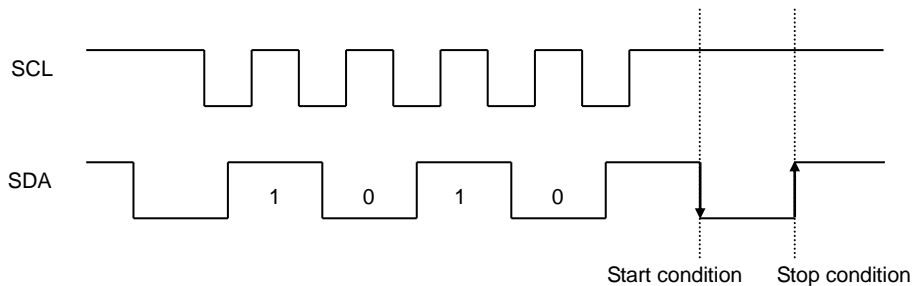


Figure 43. Case of Cancel by Start, Stop Condition during Slave Address Input

I/O Peripheral Circuit

1. Pull Up Resistance of SDA Terminal

SDA is NMOS open drain, so it requires a pull up resistor. As for this resistance value (R_{PU}), select an appropriate value from microcontroller V_{IL} , I_L , and $V_{OL}-I_{OL}$ characteristics of this IC. If R_{PU} is large, operating frequency is limited. The smaller the R_{PU} , the larger is the supply current (Read).

2. Maximum Value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

(1) SDA rise time to be determined by the capacitance (C_{BUS}) of bus line of R_{PU} and SDA should be t_r or lower.

Furthermore, AC timing should be satisfied even when SDA rise time is slow.

(2) The bus' electric potential (A) to be determined by the input leak total (I_L) of the device connected to the bus with output of 'H' to SDA line and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin of $0.2V_{CC}$.

$$V_{CC}-I_L R_{PU}-0.2 V_{CC} \geq V_{IH}$$

$$\therefore R_{PU} \leq \frac{0.8V_{CC}-V_{IH}}{I_L}$$

Ex.) $V_{CC}=3V$ $I_L=10\mu A$ $V_{IH}=0.7 V_{CC}$
From (2)

$$R_{PU} \leq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leq 30 \text{ [k}\Omega\text{]}$$

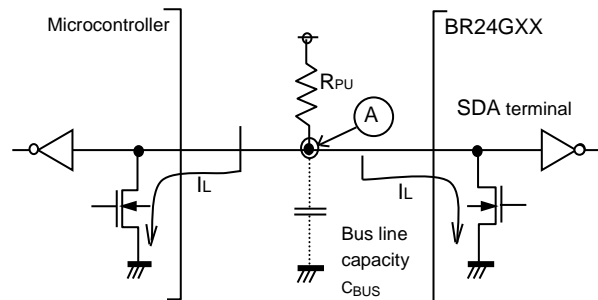


Figure 44. I/O Circuit Diagram

3. Minimum Value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

(1) When IC outputs LOW, it should be satisfied that $V_{OLMAX}=0.4V$ and $I_{OLMAX}=3mA$.

$$\frac{V_{CC}-V_{OL}}{R_{PU}} \leq I_{OL}$$

$$\therefore R_{PU} \geq \frac{V_{CC}-V_{OL}}{I_{OL}}$$

(2) $V_{OLMAX}=0.4V$ should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including recommended noise margin $0.1V_{CC}$.

$$V_{OLMAX} \leq V_{IL}-0.1 V_{CC}$$

Ex.) $V_{CC}=3V$, $V_{OL}=0.4V$, $I_{OL}=3mA$, microcontroller, EEPROM $V_{IL}=0.3V_{CC}$
from(1)

$$R_{PU} \geq \frac{3-0.4}{3 \times 10^{-3}}$$

$$\geq 867[\Omega]$$

And $V_{OL}=0.4 \text{ [V]}$
 $V_{IL}=0.3 \times 3$
 $=0.9 \text{ [V]}$

Therefore, the condition (2) is satisfied.

4. Pull Up Resistance of SCL Terminal

When SCL control is made at the CMOS output port, there is no need for a pull up resistor. But when there is a time where SCL becomes 'Hi-Z', add a pull up resistor. As for the pull up resistor value, one of several k Ω to several ten k Ω is recommended in consideration of drive performance of output port of microcontroller.

Cautions on Microcontroller Connection

1. Rs

In I²C BUS, it is recommended that SDA port is of open drain input/output. However, when using CMOS input / output of tri state to SDA port, insert a series resistance R_S between the pull up resistance R_{PU} and the SDA terminal of EEPROM. This is to control over current that may occur when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. R_S also plays the role of protecting the SDA terminal against surge. Therefore, even when SDA port is open drain input/output, R_S can be used.

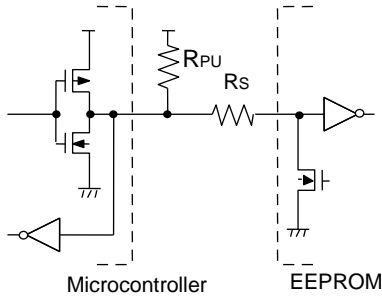


Figure 45. I/O circuit diagram

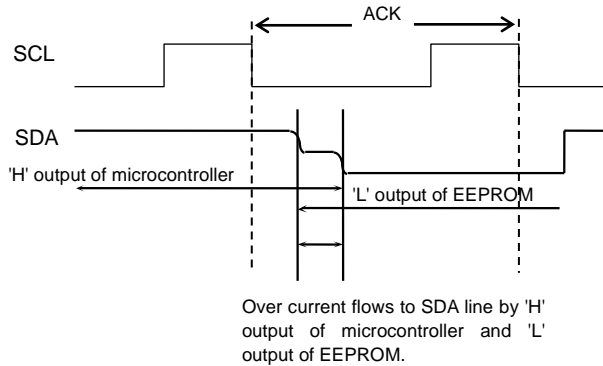


Figure 46. Input / output collision timing

2. Maximum Value of R_S

The maximum value of R_S is determined by the following relations.

- (1) SDA rise time to be determined by the capacitance (C_{BUS}) of bus line of R_{PU} and SDA should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is low.
- (2) The bus electric potential (A) to be determined by R_{PU} and R_S the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin 0.1V_{CC}.

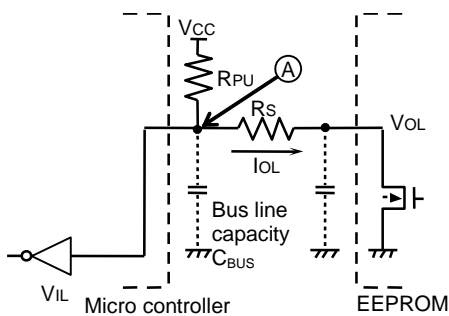


Figure 47. I/O Circuit Diagram

$$\frac{(V_{CC}-V_{OL}) \times R_S}{R_{PU}+R_S} + V_{OL} + 0.1V_{CC} \leq V_{IL}$$

$$\therefore R_S \leq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

EX) V_{CC}=3V V_{IL}=0.3V_{CC} V_{OL}=0.4V R_{PU}=20kΩ

$$R_S \leq \frac{0.3 \times 3 - 0.4 - 0.1 \times 3}{1.1 \times 3 - 0.3 \times 3} \times 20 \times 10^3$$

$$\leq 1.67 [k\Omega]$$

3. Minimum Value of R_S

The minimum value of R_S is determined by over current at bus collision. When over current flows, noises in power source line and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of the impedance of power source line in set and so forth. Set the over current to EEPROM at 10mA or lower.

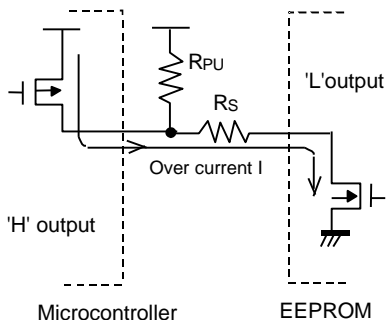


Figure 48. I/O Circuit Diagram

$$\frac{V_{CC}}{R_S} \leq I$$

$$\therefore R_S \geq \frac{V_{CC}}{I}$$

EX) V_{CC}=3V I=10mA

$$R_S \geq \frac{3}{10 \times 10^{-3}}$$

$$\geq 300 [\Omega]$$

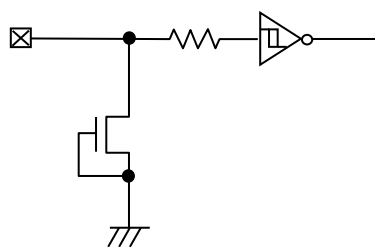
I/O Equivalence Circuit**1. Input (A2, SCL, WP)**

Figure 49. Input Pin Circuit Diagram

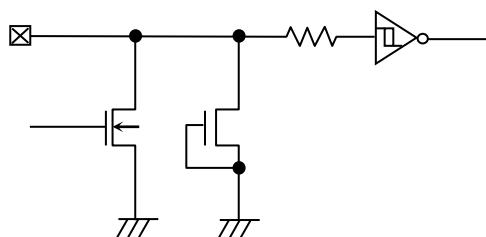
2. Input / Output (SDA)

Figure 50. Input / Output Pin Circuit Diagram

Power Up/Down Conditions

At power on, the IC's internal circuits may go through unstable low voltage area as the V_{CC} rises, making the IC's internal logic circuit not completely reset, hence, malfunction may occur. To prevent this, the IC is equipped with POR circuit and LVCC circuit. To assure the operation, observe the following conditions at power on.

1. Set SDA = 'H' and SCL = 'L' or 'H'
2. Start power source so as to satisfy the recommended conditions of t_R , t_{OFF} , and V_{bot} for operating POR circuit.

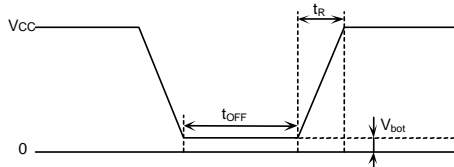


Figure 51. Rise Waveform Diagram

Recommended conditions of t_R , t_{OFF} , V_{bot}

| t_R | t_{OFF} | V_{bot} |
|----------------|----------------|---------------|
| 10ms or below | 10ms or larger | 0.3V or below |
| 100ms or below | 10ms or larger | 0.2V or below |

3. Set SDA and SCL so as not to become 'Hi-Z'.

When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

- (1) In the case when the above condition 1 cannot be observed such that SDA becomes 'L' at power on.
 - Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

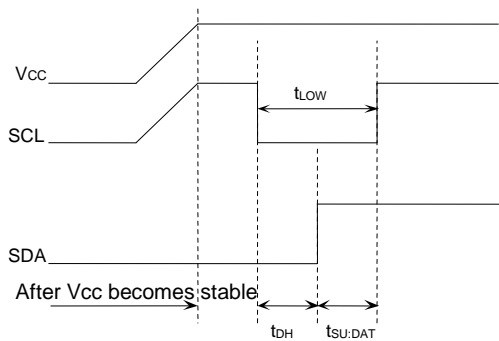


Figure 52. When SCL= 'H' and SDA= 'L'

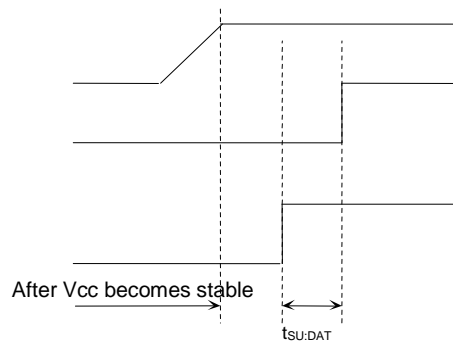


Figure 53. When SCL='L' and SDA='L'

- (2) In the case when the above condition 2 cannot be observed.
 - After power source becomes stable, execute software reset(Page16).
- (3) In the case when the above conditions 1 and 2 cannot be observed.
 - Carry out (1), and then carry out (2).

Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite operation at low power and prevents write error. At LVCC voltage (Typ =1.2V) or below, data rewrite is prevented.

Noise Countermeasures

1. Bypass Capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, it is recommended to connect a bypass capacitor (0.1 μ F) between IC's V_{CC} and GND pins. Connect the capacitor as close to the IC as possible. In addition, it is also recommended to connect a bypass capacitor between the board's V_{CC} and GND.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued**11. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

Part Numbering

| | | | | | | | | | | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| B | R | 2 | 4 | G | 0 | 8 | x | x | x | - | 3 | x | x | x | x | x |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|

BUS type24: I²C**Operating temperature/****Operating Voltage**

-40°C to +85°C / 1.6V to 5.5V

Capacity

08=8K

Package

Blank : DIP-T8*1 FJ : SOP-J8M/SOP-J8
 F : SOP8 FVT : TSSOP-B8/TSSOP-B8M
 FV : SSOP-B8 FVM : MSOP8
 FVJ : TSSOP-B8J
 NUX : VSON008X2030

Process Code

N : SOP-J8M, TSSOP-B8M
Blank : DIP-T8*1, SOP8, SOP-J8, SSOP-B8, TSSOP-B8,
 TSSOP-B8J, MSOP8, VSON008X2030

G : Halogen free**Blank** : Not Halogen free

As an exception, SOP-J8M, TSSOP-B8M, VSON008X2030 package will be Halogen free with "Blank"

T : 100% Sn**Blank** : 100% Sn**Packaging and Forming Specification**

E2 : Embossed tape and reel
 (SOP8, SOP-J8M, SOP-J8, SSOP-B8, TSSOP-B8, TSSOP-B8M, TSSOP-B8J)
 TR : Embossed tape and reel
 (MSOP8, VSON008X2030)
 None : Tube
 (DIP-T8*1)

*1 Not Recommended for New Designs.

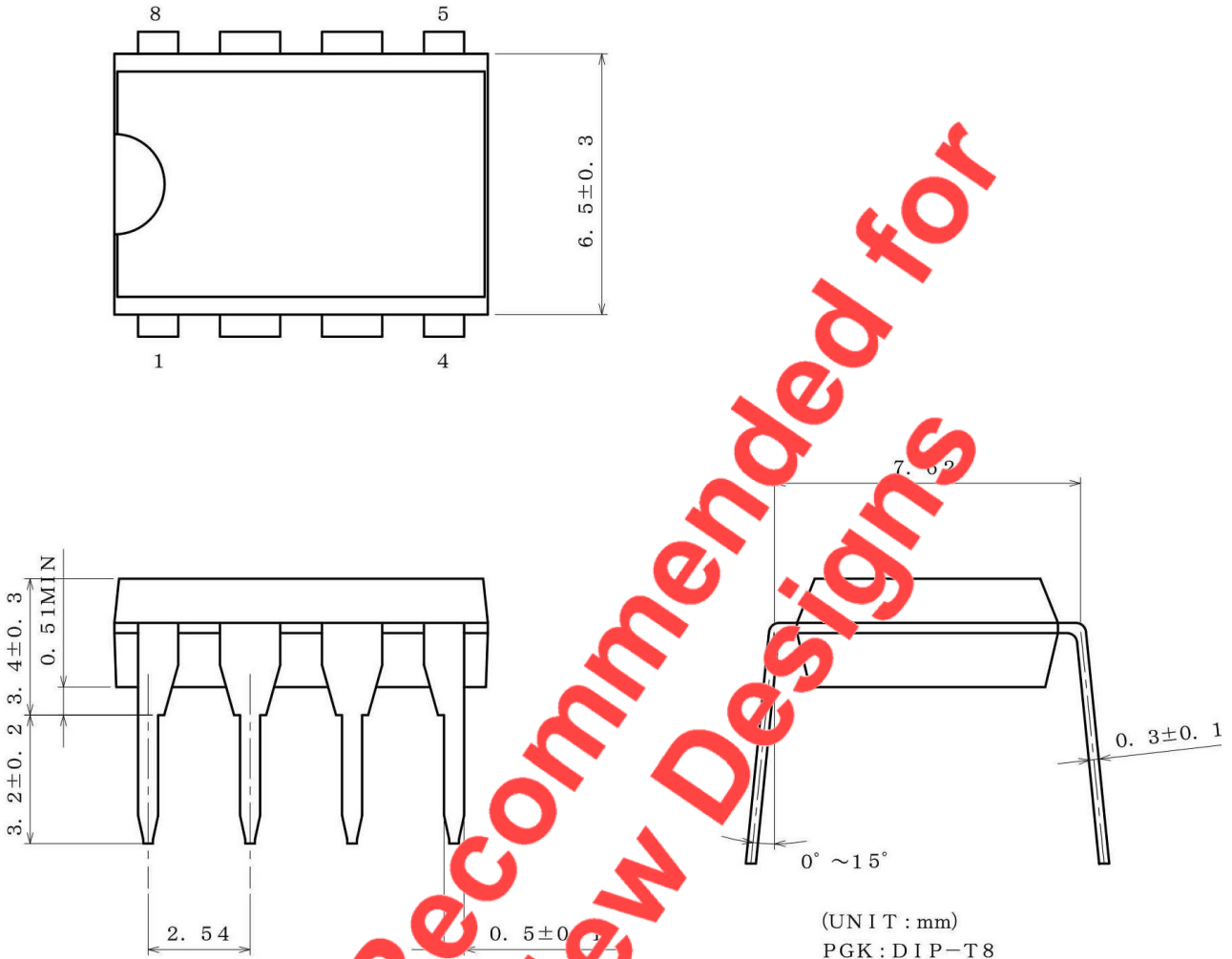
Lineup

| Capacity | Package | | Orderable Part Number | Remark | |
|----------|--------------|--------------|-----------------------|------------------|---------|
| | Type | Quantity | | | |
| 8K | DIP-T8*1 | Tube of 2000 | BR24G08 -3 | Not Halogen free | 100% Sn |
| | SOP8 | Reel of 2500 | BR24G08F -3GTE2 | Halogen free | 100% Sn |
| | SOP-J8M | Reel of 2500 | BR24G08FJ -3NE2 | Halogen free | 100% Sn |
| | SOP-J8 | Reel of 2500 | BR24G08FJ -3GTE2 | Halogen free | 100% Sn |
| | SSOP-B8 | Reel of 2500 | BR24G08FV -3GTE2 | Halogen free | 100% Sn |
| | TSSOP-B8 | Reel of 3000 | BR24G08FVT -3GE2 | Halogen free | 100% Sn |
| | TSSOP-B8M | Reel of 3000 | BR24G08FVT -3NE2 | Halogen free | 100% Sn |
| | TSSOP-B8J | Reel of 2500 | BR24G08FVJ -3GTE2 | Halogen free | 100% Sn |
| | MSOP8 | Reel of 3000 | BR24G08FVM -3GTTR | Halogen free | 100% Sn |
| | VSON008X2030 | Reel of 4000 | BR24G08NUX -3TTR | Halogen free | 100% Sn |

*1 Not Recommended for New Designs.

Physical Dimension, Tape and Reel Information

| | |
|--------------|--------|
| Package Name | DIP-T8 |
|--------------|--------|



(UNIT : mm)
 PGK : DIP-T8
 Drawing No. A0782

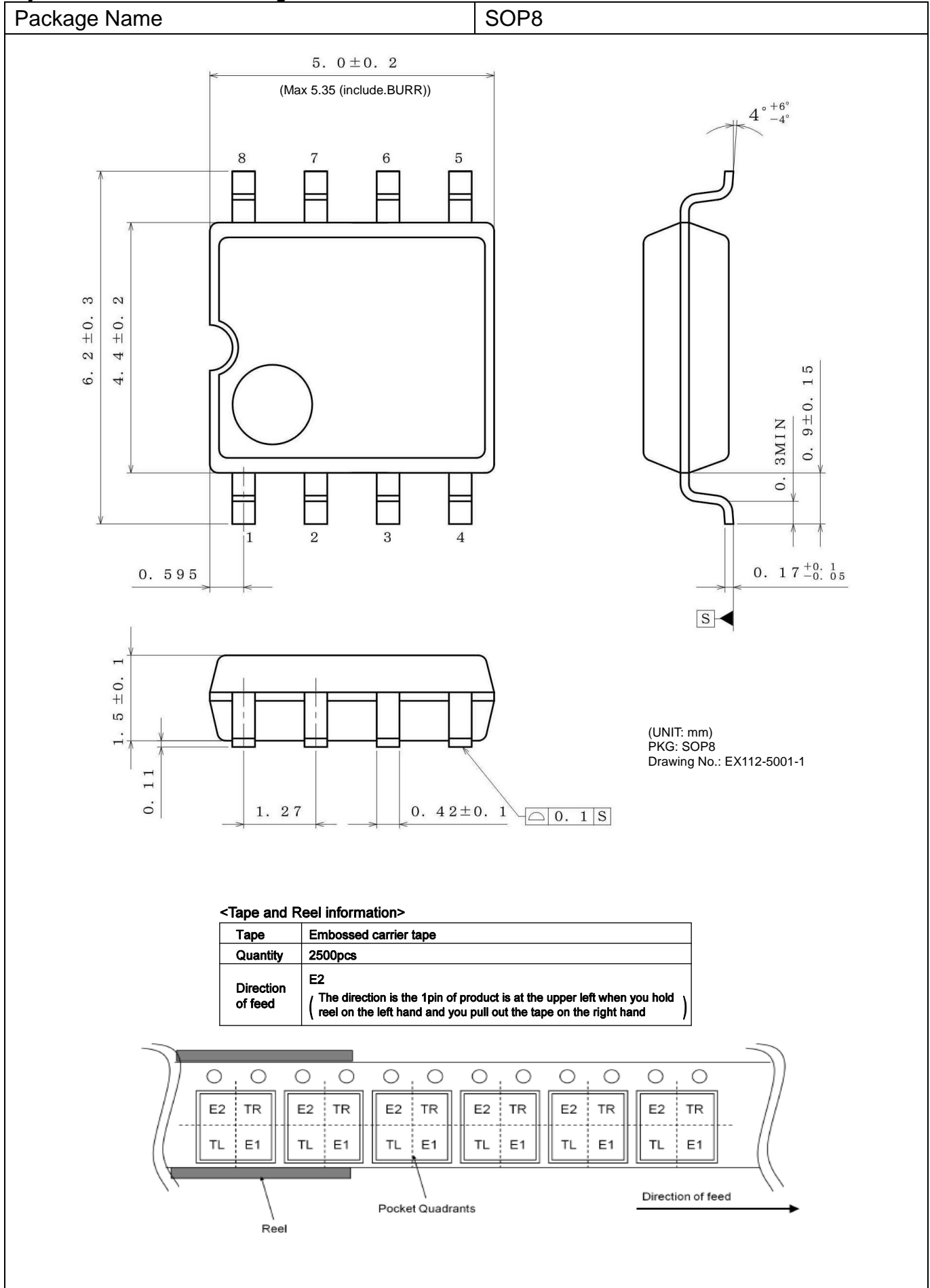
Not Recommended for New Designs

<Tape and Reel information>

| | |
|-------------------|--|
| Container | Tube |
| Quantity | 2000pcs |
| Direction of feed | Direction of products is fixed in a container tube |

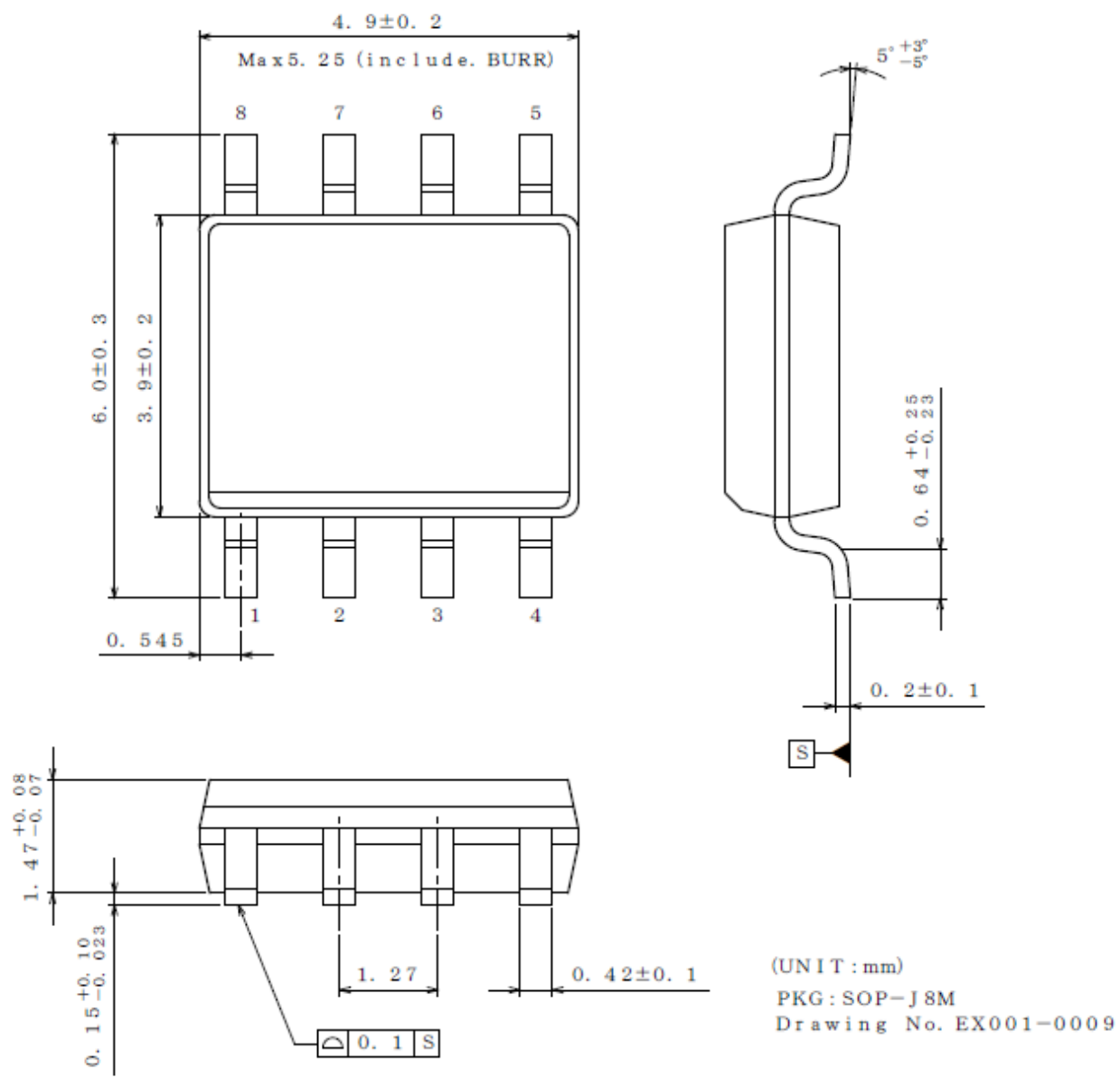
*Order quantity needs to be multiple of the minimum quantity.

Physical Dimension and Packing Information



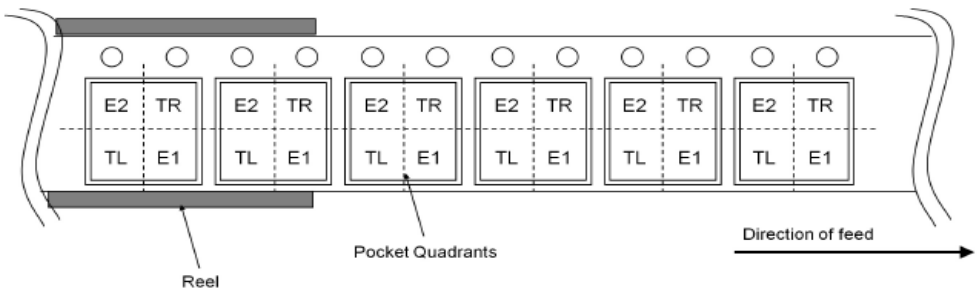
Physical Dimension and Packing Information

| | |
|--------------|---------|
| Package Name | SOP-J8M |
|--------------|---------|



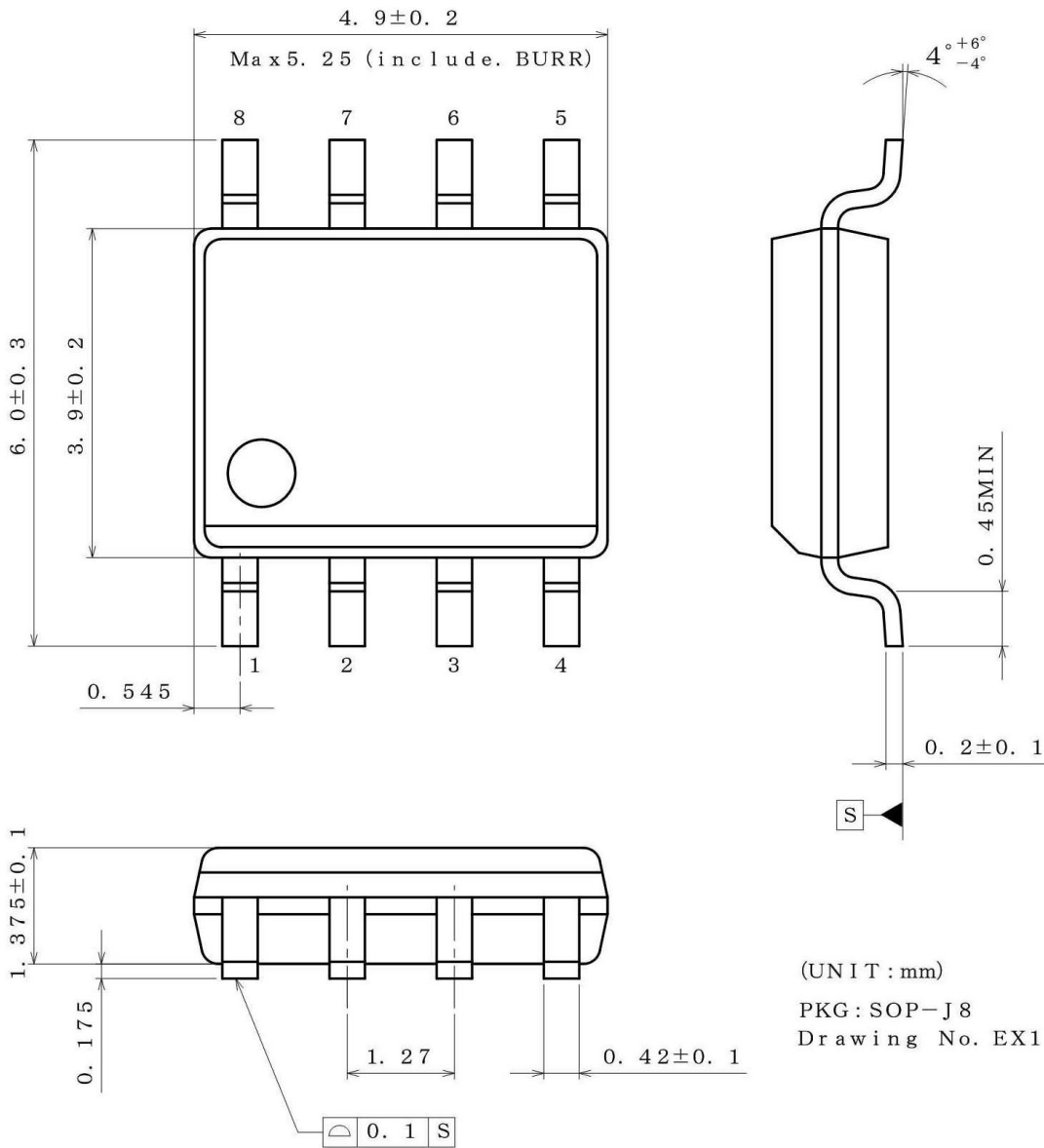
<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



Physical Dimension and Packing Information

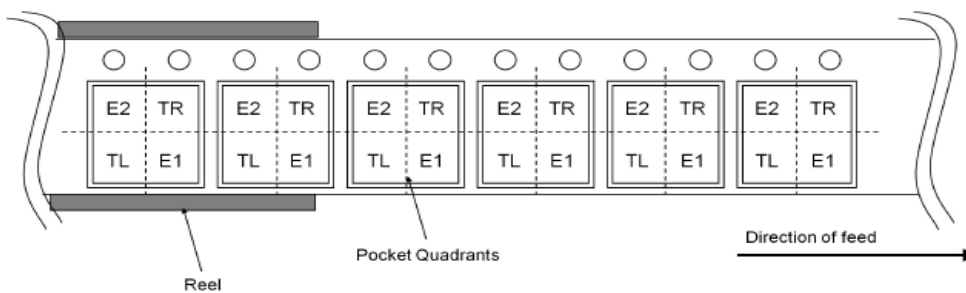
| | |
|--------------|--------|
| Package Name | SOP-J8 |
|--------------|--------|



(UNIT : mm)
 PKG : SOP-J8
 Drawing No. EX111-5002

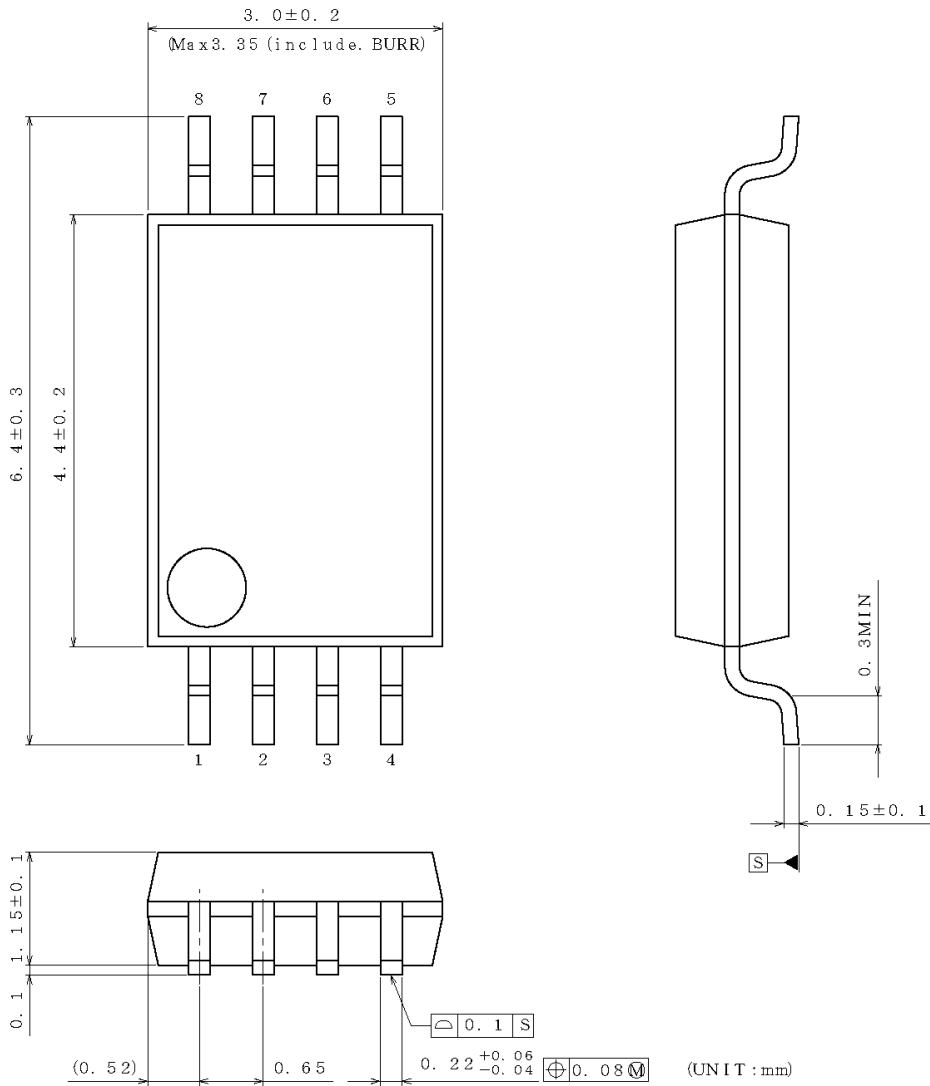
<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



Physical Dimension and Packing Information

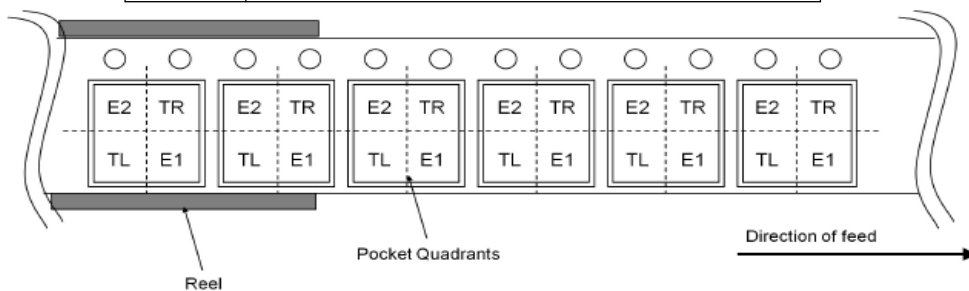
| | |
|--------------|---------|
| Package Name | SSOP-B8 |
|--------------|---------|



(UNIT : mm)
 PKG : SSOP-B8
 Drawing No. EX151-5002

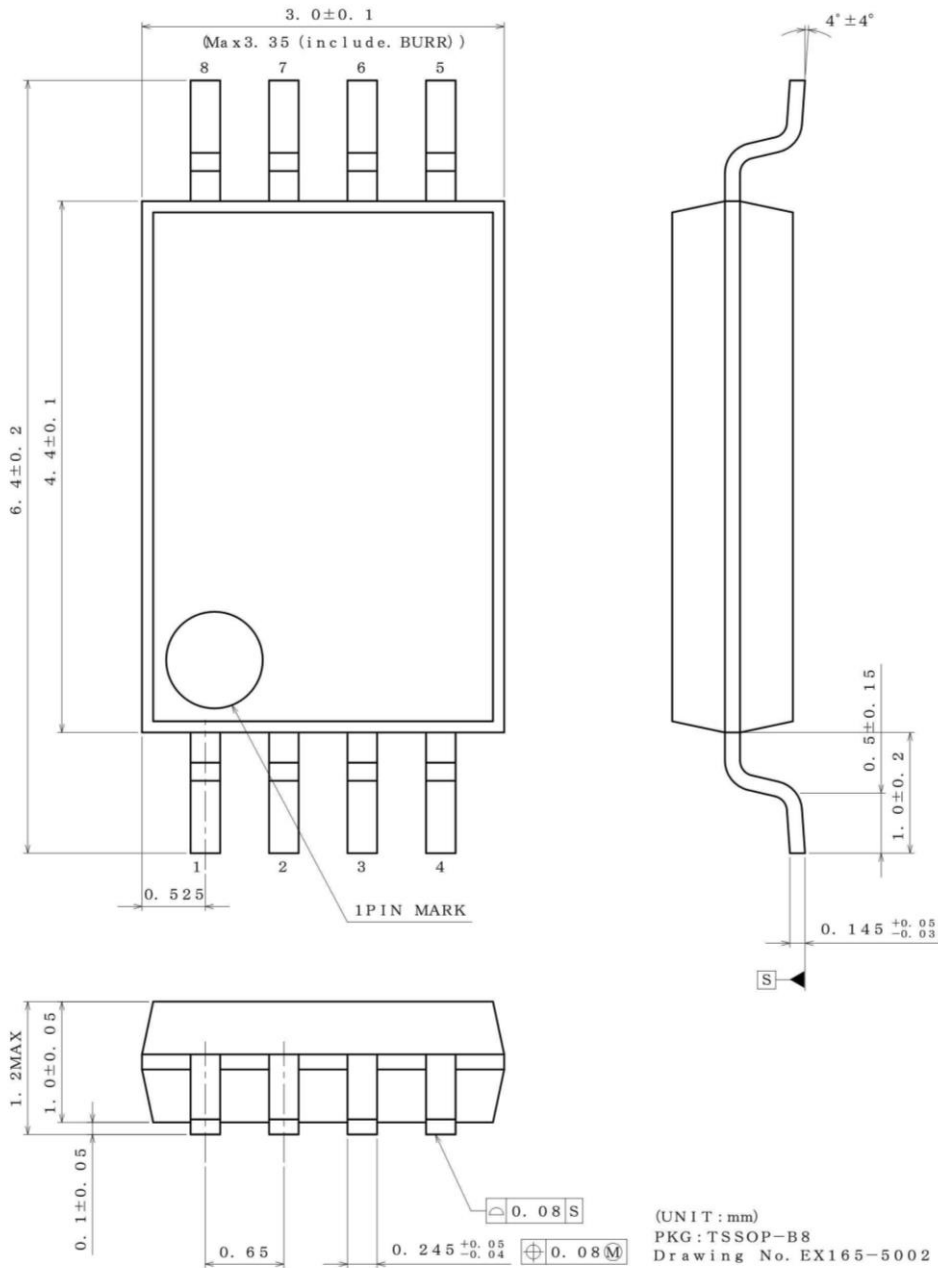
<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



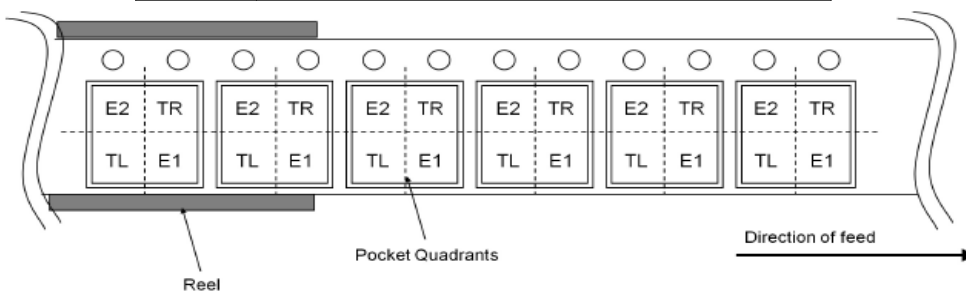
Physical Dimension and Packing Information

| | |
|--------------|----------|
| Package Name | TSSOP-B8 |
|--------------|----------|



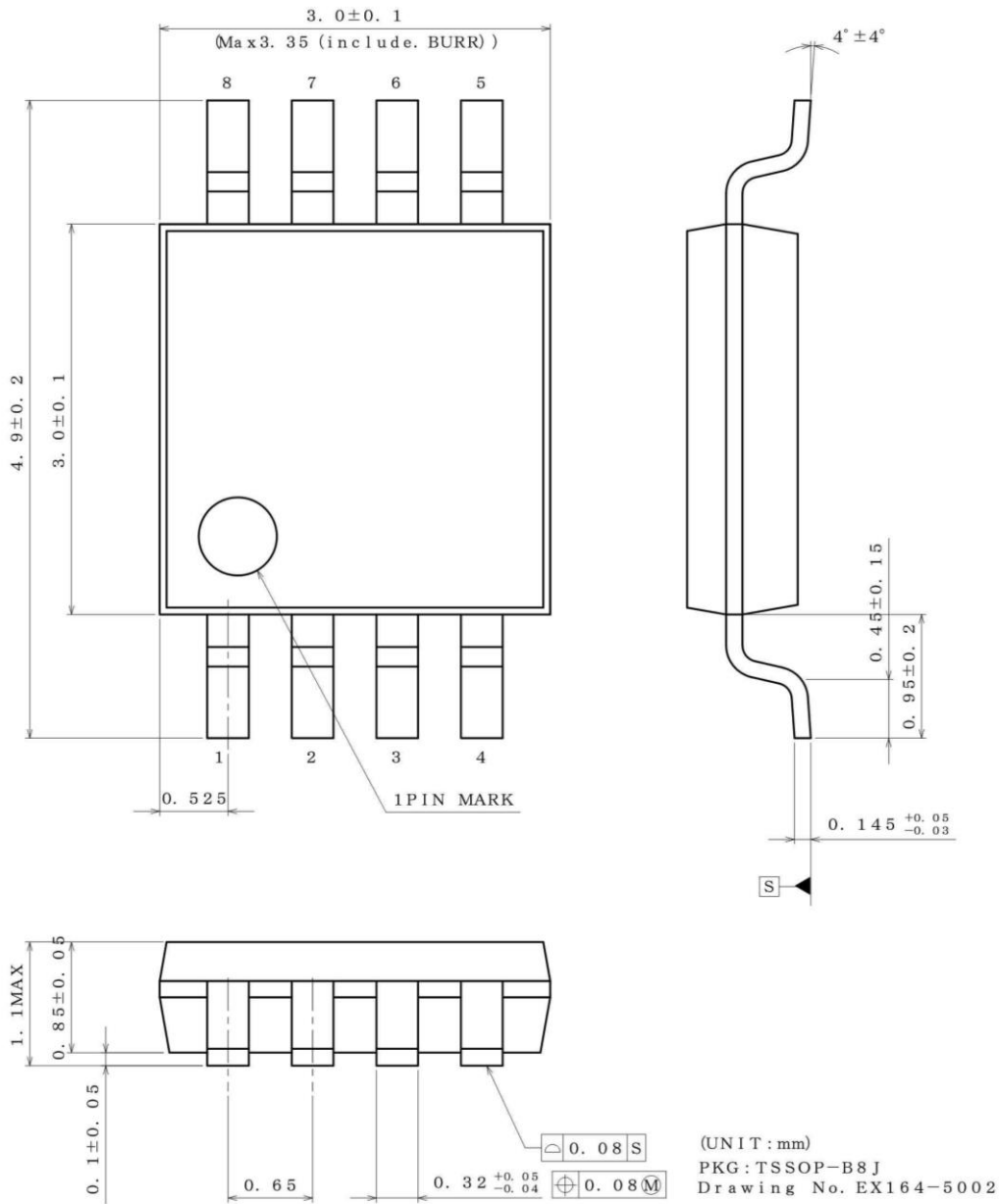
<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



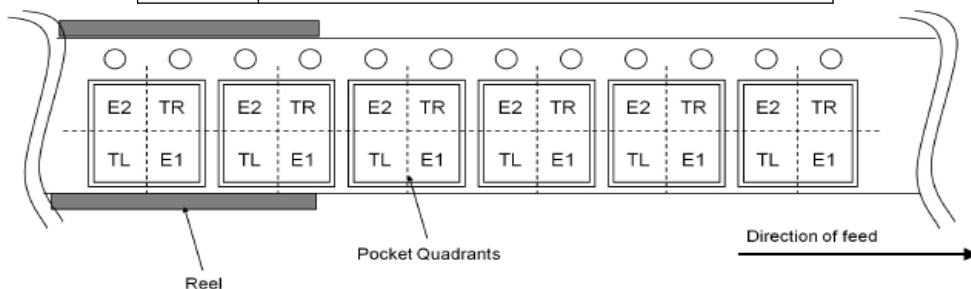
Physical Dimension and Packing Information

| | |
|--------------|-----------|
| Package Name | TSSOP-B8J |
|--------------|-----------|



<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



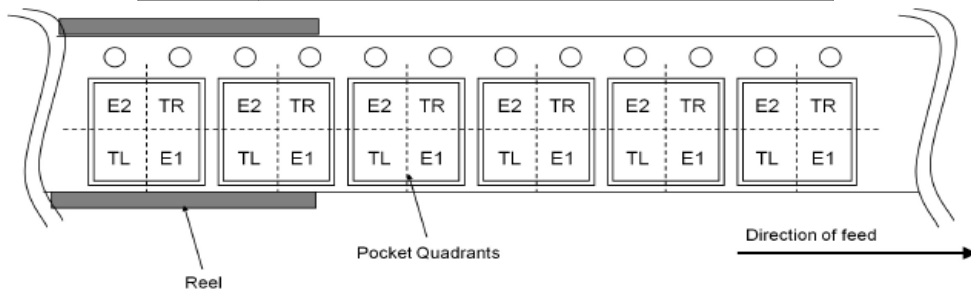
Physical Dimension and Packing Information

| | |
|--------------|-------|
| Package Name | MSOP8 |
|--------------|-------|



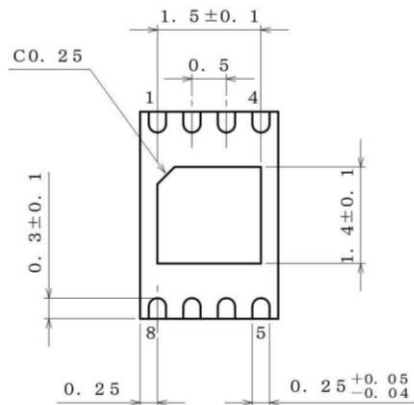
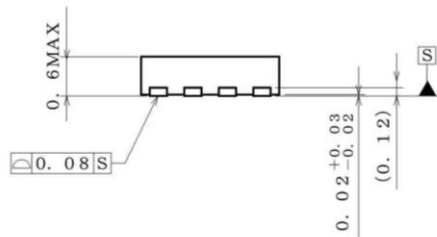
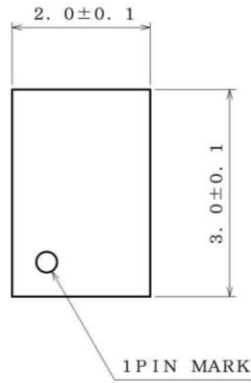
<Tape and Reel information>

| | |
|-------------------|--|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand) |



Physical Dimension and Packing Information

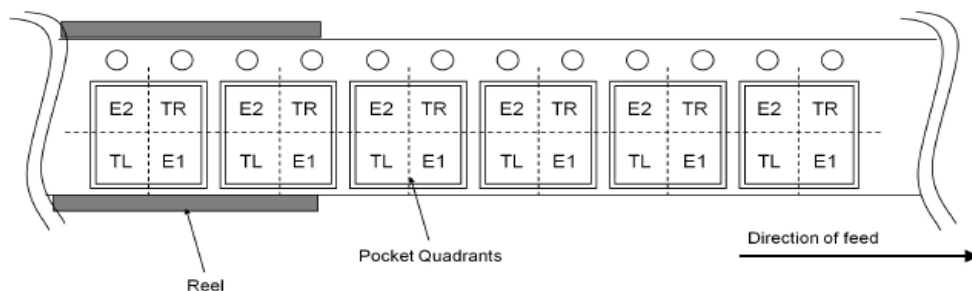
| | |
|--------------|--------------|
| Package Name | VSON008X2030 |
|--------------|--------------|



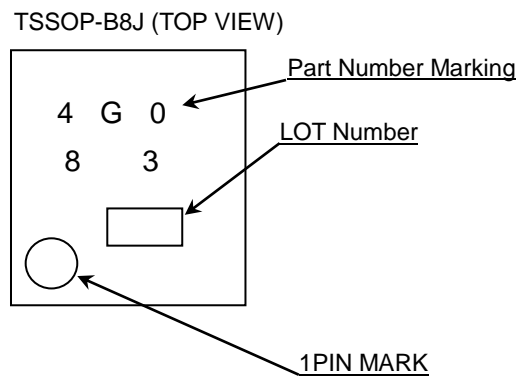
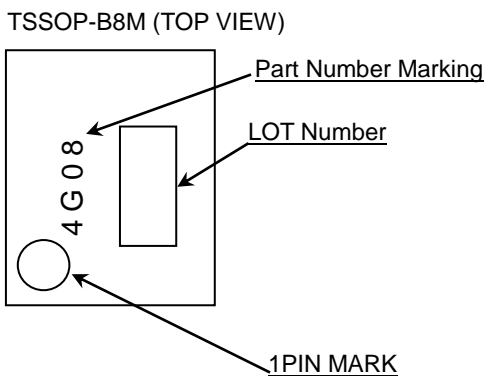
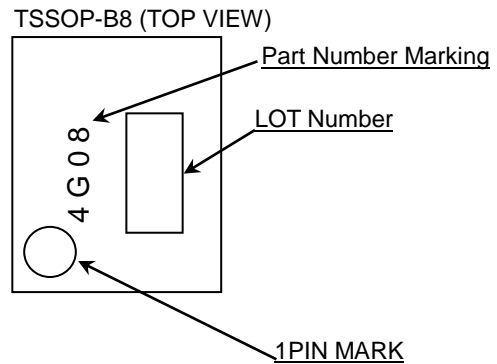
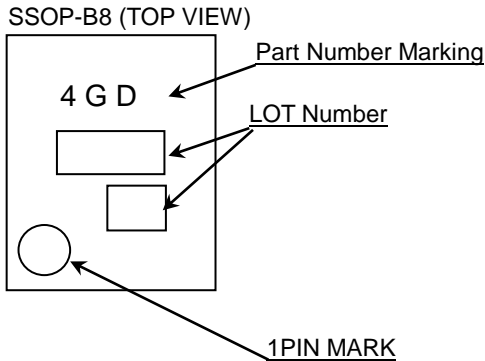
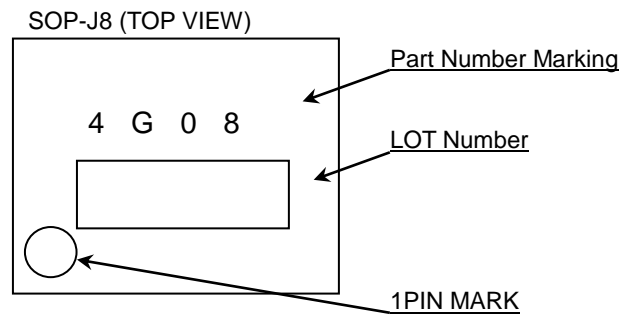
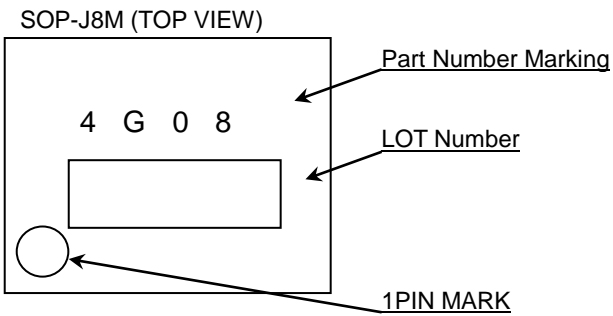
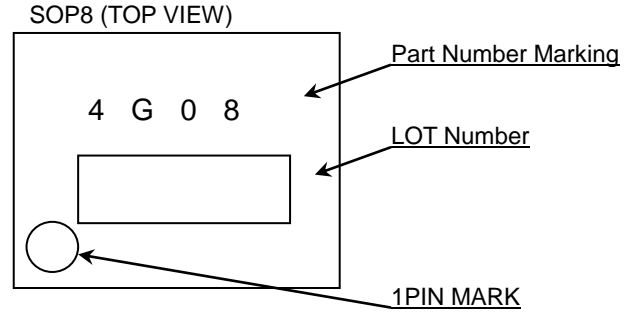
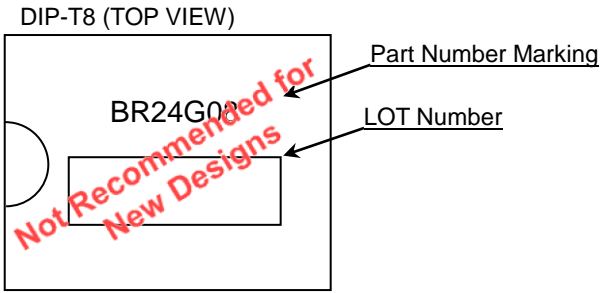
(UNIT : mm)
 PKG : VSON008X2030
 Drawing No. EX187-5001

<Tape and Reel information>

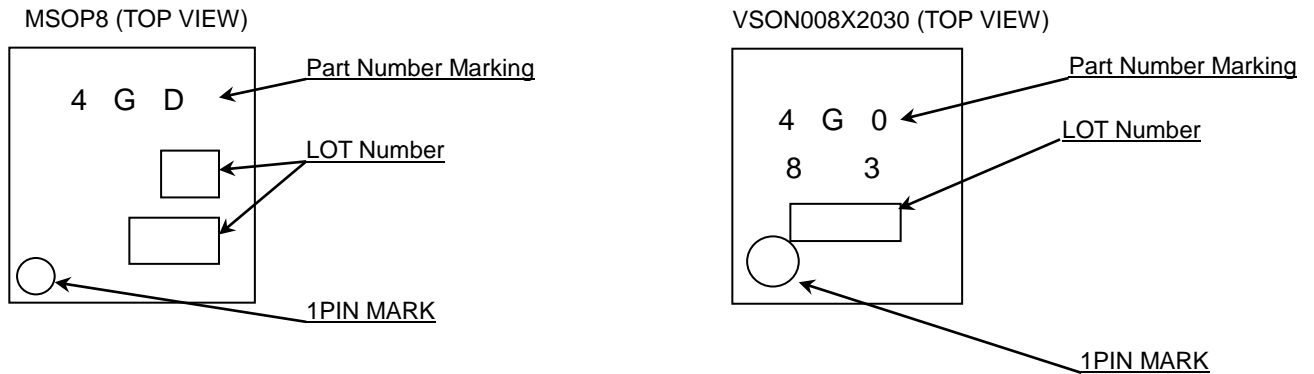
| | |
|-------------------|--|
| Tape | Embossed carrier tape |
| Quantity | 4000pcs |
| Direction of feed | TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand) |



Marking Diagrams (TOP VIEW)



Marking Diagrams (TOP VIEW)



Revision History

| Date | Revision | Changes |
|-------------|----------|---|
| 15.Jun.2012 | 001 | New Release |
| 09.Mar.2013 | 002 | Update some English words, sentences' descriptions, grammar and formatting. Add tF2 in AC Characteristic and Serial Input / Output Timing Update Fig.11 to Fig.14 |
| 31.May.2013 | 003 | P1 Change format of package line-up table. P.2 Add VESD in Absolute Maximum Ratings P.4 Add directions in Pin Descriptions |
| 27.Oct.2014 | 004 | Add SOP-J8M,TSSOP-B8M Package P1.Add 8Kbit to a General Description P1.Add "Up to 16 Byte in Page Write Mode" P1.Add "Bit Format 1K x 8" P1. List of models deletion P2. Change the unit of Power Dissipation to "W" P22. Change the Operational Notes Change notice to Rev003 |
| 11.Jun.2019 | 005 | Added watermarks and words for Not Recommended New Designs category product. Changed a format of "Physical Dimension and Packing Information". |

Notice

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- Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

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 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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