

#### **Serial EEPROM Series Automotive EEPROM**

# 125°C Operation SPI BUS EEPROM

# **BR35Hxxx-WC**

(16K 32K 64K 128K)

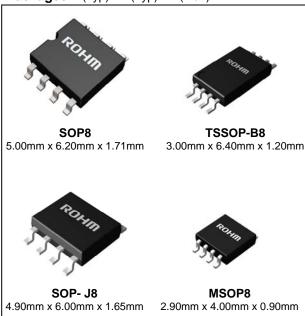
#### **General Description**

BR35Hxxx-WC is a SPI BUS interface method serial EEPROM.

#### **Features**

- High Speed Clock Operation up to 5MHz(Max)
- 2.5V to 5.5V Single Power Source Operation most suitable for Battery use.
- Page Write Mode Useful for Initial Value at Factory Shipment.
- Highly Reliable Connection by Au Pad and Au Wire.
- For SPI Bus Interface (CPOL, CPHA)=(0,0),(1,1)
- Auto Erase and Auto End Function at Data Rewrite.
- Low Operating Current
  - At Write Operation (5V): 0.6mA(Typ)
  - At Read Operation (5V): 1.3mA(Typ)
  - At Standby Operation (5V): 0.1µA(Typ)
- Address Auto Increment Function at Read Operation.
- Write Mistake Prevention Function
  - Write Prohibition at Power on.
  - Write Prohibition by Command Code (WRDI)
  - Write Mistake Prevention Function at Low Voltage.
- Data at Shipment Memory Array: FFh.
- Data Retention : 50 Years(Ta≤125°C)
- Endurance : 300,000 Cycles(Ta=125°C)
- AEC-Q100 Qualified

#### Packages W(Typ) x D(Typ) x H(Max)



#### Page write

90 111110		
Number of pages	32Byte	64Byte
Product Number	BR35H160-WC BR35H320-WC BR35H640-WC	BR35H128-WC

#### **BR35Hxxx-WC**

	•						
Capacity	Bit Format	Product Name	Supply Voltage	MSOP8	TSSOP-B8	SOP8	SOP-J8
16Kbit	2K×8	BR35H160-WC	2.5V to 5.5V	•	•	•	•
32Kbit	4K×8	BR35H320-WC	2.5V to 5.5V	•	•	•	•
64Kbit	8K×8	BR35H640-WC	2.5V to 5.5V	-	•	•	•
128Kbit	16Kx8	BR35H128-WC	2.5V to 5.5V	_	_	•	•

**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit	Remarks
Impressed Voltage	Vcc	-0.3 to +6.5	V	
		0.56(SOP8)		When using at Ta=25°C or higher, 4.5mW to be reduced per 1°C
Permissible	Dd	0.56(SOP-J8)	w	When using at Ta=25°C or higher, 4.5mW to be reduced per 1°C
Dissipation	Pd	0.41(TSSOP-B8)	VV	When using at Ta=25°C or higher, 3.3mW to be reduced per 1°C
		0.38(MSOP8)		When using at Ta=25°C or higher, 3.1mW to be reduced per 1°C
Storage Temperature Range	Tstg	-65 to +150	°C	
Operating Temperature Range	Topr	-40 to +125	°C	
Terminal Voltage	-	-0.3 to Vcc +0.3	V	

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings

Memory Cell Characteristics (Vcc=2.5V to 5.5V)

inory den onaradiensilos (voo-2.0 v to 0.0 v)								
Parameter		Limits	l lm:t	Compdition				
Farameter	Min	Тур	Max	Unit	Condition			
Endurance (Note1)	1,000,000	-	-	Times	Ta≤85°C			
	500,000	-	-	Times	Ta≤105°C			
	300,000	-	-	Times	Ta≤125°C			
	100	-	-	Years	Ta≤25°C			
Data Retention (Note1)	60	-	-	Years	Ta≤105°C			
	50	-	-	Years	Ta≤125°C			

(Note1) Not 100% TESTED

**Recommended Operating Ratings** 

Parameter	Symbol	Limits	Unit
Supply Voltage	Vcc	2.5 to 5.5	\/
Input Voltage	V <sub>IN</sub>	0 to Vcc	V

Input / Output Capacitance (Ta=25°C, frequency=5MHz)

patr Catpat Capacitailes	( : a = 0 0 ;		0		
Parameter	Symbol	Min	Max	Unit	Conditions
Input Capacitance (Note1)	C <sub>IN</sub>	_	8	pF	V <sub>IN</sub> =GND
Output Capacitance (Note1)	Соит	_	8	PΓ	V <sub>OUT</sub> =GND

(Note1) Not 100% TESTED

Electrical Characteristics (Unless otherwise specified, Ta=-40°C to +125°C, Vcc=2.5V to 5.5V)

Parameter	Cumbal	Limits		Unit	Conditions	
Farameter	Symbol	Min	Тур	Max	Offic	Conditions
"H" Input Voltage	V <sub>IH</sub>	0.7xVcc	_	Vcc+0.3	V	2.5V≤Vcc≤5.5V
"L" Input Voltage	V <sub>IL</sub>	-0.3	_	0.3xVcc	V	2.5V≤Vcc≤5.5V
"L" Output Voltage	V <sub>OL</sub>	0	_	0.4	V	I <sub>OL</sub> =2.1mA
"H" Output Voltage	V <sub>OH</sub>	Vcc-0.5	_	Vcc	V	I <sub>OH</sub> =-0.4mA
Input Leakage Current	I <sub>LI</sub>	-10	_	10	μΑ	V <sub>IN</sub> =0V to Vcc
Output Leakage Current	I <sub>LO</sub>	-10	_	10	μΑ	V <sub>OUT</sub> =0V to Vcc, CSB=Vcc
Operating Current	I <sub>CC1</sub>	_	_	2.0 <sup>(Note1)</sup> 2.5 <sup>(Note2)</sup>	mA	Vcc=2.5V, f <sub>SCK</sub> =5MHz, t <sub>E/W</sub> =5ms, V <sub>IH</sub> /V <sub>IL</sub> =0.9Vcc/0.1Vcc, SO=OPEN Byte Write, Page Write
(Write)	I <sub>CC2</sub>	_	_	3.0 <sup>(Note1)</sup> 5.5 <sup>(Note2)</sup>		Vcc=5.5V, f <sub>SCK</sub> =5MHz, t <sub>E/W</sub> =5ms, V <sub>IH</sub> /V <sub>IL</sub> =0.9Vcc/0.1Vcc, SO=OPEN Byte Write, Page Write
Operating Current	I <sub>CC3</sub>	_	_	1.5	mA	Vcc=2.5V, f <sub>SCK</sub> =5MHz, V <sub>IH</sub> /V <sub>IL</sub> =0.9Vcc/0.1Vcc SO=OPEN, Read, Read Status Register
(Read)	I <sub>CC4</sub>	_	_	2.0	mA	Vcc=5.5V, f <sub>SCK</sub> =5MHz, V <sub>IH</sub> /V <sub>IL</sub> =0.9Vcc/0.1Vcc SO=OPEN, Read, Read Status Register
Standby Current	I <sub>SB</sub>	_	_	10	μA	Vcc=5.5V CSB=Vcc, SCK=SI=Vcc or GND, SO=OPEN

(Note1) BR35H160/320-WC (Note2) BR35H640/128-WC

#### **Operating Timing Characteristics**

(Ta=-40°C to +125°C, unless otherwise specified, load capacitance C<sub>L1</sub>=100pF)

				) 
Symbol	2.	Unit		
Symbol	Min	Тур	Max	Offic
f <sub>SCK</sub>	-	-	5	MHz
t <sub>SCKWH</sub>	85	-	-	ns
t <sub>SCKWL</sub>	85	-	-	ns
t <sub>CS</sub>	85	-	-	ns
t <sub>CSS</sub>	90	-	-	ns
t <sub>CSH</sub>	85	-	-	ns
t <sub>SCKS</sub>	90	-	-	ns
t <sub>SCKH</sub>	90	-	-	ns
t <sub>DIS</sub>	20	-	-	ns
t <sub>DIH</sub>	30	-	-	ns
t <sub>PD1</sub>	-	-	70	ns
t <sub>PD2</sub>	-	-	55	ns
toH	0	-	-	ns
toz	-	-	100	ns
t <sub>RC</sub>	-	-	1	μs
t <sub>FC</sub>	-	-	1	μs
t <sub>RO</sub>	-		50	ns
t <sub>FO</sub>	-	-	50	ns
t <sub>E/W</sub>	-	-	5	ms
	Symbol  fsck tsckwh tsckwl tcs tcss tcsh tscks tsckh tpli tpp1 tpp2 toh toz trc	Symbol	Symbol     2.5≤Vcc≤5.8       Min     Typ       fsck     -     -       tsckwh     85     -       tcs     85     -       tcss     90     -       tcsh     85     -       tsck     90     -       tsckh     90     -       tplis     20     -       tplis     -     -       tplis     - <td>fsck 5  tsckwh 85  tcs 85   tcss 90   tsckh 90   tsckh 90   tsckh 90   tsckh 90   tsckh 90   tsch 90   tsch 90   tsch 90   tsckh 90   tsch 90   tsch 90   tsckh 90 -   tsckh 90   tsckh 90   tsckh 90   tsckh 90   tsc</td>	fsck 5  tsckwh 85  tcs 85   tcss 90   tsckh 90   tsckh 90   tsckh 90   tsckh 90   tsckh 90   tsch 90   tsch 90   tsch 90   tsckh 90   tsch 90   tsch 90   tsckh 90 -   tsckh 90   tsckh 90   tsckh 90   tsckh 90   tsc

(Note1) Not 100% TESTED

#### **AC** measurement Conditions

Parameter	Symbol		Unit		
Farameter	Symbol	Min	Тур	Max	Offic
Load Capacitance 1	C <sub>L1</sub>	-	-	100	pF
Load Capacitance 2	C <sub>L2</sub>	30		30	pF
Input Rise Time	-	-	-	50	ns
Input Fall Time	-	50		ns	
Input Voltage	-	0.2Vcc / 0.8Vcc		V	
Input / Output Judgment Voltage	-	0.3Vcc / 0.7Vcc			V

#### Sync Data Input / Output Timing

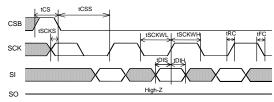


Figure 1. Input Timing

Data through SI enters the IC in sync with the data rise edge of SCK. Please input address and data starting from the most significant bit MSB.

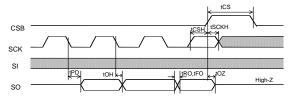


Figure 2. Input / Output Timing

Data through SO is output in sync with the data fall edge of SCK. Data is output starting from the most significant bit MSB.

#### toz Measurement Condition

IL is the load current that changes the SO voltage to  $0.5 \times Vcc$ . IL= $\pm 1 mA$ .

After CSB starts to rise, the time needed for SO to change to High-Z is defined with 10% changing point from SO=High or SO=Low.

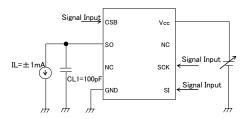


Figure 3. toz Measurement Circuit

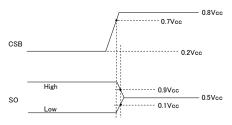
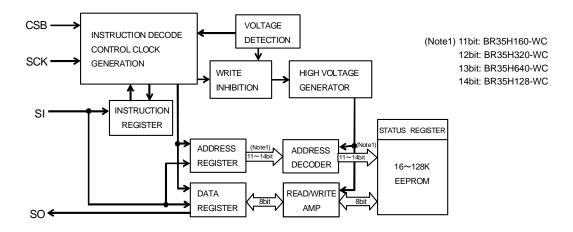
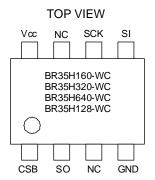


Figure 4. toz Measurement Timing

#### **Block Diagram**



#### **Pin Configuration**



### **Pin Description**

Terminal Name	Input/Output	Function
Vcc	_	Power Supply to be connected
GND	_	All input / output reference voltage, 0V
CSB	Input	Chip select input
SCK	Input	Serial clock input
SI	Input	Start bit, ope code, address, and serial data input
SO	Output	Serial data output
NC	_	Non connection

#### **Typical Performance Curves**

The following characteristic data are typ value.

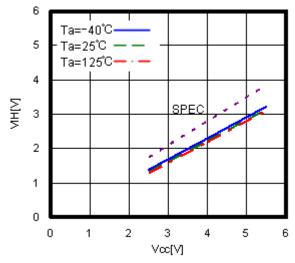


Figure 5. "H" Input Voltage vs Supplty Voltage

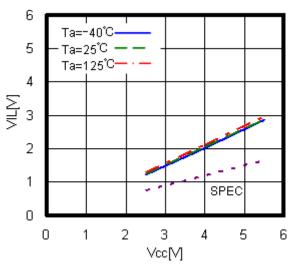


Figure 6. "L" Input Voltage vs Supply Voltage

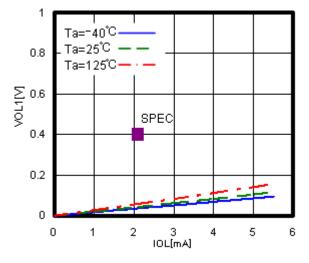


Figure 7. "L" Output Voltage vs Output Current (Vcc=2.5V)

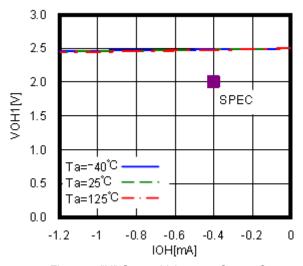


Figure 8. "H" Output Voltage vs Output Current (Vcc=2.5V)

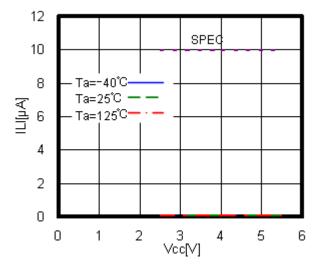


Figure 9. Input leak Current vs Supply Voltage

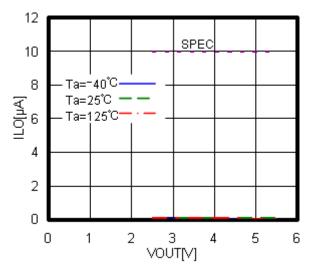


Figure 10. Output Leak Current vs Output Voltage (Vcc=5.5V)

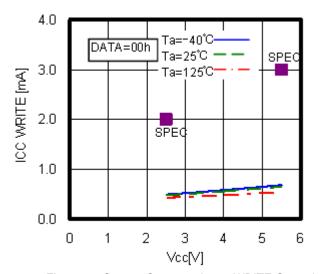


Figure 11. Current Consumption at WRITE Operation vs Supply Voltage

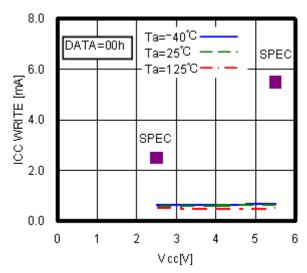


Figure 12. Current Consumption at WRITE Operation vs Supply Voltage (BR35H640/128-WC)

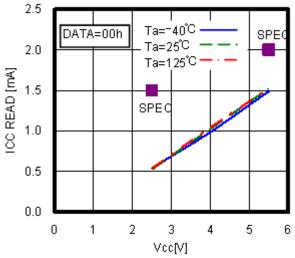


Figure 13. Consumption Current at READ Operation vs Supply Current

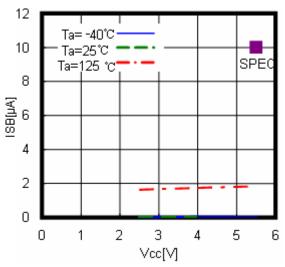


Figure 14. Standby Current vs Supply Voltage

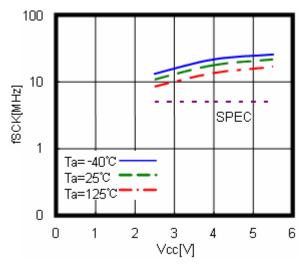


Figure 15. SCK Frequency vs Supply Voltage

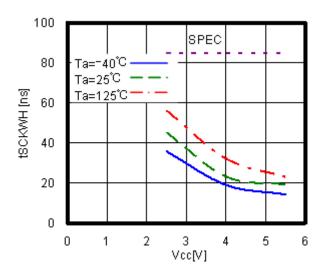


Figure 16. SCK High Time vs Supply Voltage

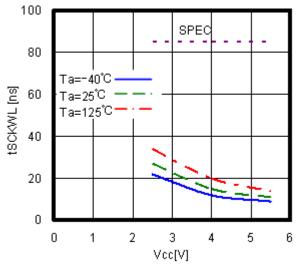


Figure 17. SCK Low Time vs Supply Voltage

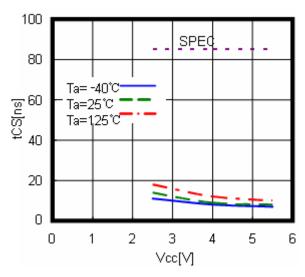


Figure 18. CSB High Time vs Supply Voltage

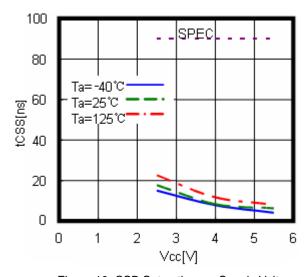


Figure 19. CSB Setup time vs Supply Voltage

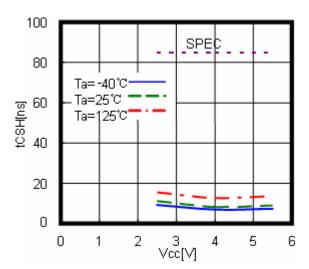


Figure 20. CSB Hold Time vs Supply Voltage

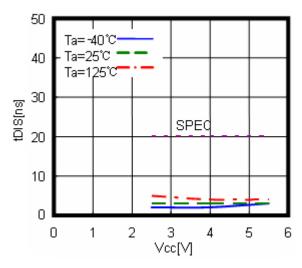


Figure 21. SI Setup Time vs Supply Voltage

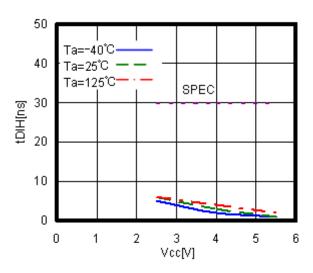


Figure 22. SI Hold Time vs Supply Voltage

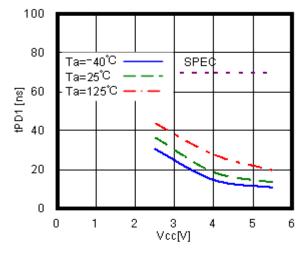


Figure 23. Data Output Delay Time vs Supply Voltage  $(C_{L1}=100pF)$ 

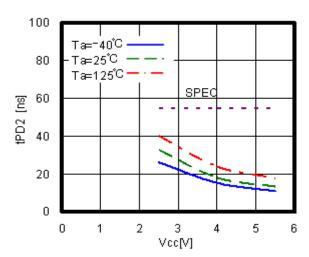


Figure 24. Data Output Delay Time vs Supply Voltage  $(C_{L2}=30pF)$ 

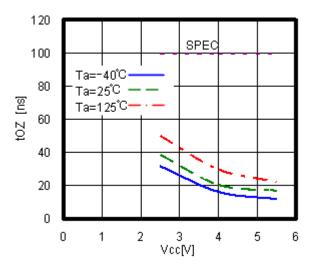


Figure 25. Output Disable Time vs Supply Voltage

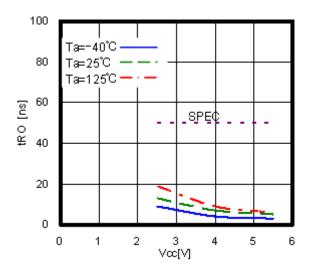


Figure 26. Output Rise Time vs Supply Voltage

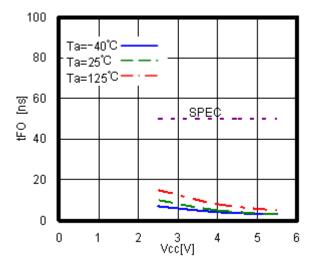


Figure 27. Output Fall Time vs Supply Voltage

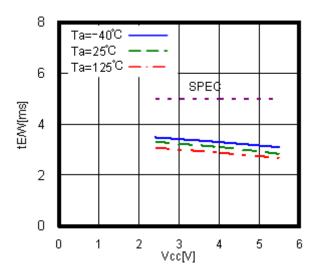


Figure 28. Write Cycle Time vs Supply Voltage

#### **Features**

#### 1. Status Registers

This IC has status registers. The status register has 8 bits and expresses the following parameters. WEN is set by the write enable command and write disable command. WEN goes into the write disable status when the power source is turned off. The  $\overline{R}/B$  bit is for write confirmation and therefore cannot be set externally. The status register value can be read by use of the read status command.

#### **Status Registers**

Product Number	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR35H160-WC								
BR35H320-WC	_	_	_	_	_	_	WEN	
BR35H640-WC	U	U	U	U	U	U	VV⊏IN	R/B
BR35H128-WC								

bit	Memory location	Function	Contents
WEN	Register	Write and write status register write enable / disable status confirmation bit WEN=0=prohibited WEN=1=permitted	This confirms prohibited status or permitted status of the write and the write status register.
R/B	Register	Write cycle status (READY / BUSY) status confirmation bit  R/B=0=READY  R/B=1=BUSY	This confirms READY status or BUSY status of the write cycle.

#### **Command Mode**

Command			Ope code		
			BR35H160-WC		
		Contents	BR35H320-WC		
			BR35H640-WC		
			BR35H128-WC		
WREN	Write enable	Write enable command	0000	0110	
WRDI	Write disable	Write disable command	0000	0100	
READ	Read	Read command	0000	0011	
WRITE	Write	Write command	0000	0010	
RDSR	RDSR Read status register Status register read command			0101	

#### **Timing Chart**

#### 1. Write Enable (WREN) / Disable (WRDI) Cycle

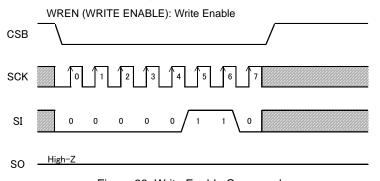


Figure 29. Write Enable Command

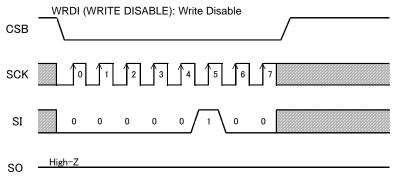
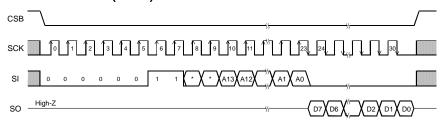


Figure 30. Write Disable

This IC has a write enable status and a write disable status. Write enable status is achieved by the write enable command and write disable status is achieved by the write disable command. As for these commands, set CSB to LOW and then input the respective ope codes. The respective commands are accepted at the 7-th clock rise. The command is also valid with Inputs over 7 clocks.

In order to perform a write command it is necessary to use the write enable command to set the IC to the write enable status. If a write command is input during write disable status the command will be cancelled. After a write command is input during write enable status the IC will return to the write disable status. When turning on the power the IC will be in write disable status.

#### 2. Read Command (READ)

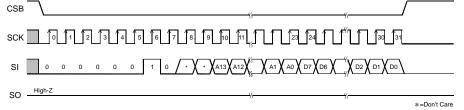


Product	Address
number	Length
BR35H160-WC	A10-A0
BR35H320-WC	A11-A0
BR35H640-WC	A12-A0
BR35H128-WC	A13-A0

Figure 31. Read Command (BR35H160/320/640/128-WC)

By use of the read command, the data of the EEPROM can be read. As for this command, set CSB to LOW, then input the address after the read ope code. EEPROM starts data output of the designated address. Data output is started from the SCK fall of 23 clock and from D7 to D0 sequentially. The IC features an increment read function. After the output of 1 byte (8bits) of data, by continuing input of SCK the next data addresses can be read. Increment read can read all addresses of the EEPROM. After reading the data of the most the significant address, by continuing with the increment read the data of the most insignificant address is read.

#### 3. Write Command (WRITE)



Product	Address
number	Length
BR35H160-WC	A10-A0
BR35H320-WC	A11-A0
BR35H640-WC	A12-A0
BR35H128-WC	A13-A0

Figure 32. Write Command (BR35H160/320/640/128-WC)

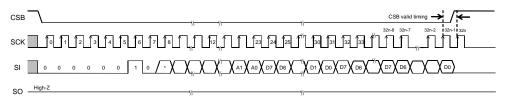


Figure 33. n Byte Page Write Command (BR35H160/320/640-WC)

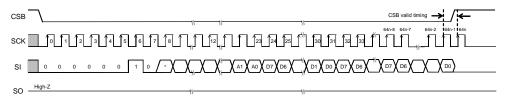


Figure 34. n Byte Page Write Command (BR35H128-WC)

With the write command data can be written to the EEPROM. As for this command, set CSB to LOW, then input address and data after inputting the write ope code. Then, by making CSB HIGH, the EEPROM starts writing. The write time of EEPROM requires time of  $t_{\text{EW}}$  (Max 5ms). During  $t_{\text{EW}}$ , commands other than the status read command are not accepted. Start CSB after taking the last data (D0) and before the next SCK clock starts. At other timings the write command will not be executed and will be cancelled. The IC has page write functionality. After input 1 byte (8bits) of data, by continuing data input without starting CSB, data up to  $32/64^{\text{(Note1)}}$  bytes can be written in one  $t_{\text{EW}}$ . In page write, the insignificant  $5/6^{\text{(Note2)}}$  bit of the designated address is incremented internally every time 1 byte of data is input, and data is written to the respective addresses. When data larger then the maximum bytes is input the address rolls over and previously input data is overwritten.

Write command is executed when CSB rises between the SCK clock rising edge to recognize the 8th bit's of data input and the next SCK rising edge. At other timings the write command is not executed and cancelled (Figure 40 valid timing c). In page write, the CSB valid timing is every 8 bits. If CSB rises at other timings page write is cancelled together with the write command and the input data is reset.

(Note1) BR35H160/320/640-WC = Max 32 Bytes

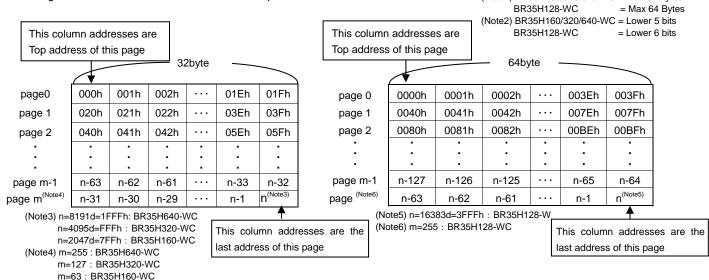


Figure 35. EEPROM Physical Address for Page Write Command (32/64Byte)

#### **Example of Page Write Command**

and the difference of the contract of the cont							
No.	Addresses of Page0	000h	001h	002h		01Eh	01Fh
1	Previous data		01h	02h		1Eh	1Fh
2	2 bytes input data		55h	-		-	-
3	2 bytes last data	AAh	55h	02h		1Eh	1Fh
	OA boda a in not data	AAh	55h	AAh		AAh	55h
4	34 bytes input data	FFh	00h	-		-	-
5	34 bytes last data	FFh	00h	AAh		AAh	55h

- a: In case of input the data of No.② which is 2 bytes page write command for the data of No.①, EEPROM data changes like No.③.
- b : In case of input the data of No. 4 which is 34 bytes page write command for the data of No. 1, EEPROM data changes like No. 5.
- c : In case of a or b, when write command is cancelled, EEPROM data keep No. ①.

In page write command, when data is set to the last address of a page (e.g. address "03Fh" of page 1), the next data will be set to the top address of the same page (e.g. address "020h" of page 1). This is why page write address increment is available in the same page. As a reference, if of 32 bytes, page write command is executed for 2 bytes the data of the other 30 bytes without addresses will not be changed.

#### 4. Status Register Read Command

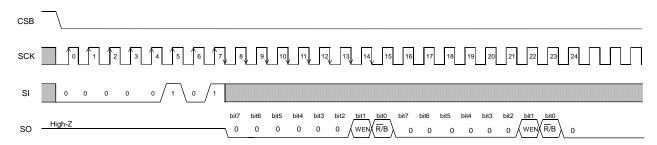


Figure 36. Status Register Read Command (BR35H160/320/640/128-WC)

The EEPROM status can be read by use of the status register read command. For this command set CSB to Low then input the ope code of the status register read command followed by the clock input as shown above. The data of status register will then be read out. This command features increment functionality. When clock input is continued during CSB=Low, 8 bytes of status register data will be continuously read out. When this command is executed from the start of write programming to the end of write programming, the end of write programming can be confirmed by checking the following changes: WEN=Low followed by  $\overline{R}/B$ =Low. After confirming the end of write programming, before inputting the next command CSB first needs to be High and then put back to Low.

#### At Standby

#### 1. Current at Standby

Set CSB "H", and be sure to set SCK, SI input "L" or "H". Do not input intermediate electric potantial.

#### 2. Timing

As shown in Figure 37, at standby, when SCK is "H", even if CSB falls, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB "H" status.

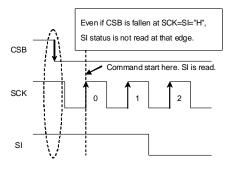
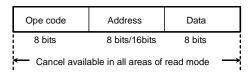


Figure 37. Operating Timing

#### **Method to Cancel Each Command**

#### 1. READ. RDSR

· Cancellation method: cancel by CSB = "H"



Ope code Data

8 bits 8 bits

Cancel available in all areas of rdsr mode

Figure 38. READ Cancel Valid Timing

Figure 39. RDSR Cancel Valid Timing

#### 2. WRITE, PAGE WRITE

- a : Ope code, address input area. Cancellation possible by CSB="H"
- b : Data input area (D7 to D1 input area) Cancellation possible by CSB="H"
- c : Data input area (D0 area)
  Write starts after CSB rise.
  After CSB rise, cancellation is no longer possible.
- d : t<sub>E/W</sub> area. Cancellation is possible by CSB = "H". However, when write starts (CSB rise) in area c, cancellation is no longer possible. Also, cancellation is not possible by continues inputting of SCK clock. In page write mode, there is a write enable area at every 8 clocks.



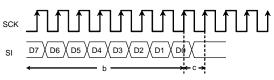


Figure 40. WRITE Cancel Valid Timing

Note 1) If Vcc is set to OFF during execution of write the data of the designated address is not guaranteed. Please execute write again. Note 2) If CSB rises at the same timing as that the SCK rises, write execution / cancel will become unstable.

Therefore, it is recommended to let CSB rise in the SCK = "L" area. As for SCK rise, ensure a timing of t<sub>CSS</sub> / t<sub>CSH</sub> or higher.

#### 3. WREN, WRDI

- a : From ope code to 7-th clock rise, cancel by CSB = "H".
- b: Cancellation is not possible when CSB rises after the 7-th clock.

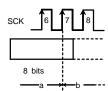


Figure 41. WREN/WRDI Cancel Valid Timing

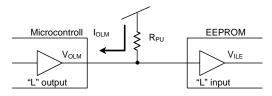
#### **High Speed Operations**

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

#### 1. Input Pin Pull up, Pull down Resistance

When attaching pull up, pull down resistance to the EEPROM input pin, select an appropriate value for the microcontroller  $V_{OL}$ ,  $I_{OL}$  from the  $V_{IL}$  characteristics of this IC.

#### 2. Pull up Resistance



- V<sub>ILE</sub> :EEPROM V<sub>IL</sub> specifications
- V<sub>OLM</sub>:Microcontroller V<sub>OL</sub> specifications
- · I<sub>OLM</sub> :Microcontroller I<sub>OL</sub> specifications

Figure 42. Pull up Resistance

$$R_{PU} \ge \frac{V_{CC} - V_{OLM}}{I_{OLM}}$$
 ... ①
 $V_{OLM} \le V_{ILE}$  ... ②

Example) When Vcc=5V,  $V_{ILE}$ =1.5V,  $V_{OLM}$ =0.4V,  $I_{OLM}$ =2mA, from the equation ①,

$$R_{PU} \ge \frac{5 - 0.4}{2 \times 10^{-3}}$$

$$\therefore R_{PU} \geq 2.3 \quad [k\Omega]$$

With the value of Rpu to satisfy the above equation,  $V_{OLM}$  becomes 0.4V or lower, and with  $V_{ILE}$  (=1.5V), the equation ② is also satisfied.

Also, in order to prevent malfunction or erroneous write at power ON/OFF, be sure to make CSB pull up.

#### 3. Pull down Resistance

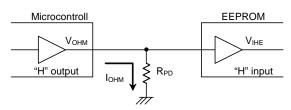


Figure 43. Pull down Resistance

$$R_{PD} \ge \frac{V_{OHM}}{I_{OHM}}$$
 ... 3

Example) When  $V_{CC}$ =5V,  $V_{OHM}$ = $V_{CC}$ -0.5V,  $I_{OHM}$ =0.4mA,  $V_{IHE}$ = $V_{CC}$ ×0.7V, from the equation③,

$$RPD \ge \frac{5 - 0.5}{0.4 \times 10^{-3}}$$

The operations speed changes according to the amplitude  $V_{IHE}$ ,  $V_{ILE}$  of the signals input to the EEPROM. More stable high speed operations can be realized by inputting signals with Vcc / GND levels of amplitude. On the contrary, when signals with an amplitude of 0.8 Vcc / 0.2 Vcc are input, operation speed slows down. (Note1)

In order to realize more stable high speed operation, it is recommended to set the values of  $R_{PU}$ ,  $R_{PD}$  as large as possible, and to have the amplitude of the signals input to the EEPROM close to the Vcc / GND amplitude level. (Note1) In this case, the guaranteed value of operating timing is guaranteed.

#### 4. SO Load Capacitance Condition

The load capacitance of the SO output pin affects the SO output delay characteristic. (Data output delay time, time from HOLDB to High-Z, output rise time, output fall time.). Make the SO load capacitance small to improve the output delay characteristic.

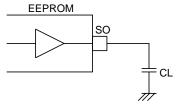


Figure 44. SO Load Dependency of Data Output Delay Time tPD

#### 5. Other Cautions

Make all wires from the microcontroller to EEPROM input pin the same length. This in order to prevent setup / hold violation to the EEPROM.

# Equivalent Circuit 1. Output Circuit

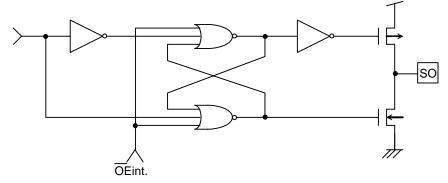


Figure 45. SO Output Equivalent Circuit

#### 2. Input Circuit

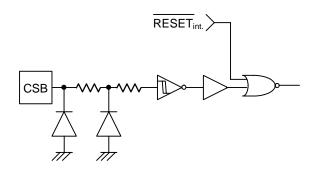


Figure 46. CSB Input Equivalent Circuit

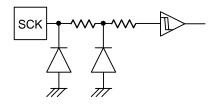


Figure 47. SCK Input Equivalent circuit

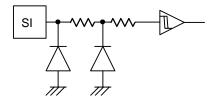


Figure 48. SI Input Equivalent Circuit

#### **Notes on Power ON/OFF**

#### 1. At Power ON/OFF set CSB="H" (=Vcc).

When CSB is "L", the IC goes into input accept status (active). If power is turned on in this status noises, etc. may cause malfunction or erroneous write. To prevent this, set CSB to "H" at power ON. (When CSB is in "H" status, all inputs are canceled.)

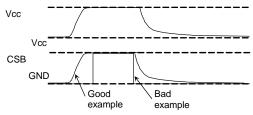


Figure 49. CSB Timing at Power ON/OFF

(Good example) CSB terminal is pulled up to Vcc.

After turning power off allow for 10ms or more before turning power on again. If power is turned on without observing this condition, the IC internal circuit may not be reset.

(Bad example) CSB terminal is "L" at power ON/OFF.

In this case, CSB always becomes "L" (active status), and the EEPROM may malfunction or perform an erroneous write due to noises, etc.

This can even occur when CSB input is High-Z.

#### 2. LVCC Circuit

LVCC (Vcc-Lockout) circuit prevents data rewrite action at low power and prevents erroneous write.

At LVCC voltage (Typ =1.9V) or below, it prevents data rewrite.

#### 3. P.O.R. Circuit

This IC has a POR (Power On Reset) circuit as countermeasure against erroneous write. After the POR operation is performed, write disable status is entered. The POR circuit is only valid when power is ON and does not work when power is OFF. When power is ON and the following recommended  $t_R$ ,  $t_{OFF}$ ,  $V_{bot}$  conditions are not satisfied, write enable status might be entered due to noise etc.

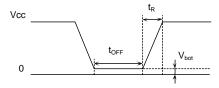


Figure 50. Rise Waveform

	Recommended Conditions for t <sub>R</sub> , t <sub>OFF</sub> , V <sub>bot</sub>						
t <sub>R</sub> t <sub>OFF</sub> V <sub>bot</sub>							
	10ms or below	10ms or higher	0.3V or below				
	100ms or below	10ms or higher	0.2V or below				

#### **Noise Countermeasures**

#### 1. Vcc Noise (Bypass Capacitor)

When noise or surge gets in the power source line, malfunction may occur. To prevent this, it is recommended to attach a bypass capacitor (0.1µF) between IC Vcc and GND, as close to IC as possible.

It is also recommended to attach a bypass capacitor between the board Vcc and GND.

#### 2. SCK Noise

When the rise time of SCK ( $t_{RC}$ ) is long and a there is a certain degree of noise, malfunction may occur due to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in the SCK input. The hysteresis width of this circuit is set to about 0.2V. If noises exist at the SCK input set the noise amplitude to 0.2Vp-p or below. Also, it is recommended to set the rise time of SCK ( $t_{RC}$ ) to 100ns or below. In case the rise time is 100ns or higher, sufficient noise countermeasures are needed. Clock rise, fall time should be as small as possible.

#### **Operational Notes**

#### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

#### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

#### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

#### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

#### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

#### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

#### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

#### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

#### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

#### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

#### **Operational Notes - continued**

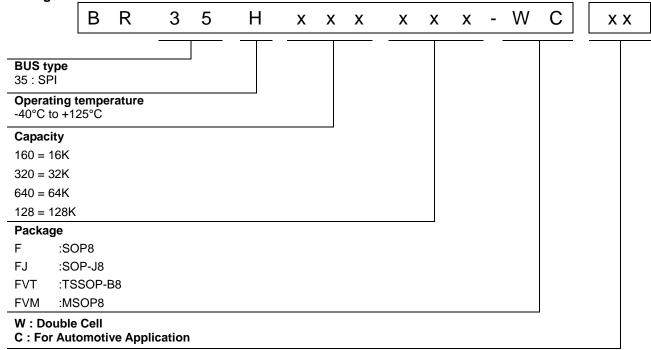
#### 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

#### 12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.





#### Packaging and forming specification

E2 : Embossed tape and reel

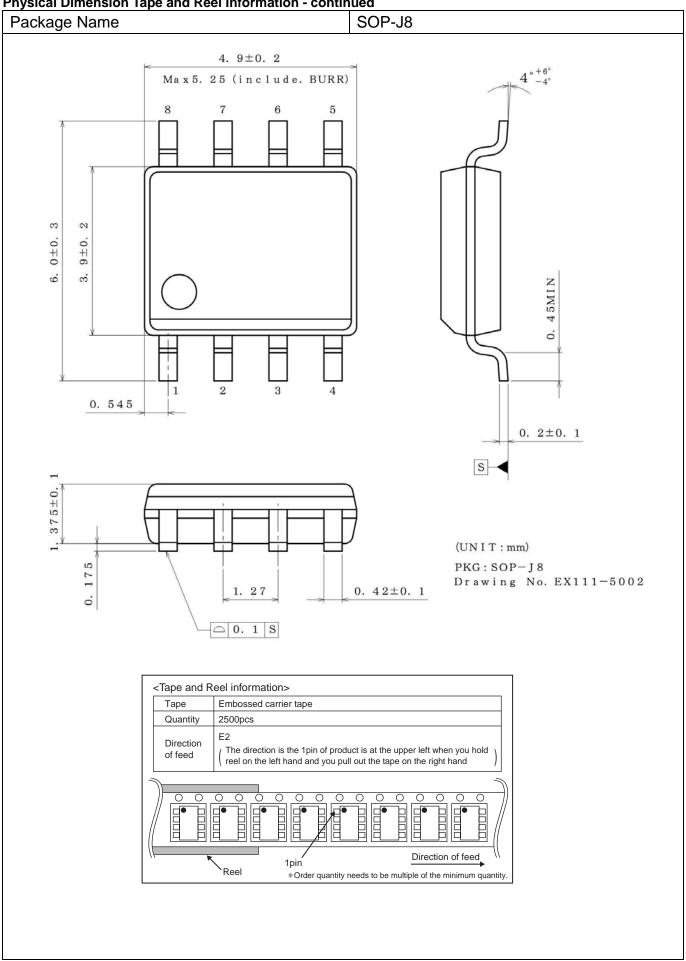
TR : Embossed tape and reel (MSOP8 package only)

#### Lineup

Consoitu	Pack	Package		
Capacity	Туре	Quantity		
	SOP8	Reel of 2500		
16K	SOP-J8	Reel of 2500		
ION	TSSOP-B8	Dool of 2000		
	MSOP8	Reel of 3000		
	SOP8	Reel of 2500		
2017	SOP-J8	Reel of 2500		
32K	TSSOP-B8	Deal of 2000		
	MSOP8	Reel of 3000		
	SOP8	Deal of 0500		
64K	SOP-J8	Reel of 2500		
	TSSOP-B8	Reel of 3000		
1001/	SOP8	Dool of 2500		
128K	SOP-J8	Reel of 2500		

**Physical Dimension, Tape and Reel Information** Package Name SOP8 5.  $0 \pm 0$ . 2 (Max 5.35 (include. BURR) 5 3 N +0. +0 4 3MIN 0 0 0.  $17^{+0.1}_{-0.05}$ 0.595 S +0 (UNIT : mm) PKG : SOP8 Drawing No.: EX112-5001-1 0 0. 42±0. 1 0. 1 S 1. 27 <Tape and Reel information> Embossed carrier tape Tape Quantity 2500pcs Direction The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand of feed Direction of feed \*Order quantity needs to be multiple of the minimum quantity.

Physical Dimension Tape and Reel Information - continued



BR35Hxxx-WC (16K 32K 64k 128k) Physical Dimension Tape and Reel Information - continued Package Name TSSOP-B8  $3.0\pm0.1$  $4^{\circ}\pm4^{\circ}$ (Max3. 35 (include. BURR)) 0 + 0 0. 525 1PIN MARK  $0.\ \ 1\ 4\ 5\ ^{+0.\ 0\ 5}_{-0.\ 0\ 3}$ S 1. 2MAX  $0.1\pm0.05$ □ 0. 08 S (UNIT: mm) PKG:TSSOP-B8 Drawing No. EX165-5002 0.  $245^{+0.05}_{-0.04}$   $\oplus$  0. 08  $\bigcirc$ 0.65 <Tape and Reel information> Tape Embossed carrier tape Quantity 3000pcs Direction The direction is the 1pin of product is at the upper left when you hold of feed reel on the left hand and you pull out the tape on the right hand

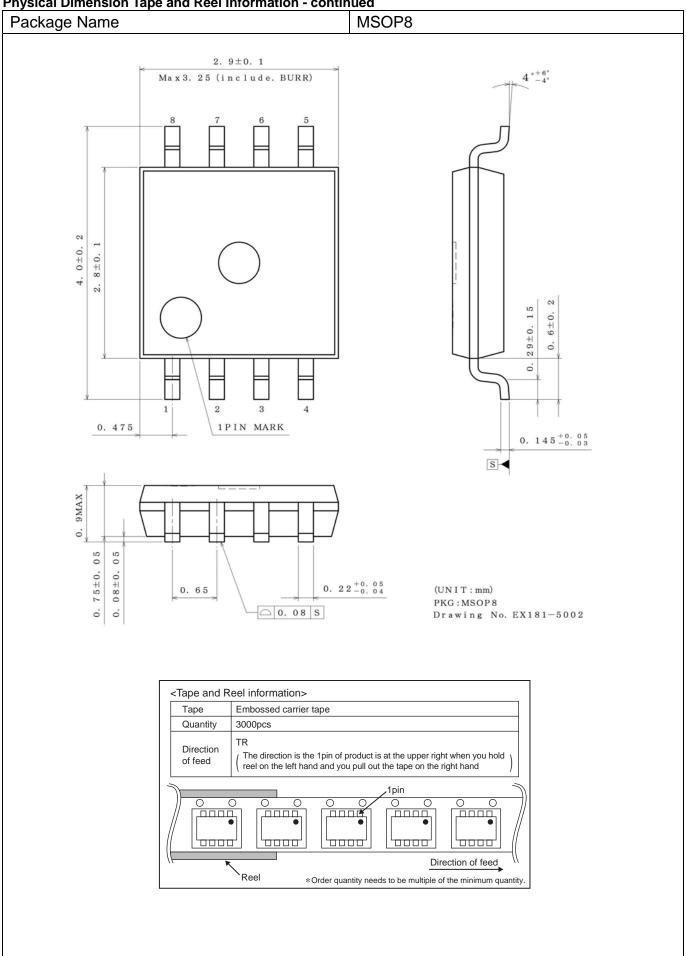
1pin

Reel

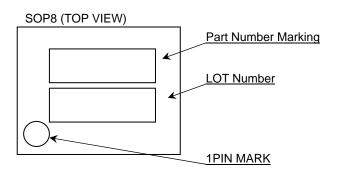
Direction of feed

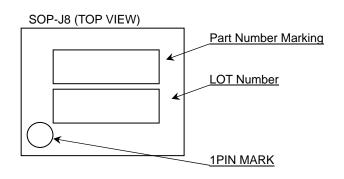
\*Order quantity needs to be multiple of the minimum quantity.

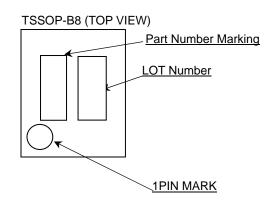
Physical Dimension Tape and Reel Information - continued

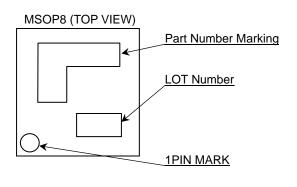


#### **Marking Diagrams (TOP VIEW)**









#### **Marking Information**

Capacity	Product Name Marking	Package Type	
	16H	SOP8	
16K	16H	SOP-J8	
ION	16H	TSSOP-B8	
	16H	MSOP8	
	32H	SOP8	
32K	32H	SOP-J8	
32N	32H	TSSOP-B8	
	32H	MSOP8	
	64H	SOP8	
64K	64H	SOP-J8	
	64H	TSSOP-B8	
128K	128H	SOP8	
IZON	128H	SOP-J8	

#### **Revision History**

Date	Revision	Changes	
10.Sep.2012	001	New Release	
31.Oct.2013	002	All Page Document converted to new format.	
22.Nov.2013	003	Modified a data retention years.	

# **Notice**

#### **Precaution on using ROHM Products**

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JÁPAN	USA	EU	CHINA	
CLASSⅢ	CLACCIII	CLASS II b	СГУССШ	
CLASSIV	CLASSⅢ	CLASSⅢ	CLASSⅢ	

- 2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
  - [a] Installation of protection circuits or other protective devices to improve system safety
  - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
- 3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
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  - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
  - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - [f] Sealing or coating our Products with resin or other coating materials
  - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

#### **Precaution for Mounting / Circuit board design**

- 1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

#### **Precautions Regarding Application Examples and External Circuits**

- If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
- You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

#### **Precaution for Electrostatic**

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

#### **Precaution for Storage / Transportation**

- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
- 2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

#### **Precaution for Product Label**

QR code printed on ROHM Products label is for ROHM's internal use only.

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#### **Precaution for Foreign Exchange and Foreign Trade act**

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