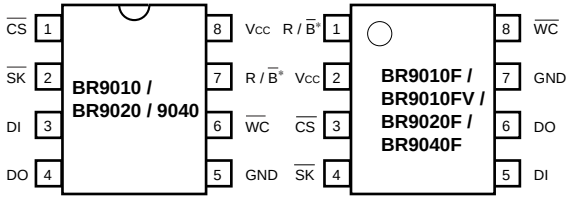
1, 2, and 4k bit EEPROMs for direct connection to serial ports

BR9010 / BR9010F / BR9010FV / BR9020 / BR9020F / BR9040 / BR9040F

●Features

- BR9010 / F / FV (1k bit): 64 words × 16 bits
  BR9020 / F (2k bit): 128 words × 16 bits
  BR9040 / F (4k bit): 256 words × 16 bits
- Single power supply operation
- Serial data input and output
- Automatic erase-before-write
- Low current consumption
  –1.5mA (max.) active current: 3V
  –2μA (max.) standby current: 3V
- Noise filter built into $\overline{SK}$ pin
- Compact DIP8, SOP8, SSOP-B8 packages (SSOP-B8 is available only with BR9010).
- 100,000 ERASE / WRITE cycles
- 10 years Data Retention
- Easily connects to serial port

●Pin assignments



∗ This pin is N.C. (non connection) on BR9010.

●Pin description

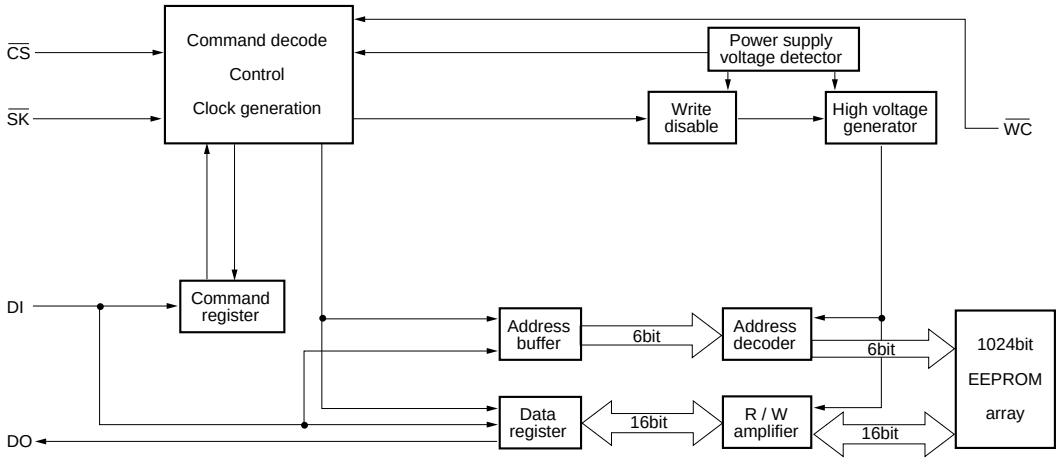
Pin name	Function
$\overline{CS}$	Chip select input
$\overline{SK}$	Serial data clock input
DI	Operating code, address, and serial data input
DO	Serial data output
GND	Reference voltage for all I / O, 0V
$\overline{WC}$	Write control input
R / $\overline{B}$	READY, $\overline{BUSY}$ status signal output
V_{CC}	Power supply connection

●Overview

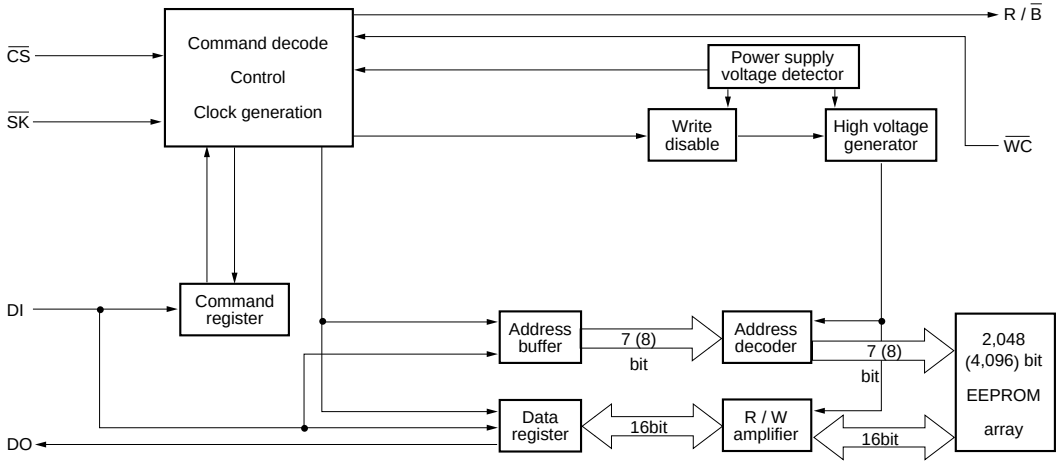
The BR90 series are serial EEPROMs that can be connected directly to a serial port and can be erased and written electrically. Writing and reading is performed in word units, using four types of operation commands. Communication occurs through $\overline{CS}$, $\overline{SK}$, DI, and DO pins, $\overline{WC}$ pin control is used to initiate a write disabled state, enabling these EEPROMs to be used as one-time ROMs. During writing, operation is checked via the internal status check.

●Block diagram

BR9010 / F / FV



BR9020 / F, **BR9040 / F**



✻ Values in parentheses are for the BR9040 / F.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits		Unit
Applied voltage	V_{CC}	– 0.3 ~ + 7.0		V
Power dissipation	P_d	DIP8	500*1	mW
		SOP8	350*2	
		SSOP-B8	300*3	
Storage temperature	T_{stg}	– 65 ~ + 125		°C
Operation temperature	T_{opr}	– 40 ~ + 85		°C
Input voltage	—	– 0.3 ~ V_{CC} + 0.3		V

* Reduced by 5.0mw*1 / 3.5mw*2 / 3.0mw*3 for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	2.7 to 5.5 (write)	V
		2.0 to 5.5 (read)	V
Input voltage	V_{IN}	0 ~ V_{CC}	V

●Electrical characteristics

BR9010 / F / FV: At 5V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage 1	V_{IL1}	—	—	0.3 × V_{CC}	V	DI Pin
Input high level voltage 1	V_{IH1}	0.7 × V_{CC}	—	—	V	DI Pin
Input low level voltage 2	V_{IL2}	—	—	0.2 × V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Input high level voltage 2	V_{IH2}	0.8 × V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Output low level voltage	V_{OL}	0	—	0.4	V	I_{OL} = 2.1mA
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	V_{CC}	V	I_{OH} = – 0.4mA
Input leak current	I_{LI}	– 1	—	1	µA	V_{IN} = 0V ~ V_{CC}
Output leak current	I_{LO}	– 1	—	1	µA	V_{OUT} = 0V ~ V_{CC} $\overline{CS}$ = V_{CC}
Consumption current during operation	I_{CC1}	—	—	2	mA	f = 1MHz tE / W = 10ms (WRITE)
	I_{CC2}	—	—	1	mA	f = 1MHz (READ)
Standby current	I_{SB}	—	—	3	µA	$\overline{CS}$, $\overline{SK}$, DI, $\overline{WC}$, = V_{CC} DO = OPEN
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz	—

BR9010 / F / FV: At 3V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 3V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage 1	V_{IL1}	—	—	0.3 × V_{CC}	V	DI Pin
Input high level voltage 1	V_{IH1}	0.7 × V_{CC}	—	—	V	DI Pin
Input low level voltage 2	V_{IL2}	—	—	0.2 × V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Input high level voltage 2	V_{IH2}	0.8 × V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Output low level voltage	V_{OL}	0	—	0.4	V	I_{OL} = 100µA
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	V_{CC}	V	I_{OH} = – 100µA
Input leak current	I_{LI}	–1	—	1	µA	V_{IN} = 0 ~ V_{CC}
Output leak current	I_{LO}	–1	—	1	µA	V_{OUT} = 0 ~ V_{CC} $\overline{CS}$ = V_{CC}
Consumption current during operation	I_{CC1}	—	—	1.5	mA	f = 1MHz tE / W = 15ms (WRITE)
	I_{CC2}	—	—	500	µA	f = 1MHz (READ)
Standby current	I_{SB}	—	—	2	µA	$\overline{CS}$, $\overline{SK}$, DI, $\overline{WC}$, = V_{CC} DO = OPEN
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz	—

○ Not designed for radiation resistance

●Electrical characteristics

●BR9020 / F: At 5V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage 1	V_{IL1}	—	—	0.3 × V_{CC}	V	DI Pin
Input high level voltage 1	V_{IH1}	0.7 × V_{CC}	—	—	V	DI Pin
Input low level voltage 2	V_{IL2}	—	—	0.2 × V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Input high level voltage 2	V_{IH2}	0.8 × V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Output low level voltage	V_{OL}	0	—	0.4	V	I_{OL} = 2.1mA
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	V_{CC}	V	I_{OH} = – 0.4mA
Input leak current	I_{LI}	– 1	—	1	µA	V_{IN} = 0V ~ V_{CC}
Output leak current	I_{LO}	– 1	—	1	µA	V_{OUT} = 0V ~ V_{CC} $\overline{CS}$ = V_{CC}
Consumption current during operation	I_{CC1}	—	—	2	mA	$f_{\overline{SK}}$ = 1MHz tE / W = 10ms (WRITE)
	I_{CC2}	—	—	1	mA	$f_{\overline{SK}}$ = 1MHz (READ)
Standby current	I_{SB}	—	—	3	µA	$\overline{CS}$, $\overline{SK}$, DI, $\overline{WC}$, = V_{CC} DO, R / $\overline{B}$ = OPEN
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz	—

●BR9020 / F: At 3V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 3V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage 1	V_{IL1}	—	—	0.3 × V_{CC}	V	DI Pin
Input high level voltage 1	V_{IH1}	0.7 × V_{CC}	—	—	V	DI Pin
Input low level voltage 2	V_{IL2}	—	—	0.2 × V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Input high level voltage 2	V_{IH2}	0.8 × V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Output low level voltage	V_{OL}	0	—	0.4	V	I_{OL} = 100µA
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	V_{CC}	V	I_{OH} = – 100µA
Input leak current	I_{LI}	– 1	—	1	µA	V_{IN} = 0V ~ V_{CC}
Output leak current	I_{LO}	– 1	—	1	µA	V_{OUT} = 0V ~ V_{CC} $\overline{CS}$ = V_{CC}
Consumption current during operation	I_{CC1}	—	—	1.5	mA	$f_{\overline{SK}}$ = 1MHz tE / W = 15ms (WRITE)
	I_{CC2}	—	—	500	µA	$f_{\overline{SK}}$ = 1MHz (READ)
Standby current	I_{SB}	—	—	2	µA	$\overline{CS}$, $\overline{SK}$, DI, $\overline{WC}$, = V_{CC} DO, R / $\overline{B}$ = OPEN
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz	—

●Electrical characteristics

●BR9040 / F: At 5V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage 1	V_{IL1}	—	—	0.3 × V_{CC}	V	DI Pin
Input high level voltage 1	V_{IH1}	0.7 × V_{CC}	—	—	V	DI Pin
Input low level voltage 2	V_{IL2}	—	—	0.2 × V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Input high level voltage 2	V_{IH2}	0.8 × V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Output low level voltage	V_{OL}	0	—	0.4	V	I_{OL} = 2.1mA
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	V_{CC}	V	I_{OH} = – 0.4mA
Input leak current	I_{LI}	– 1	—	1	µA	V_{IN} = 0V ~ V_{CC}
Output leak current	I_{LO}	– 1	—	1	µA	V_{OUT} = 0V ~ V_{CC} $\overline{CS}$ = V_{CC}
Consumption current during operation	I_{CC1}	—	—	2	mA	$f_{\overline{SK}}$ = 1MHz tE / W = 10ms (WRITE)
	I_{CC2}	—	—	1	mA	$f_{\overline{SK}}$ = 1MHz (READ)
Standby current	I_{SB}	—	—	3	µA	$\overline{CS}$, $\overline{SK}$, DI, $\overline{WC}$, = V_{CC} DO, R / $\overline{B}$ = OPEN
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz	—

●BR9040 / F: At 3V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 3V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input low level voltage 1	V_{IL1}	—	—	0.3 × V_{CC}	V	DI Pin
Input high level voltage 1	V_{IH1}	0.7 × V_{CC}	—	—	V	DI Pin
Input low level voltage 2	V_{IL2}	—	—	0.2 × V_{CC}	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Input high level voltage 2	V_{IH2}	0.8 × V_{CC}	—	—	V	$\overline{CS}$, $\overline{SK}$, $\overline{WC}$ Pin
Output low level voltage	V_{OL}	0	—	0.4	V	I_{OL} = 100µA
Output high level voltage	V_{OH}	V_{CC} – 0.4	—	V_{CC}	V	I_{OH} = – 100µA
Input leak current	I_{LI}	– 1	—	1	µA	V_{IN} = 0V ~ V_{CC}
Output leak current	I_{LO}	– 1	—	1	µA	V_{OUT} = 0V ~ V_{CC} $\overline{CS}$ = V_{CC}
Consumption current during operation	I_{CC1}	—	—	1.5	mA	$f_{\overline{SK}}$ = 1MHz tE / W = 15ms (WRITE)
	I_{CC2}	—	—	500	µA	$f_{\overline{SK}}$ = 1MHz (READ)
Standby current	I_{SB}	—	—	2	µA	$\overline{CS}$, $\overline{SK}$, DI, $\overline{WC}$, = V_{CC} DO, R / $\overline{B}$ = OPEN
$\overline{SK}$ frequency	f_{SK}	—	—	1	MHz	V_{CC} = 3.0 ~ 3.3V
		—	—	750	kHz	V_{CC} = 2.7 ~ 3.0V

●Operation timing characteristics

BR9010 / F / FV: At 5V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	t_{CSS}	200	—	—	ns
$\overline{CS}$ hold time	t_{CSH}	0	—	—	ns
Data setup time	t_{DIS}	150	—	—	ns
Data hold time	t_{DIH}	150	—	—	ns
DO rise delay time	t_{PD1}	—	—	350	ns
DO fall delay time	t_{PD0}	—	—	350	ns
Self-timing programming cycle	$t_{E/W}$	—	—	10	ms
$\overline{CS}$ minimum high level time	t_{CS}	1	—	—	µs
Time when DO goes High-Z (via $\overline{CS}$)	t_{OH}	0	—	400	ns
Data clock high level time	t_{WH}	450	—	—	ns
Data clock low level time	t_{WL}	450	—	—	ns
Write control setup time	t_{WCS}	0	—	—	ns
Write control hold time	t_{WCH}	0	—	—	ns

●BR9010 / F / FV: At 3V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 3V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	t_{CSS}	200	—	—	ns
$\overline{CS}$ hold time	t_{CSH}	0	—	—	ns
Data setup time	t_{DIS}	150	—	—	ns
Data hold time	t_{DIH}	150	—	—	ns
DO rise delay time	t_{PD1}	—	—	350	ns
DO fall delay time	t_{PD0}	—	—	350	ns
Self-timing programming cycle	$t_{E/W}$	—	—	15	ms
$\overline{CS}$ minimum high level time	t_{CS}	1	—	—	µs
Time when DO goes High-Z (via $\overline{CS}$)	t_{OH}	0	—	400	ns
Data clock high level time	t_{WH}	450	—	—	ns
Data clock low level time	t_{WL}	450	—	—	ns
Write control setup time	t_{WCS}	0	—	—	ns
Write control hold time	t_{WCH}	0	—	—	ns

●Operation timing characteristics

BR9020 / F / FV: At 5V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	t_{CSS}	200	—	—	ns
$\overline{CS}$ hold time	t_{CSH}	0	—	—	ns
Data setup time	t_{DIS}	150	—	—	ns
Data hold time	t_{DIH}	150	—	—	ns
DO rise delay time	t_{PD1}	—	—	350	ns
DO fall delay time	t_{PD0}	—	—	350	ns
Self-timing programming cycle	$t_{E/W}$	—	—	10	ms
$\overline{CS}$ minimum high level time	t_{CS}	1	—	—	µs
READY / $\overline{BUSY}$ display valid time	t_{SV}	—	—	1	µs
Time when DO goes High-Z (via $\overline{CS}$)	t_{OH}	0	—	400	ns
Data clock high level time	t_{WH}	450	—	—	ns
Data clock low level time	t_{WL}	450	—	—	ns
Write control setup time	t_{WCS}	0	—	—	ns
Write control hold time	t_{WCH}	0	—	—	ns

●BR9020 / F / FV: At 3V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 3V ± 10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	t_{CSS}	200	—	—	ns
$\overline{CS}$ hold time	t_{CSH}	0	—	—	ns
Data setup time	t_{DIS}	150	—	—	ns
Data hold time	t_{DIH}	150	—	—	ns
DO rise delay time	t_{PD1}	—	—	350	ns
DO fall delay time	t_{PD0}	—	—	350	ns
Self-timing programming cycle	$t_{E/W}$	—	—	15	ms
$\overline{CS}$ minimum high level time	t_{CS}	1	—	—	µs
READY / $\overline{BUSY}$ display valid time	t_{SV}	—	—	1	µs
Time when DO goes High-Z (via $\overline{CS}$)	t_{OH}	0	—	400	ns
Data clock high level time	t_{WH}	450	—	—	ns
Data clock low level time	t_{WL}	450	—	—	ns
Write control setup time	t_{WCS}	0	—	—	ns
Write control hold time	t_{WCH}	0	—	—	ns

●Operation timing characteristics

BR9040 / F: At 5V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 5V ± 10%)

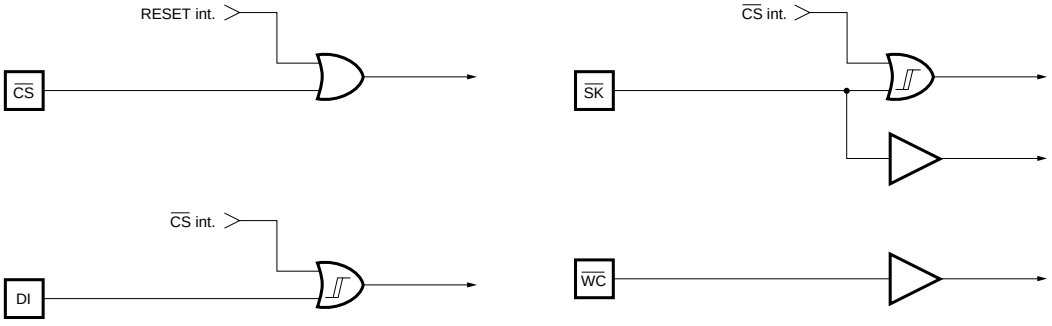
Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	t_{CSS}	200	—	—	ns
$\overline{CS}$ hold time	t_{CSH}	0	—	—	ns
Data setup time	t_{DIS}	150	—	—	ns
Data hold time	t_{DIH}	150	—	—	ns
DO rise delay time	t_{PD1}	—	—	350	ns
DO fall delay time	t_{PD0}	—	—	350	ns
Self-timing programming cycle	$t_{E/W}$	—	—	10	ms
$\overline{CS}$ minimum high level time	t_{CS}	1	—	—	µs
READY / $\overline{BUSY}$ display valid time	t_{SV}	—	—	1	µs
Time when DO goes High-Z (via $\overline{CS}$)	t_{OH}	0	—	400	ns
Data clock high level time	t_{WH}	500	—	—	ns
Data clock low level time	t_{WL}	500	—	—	ns
Write control setup time	t_{WCS}	0	—	—	ns
Write control hold time	t_{WCH}	0	—	—	ns

●BR9040 / F: At 3V (unless otherwise noted, Ta = – 40 to + 85°C, V_{CC} = 3V ± 10%)

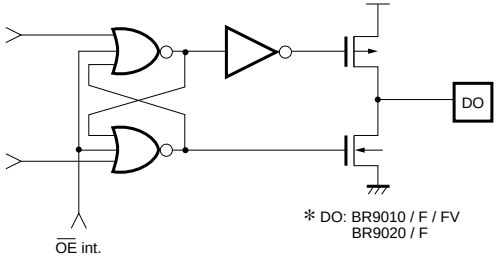
Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{CS}$ setup time	t_{CSS}	200	—	—	ns
$\overline{CS}$ hold time	t_{CSH}	0	—	—	ns
Data setup time	t_{DIS}	150	—	—	ns
Data hold time	t_{DIH}	150	—	—	ns
DO rise delay time V_{CC} = 3.0 ~ 3.3V	t_{PD1}	—	—	350	ns
DO fall delay time V_{CC} = 3.0 ~ 3.3V	t_{PD0}	—	—	350	ns
DO rise delay time V_{CC} = 2.7 ~ 3.0V	t_{PD1}	—	—	500	ns
DO fall delay time V_{CC} = 2.7 ~ 3.0V	t_{PD0}	—	—	500	ns
Self-timing programming cycle	$t_{E/W}$	—	—	15	ms
$\overline{CS}$ minimum high level time	t_{CS}	1	—	—	µs
READY / $\overline{BUSY}$ display valid time	t_{SV}	—	—	1	µs
Time when DO goes High-Z (via $\overline{CS}$)	t_{OH}	0	—	400	ns
Data clock high level time V_{CC} = 3.0 ~ 3.3V	t_{WH}	500	—	—	ns
Data clock low level time V_{CC} = 3.0 ~ 3.3V	t_{WL}	500	—	—	ns
Data clock high level time V_{CC} = 2.7 ~ 3.0V	t_{WH}	650	—	—	ns
Data clock low level time V_{CC} = 2.7 ~ 3.0V	t_{WL}	650	—	—	ns
Write control setup time	t_{WCS}	0	—	—	ns
Write control hold time	t_{WCH}	0	—	—	ns

●Input / output circuits

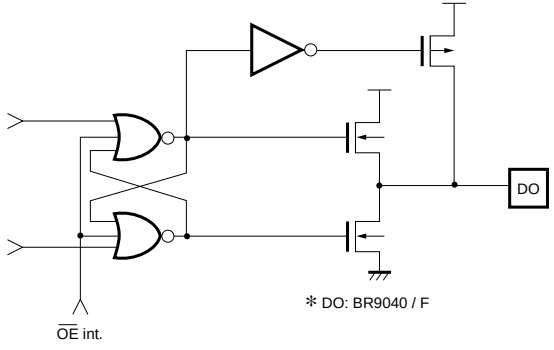
(1) Input circuits



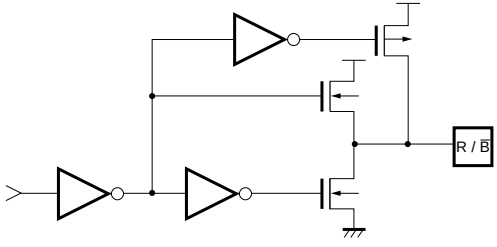
(2) Output circuits



✻ DO: BR9010 / F / FV
BR9020 / F



✻ DO: BR9040 / F



R / B: BR9020 / F, BR9040 / F

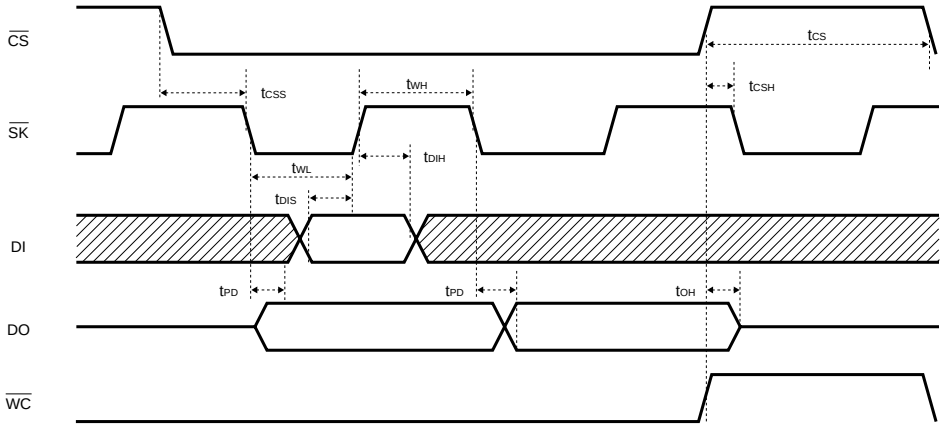
●Circuit operation

(1) Command mode

Command		Start bit	Operating code	Address	Data
Read	(READ)	1010	1000	A0 A1 A2 A3 A4 A5 (A6) ☆2 (A7) ☆1	
Write	(WRITE)	1010	0100	A0 A1 A2 A3 A4 A5 (A6) ☆2 (A7) ☆1	D0 D1—D14 D15
Erase / Write enabled	(EWEN)	1010	0011	✻ ✻ ✻ ✻ ✻ ✻ ✻ ✻	
Erase / Write disable	(EWDS)	1010	0000	✻ ✻ ✻ ✻ ✻ ✻ ✻ ✻	

✻ Either V_{IH} or V_{IL}
With BR9020 / F, ☆1 is '0'
With BR9010 / F / FV, ☆1 and 2 are '0'

(2) Timing chart



- Data is read in on the rising edge of SK. Data is output in synchronism with the SK falling edge.
- During a READ operation, data is output from DO in synchronization with the SK rise.
- WC is related to the write command only. Read, erase / write enable, erase / write disable commands can be executed irrespective of the state of WC.

(3) Writing enabled / disabled

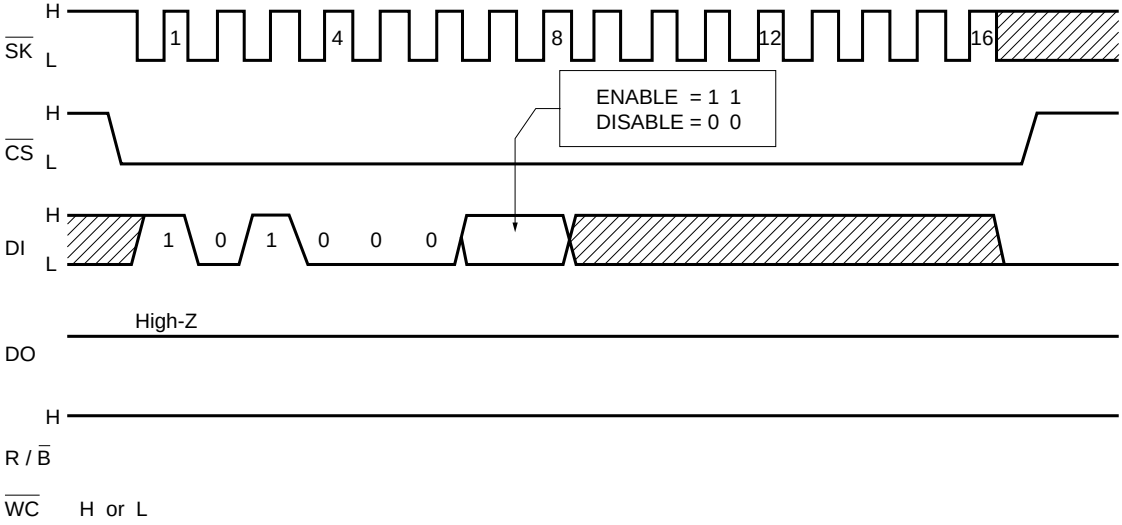


Fig.1

1) When the power supply is turned on, the latch used to acknowledge writing is reset in the same way as when the write disable command is executed. Before entering the write mode, the write enabled mode must first be entered. Once the write enabled mode has been recognized, it remains valid until the write disabled mode is entered, or the power supply is turned off.
2) The clock is no longer necessary after the first 16 clock pulses have been received. Any subsequent input will be ignored.
3) WC does not exist for either the write enabled or write disabled command, so WC may be either HIGH or LOW when the command is being input.
4) Commands are received in these modes by means of 8-bit operating codes. Please be aware that, after an operating code has been entered, commands will not be canceled even if CS is set to HIGH. (To cancel a command, either turn off the power supply, or input the command once again.)

●Circuit operation

(4) Read cycle

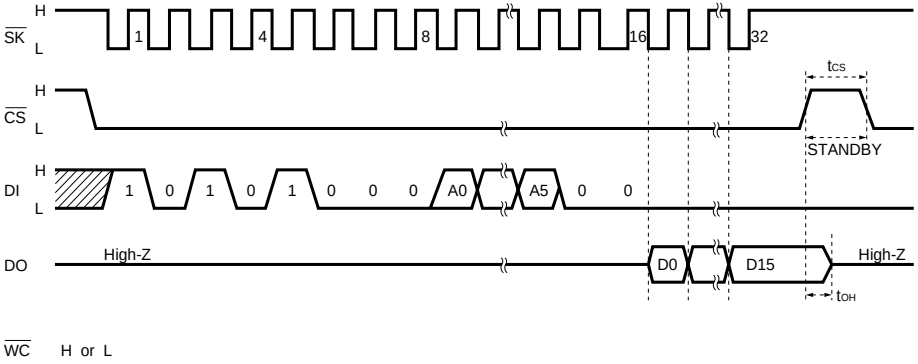


Fig.2 BR9010 / F / FV

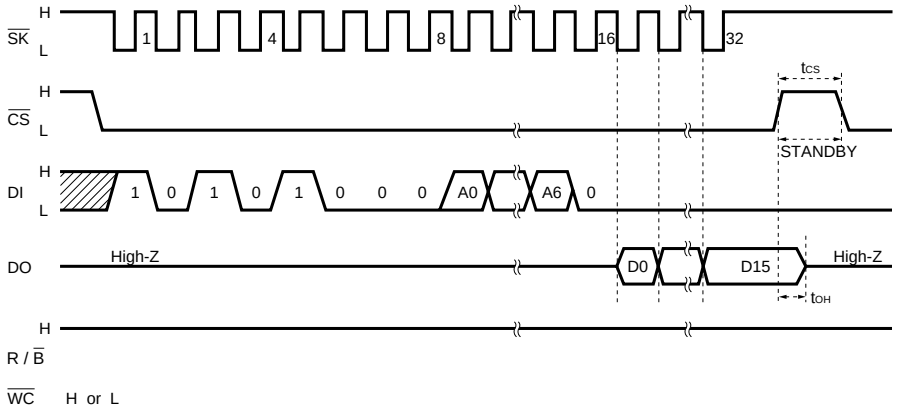


Fig.3 BR9020 / F

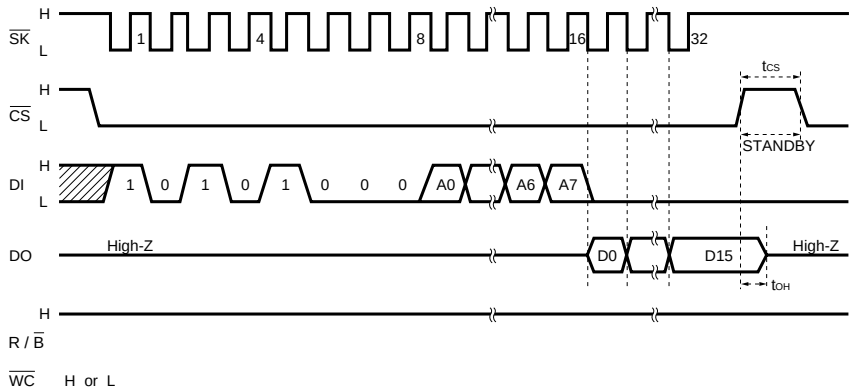


Fig.4 BR9040 / F

1) After the fall of the 16th clock pulse, 16-bit data is output from the DO pin in synchronization with the falling edge of the $\overline{SK}$ signal. (DO output changes at a time lag of t_{PD0}, t_{PD1} because of internal circuit delay following the falling edge of the $\overline{SK}$ signal. During the t_{PD0} and t_{PD1} timing, the t_{PD} time should be assured before data is read, to avoid the previous data being lost. See the synchronized data input / output timing chart in Fig. 1.)

●Circuit operation

(5) Writing cycle

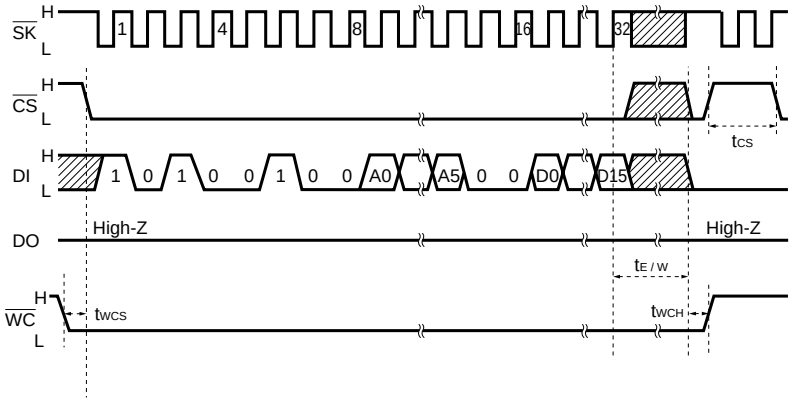


Fig.5 BR9010 / F / FV

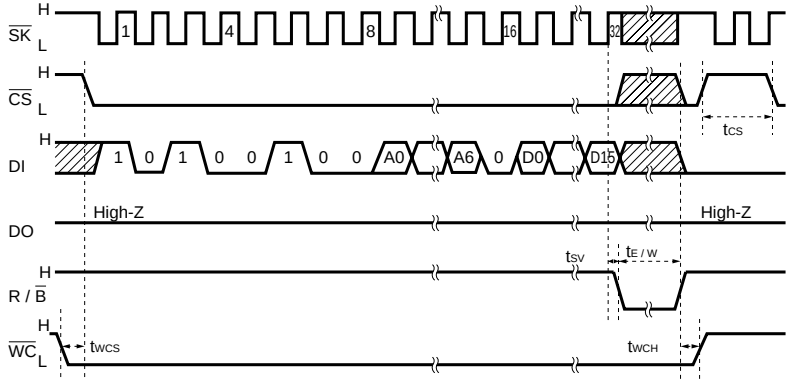


Fig.6 BR9020 / F

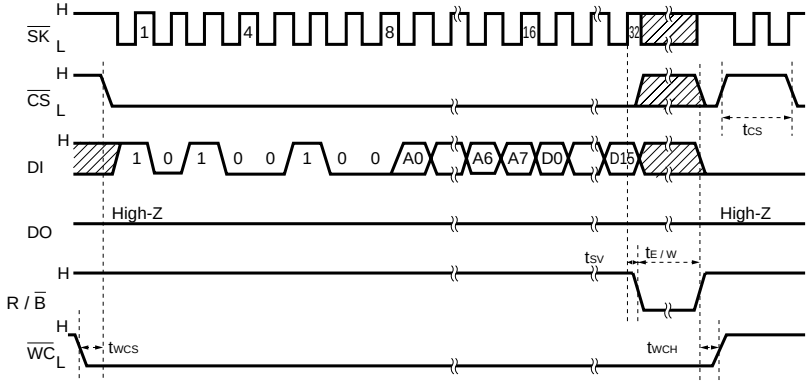


Fig.7 BR9040 / F

1) During input in the write mode, $\overline{CS}$ must be LOW, but once writing starts, $\overline{CS}$ may be either HIGH or LOW. However, if $\overline{CS}$ and $\overline{WC}$ share the same connection, both $\overline{CS}$ and $\overline{WC}$ should be set to LOW during writing operations.
   (If the $\overline{WC}$ pin is set to HIGH during a writing operation, writing will be forcibly interrupted at that point. If this happens, the data for that address may be lost, in which case it should be rewritten to that address.)
2) Following input of a write command, $\overline{CS}$ goes HIGH. If $\overline{CS}$ is then set to LOW, data will be received from $\overline{SK}$ and DI, because the command reception status has been entered.
   If $\overline{CS}$ remains LOW following command input, however, without first going HIGH, command input will be canceled until $\overline{CS}$ is set to HIGH.
3) Starting from the rising edge of the 32nd clock, the R / $\overline{B}$ pin goes LOW after RSV has elapsed.
4) The R / $\overline{B}$ pin is LOW during writing operations. (Following the rising edge of $\overline{SK}$ after the last data D15 has been read, the internal timer circuit is activated, and writing of data in the memory cell is automatically completed during $t_{E/W}$.) At this point, $\overline{SK}$ input may be either HIGH or LOW during $t_{E/W}$.
5) Following input of a write command, if $\overline{CS}$ falls while $\overline{SK}$ is LOW, the R / $\overline{B}$ status can be displayed from the DO pin. (See the section on READY / $\overline{BUSY}$ states.)

(6) READY / $\overline{BUSY}$ display (R / $\overline{B}$ pin and DO pin)

1) This display outputs the internal status signal; the R / $\overline{B}$ pin outputs the HIGH or LOW status at all times. The display can also be output from the DO pin. Following completion of the writing command, if $\overline{CS}$ falls while $\overline{SK}$ is LOW, either HIGH or LOW is output. (The display can also be output without using the R / $\overline{B}$ pin, leaving it open.)
2) When writing data to a memory cell, the READY / $\overline{BUSY}$ display is output from the rise of the 32nd clock pulse of the $\overline{SK}$ signal after t_{SV}, from the R / $\overline{B}$ pin.
   R / $\overline{B}$ display = LOW: writing in progress
   (The internal timer circuit is activated, and after the $t_{E/W}$ timing has been created, the timer circuit stops automatically. Writing of data to the memory cell is done during the $t_{E/W}$ timing, during which time other commands cannot be received.)
   R / $\overline{B}$ display = HIGH: command standby state
   (Writing of data to the memory cell has been completed and the next command can be received.)

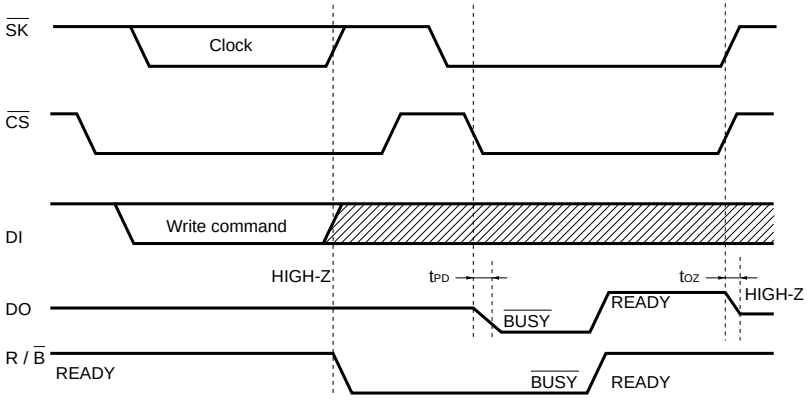


Fig.8 R / $\overline{B}$ status output timing

●Operation notes

(1) Turning the power supply on and off

1) When the power supply is turned on and off, $\overline{CS}$ should be set to HIGH (= V_{CC}).

2) When $\overline{CS}$ is LOW, the command input reception state (active) is entered. If the power supply is turned on in this state, erroneous operations and erroneous writing can occur because of noise and other factors. To avoid this, make sure $\overline{CS}$ is set to HIGH (= V_{CC}) before turning on the power supply.

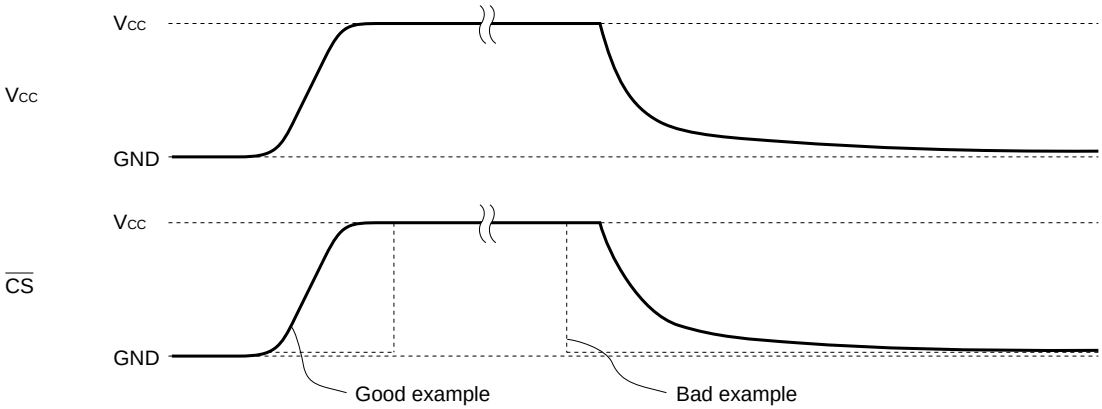
(Good example) Here, the $\overline{CS}$ pin is pulled up to V_{CC}.

When turning off the power supply, wait at least 10msec before turning it on again. Failing to observe this condition can result in the internal circuit failing to be reset when the power supply is turned on.

(Bad example) $\overline{CS}$ is LOW when the power supply is turned on or off

In this case, because $\overline{CS}$ remains LOW, the EEPROM may perform erroneous operations or write erroneous data because of noise or other factors.

∗ Please be aware that the case shown in this example can also occur if $\overline{CS}$ input is HIGH-Z.



(2) Noise countermeasures

1) $\overline{SK}$noise

If noise occurs at the rise of the $\overline{SK}$ clock input, the clock is assumed to be excessive, and this can cause malfunction because the bits are out of alignment.

2) $\overline{WC}$ noise

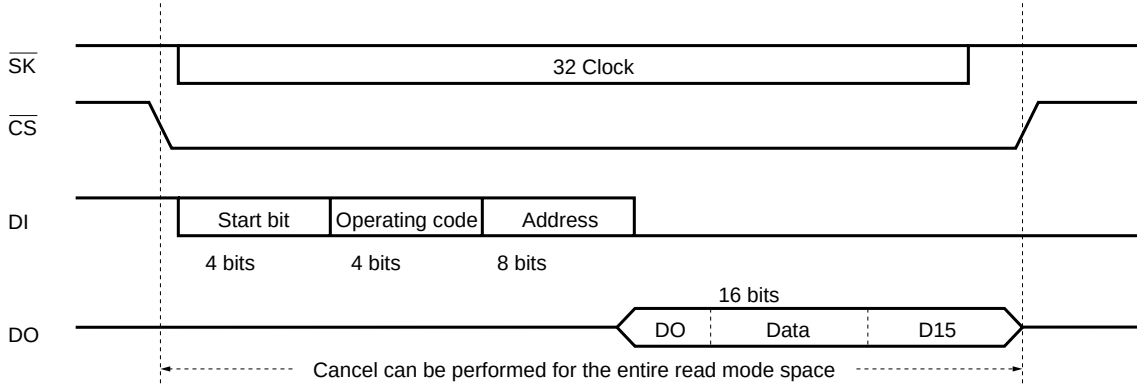
During a writing operation, noise at the $\overline{WC}$ pin can be erroneously judged to be data, and this can cause writing to be forcibly interrupted.

3) V_{CC} noise

Noise and surges on the power supply line can cause malfunction. We recommend installing a bypass capacitor between the power supply and ground to eliminate this problem.

(3) Canceling modes

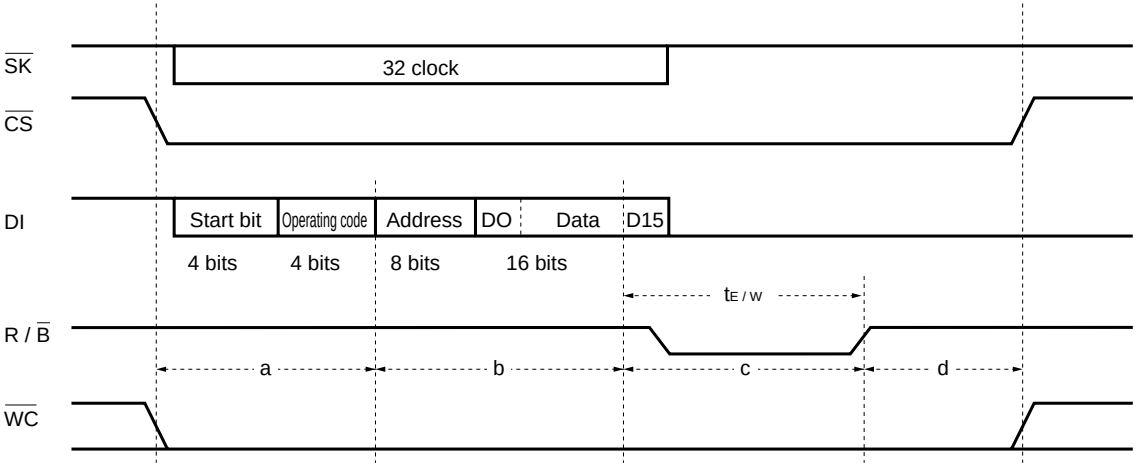
1) Read commands



WC H or L

Cancellation method: CS HIGH

2) Write commands



Canceling methods

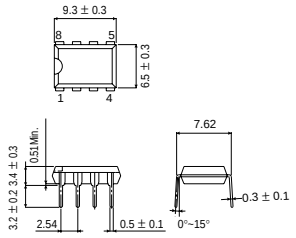
a: Canceled by setting CS HIGH. The WC pin is not involved.

b: If the WC pin goes HIGH for even a second, writing is forcibly interrupted. Cancellation occurs even if the CS pin is HIGH. At this point, data has not been written to the memory, so the data in the designated address has not yet been changed.

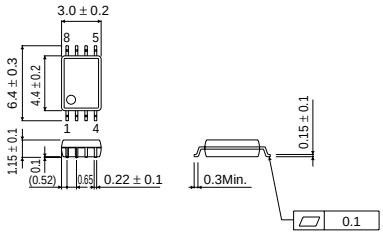
c: The operation is forcibly canceled by setting the WC pin to HIGH or turning off the power supply (although we do not recommend using this method). The data in the designated address is not guaranteed and should be written once again.

d: If CS is set to HIGH while the R / B signal is HIGH (following the $t_{E/W}$ timing), the IC is reset internally, and waits for the next command to be input.

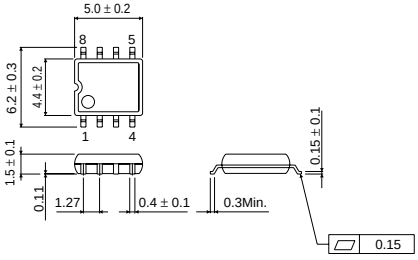
●External dimensions (Units: mm)



DIP8



SSOP-B8



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