

- ◇ STRUCTURE Silicon Monolithic Integrated Circuit
- ◇ PRODUCT SPI BUS Serial EEPROMs
- ◇ SERIES SIGNATURE SERIES
- ◇ FAMILY BR95□□0 family
- ◇ TYPE Supply voltage 2.5V~5.5V/Operating temperature -40°C~+85°Ctype
- ◇ PART NUMBER BR95□□0-W□□6TP

PART NUMBER	PACKAGE	DENSITY
BR95010-WMN6TP	SO8 narrow	1Kbit
BR95020-WMN6TP		2Kbit
BR95040-WMN6TP		4Kbit
BR95080-WMN6TP		8Kbit
BR95160-WMN6TP		16Kbit
BR95320-WMN6TP		32Kbit
BR95640-WMN6TP		64Kbit
BR95010-WDW6TP	TSSOP8	1Kbit
BR95020-WDW6TP		2Kbit
BR95040-WDW6TP		4Kbit
BR95080-WDW6TP		8Kbit
BR95160-WDW6TP		16Kbit
BR95010-WDS6TP	TSSOP8 3 × 3mm ²	1Kbit
BR95020-WDS6TP		2Kbit
BR95040-WDS6TP		4Kbit

◇ FEATURES

- SPI BUS interface
- Endurance : 1,000,000 erase/write cycles
- Data retention : 40 years
- Initial Data: Memory array FFh

◇ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
T _{STG}	Storage Temperature	-65	125	°C
V _I	Input Voltage	-0.3	V _{CC} +0.3	V
V _{CC}	Supply Voltage	-0.3	6.5	V

◇ POWER DISSIPATION (Ta=25°C)

PACKAGE	Rating	Unit
SO8 narrow	450 *1	mW
TSSOP8	330 *2	mW
TSSOP8 3 × 3mm ²	310 *3	mW

* Degradation is done at 4.5mW/°C(*1), 3.3mW/°C(*2), 3.1mW/°C(*3) for operation above 25°C

◇ DC OPERATING CHARACTERISTICS

(Unless otherwise specified Ta=-40~85°C, Vcc=2.5~5.5V)

Parameter	Symbol	Min.	Max.	Unit	Test condition
Input Leakage Current	I _I	-	±2	μA	V _I =V _{SS} or V _{CC}
Output Leakage Current	I _O	-	±2	μA	$\bar{S}=V_{CC}, V_{OUT}=V_{SS}$ or V _{CC}
Supply Current (BR95010/020/040/080/160)	I _{CC}	-	2	mA	V _{CC} =2.5V, f _C =5MHz, t _W =5ms
Supply Current (BR95320/640)		-	3	mA	V _{CC} =2.5V, f _C =5MHz, t _W =5ms
Supply Current (Standby Power mode)	I _{CC1}	-	1	μA	$\bar{S}=V_{CC}, V_{CC}=2.5V, V_{IN}=V_{SS}$ or V _{CC}
Input Low Voltage	V _{IL}	-0.3	0.3V _{CC}	V	
Input High Voltage	V _{IH}	0.7V _{CC}	V _{CC} +0.3	V	
Output Low Voltage	V _{OL}	-	0.4	V	I _{O1} =1.5mA, V _{CC} =2.5V
Output High Voltage	V _{OH}	0.8V _{CC}	-	V	I _{O1} =-0.4mA, V _{CC} =2.5V

○ This product is not designed for protection against radioactive rays.

◇ AC OPERATING CHARACTERISTICS

(Unless otherwise specified Ta=-40~85°C, Vcc=2.5~5.5V, C_L=100pF)

Parameter	Symbol	Min.	Max.	Unit
Clock Frequency	f _C	-	5	MHz
\bar{S} Active Setup Time	t _{SLCH}	90	-	ns
\bar{S} Not Active Setup Time	t _{SHCH}	90	-	ns
\bar{S} Deselect Time	t _{SHSL}	100	-	ns
\bar{S} Active Hold Time	t _{CHSH}	90	-	ns
\bar{S} Not Active Hold Time	t _{CHSL}	90	-	ns
Clock High Time	t _{CH} *1	90	-	ns
Clock Low Time	t _{CL} *1	90	-	ns
Clock Rise Time	t _{CLCH} *2	-	1	μs
Clock Fall Time	t _{CHCL} *2	-	1	μs
Data In Setup Time	t _{DVCH}	20	-	ns
Data In Hold Time	t _{DCHX}	40	-	ns
Clock Low Hold Time after HOLD not Active	t _{HCHL}	70	-	ns
Clock Low Hold Time after HOLD Active	t _{HCH}	40	-	ns
Clock High Set-up Time before HOLD Active (BR95010/020/040)	t _{CHHL}	60	-	ns
Clock Low Set-up Time before HOLD Active (BR95080/160/320/640)	t _{CLHL}	0	-	ns
Clock High Set-up Time before HOLD not Active (BR95010/020/040)	t _{CHHH}	60	-	ns
Clock Low Set-up Time before HOLD not Active (BR95080/160/320/640)	t _{CLHH}	0	-	ns
Output Disable Time	t _{SHOZ} *2	-	100	ns
Clock Low to Output Valid	t _{CLQV}	-	70	ns
Output Hold Time	t _{CLQX}	0	-	ns
Output Rise Time	t _{OLQH} *2	-	50	ns
Output Fall Time	t _{OHQL} *2	-	50	ns
HOLD High to Output Valid	t _{HIOV}	-	70	ns
HOLD Low to Output High-Z	t _{HLOZ} *2	-	100	ns
Write Time	t _W	-	5	ms

*1 t_{CH}+t_{CL} ≥ 1/f_C

*2 This parameter is not 100% tested.

◇ BLOCK DIAGRAM

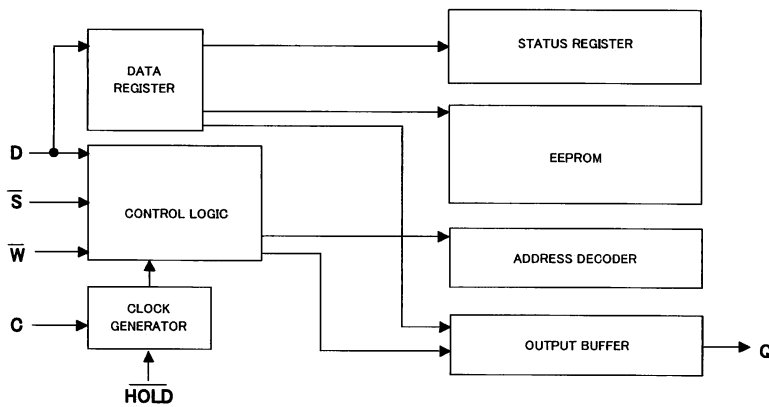


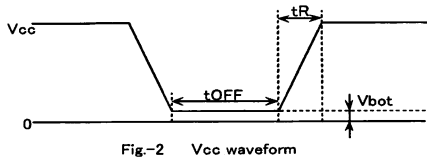
Fig.-1 BLOCK DIAGRAM

◇ PIN No., PIN NAME

PIN No.	PIN NAME
1	\bar{S}
2	Q
3	\bar{W}
4	V _{SS}
5	D
6	C
7	$\overline{\text{HOLD}}$
8	V _{CC}

◇NOTES FOR POWER SUPPLY

In order to prevent an inadvertent write, the device has the feature of P.O.R.
 After the power is on, the device is in the write disable mode. P.O.R. works only during power up. The noise may force the device write enable mode with \overline{S} ="H" during power ON/OFF. In the case of power up, keep the following conditions to ensure to make the function of P.O.R.



◇RECOMMENDED CONDITIONS OF tR, tOFF, Vbot

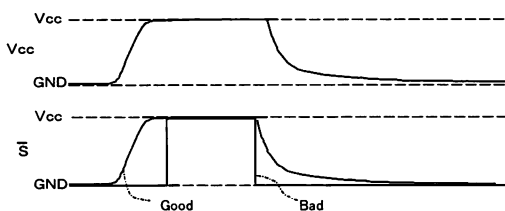
tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

Please keep \overline{S} "H" during power ON/OFF.

The device is an active state during \overline{S} is low. The extraordinary function or data collaption may occur because of noise etc., if power-up is done with \overline{S} "L". In order to prevent above errors from happening, keep \overline{S} "H" (=Vcc) during power ON. (The device does not receive any command during \overline{S} is high.)

It may continue at low Vcc by capacitance of Vcc line during power off.

Please keep \overline{S} "H" during power off because of the device may make malfunction and inadvertent write.



(Good example)
 \overline{S} follows Vcc. (\overline{S} is pull up to Vcc)

(Bad example)
 \overline{S} is low during power ON/OFF.
 Please take more than 10ms between power ON and power OFF, or the internal circuit is not always reset.

Fig.-3 \overline{S} TIMING DURING POWER ON/OFF

◇CAUTIONS ON USE

(1) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) Vss electric potential

Set the voltage of Vss terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of Vss terminal.

(3) Thermal design

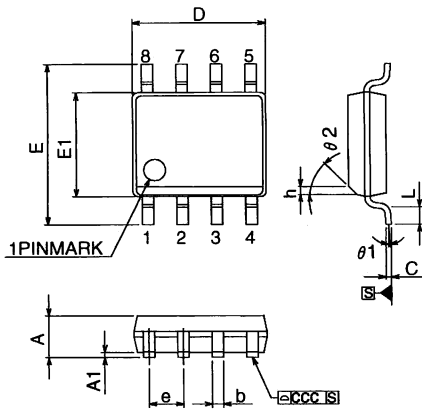
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and Vss owing to foreign matter, LSI may be destructed.

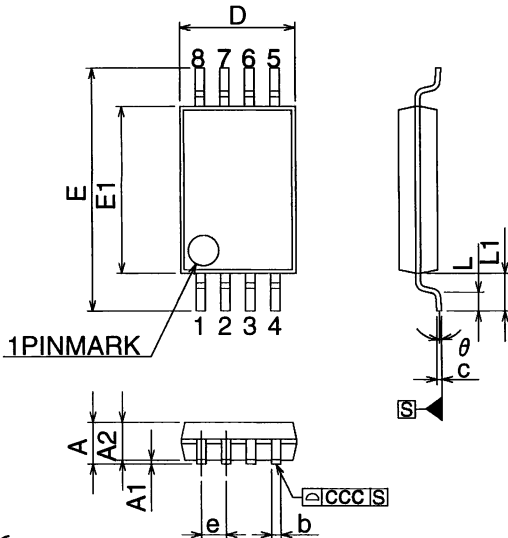
(5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇ PHYSICAL DIMENSION



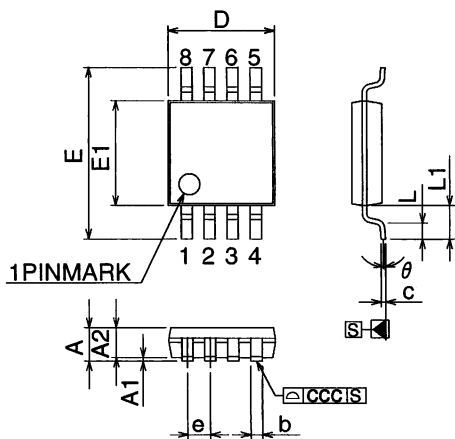
- Notes
- 1.This drawing is subject to change without notice.
 - 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 - 3.Reference JEDEC MS-012 variation AA.

Fig.-4 SO8 narrow Package Outline



- Notes
- 1.This drawing is subject to change without notice.
 - 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 - 3.Reference JEDEC MO-153.

Fig.-5 TSSOP8 Package Outline



- Notes
- 1.This drawing is subject to change without notice.
 - 2.Body dimensions do not include mold flash or protrusion, or gate burns.
 - 3.Reference JEDEC MO-187 variation AA.

Fig.-6 TSSOP8 3 x 3mm² Package Outline

◇ SO8 narrow Package size data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	1.35	1.75	-	0.053	0.069
A1	-	0.10	0.25	-	0.004	0.010
b	-	0.33	0.51	-	0.013	0.020
c	-	0.19	0.25	-	0.007	0.010
D	-	4.80	5.00	-	0.189	0.197
e	1.27	-	-	0.050	-	-
E	-	5.80	6.20	-	0.228	0.244
E1	-	3.80	4.00	-	0.150	0.157
L	-	0.40	1.27	0.050	0.016	0.050
theta 1	-	0°	8°	-	0°	8°
ccc	-	-	0.10	-	-	0.004
h	-	0.25	0.50	-	0.010	0.020
theta 2	45°	-	-	45°	-	-

◇ TSSOP8 Package size data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.200	-	-	0.0472
A1	-	0.050	0.150	-	0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b	-	0.190	0.300	-	0.0075	0.0118
c	-	0.090	0.200	-	0.0035	0.0079
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000	-	-	0.0394	-	-
ccc	-	-	0.100	-	-	0.0039
theta	-	0°	8°	-	0°	8°

◇ TSSOP8 3 x 3mm² Package size data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	-	-	1.100	-	-	0.0433
A1	-	0.050	0.150	-	0.0020	0.0059
A2	0.850	0.750	0.950	0.0335	0.0295	0.0374
b	-	0.250	0.400	-	0.0098	0.0157
c	-	0.120	0.230	-	0.0047	0.0091
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	-	-	0.0256	-	-
E	4.900	4.650	5.150	0.1929	0.1831	0.2028
E1	3.000	2.900	3.100	0.1181	0.1142	0.1220
L	0.550	0.400	0.700	0.0217	0.0157	0.0276
L1	0.950	-	-	0.0374	-	-
ccc	-	-	0.100	-	-	0.0039
theta	-	0°	6°	-	0°	6°

Notes

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