For Home Electronics and Security Devices Camera Image Processor Series

Camera Image Processor Compatible with MPEG4 Video

BU6582GVW

No.09061EBT03

●Description

BU6582GVW is a camera image processor compatible with MPEG4 movies.
MPEG4 compatibility enables seamless video transmission with other devices.

●Features

1)Built-in Camera Module Interface

SXGA size (1280×1024) for input of image data up to 15 fps and VGA size (640×480) for input of image data up to 30fps (zooming function available).
Input data format for YUV=4:2:2, RGB=4:4:4.
Filter processing (image processing) to input images (2 gradations / gray scale / sepia / emboss / edge enhancement/ negative).
Multi-step size reduction down to 1/16 in X- and Y-direction possible.
Cutting out into an arbitrary size after resizing.
D range enlargement processing of Y (brightness) available in YUV color space to cut images.
Cut images to be stored into an arbitrary position in frame memory in YUV=4:2:2 or RGB=5:6:5 format.
2-line serial interface built in for camera module control.
Image processing of data written by HOST CPU in YUV or RGB format possible through camera module interface.

2)Built-in frame memory / JPEG code memory

Image frame memory built in (160KB to store 1 frame of 320 × 240@16bit/pixel during normal mode or 50KB/frame to store 2 frames of 176 × 144@16bit/pixel during MPEG4/H.263 mode).
Display area settable to an arbitrary LCD size.
Data to be stored into image frame memory in YUV=4:2:2 or RGB=5:6:5 (16bit/pixel) format.
Mask data to be stored into mask frame memory in 1bit/2pixels in YUV=4:2:2 or 1bit/1pixels in RGB=5:6:5 format.
An arbitrary position of frame memory to be updated to camera image according to mask memory.
Image frame memory accessible from host CPU (access available both in RGB and YUV).
Rectangular writing function and rectangular reading function for transparent color to image frame memory.
Frame memory usable as JPEG code memory (160KB) to store JPEG compressed images.
Frame memory usable as a ring buffer for JPEG code of 160KB or more.

3)Built-in LCD controller interface

Built-in input/output interface to LCD controller
For display colors of 262144 colors / 65536 colors / 4096 colors.
Up to 2 LCD module controllers controllable.
Arbitrary rectangular selection in frame memory to be transferred to LCD controller.
Multi-step scaling process in the range of 1/4× to 2× in X- and Y-direction is available to display images from the frame memory to the LCD.

4)Built-in MPEG4 Codec

ISO/IEC14496 conforming simple profile level 0.

ISO/IEC 14496 conforming simple profile level 1 (4 objects can be supported in decode mode).

ITU-T H.263 conforming profile 0 level 10.

ITU-T H.263 conforming profile 3 level 10.

MAX QCIF (176x144), SQCIF (128x96), 96x80.

For input image data up to 15fps.

5)Built-in JPEG CODEC

ISO/IEC10918 conforming base line method.

・Compression

For YUV=4:2:2 only.

Quantization table selectable from 20 built-in tables.

・Decompression

For YUV=4:4:4, 4:2:2(horizontal sub-sampling), 4:2:0, 4:1:1(horizontal sub-sampling), and gray scale.

6) Built-in HOST CPU interface

Adaptable to 16bit bus interface.

Read/ write access to frame memory.

Read/ write access to internal registers (Indirect access with a index register as the address).

Read/ write access to the LCD controller: Parallel/Serial (Direct access available via the LCD interface).

7) Extended overlay function

Supporting overlay of icon-data/font-data of up to two points during LCD data transfer.

Both icon-data and font-data corresponding to 65536 display colors. Possible to setting transparent colors.

8) LED interface, GIO function

Built-in PWM output of 4 systems for 3 color LED controls and white LED control.

A total of 19 pins available for the GIO function (7 out of the 19 pins can be shared for other functions.)

9) Clock generation, power management function

Oscillation circuit configuration by XIN and XOUT terminals, or clock input from XIN terminal available.

Built-in PLL.

Clock control of IC inside in unit of block (suspend mode available).

10) Key interfaces built in

3 systems of key interfaces built in. Interruption to be generated at key input.

Useable for removing software chattering.

∗ Data is prepared separately about each register setup. Please refer to the Development Scheme on page 14.

System 1 (VDDIO1)	System 2 (VDDIO2)
P3-P10(D15-8), P13-P14(SGIO3-2), P17(SGIO1), P19(D7), P21-29(D6-5,SGIO0,D4-0,A2), P33-P36(A1,CSB,WRB,RDB), P118-P119(XOUT,XIN)	P37(INT), P39-P43(SGIO11-10, CAMVS, CAMHS, CAMD0), P46-P47(CAMD1-2), P49-P53(SGIO9, CAMD3, GIO2/KEY2, CAMD4, CAMD5), P55-P56(CAMD6, CAMD7), P58-P59(CAMCKI-CAMCKO), P63-P68(SDA, SDC, LEDCNT/GIO1, PWM1/GIO3, PWM2/GIO4, PWM3/GIO5), P70-P75(VD/GIO6, LCDCS1B, LCDCS2B, KEY0, LCDD16, SGIO8), P77-P79(LCDWRB, SGIO7, LCDRDB), P81-P82(LCDA0, SGIO4), P84-P88(LCDD0-4), P92-98(LCDD5, LCDD6/SCL, SGIO6, LCDD7/SI, SGIO5, TEST, LCSS17), P100(LCDD8), P103-105(LCDD9-11), P107-109(LCDD12, KEY1, LCDD13), P111-P114(LCDD14-15, RESETB, PWM0/GIO0)

●Application

Security camera, Intercom with camera, Drive recorder, and Web camera etc.

●Lineup

Parameter	Power source voltage IO1:HOST CPU I/F IO2:Camera, LCD	Camera interface	HOST CPU interface	LCD interface	Codec [Image]	Multimedia interface	Package
BU6582GVW	1.45-1.55V(V_{DD}Core) 1.7-3.15V(V_{DD}IO1) 2.55-3.15V(V_{DD}IO2)	Supported up to 1.3M pixels. (1280×1024)	16bit bus 80 systems CPU Interface	Supported up to QVGA (320×240)	MPEG4/H.263 Codec 1.3M pixels JPEG Codec Motion-JPEG	-	SBGA120W080

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Applied power source voltage 1	VDDIO1	-0.3～+4.2	V
Applied power source voltage 2	VDDIO2	-0.3～+4.2	V
Applied power source voltage 3	VDD	-0.3～+2.1	V
Input voltage1	VIN1	-0.3～VDDIO1+0.3	V
Input voltage 2	VIN2	-0.3～VDDIO2+0.3	V
Storage temperature range	Tstg	-40～+150	℃
Power dissipation	PD	380	mW

∗ IC only. In the case exceeding 25ºC, 3.8mW should be reduced at the rating 1ºC.

●Recommended operating range

Parameter	Symbol	Rating	Unit
Applied power source voltage 1（IO）	VDDIO1	1.70～3.15(Typ:1.80V)	V
Applied power source voltage 2（IO）	VDDIO2	2.55～3.15(Typ:2.85V)	V
Applied power source voltage 3（CORE）	VDD	1.45～1.55(Typ:1.50V)	V
Input voltage range	VIN-VDDIO1,2	0～VDDIO	V
Operating temperature range	Topr	-30～+85	℃

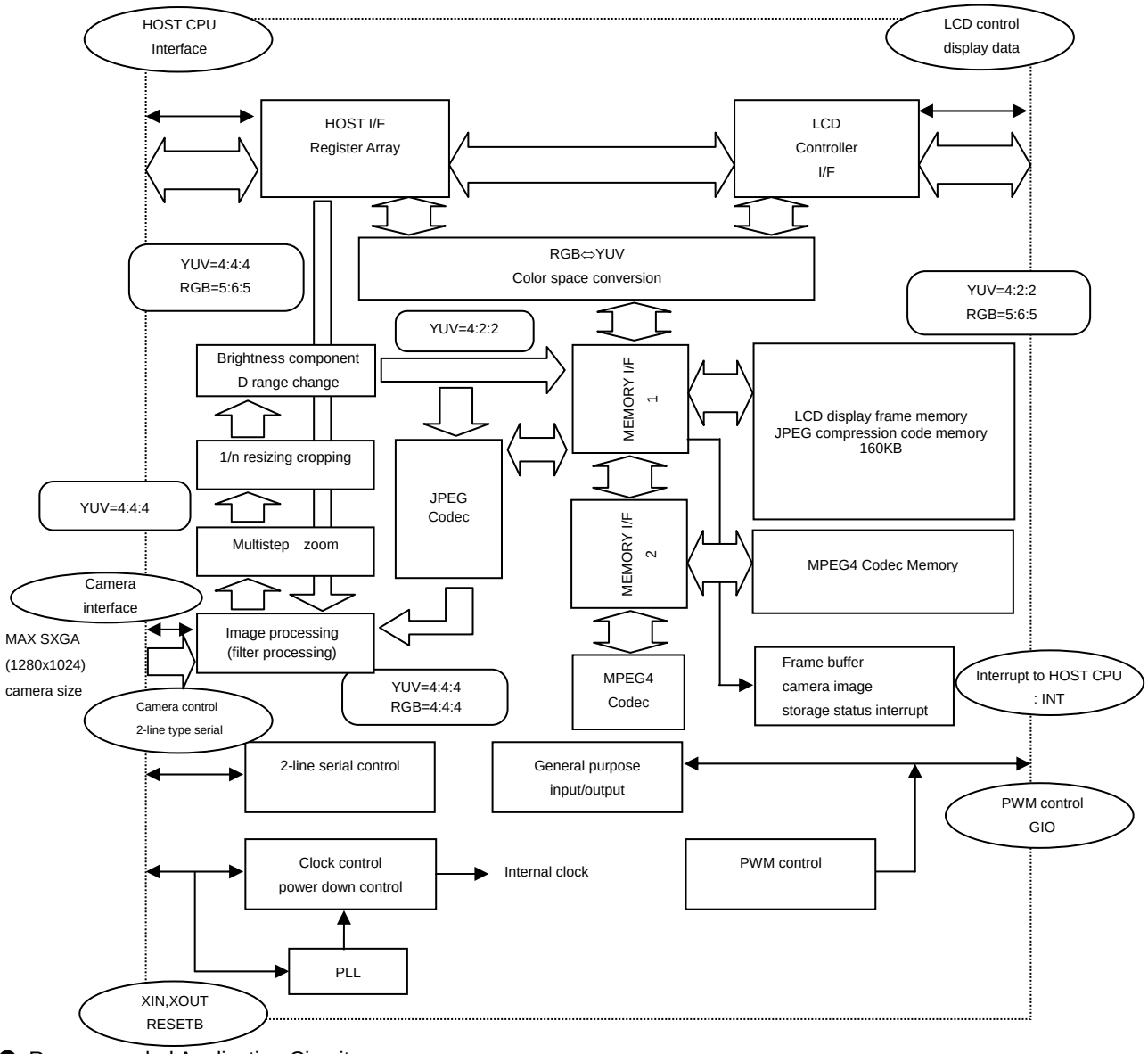
∗ Please supply power source in order of VDD→VDDIO1→VDDIO2.

●Electric characteristics

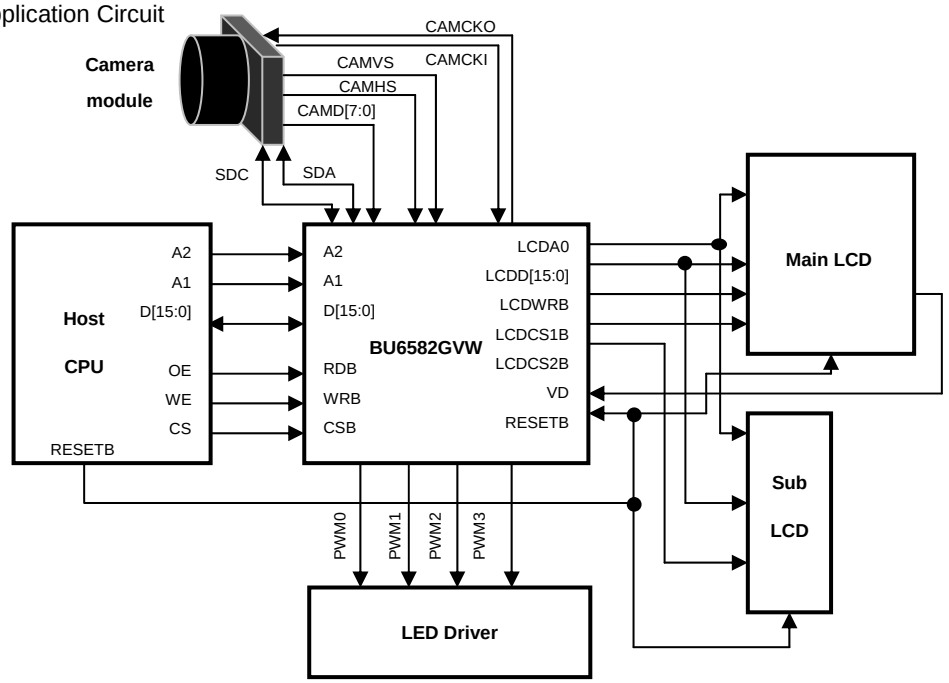
(Unless otherwise specified, VDDIO=2.85V, GND=0.0V, Ta=25℃,fin=12.0MHz,fSYS=48.0MHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input frequency	f_{IN}	10.0	-	30.0	MHz	XIN(DUTY45%～55%)
Internal operating frequency 1	f_{HSYS}	-	-	66.0	MHz	Internal HCLK,ACLK frequency
Internal operating frequency 2	f_{SSYS}	-	-	50.0	MHz	Internal SCLK frequency
Internal PLL input frequency	f_{PIN}	2.5	-	7.5	MHz	Internal PLL input frequency
Internal PLL output frequency	f_{POUT}	100	-	200	MHz	Internal PLL output frequency
Operating consumption current 1	IDD1	-	15	-	mA	At camera ON, LCD display ON At viewer operating
Operating consumption current 2	IDD2	-	65	-	mA	At camera ON, LCD display ON At MPEG4 encoding operating (at HCLK=60MHz)
Static consumption current	IDDst	-	-	150	μA	At suspend mode setting
Input "H" current 1	IIH1	-10	-	10	μA	VIH=VDDIO
Input "H" current 2	IIH2	25	50	100	μA	Pull-Down terminal, VIH=VDDIO
Input "H" current 3	IIH3	-10	-	10	μA	Pull-Up terminal, VIH=VDDIO
Input "L" current 1	IIL1	-10	-	10	μA	VIL=GND
Input "L" current 2	IIL2	-10	-	10	μA	Pull-Down terminal, VIL=GND
Input "L" current 3	IIL3	-160	-80	-25	μA	Pull-Up terminal, VIL=GND
Input "H" voltage 1	VIH1	VDDIO ×0.8	-	VDDIO +0.3	V	Normal input (including input mode of I/O terminal)
Input "L" voltage 1	VIL1	-0.3	-	VDDIO ×0.2	V	Normal input (including input mode of I/O terminal)
Input "H" voltage 2	VIH2	VDDIO ×0.85	-	VDDIO +0.3	V	Hysteresis input (RESETB, CSB, WRB, RDB, XIN)
Input "L" voltage 2	VIL2	-0.3	-	VDDIO ×0.15	V	Hysteresis input (RESETB, CSB, WRB, RDB, XIN)
Hysteresis voltage width	Vhys	-	0.7	-	V	Hysteresis input (RESETB, CSB, WRB, RDB, XIN)
Output "H" voltage 1	VOH1	VDDIO -0.4	-	VDDIO	V	IOH1=-1.0mA(DC) (including input mode of I/O terminal)
Output "L" voltage 1	VOL1	0.0	-	0.4	V	IOL1=1.0mA(DC) (including input mode of I/O terminal)
Output "H" voltage 2	VOH2	VDDIO -0.4	-	VDDIO	V	IOH2=-1.0mA(DC), XOUT terminal
Output "L" voltage 2	VOL2	0.0	-	0.4	V	IOL2=1.0mA(DC), XOUT terminal

●Block Diagram



● Recommended Application Circuit



∗ Data is prepared separately about each register setup. Please refer to the Development Scheme on page 14.

●Terminal functions

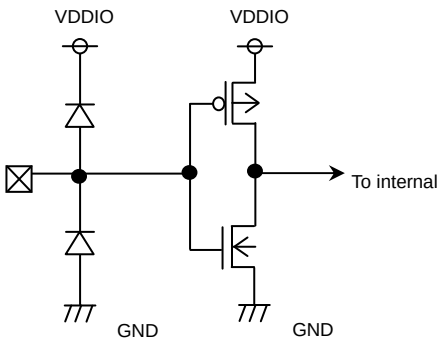
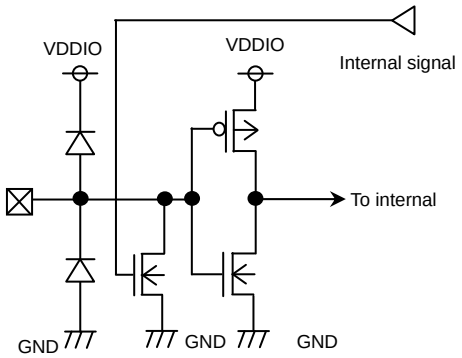
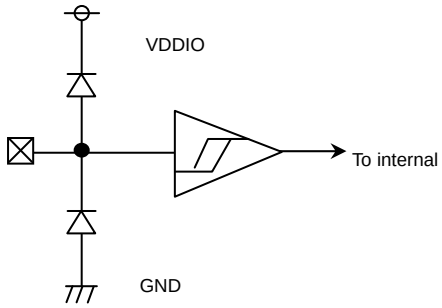
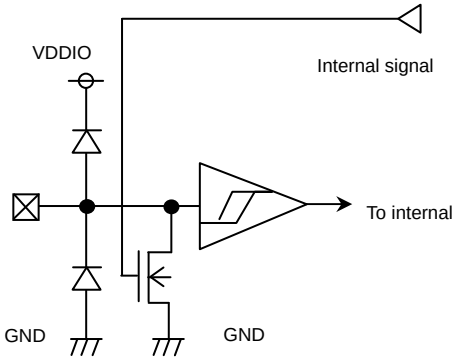
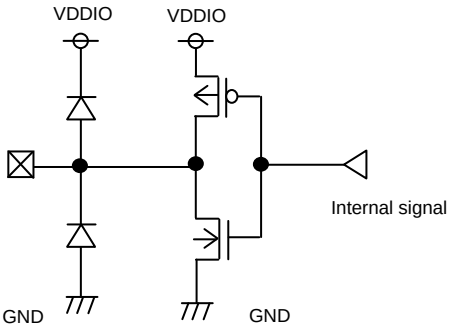
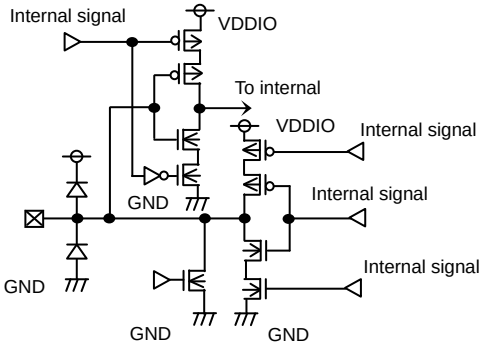
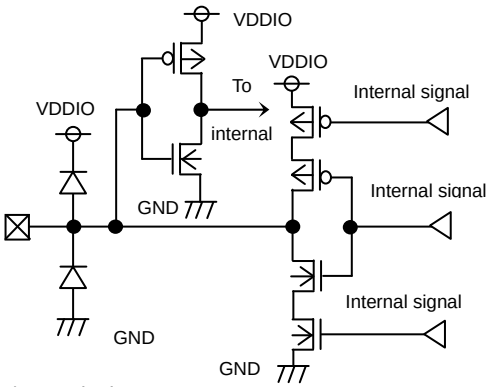
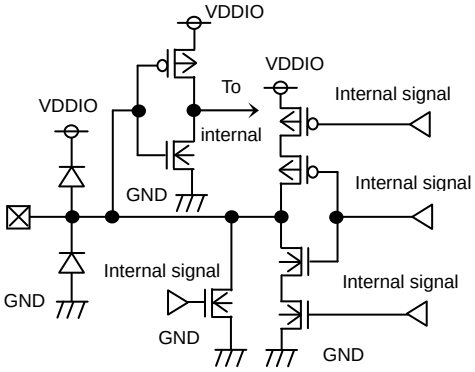
PIN No.	Land No.	PIN Name	In /Out	Active Level	Init	Function explanation	Power source system	Function division	I/O type
1	A1	N.C.	-	-	-	-	-	-	-
2	C3	VDDIO1	-	PWR	-	Digital I/O power source (system 1)	1	-	-
3	B2	D15	In/Out	DATA	In *1	Host data bus bit 15	1	HOST	F*3
4	B1	D14	In/Out	DATA	In *1	Host data bus bit 14	1	HOST	F*3
5	C2	D13	In/Out	DATA	In *1	Host data bus bit 13	1	HOST	F*3
6	D3	D12	In/Out	DATA	In *1	Host data bus bit 12	1	HOST	F*3
7	D2	D11	In/Out	DATA	In *1	Host data bus bit 11	1	HOST	F*3
8	D1	D10	In/Out	DATA	In *1	Host data bus bit 10	1	HOST	F*3
9	E3	D9	In/Out	DATA	In *1	Host data bus bit 9	1	HOST	F*3
10	E2	D8	In/Out	DATA	In *1	Host data bus bit 8	1	HOST	F*3
11	E1	GND	-	GND	-	Common ground	-	-	-
12	E5	N.C.	-	-	-	-	-	-	-
13	E4	SGIO3	In/Out	-	In *4	General-purpose I/O port	1	SYS	H
14	F2	SGIO2	In/Out	-	In *4	General-purpose I/O port	1	SYS	H
15	F1	VDD	-	PWR	-	Core power supply	-	-	-
16	F5	N.C.	-	-	-	-	-	-	-
17	F4	SGIO1	In/Out	-	In *4	General-purpose I/O port	1	SYS	H
18	F3	N.C.	-	-	-	-	-	-	-
19	G1	D7	In/Out	DATA	In *1	Host data bus / bit 7	1	HOST	F*3
20	G2	GND	-	GND	-	Common ground	-	-	-
21	G3	D6	In/Out	DATA	In *1	Host data bus / bit 6	1	HOST	F*3
22	G4	D5	In/Out	DATA	In *1	Host data bus / bit 5	1	HOST	F*3
23	H1	SGIO0	In/Out	-	In *4	General-purpose I/O port	1	SYS	H
24	H3	D4	In/Out	DATA	In *1	Host data bus / bit 4	1	HOST	F*3
25	J1	D3	In/Out	DATA	In *1	Host data bus / bit 3	1	HOST	F*3
26	J2	D2	In/Out	DATA	In *1	Host data bus / bit 2	1	HOST	F*3
27	H4	D1	In/Out	DATA	In *1	Host data bus / bit 1	1	HOST	F*3
28	H2	D0	In/Out	DATA	In *1	Host data bus / bit 0	1	HOST	F*3
29	K1	A2	In	DATA	-	Host address bus / bit 2	1	HOST	F*5
30	G5	GND	-	GND	-	Common ground	-	-	-
31	L1	N.C.	-	-	-	-	-	-	-
32	L2	VDDIO1	-	PWR	-	Digital I/O power supply (System 1)	1	-	-
33	K3	A1	In	DATA	-	Host address bus / bit 1	1	HOST	F *5
34	H5	CSB	In	Low	-	Chip select signal	1	HOST	K*6
35	K2	WRB	In	Low	-	Write enable signal	1	HOST	K
36	J3	RDB	In	Low	-	Read enable signal	1	HOST	K
37	K4	INT	Out	*	Low	Interrupt signal	2	HOST	E
38	L3	VDD	-	PWR	-	Core power supply	-	-	-
39	F6	SGIO11	In/Out	-	In *4	General-purpose I/O port	2	SYS	H
40	G6	SGIO10	In/Out	-	In *4	General-purpose I/O port	2	SYS	H
41	J4	CAMVS	In	*	-	Camera vertical timing signal (Pull-down during CAMOFF mode)	2	CAM	B
42	L4	CAMHS	In	*	-	Camera horizontal timing signal (Pull-down during CAMOFF mode)	2	CAM	B
43	K5	CAMD0	In	DATA	-	Camera data input / bit 0 (Pull-down in CAMOFF mode)	2	CAM	B
44	H6	GND	-	GND	-	Common ground	-	-	-
45	J5	VDDIO2	-	PWR	-	Digital I/O power supply (System 2)	2	-	-

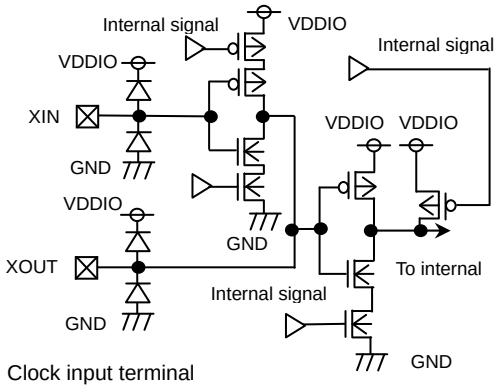
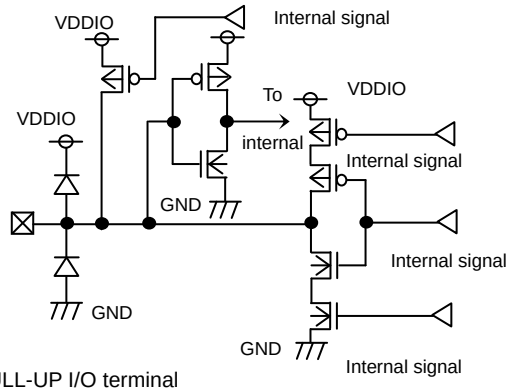
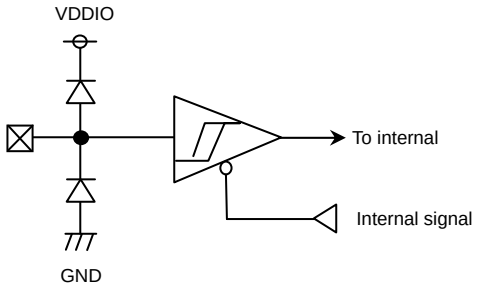
PIN No.	Land No.	PIN Name	In /Out	Active Level	Init	Function explanation	Power source system	Function division	I/O type
46	L5	CAMD1	In	DATA	-	Camera data input / bit 1 (Pull-down during CAMOFF mode)	2	CAM	B
47	K6	CAMD2	In	DATA	-	Camera data input / bit 2 (Pull-down during CAMOFF mode)	2	CAM	B
48	F7	GND	-	GND	-	Common ground	-	-	-
49	G7	SGIO9	In/Out	-	In *4	General-purpose I/O port	2	SYS	H
50	L6	CAMD3	In	DATA	-	Camera data input / bit 3 (Pull-down during CAMOFF mode)	2	CAM	B
51	H7	GIO2/KEY2	In/Out	DATA	Out/Low	General-purpose I/O port/key input	2	SYS	H
52	K7	CAMD4	In	DATA	-	Camera data input / bit 4 (Pull-down during CAMOFF mode)	2	CAM	B
53	J6	CAMD5	In	DATA	-	Camera data input / bit 5 (Pull-down during CAMOFF mode)	2	CAM	B
54	L7	N.C.	-	-	-	-	-	-	-
55	F8	CAMD6	In	DATA	-	Camera data input / bit 6 (Pull-down during CAMOFF mode)	2	CAM	B
56	G8	CAMD7	In	DATA	-	Camera data input / bit 7 (Pull-down during CAMOFF mode)	2	CAM	B
57	L8	VDDIO2	-	PWR	-	Digital I/O power supply (System 2)	2	-	-
58	K8	CAMCKI	In	CLK	-	Camera clock input (Pull-down during CAMOFF mode)	2	CAM	B
59	J7	CAMCKO	Out	CLK	Low	Camera clock output	2	CAM	E
60	L9	GND	-	GND	-	Common ground	-	-	-
61	L10	VDD	-	PWR	-	Core power supply	-	-	-
62	L11	N.C.	-	-	-	-	-	-	-
63	H8	SDA	In/Out	DATA	Out/Low	I/O serial data	2	SYS	J
64	K9	SDC	In/Out	CLK	Out/Low	I/O serial clock	2	SYS	J
65	K10	LEDCNT/GIO1	In/Out	*	In *4	LED PWM control signal from melody IC/general-purpose I/O port	2	SYS	H
66	K11	PWM1/GIO3	In/Out	-	In *4	LED PWM control signal/general-purpose I/O port	2	SYS	H
67	J8	PWM2/GIO4	In/Out	-	In *4	LED PWM control signal/general-purpose I/O port	2	SYS	H
68	J9	PWM3/GIO5	In/Out	-	In *4	LED PWM control signal/general-purpose I/O port	2	SYS	H
69	J11	GND	-	GND	-	Common ground	-	-	-
70	J10	VD/GIO6	In/Out	*	In *4	LCD controller vertical sync signal/general-purpose I/O port	2	LCD	H
71	H9	LCDCS1B	Out	Low	-	LCD controller chip select signal 1	2	LCD	G *2
72	H10	LCDCS2B	Out	Low	High	LCD controller chip select signal 2	2	LCD	G *2
73	H11	KEY0	In	*	-	Key input	2	SYS	H *7
74	G11	LCDD16	In/Out	DATA	Out/Low	LCD controller data bus / bit 16	2	LCD	H
75	F11	SGIO8	In/Out	-	In *4	General-purpose I/O port	2	SYS	H
76	G10	VDD	-	PWR	-	Core power supply	-	-	-
77	F10	LCDWRB	Out	Low	-	LCD controller write enable signal	2	LCD	G *2
78	E11	SGIO7	In/Out	-	In *4	General-purpose I/O port	2	SYS	H
79	G9	LCDRDB	Out	Low	-	LCD controller read enable signal	2	LCD	G *2
80	F9	GND	-	GND	-	Common ground	-	-	-
81	D11	LCDA0	Out	*	-	LCD controller command parameter identification	2	LCD	G *2
82	E10	SGIO4	In/Out	-	In *4	General-purpose I/O port	2	SYS	H
83	C11	VDDIO2	-	PWR	-	Digital I/O power supply (System 2)	2	-	-
84	D10	LCDD0	In/Out	DATA	Out/Low	LCD controller data bus / bit 0	2	LCD	H
85	C10	LCDD1	In/Out	DATA	Out/Low	LCD controller data bus / bit 1	2	LCD	H
86	B11	LCDD2	In/Out	DATA	Out/Low	LCD controller data bus / bit 2	2	LCD	H
87	E9	LCDD3	In/Out	DATA	Out/Low	LCD controller data bus / bit 3	2	LCD	H
88	E8	LCDD4	In/Out	DATA	Out/Low	LCD controller data bus / bit 4	2	LCD	H
89	B10	GND	-	GND	-	Common ground	-	-	-
90	A11	N.C.	-	-	-	-	-	-	-

PIN No.	Land No.	PIN Name	In /Out	Active Level	Init	Function explanation	Power source system	Function division	I/O type
91	A10	VDD	-	PWR	-	Core power supply	-	-	-
92	D9	LCDD5	In/Out	DATA	Out/Low	LCD controller data bus / bit 5	2	LCD	H
93	C9	LCDD6/SCL	In/Out	DATA	Out/Low	LCD controller data bus / bit 6	2	LCD	H
94	B9	SGIO6	In/Out	-	In *4	General-purpose I/O port	2	SYS	H
95	A9	LCDD7/SI	In/Out	DATA	Out/Low	LCD controller data bus / bit 7	2	LCD	H
96	D8	SGIO5	In/Out	-	In *4	General-purpose I/O port	2	SYS	H
97	C8	TEST	In	Low	-	Test mode terminal (Connect to GND.)	2	SYS	B
98	A8	LCDD17	In/Out	DATA	Out/Low	LCD controller data bus / bit 17	2	LCD	H
99	B8	GND	-	GND	-	Common ground	-	-	-
100	A7	LCDD8	In/Out	DATA	Out/Low	LCD controller data bus / bit 8	2	LCD	H
101	E7	N.C.	-	-	-	-	-	-	-
102	D7	VDDIO2	-	PWR	-	Digital I/O power supply (System 2)	2	-	-
103	C7	LCDD9	In/Out	DATA	Out/Low	LCD controller data bus / bit 9	2	LCD	H
104	A6	LCDD10	In/Out	DATA	Out/Low	LCD controller data bus / bit 10	2	LCD	H
105	B7	LCDD11	In/Out	DATA	Out/Low	LCD controller data bus / bit 11	2	LCD	H
106	B6	GND	-	GND	-	Common ground	-	-	-
107	A5	LCDD12	In/Out	DATA	Out/Low	LCD controller data bus / bit 12	2	LCD	H
108	C6	KEY1	In	-	-	Key input	2	SYS	H *7
109	D6	LCDD13	In/Out	DATA	Out/Low	LCD controller data bus / bit 13	2	LCD	H
110	E6	N.C.	-	-	-	-	-	-	-
111	A4	LCDD14	In/Out	DATA	Out/Low	LCD controller data bus / bit 14	2	LCD	H
112	B5	LCDD15	In/Out	DATA	Out/Low	LCD controller data bus / bit 15	2	LCD	H
113	B3	RESETB	In	Low	-	System reset signal	2	SYS	C
114	C5	PWM0/GIO0	In/Out	DATA	In *4	LED PWM control signal/general-purpose I/O port	2	SYS	H
115	D5	N.C.	-	-	-	-	-	-	-
116	A3	VDD	-	PWR	-	Core power supply	-	-	-
117	B4	VDDIO1	-	PWR	-	Digital I/O power supply (System 1)	1	-	-
118	C4	XOUT	Out	CLK	High	Clock output (Normally HIGH output while in external input setting mode)	1	SYS	I
119	D4	XIN	In	CLK	-	Clock input *8	1	SYS	I, K *9
120	A2	GND	-	GND	-	Common ground	-	-	-

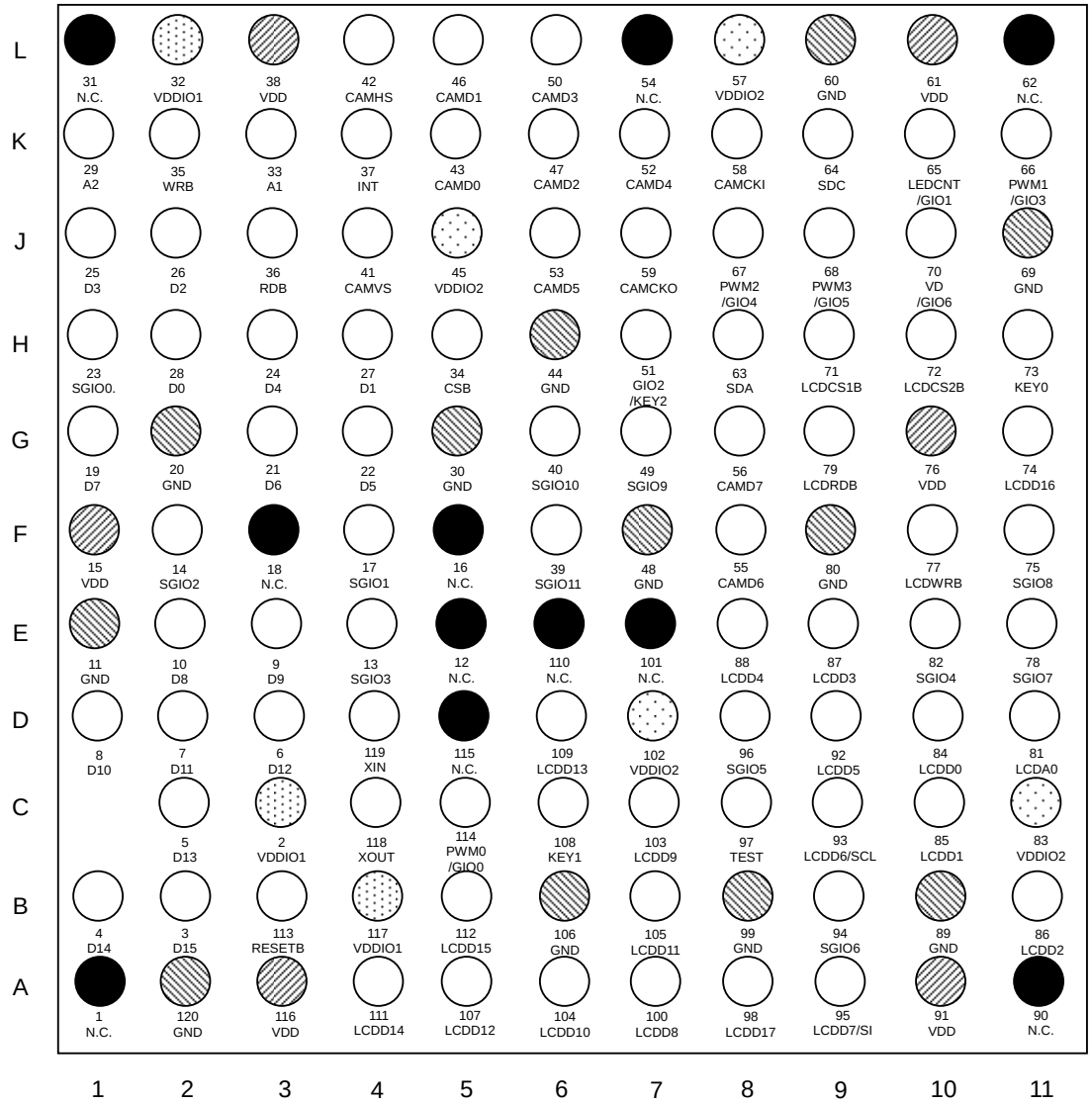
Concerning function category, HOST represents HOST IF, SYS→SYSTEM, CAM→CAMERA IF, and LCD→LCD IF.
"1" of the power source system represents System 1 (VDDIO1) and "2" of that represents System 2 (VDDIO2).
＊"＊" in Active Level column means active level can be changed by setting of register. Moreover, Init is a pin state at the time of reset release.
*1: RESETB='L'
*2: Input only except for a test mode.
*3: Pull down only except for a test mode.
*4: Pull down while RESETB='L'(initial state).
*5: Output status or pull-down function are only enabled during test mode.
*6: Suspend function is only enabled during test mode.
*7: Output only except for a test mode.
*8: The crystal oscillation circuit does not include a return resistance, so it is needed to examine an external circuit including return resistance.
*9: I/O type is I at oscillation mode, it is K at external clock input mode.

●Equivalent Circuit Structures of input / output pins

Type	The equivalent circuit structure	Type	The equivalent circuit structure
A	 Input terminal	**B**	 PULL-DOWN Input terminal
C	 Hysteresis input terminal	**D**	 PULL-DOWN Hysteresis input terminal
E	 Output terminal	**F**	 PULL-DOWN I/O terminal with SUSPEND
G	 I/O terminal	**H**	 PULL-DOWN I/O terminal

Type	The equivalent circuit structure
I	 Clock input terminal
J	 PULL-UP I/O terminal
K	 Hysteresis Input terminal with SUSPEND

●Terminal Layout



（Bottom View）

●Timing Chart

1. HOST interface timing

1.1 System timing

Table 1.1-1 BU6582GVW timing conditions (system)

Symbol	Details	MIN.	TYP.	MAX.	Unit	Conditions
tXIN	BU6582GVW Clock input cycle	33.3	-	100.0	ns	
DutyXIN	BU6582GVW Clock duty	45.0	50.0	55.0	%	"H" width / cycle
tHCLK	BU6582GVW HCLK clock cycle	15.15	-	-	ns	
DutyHCLK	BU6582GVW HCLK clock duty	33.3	50.0	66.6	%	"H" width / cycle
tSCLK	BU6582GVW SCLK clock cycle	20.0	-	-	ns	
DutySCLK	BU6582GVW SCLK clock duty	33.3	50.0	66.6	%	"H" width / cycle
tCAMCKO	Camera clock output cycle	20.0	-	-	ns	
DutyCAMCKO	Camera clock output duty	33.3	50.0	66.6	%	""H" width / cycle
tCAMCKI	Camera clock input cycle	20.0	-	-	ns	
DutyCAMCKI	Camera clock input duty	40.0	50.0	60.0	%	"H" width / cycle
tRESETB	RESETB "L" pulse width	1.0	-	-	us	

∗ Regulation all at threshold of VDDIO×1/2

1.2 Register (including RAM via register) write timing.

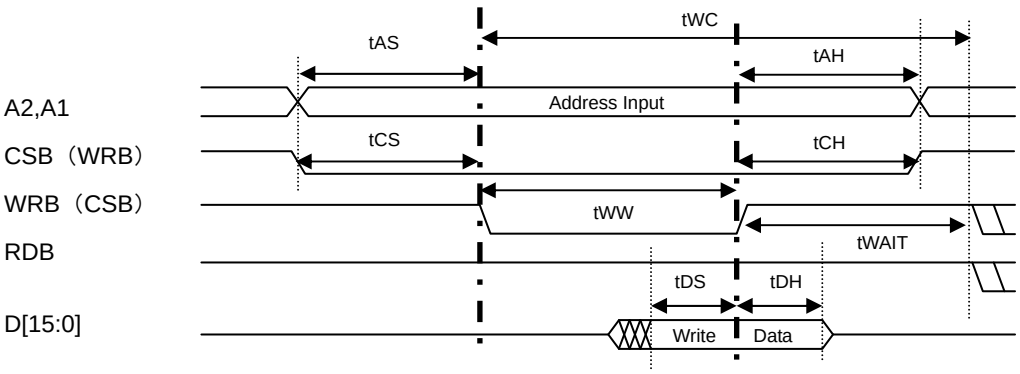


Table 1.2-1 BU6582GVW timing conditions（RAM, register write cycle）

Symbol	Details	MIN.	TYP.	MAX.	Unit
tWC	Write cycle time	75	-	-	ns
tAS	Address setup time before WRB(CSB) falling	-7	-	-	ns
tAH	Address hold time after WRB(CSB) rising	-1	-	-	ns
tCS	CSB(WRB) input setup time before WRB(CSB) falling	0	-	-	ns
tCH	CSB(WRB) input hold time after WRB(CSB) falling	0	-	-	ns
tWW	WRB(CSB) active time width	45	-	-	ns
tWAIT	Wait time from WRB(CSB) rising to the next WRB(CSB) or to RDB falling	5.5	-	-	ns
tDS	Data setup time before WRB(CSB) rising	40	-	-	ns
tDH	Data hold time after WRB(CSB) rising	-1	-	-	ns

∗ Regulation all at threshold of VDDIO1×1/2 (VDD=1.50V,VDDIO=2.85V,GND=0.0V,Ta=25ºC)

∗ It is possible to use it with either CSB or WRB active. However, either of them must do LOW pulse operation.

1.3 Register (including RAM via register) read timing.

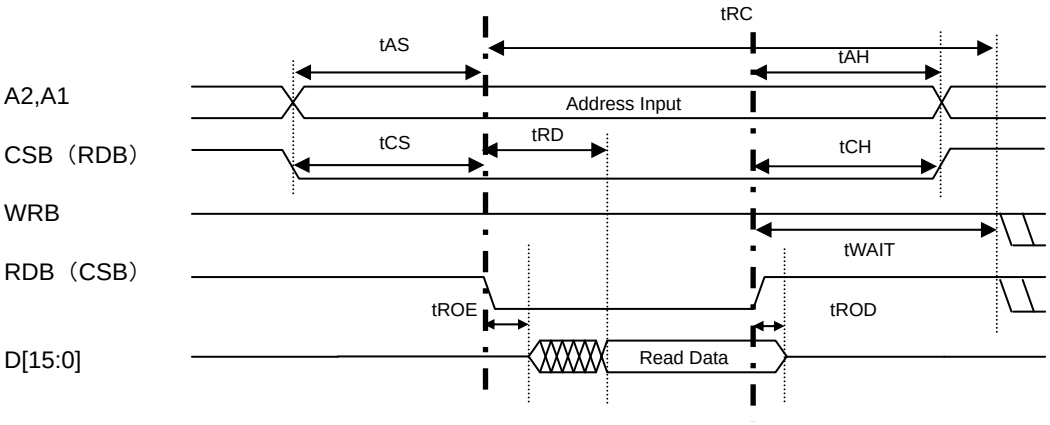


Table 1.3-1 BU6582GVW timing conditions (RAM, register read cycle)

Symbol	Details	MIN.	TYP.	MAX.	Unit
tRC	Read cycle time	75.5	-	-	ns
tAS	Address setup time before RDB(CSB) falling	-7	-	-	ns
tAH	Address hold time after RDB(CSB) rising	-1	-	-	ns
tCS	CSB(RDB) input setup time before RDB(CSB) falling	0	-	-	ns
tCH	CSB(RDB) input hold time after RDB(CSB) rising	0	-	-	ns
tRD	Access time after RDB(CSB) falling	-	-	70	ns
tWAIT	Wait time from RDB(CSB) falling to the next RDB(CSB) falling or to WRB falling	5.5	-	-	ns
tROE,tROD	Data output enable time after RDB(CSB) rising, Data output disable time after RDB(CSB) falling	-	-	15	ns

∗ Regulation all at threshold of VDDIO1×1/2 (VDD=1.80V,VDDIO1,2=2.85V,GND=0.0V,Ta=25ºC)
∗ It is possible to use it with either CSB or WRB active. However, either of them must do LOW pulse operation.

2. Camera Module Interface Timing

2.1. System clock and camera clock

BU6582GVW external clock input (XIN) can be divided set and supplied as CAMCKO clock to camera module. (As for division setting, refer to 3.2.2.)
The relation between data synchronization CAMCKI clock from camera and system clock SCLK must be set in order to meet the following formula by setting of ACTSW (IDX:0D3h CLKDIV3[5:4]).

When ACTSW=1h fSCLK ＝ fCAMCK1 ·····(Formula : 3.3-1)
When ACTSW=2h fSCLK ≧ 2×fCAMCKI ·····(Formula : 3.3-2)
Wherein, fSCLK BU6582GVW system clock frequency
fCAMCKI CAMCKI terminal input clock frequency
ACTSW=0h,3h is forbidden.

(note) fCAMCKI ＞ fSCLK, 2×fCAMCKI ＞ fSCLK ＞ fCAMCKI is forbidden.

2.2. Camera module interface timing

The timing of the camera image signal in camera I/F is shown in Table 2.2-1.

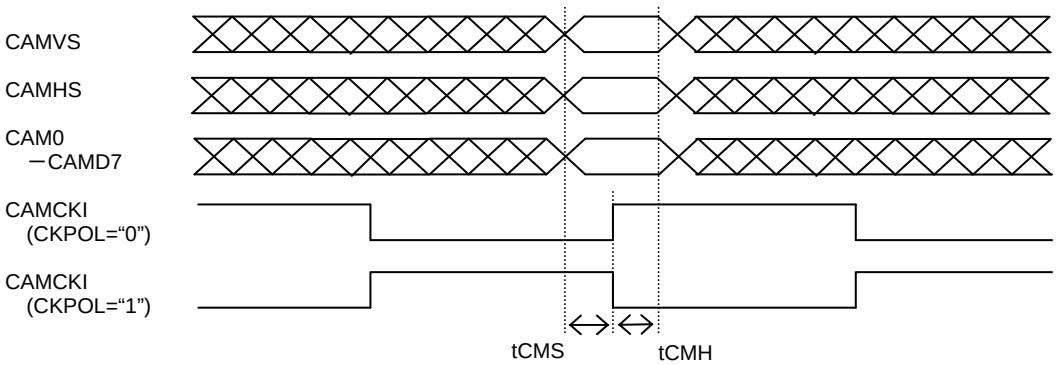


Table 2.2-1 BU6582GVW timing (camera data)

Symbol	Details	MIN.	TYP.	MAX.	Unit
tCMS	CAMCKI rising/falling camera set up time	4	-	-	ns
tCMH	CAMCKI rising/falling camera hold time	4	-	-	ns

3. LCD direct access

・Transparent terminal timing at LCD module direct access

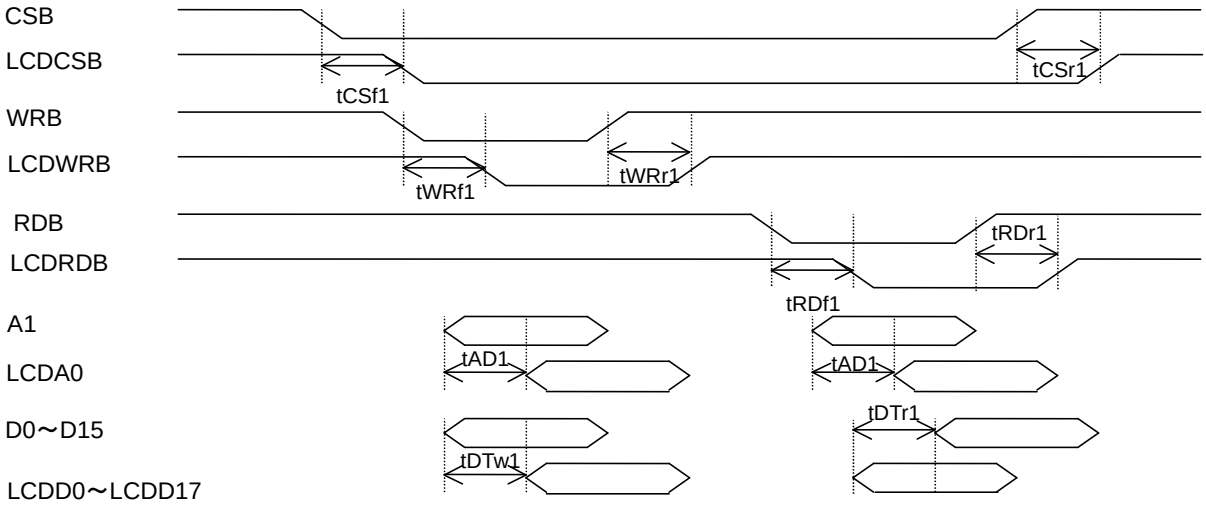


Table 3-1 BU6582GVW timing conditions（LCD direct access）

Symbol	Details	MIN.	TYP.	MAX.	Unit
tCSf1	Delay from CSB to LCDCSB falling	2.5	-	12.2	ns
tCSr1	Delay from CSB to LCDCSB rising	2.1	-	11.3	ns
tWRf1	Delay from WRB to LCDWRB falling	2.3	-	12.2	ns
tWRr1	Delay from WRB to LCDWRB rising	1.9	-	11.0	ns
tRDf1	Delay from RDB to LCDRDB falling	2.5	-	12.2	ns
tRDr1	Delay from RDB to LCDRDB rising	2.2	-	11.1	ns
tAD1	Delay from A1 to LCDA0	2.6	-	12.1	ns
tDTw1	Delay from D0～D15 to LCDD0～LCDD17	2.7	-	11.0	ns
tDTr1	Delay from LCDD0～LCDD17 to D0～D15	2.3	-	13.8	ns

4. LCD transfer timing

Transfer timing to LCD is shown below.

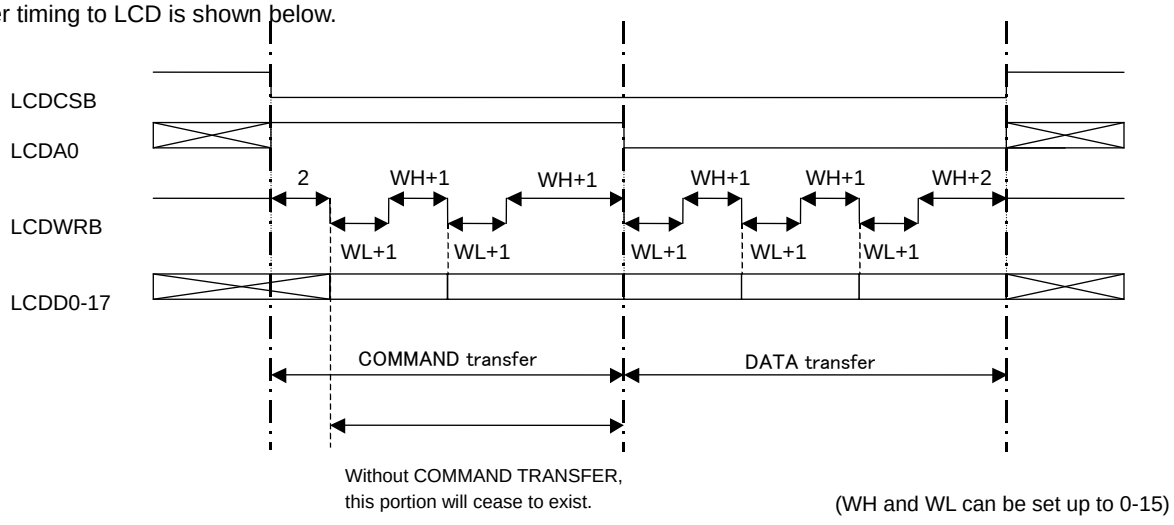


Figure 4-1 MAIN LCD data transfer waveform（Unit：tSCLK）

● Development Scheme

This technical note is aimed at trying the connectivity in the hardware between customer's system and our camera image processor series.

We prepare various data and tools for every development STEP as follows other than this technical note, please contact the sales staff in your duty also including the support system.

(1) Demonstration STEP

(You can try the standard image processing functions by the standard Demonstration kit at once.)

You can confirm the standard functions such as camera image preview, memory data display to LCD, camera image composition JPEG compression/ expansion, frame composition, divided display, and LED lighting, and so forth on the Demonstration board.

・Standard Demonstration board kit

◎Demonstration board

（LCD module provided by ROHM, Camera module provided by ROHM, Check board equipped with the camera image processor, ARM-equipped controller board）

◎Demonstration board operation manual

◎Demonstration software

If the software for the trial board is installed in your Windows PC(Windows 2000/XP/ME/98), more detailed setting is possible.

(Execution tools for the macro command, sample macro command file)

◎USB cable

(2) Confirmation STEP

(We will respond to customer's camera module, LCD module, HOST CPU.)

・Specifications

We will provide specifications for camera image processor according to customer's requirements.

・Function explanation

We will deliver you the function explanation describing detailed functions, register settings, external interfaces, timing, and so forth of camera image processor according to your requests.

・Application note

We will deliver you the detailed explanation data on application development of camera image processor according to your requests.

(3) System check STEP

(You can check the application operation as a system by the kit of system check tools and your module(camera/LCD).)

ROHM creates the system check board using your camera/LCD module.

You can check the interface with your module and the application operation on the system check board using the tools for user's only.

・System check tools kit

・System check software (For Windows PC)

◎Reference C source code summarizing ARM –compatible application program interface(API)

◎The application software (API) as a reference C source code

◎The execution tools for the macro command (BU65XX_USB) for the check by your PC.

◎The macro command file for the check by your PC.

・System check document

◎System check board manual

◎BU65XX Demo_Board Application using API

◎Board circuit diagram

*You can check the detailed functions of the application operation by your PC using the macro command file.

(4) Integrated check STEP with user's system

(You can check the application operation as a system on your system check board using the integrated check software.)

You can check the application operation on the sample LSI-equipped system check board by your camera / LCD module using the integrated check software.

・On line Support；We will answer your questions about the software development.

How to use the macro command file, API file, and APL file.

Setting flow of the camera function (camera JPEG, preview, etc.)

Interface setting of the camera module, LCD module and the camera image processor.

Header analysis method oh JPEG decode, etc.

・On site Support；We will help you clarify the questions about the software development on site together on spot.

Check of the operation of each function and the basic operation at each register setting, etc. based on the specification.

Explanation about the specific usage of the macro command file, API file and APL file and relative questions.

How to develop the overlay or special functions, etc.

●Cautions on use

(1)Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2)Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3)Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4)Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5)GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6)Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7)Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8)Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9)Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10)Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11)External capacitor

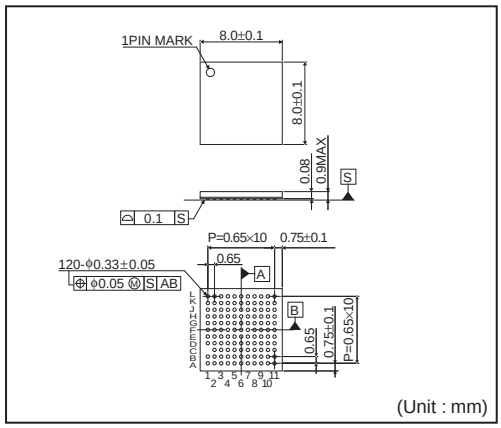
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

●Order Model Name Selection

B U	6 5 8 2	G V W	—	E 2
ROHM model name	Product number	Package type GVW:SBGA120W080		Taping model name E2: Embossed reel tape

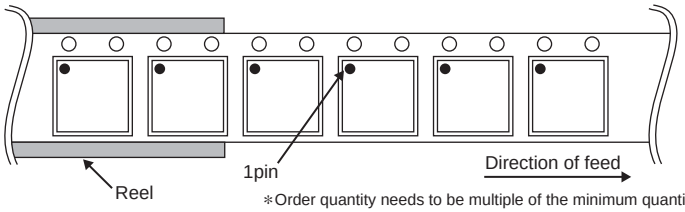
● Tape and Reel information

SBGA120W080



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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