# Data rate 1350Mbps RGB Interface 

## BU7963GUW

## - Description

BU7963GUW is a differential serial interface connecting mobile phone LCD modules to the host CPU. Unique technology is utilized for lower power consumption and EMI. MSDL minimizes the number of wires required - an important consideration in hinge phones - resulting in greater reliability and design flexibility.

## -Features

1) MSDL3 high-speed differential interface with a maximum transfer rate of 1350 Mbps .
2) Compatible with24-bit RGB video mode for LCD controller-to-LCD interface.
3) Pixel clock frequency range from 4 to 45 MHz .
4) Depending on the data transfer rate, one, two or three differential data channels can be selected.

## - Applications

Serial Interface for LCD Display Interface of Mobile Devices Application.

- Absolute Maximum Ratings:

| Parameter | Symbol | Ratings | Unit | Remarks |
| :--- | :---: | :---: | :---: | :---: |
| Power Supply Voltage | DVDD | $-0.3 \sim+2.5$ | V | - |
|  | MSVDD | $-0.3 \sim+2.5$ | V | - |
| Input Voltage | VIN | $-0.3 \sim$ MSVDD+0.3 | V | I/O terminals of MSVDD line |
|  |  | $-0.3 \sim$ DVDD +0.3 | V | I/O terminals of DVDD line |
| Output Voltage | VOUT | $-0.3 \sim$ MSVDD+0.3 | V | I/O terminals of MSVDD line |
|  |  | $-0.3 \sim$ DVDD+0.3 | V | I/O terminals of DVDD line |
| Input Current | IIN | $-10 \sim+10$ | mA | - |
| Output Current | IOUT | $-70 \sim+70$ | mA | - |
| Preservation Temperature | Tstg | $-55 \sim+125$ | ${ }^{\circ} \mathrm{C}$ | - |

-Operating Conditions:

| Parameter | Symbol | Ratings |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| Supply Voltage for DVDD | V ${ }_{\text {DVDD }}$ | 1.65 | 1.80 | 1.95 | V | $\mathrm{V}_{\text {DVDD }}=\mathrm{V}_{\mathrm{MSVDD}}$ |
| Supply Voltage for MSVDD | $\mathrm{V}_{\text {MSVDD }}$ | 1.65 | 1.80 | 1.95 | V |  |
| Data Transmission Rate | DR | 120 | - | 450 | Mbps/ch | - |
| Operating Temperature Range | Topr | -30 | 25 | 85 | ${ }^{\circ} \mathrm{C}$ | - |


(UNIT:mm)
Fig.1. Package View (VBGA063W050)

## -Block Diagram



Fig.2. Block Diagram

## -Pin Layout

|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A | TESTO | PD19 | PD17 | PD16 | PD14 | PD13 | PD10 | CKD |
| B |  | PCLK | PD18 | PD15 | PD12 | PD11 | PD9 | PD8 |
| C | PD22 | PD20 | PLL_BW | DVDD | N.C. | RVS | PD7 | PD6 |
| D | PD23 | PD21 | N.C. | DGND | DGND | DVDD | PD4 | PD5 |
| E | PD25 | PD24 | DVDD | DGND | MSGND | N.C. | PD1 | PD3 |
| F | PD26 | LSO | MSVDD | MSGND | MSVDD | N.C. | XSD | PD2 |
| G | LS1 | POL PCLK | $\begin{gathered} \text { D2+ } \\ \text { (D0+) } \end{gathered}$ | $\begin{gathered} \text { D1+ } \\ \text { (CLK+ }) \end{gathered}$ | $\begin{aligned} & \text { CLK+ } \\ & \text { (D1+) } \end{aligned}$ | $\begin{gathered} \text { D0+ } \\ \text { (D2+) } \end{gathered}$ | N.C. | PDO |
| H | N.C. | N.C. | $\begin{aligned} & \text { D2- } \\ & \text { (D0-) } \end{aligned}$ | $\begin{aligned} & \text { D1- } \\ & \text { (CLK-) } \end{aligned}$ | $\begin{aligned} & \text { CLK- } \\ & \text { (D1-) } \end{aligned}$ | $\begin{aligned} & \text { D0- } \\ & \text { (D2-) } \end{aligned}$ | DRVR | TEST1 |

Fig.3. Pin Layout (Top View)

## -Pin Functions

Table 1. Power Supply and Ground

| Power Supply / Ground : 10-pin |  |  |  |
| :---: | :---: | :--- | :--- |
| Name | Width |  | Functions |
| DVDD | 3 | CMOS I/O and logic core power supply. |  |
| MSVDD | 2 | Analog core power supply. |  |
| DGND | 3 | CMOS I/O and logic core ground. |  |
| MSGND | 2 | Analog core ground. |  |

Table 2. MSDL3

| High-Speed Serial Interface |  |  |  | 8-pin |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Name | Width | Level | I/O | Functions | Shutdown | Equivalent Schematic |
| CLK+ | 1 | Analog | O | ```CLK+ pin When RVS = 'L' : CLK+ When RVS = 'H' : D1+``` | Hi-Z | D |
| CLK- | 1 | Analog | O | $\begin{aligned} & \text { CLK- pin } \\ & \text { When RVS = 'L' : CLK- } \\ & \text { When RVS = 'H' : D1- } \end{aligned}$ | Hi-Z | D |
| D0+ | 1 | Analog | O | $\begin{aligned} & \text { D0+ pin } \\ & \text { When RVS = 'L' : D0+ } \\ & \text { When RVS = 'H' : D2+ } \end{aligned}$ | Hi-Z | D |
| D0- | 1 | Analog | O | $\begin{aligned} & \text { D0- pin } \\ & \text { When RVS = 'L' : D0- } \\ & \text { When RVS = 'H' : D2- } \end{aligned}$ | Hi-Z | D |
| D1+ | 1 | Analog | O | $\begin{aligned} & \text { D1+ pin } \\ & \text { When RVS = 'L' : D1+ } \\ & \text { When RVS = 'H' : CLK+ } \end{aligned}$ | Hi-Z | D |
| D1- | 1 | Analog | O | D1- pin When RVS = 'L' : D1When RVS = 'H' : CLK- | Hi-Z | D |
| D2+ | 1 | Analog | O | $\begin{aligned} & \text { D2+ pin } \\ & \text { When RVS = 'L' : D2+ } \\ & \text { When RVS = 'H' : D0+ } \end{aligned}$ | Hi-Z | D |
| D2- | 1 | Analog | O | $\begin{aligned} & \text { D2- pin } \\ & \text { When RVS = 'L' : D2- } \\ & \text { When RVS = 'H' : D0- } \end{aligned}$ | Hi-Z | D |

Table 3. Analog

| Analog |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1-pin |  |  |  |  |  |  |
| Name | Width | Level | I/O | Functions | Shutdown | Equivalent <br> Schematic |
| DRVR | 1 | Analog | - | $10 \mathrm{k} \Omega \pm 5 \%$ register should be connected between <br> DRVR and MSGND. | - | D |

Table 4. Parallel Data Interface

| Parallel Data Interface 29 -pin |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :--- | :---: | :---: |
| Name | Width | Level | I/O | Functions | Shutdown | Equivalent <br> Schematic |
| PCLK | 1 | CMOS | I | PCLK interface. | Input | A |
| PD[26:0] | 27 | CMOS | I | Parallel data interface. | Input | A |
| CKD | 1 | CMOS | O | Output of PCLK detection result. <br> 'L' clock stop. <br> 'H': clock detect. | 'L' | C |

Table 5. Control

| Control | 8-pin |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Name | Width | Level | I/O | Functions | Shutdown | Equivalent Schematic |
| XSD | 1 | CMOS | 1 | Shutdown pin. <br> 'L': shutdown. <br> 'H': normal operation. | Input | A |
| LS0 LS1 | 1 1 | CMOS | 1 | Selection of the number of data channel and the data format. <br> * Refer to "Selection of the number of MSDL3 channels". <br> * Set the same number of data channel between the TX device and the RX device. | Input | A |
| RVS | 1 | CMOS | 1 | Selection of MSDL3 pins assignment. <br> ' L ': Default matrix. <br> ' H ': Flipped matrix. | Input | A |
| PLL_BW | 1 | cmos | 1 | Selection of PLL bandwidth. | Input | A |
| POL_PCLK | 1 | CMOS | 1 | Selection of input clock polarity. <br> ' L ': sample parallel data at falling. <br> ' H ': sample parallel data at rising. | Input | A |
| TESTO | 1 | Pull down | 1 | Test mode pin. 'L': normal mode. ' H ': test mode. Must be 'L.' | Input | B |
| TEST1 | 1 |  |  |  |  | B |



Fig.4. Equivalent Schematics

## -Operation Control

MSDL3 Channel Count Selection
Pin LS is used to control the high-speed data channel count and data format. The LS pin settings (i.e., high-speed data channel count, data format) should be the same between the transmitting and receiving devices (the BU7963GUW and BU7964GUW, respectively). Table 6 shows the PCLK input frequency ranges and transmission data rate ranges for the LS pin settings.

Table 6. The Range of The Transmission Data rate

| LS1 | LS0 | The Number of Data Channel | The Range of PCLK Input <br> Frequency [MHz] | The Range of The Data <br> Transmission Rate <br> [Mbits/sec] |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ' $\mathrm{L}^{\prime}$ | 'L' | 1-channel | $4.0-15.0$ | $120-450$ |  |
| 'L' | 'H' | 2-channel | $8.0-30.0$ | $240-900$ |  |
| 'H' | 'L' | 3-channel | $12.0-45.0$ | $360-1350$ |  |
| 'H' | 'H' |  |  |  |  |

MSDL3 Pin Assignment
RVS determines the assignment of MSDL3 pins, CLK+ / CLK-, D0+ / D0-, D1+ / D1- and D2+ / D2-. Only the MSDL3 high-speed signaling pins are affected by RVS, while pin assignment of other functions does not change. User can select the assignment from 'straight' (default) and 'flipped' assignment in order to minimize channel-to-channel skew in PWB design. Table 7 shows the MSDL3 pin assignment, and Fig. 5 shows the 'straight' and 'flipped'

Table 7. MSDL3 Pin Assignment

| RVS | MSDL3 Pin Assignment |
| :---: | :---: |
| ' L ' | 'Straight' (default matrix) |
| ' $\mathrm{H}^{\prime}$ | 'Flipped' |



Fig.5. MSDL3 Pin Assignment

PCLK Polarity Selection
BU7963GUW controls PCLK input polarity by POL_PCLK setting. Table 8 shows PCLK input polarity.
Table 8. PCLK Polarity Selection

| POL_PCLK | Parallel Data Capturing Polarity |
| :---: | :---: |
| 'L' | Capture parallel data at falling edge. |
| 'H' <br> (default) | Capture parallel data at rising edge. |

PLL Bandwidth Selection
BU7963GUW controls the range of the CLK+ / CLK- input frequency (= PCLK output frequency) by the setting of the data format (LS1, and LSO) of the high-speed data channel and the bandwidth setting of PLL_BW.

Table 9. PLL_BW Setting

| LS1 | LSO | PLL_BW | CLK+ / CLK- Frequency Range [MHz] <br> (PCLK Input Frequency) |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |
| 'L' | 'L' | 'L' | 4 | 8 |
| 'L' | 'L' | 'H' | 7 | 15 |
| 'L' | 'H' | 'L' | 8 | 16 |
| 'L' | 'H' | 'H' | 14 | 30 |
| 'H' | 'L' | 'L' | 12 | 24 |
| 'H' | 'L' | 'H' | 21 | 45 |

## -Power Modes

BU7963GUW has three power modes.

1) Shutdown Mode BU7963GUW goes to Shutdown Mode when XSD = 'L'. All logic circuits are initialized in the Shutdown Mode. All high-speed signaling channels are disabled, and the outputs keep Hi-Z status.
2) Standby Mode

BU7963GUW goes to Standby Mode when XSD = 'H' and PCLK is not provided. All high-speed signaling channel outputs keep Hi-Z status. BU7963GUW is monitoring whether PCLK input is running or not and the link switches to Active Mode when PCLK running is detected.
3) Active Mode

BU7963GUW goes to Active Mode when XSD = ' H ' and PCLK is running. All high-speed signaling channels are enabled.

| Table 10. Power Modes |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Input |  | Operation |  |
|  | XSD | PCLK | Functions | MSDL3 Terminals |
| Shutdown | 'L' | Static ('L' or 'H') | Initialized | Disabled (Hi-Z) |
| Standby | 'H' | Static ('L' or 'H') | PCLK detection | Disabled (Hi-Z) |
| Active | 'H' | Clock input is active | PCLK detection <br> Normal operation <br> (P2S conv) | Enabled |

4) Power Modes Transition

Fig. 6 shows the transition of power modes.


Fig.6. Power Modes Transition

## -High-Speed Data Channel Protocols

Fig.7, Fig. 8 and Fig. 9 show high-speed data channel protocols.


Fig.7. MSDL3 Protocol for 1-channel Data (27-bit)


Fig.8. MSDL3 Protocol for 2-channel Data (27-bit)


Fig.9. MSDL3 Protocol for 1-channel Data (13-bit)
"res" is reserved bit for the future use, the default state of those is ' 0 .'
CP is the parity bit of data payload. BU7961GUW adds an odd parity on CP of the high-speed channel data.

- When the number of ' H ' bits in parallel data is even, CP bit is ' H .'
- When the number of ' H ' bits in parallel data is odd, CP bits is ' L .'


## -Electrical Characteristics

1) DC Characteristics

Table 11. Digital Input / Output DC Characteristics
$\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{DVDD}=\mathrm{MSVDD}=1.80 \mathrm{~V}$ and $\mathrm{DGND}=\mathrm{MSGND}=0.00 \mathrm{~V}$, unless otherwise noted.

| Parameter | Symbol | Limits |  |  | Unit | Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :--- |

Table 12 Current Consumption

| Parameter | Symbol | Limits |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| Shutdown Current | Iop _st_rx | - | 0.2 | 10 | $\mu \mathrm{A}$ | $\begin{aligned} & \text { XSD = 'L', } \\ & \text { IDVDD + IMSVDD } \end{aligned}$ |
| Standby Current | $l_{\text {op_stb_rx }}$ | - | 0.2 | 10 | $\mu \mathrm{A}$ | $\begin{aligned} & \text { XSD = 'H', } \\ & \text { IDVDD + IMSVDD } \end{aligned}$ |
| Active Current <br> 1-channel / 27-bit Format | Iop_act_rx1 | - | 14.0 | 18.5 | mA | $\begin{aligned} & \text { LS[1:0] = 'LL,'PLL_BW[1:0] = 'H' } \\ & \text { DVDD = MSVDD } \\ & \text { PCLK=15MHz,XSD='H } \\ & \text { CL=10pF } \\ & \text { Total operating current (IDVDD + } \\ & \text { IMSVDD ) with PD[26:0] inputs to ggling } \\ & \text { Ox2AAAAAA and 0x5555555 } \end{aligned}$ |
| Active Current 2-channel / 27-bit Format | $\mathrm{I}_{\text {op_act_rx }}$ | - | 19.7 | 25.7 | mA | $\begin{aligned} & \text { LS[1:0] = 'LH,' PLL_BW[1:0] = 'H' } \\ & \text { DVDD = MSVDD } \\ & \text { PCLK=30MHz,XSD='H' } \\ & \text { CL=10pF } \\ & \text { Total operating current (IDVDD + } \\ & \text { IMSVDD) with PD[26:0] inputs to ggling } \\ & \text { Ox2AAAAAA and 0x5555555 } \end{aligned}$ |
| Active Current <br> 3-channel/ 27-bit Format | $\mathrm{I}_{\text {op_act_rx }}$ | - | 25.4 | 32.9 | mA | $\begin{aligned} & \text { LS[1:0] = 'HL,' PLL_BW[1:0] = 'H' } \\ & \text { DVDD = MSVDD } \\ & \text { PCLK=45MHz,XSD='H' } \\ & \text { CL=10pF } \\ & \text { Total operating current (IDVDD + } \\ & \text { IMSVDD) with PD[26:0] inputs to ggling } \\ & \text { Ox2AAAAAA and 0x55555555 } \end{aligned}$ |

2) AC Characteristics

Parallel Data Input Timing


Fig. 10 Parallel Data Input AC Timing

Table 13. Parallel Data Input AC Timing
$\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{DVDD}=\mathrm{MSVDD}=1.80 \mathrm{~V}$ and $\mathrm{DGND}=\mathrm{MSGND}=0.00 \mathrm{~V}$, unless otherwise noted.

| Parameter | Symbol | Limits |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| PCLK Input Frequency | $\mathrm{f}_{\text {TX_PCLK1 }}$ | 4 | - | 15 | MHz | LS0=L, LS1=L |
|  | $\mathrm{f}_{\text {TX_PCLK2 }}$ | 8 | - | 30 | MHz | LS0=H, LS1=L |
|  | $\mathrm{f}_{\text {TX_PCLK }}$ | 12 | - | 45 | MHz | LS0=L, LS1=H |
| PCLK Input Duty Cycle | tex_Duty | 33 | - | 67 | \% |  |
| Input Data Setup Time | $\mathrm{t}_{\text {TX_DS }}$ | 5.0 | - | - | ns | POL_PCLK=H |
| Input Data Hold Time | $\mathrm{t}_{\text {TX_D }}$ | 5.0 | - | - | ns | POL_PCLK=H |
| Input Signal Rise Time 1 | $\mathrm{t}_{\text {TX_R1 }}$ | - | - | 10 | ns | PCLK Frequency $\leqq 30 \mathrm{MHz}$ |
| Input Signal Rise Time 2 | $\mathrm{t}_{\text {TX_R2 }}$ | - | - | 5 | ns | PCLK Frequency $>30 \mathrm{MHz}$ |
| Input Signal Fall Time 1 | $\mathrm{t}_{\text {TX_F1 }}$ | - | - | 10 | ns | PCLK Frequency $\leqq 30 \mathrm{MHz}$ |
| Input Signal Fall Time 2 | $\mathrm{t}_{\text {TX_F2 }}$ | - | - | 5 | ns | PCLK Frequency $>30 \mathrm{MHz}$ |

## 3) Serial Data Input Timing

Fig. 11 and Table 14 shows Serial Data Input Timing of BU7963GUW.

$\mathrm{UI}=(1$ cycle time of $\mathrm{CLK}+/-) / 30$
$\mathrm{N}=$ Bit position $(0 \leqq \mathrm{~N} \leqq 30)$
Fig.11. Serial Data input AC Timing
Table 14. Serial Data input AC Timing
$\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{DVDD}=\mathrm{MSVDD}=1.80 \mathrm{~V}$ and $\mathrm{DGND}=\mathrm{MSGND}=0.00 \mathrm{~V}$, unless otherwise noted.

| Parameter | Symbol | Limits |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Typ | Max |  |  |  |
| Output location CLKL+/- of N bit | $\mathrm{t}_{\mathrm{T} \times \mathrm{O}} \mathrm{N}$ | $-0.1845 \times \mathrm{UI}$ <br> $+\mathrm{UII} \times \mathrm{N}$ | $\mathrm{UI} \mathrm{\times N}$ | $0.1845 \times \mathrm{UI}$ <br> $+\mathrm{UI} \times \mathrm{N}$ | sec |  |

4) Power-On / Off Sequence

Power-On Sequence
Fig. 12 shows power-on sequence of BU7963GUW.


Fig.12. Power-On / Off Sequence

Table 15. Power-On Sequence Timing
$\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{DVDD}=\mathrm{MS}$ VDD $=1.80 \mathrm{~V}$, and $\mathrm{DGND}=\mathrm{MSGND}=0.00 \mathrm{~V}$, unless otherwise noted.

| Parameter | Symbol | Limits |  |  | Unit | Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| Core power supply startup time | $\mathrm{t}_{\text {TX_VDD_IOV }}$ | 0.0 | - | 2 | ms |  |
| Reset Valid After Power Supplied | $\mathrm{t}_{\text {TX_VDD_XSD }}$ | 10 | - | - | $\mu \mathrm{s}$ |  |
| PCLK clock input startup time | $\mathrm{t}_{\text {TX_IN_VAL }}$ | 10 | - | - | $\mu \mathrm{s}$ |  |
| MSDL3 output delay time | $\mathrm{t}_{\text {TX_OUT_VAL }}$ | - | - | 2 | ms |  |

Power-Off Sequence
Fig. 13 shows the power-off sequence of BU7963GUW.


Tx: BU7963GUW Rx: BU7964GUW
Fig.13. Power-Off Sequence
Table 16. Power-Off Sequence Timing
$\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{DVDD}=\mathrm{MSVDD}=1.80 \mathrm{~V}$, and $\mathrm{DGND}=\mathrm{MSGND}=0.00 \mathrm{~V}$, unless otherwise noted.

| Parameter |  | Symbol | Limits |  |  | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
|  |  |  | Min | Typ | Max |  |  |
| MSDL3 output delay time | $\mathrm{t}_{\text {TX_OUT_INV }}$ | - | - | 100 | $\mu \mathrm{~s}$ |  |
| XSD hold time | $\mathrm{t}_{\text {TX_XSD_VDD }}$ | 10 | - | - | $\mu \mathrm{s}$ |  |
| Core power off time | $\mathrm{t}_{\text {TX_VDD_IOV }}$ | 0.0 | - | 2 | ms |  |

Frequency Change Sequence
Fig. 14 shows the frequency change sequence of BU7963GUW.


Fig.14. Frequency Change Sequence
Table 17. Frequency Change Sequence
$\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{DVDD}=\mathrm{MSVDD}=1.80 \mathrm{~V}$, and $\mathrm{DGND}=\mathrm{MSGND}=0.00 \mathrm{~V}$, unless otherwise noted.

| Parameter | Symbol | Limits |  |  | Unit | Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| PCLK Clock Input Suspend Time | $\mathrm{t}_{\text {TX_XSD_OUT }}$ | 1.0 | - | - | $\mu \mathrm{s}$ |  |
| PCLK Clock Input Restart Time | $\mathrm{t}_{\text {TX_I__XSD }}$ | 1.0 | - | - | $\mu \mathrm{s}$ |  |
| Control Signal Hold Time | $\mathrm{t}_{\text {TX_XSD_CTL }}$ | 2.0 | - | - | $\mu \mathrm{s}$ |  |
| Control Signal Setup Time | $\mathrm{t}_{\text {TX_CTL_XSD }}$ | 2.0 | - | - | $\mu \mathrm{s}$ |  |

## -High-speed Channel Characteristic

Table 18. High-speed channel characteristic

| Ta $=25^{\circ} \mathrm{C}$, DVDD=MSVDD $=1.80 \mathrm{~V}$ and DGND=MSGND=0.00V, unless otherwise noted. |
| :--- |
| Parameter  Symbol Limits   Unit |



Differential (OutP-OutN)


Fig.15. High-Speed Channel Electrical Characteristics
Fig. 16 shows high-speed channel equivalent schematic.


Fig.16. high-speed channel equivalent schematic.

## - Application Circuit Example



Fig.17. Application circuit

## - PCB Layout for MSDL3

The following points should be considered about the wiring for PCB of MSDL3.

- Wire for the PCB wiring pattern of high-speed channel (CLK, D0+/-, D1+/-, D2+/-) as short as possible.
- The PCB wiring for high-speed channel must not use the through-hole.
- Do not bend the wiring for high-speed channel squarely.
- Make the wiring length of each high-speed channel the same length (within 0.5 mm ).


## - Ordering Part Number



Part No.


Part No.


Package GUW: VBGA063W050


Packaging and forming specification E2: Embossed tape and reel

## VBGA063W050



## Notice

## Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ${ }^{(N o t e}{ }^{1}$ ), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.
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| CLASSIII | CLASSIII | CLASS II b | CLASSIII |
|  |  | CLASSIII |  |

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3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
[a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
[b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
[c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl 2 , $\mathrm{H}_{2} \mathrm{~S}, \mathrm{NH}_{3}, \mathrm{SO}_{2}$, and $\mathrm{NO}_{2}$
[d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
[e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
[f] Sealing or coating our Products with resin or other coating materials
[g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
[h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
[a] the Products are exposed to sea winds or corrosive gases, including $\mathrm{Cl} 2, \mathrm{H} 2 \mathrm{~S}, \mathrm{NH} 3, \mathrm{SO} 2$, and NO 2
[b] the temperature or humidity exceeds those recommended by ROHM
[c] the Products are exposed to direct sunshine or condensation
[d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

## Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

## Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

## Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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