Multifunction LCD Segment Driver

BU97500KV MAX 204 segments (SEG51×COM4)

●Features

- Integrated RAM for display data (DDRAM): 51 x 4bit (Max 204 Segment)
- LCD drive output: 4 Common output, Max 51Segment output
- Segment/GPO (Max 4port) output mode selectable
- Support standby mode
- Integrated Power-on Reset circuit
- Integrated Oscillator circuit
- No external component
- Low power consumption design
- Independent power supply for LCD driving

●Applications

- Telephone
- FAX
- Portable equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car audio
- Home electrical appliance
- Meter equipment

etc.

●Key Specifications

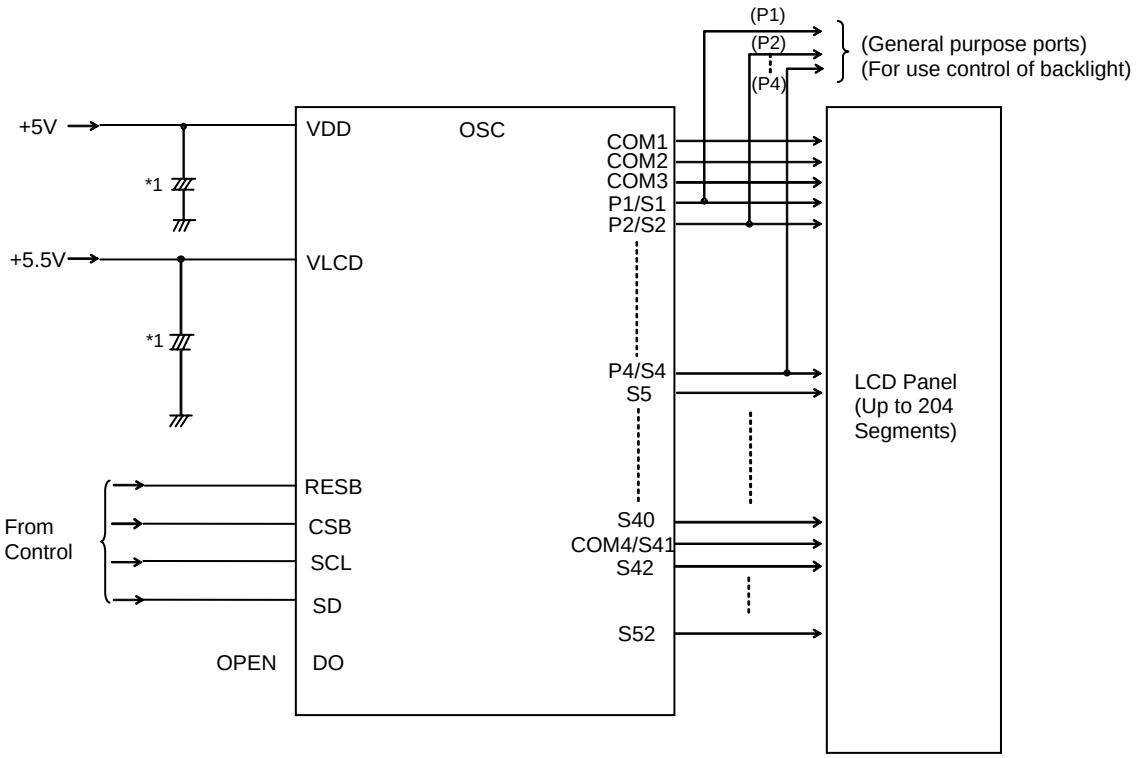
Supply Voltage Range:	+2.7V to +5.5V
LCD drive power supply Range:	+4.5V to +5.5V
Operating Temperature Range:	-40°C to +85°C
Max Segments:	204 Segments
Display Duty:	1/3, 1/4 selectable
Bias:	1/2, 1/3 selectable
Interface:	3wire serial interface

●Package

W (Typ.) x D (Typ.) x H (Max.)

VQFP64
12.00mm x 12.00mm x 1.60mm

●Typical Application Circuit



*1 Insert capacitors between VDD and VSS
C≥0.1uF

Figure 1. Typical application circuit

○Product structure：Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays.

●Block Diagram / Pin Configuration / Pin Description

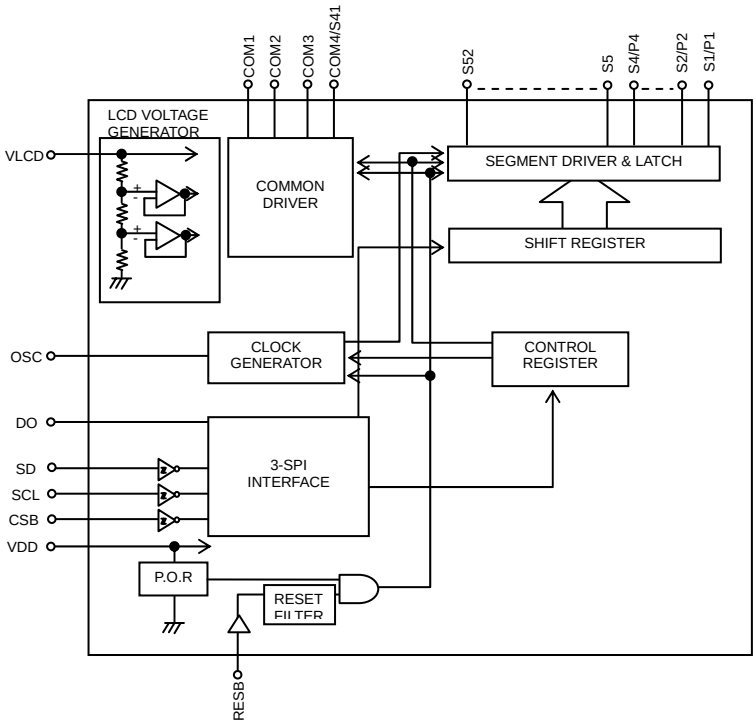


Figure 2. Block Diagram

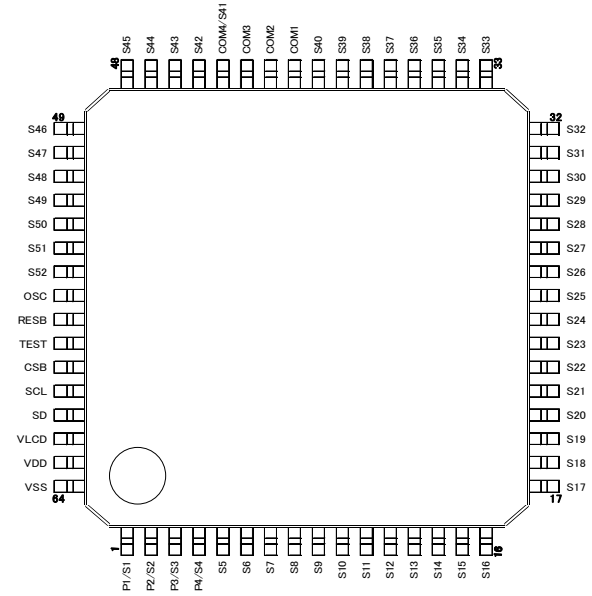


Figure 3. Pin Configuration (TOP VIEW)

Table 1 Pin Description

Terminal	Terminal No.	I/O	Unused case	Function
CSB	59	I	VDD	Chip select : “L” active
SCL	60	I	VSS	Serial data transfer clock
SD	61	I	VSS	Input serial data
VDD	63	-	-	Power Supply for the logic
OSC	56	I/O	OPEN/VSS	External clock input terminal Supported Hi-Z input if the internal clock mode.
VSS	64	-	-	GND
VLCD	62	-	-	Power Supply for the LCD driver
COM1 to 3	41 to 43	O	OPEN	COMMON output for LCD driving
COM4/S41	44	O	OPEN	COMMON / SEGMENT output for LCD driving Assigned as SEGMENT output in 1/3Duty mode.
S1/P1 to S4/P4	1 to 4	O	OPEN	SEGMENT output for LCD driving / General Purpose output
S5 to S40 S42 to S52	5 to 40 45 to 55	O	OPEN	SEGMENT output for LCD driving
RESB	57	I	VDD	Reset Input: RESB=“L” : Display is disabled RESB=“H” : Display is controllable NOTE) 3-SPI is NOT available if RESET is “L”.
DO	58	O	OPEN	Output for manufacturing test:

●**Absolute Maximum Ratings (VSS=0V)**

Parameters	Symbol	Ratings	Unit	Remarks
Power Supply voltage 1	VDD	-0.5 to +7.0	V	Power supply
Power Supply voltage 2	VLCD	-0.5 to +7.0	V	LCD drive voltage
Power Dissipation	Pd	1.0*1	W	
Input voltage range	VIN	-0.5 to VDD+0.5	V	
Operating temperature range	Topr	-40 to +85	°C	
Storage temperature range	Tstg	-55 to +125	°C	

*1 When operated higher than Ta=25°C, subtract 10mW per degree. (Using ROHM standard board)
(Board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)

●**Recommended Operating Ratings(Ta=-40°C to +85°C,VSS=0V)**

Parameters	Symbol	Ratings			Unit	Remarks
		MIN	TYP	MAX		
Power Supply voltage 1	VDD	2.7	-	5.5	V	Power supply
Power Supply voltage 2	VLCD	4.5	-	5.5	V	LCD driver voltage

Note. The power supply condition shall be met VLCD ≥ VDD.

●**Electrical Characteristics**

DC Characteristics (Unless otherwise indicated, VDD=2.7 to 5.5V, VLCD=4.5 to 5.5V, VSS=0V, Ta=-40°C to +85°C)

Parameters	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
“H” Input Voltage	VIH	0.7VDD	-	VDD	V	SD, SCL, CSB, RESB, OSC
“L” Input Voltage	VIL	VSS	-	0.3VDD	V	SD, SCL, CSB, RESB, OSC
“H” Input Current	IIH			5.0	μA	SD,SCL,CSB,RESB, OSC VI=5.5V
“L” Input Current	IIL	-5.0			μA	SD,SCL,CSB,RESB, OSC VI=0V
“H” Level Output Voltage	VOH1	VLCD -1.0			V	P1 to P4, Io=1mA
	VOH2	VLCD -1.0				S1 to S52, Io=20μA
	VOH3	VLCD -1.0				COM1 to COM4, Io=100μA
“L” Level Output Voltage	VOL1	-	-	1.0	V	P1 to P4, Io=1mA
	VOL2	-	-	1.0		S1 to S52, Io=20μA
	VOL3	-	-	1.0		COM1 to COM4, Io=100μA
LCD Bias Voltage	VMID1	1/2VLCD -1.0	-	1/2VLCD +1.0	V	S1 to S52 1/2 Bias, Io=±100μA
	VMID2	1/2VLCD -1.0	-	1/2VLCD +1.0		COM1 to COM4 1/2 Bias, Io=±100μA
	VMID3	2/3VLCD -1.0	-	2/3VLCD +1.0		S1 to S52 1/3 Bias, Io=±20μA
	VMID4	1/3VLCD -1.0	-	1/3VLCD +1.0		S1 to S52 1/3 Bias, Io=±20μA
	VMID5	2/3VLCD -1.0	-	2/3VLCD +1.0		COM1 to COM4 1/3Bias, Io=±100μA
	VMID6	1/3VLCD -1.0	-	1/3VLCD +1.0		COM1 to COM4 1/3 Bias, Io=±100μA
Current consumption	IstVDD	-	1	5	μA	Input Pin ALL ”L” Display off, Disable oscillator
	IstVLCD	-	1	5		Input Pin ALL ”L” Display off, Disable oscillator
	IVDD1	-	2	10		VDD=VLCD=5.0V, Output unloaded fFR=80Hz
	IVLCD1	-	40	95		VDD=VLCD=5.0V,Output unloaded 1/2 Bias, fFR=80Hz
	IVLCD2	-	65	140		VDD=VLCD=5.0V, Output unloaded 1/3 Bias, fFR=80Hz

●**Electrical Characteristics – continued**

Oscillation Characteristics (Ta=-40°C to +85°C, VDD=2.7 to 5.5V, VLCD=4.5V to 5.5V, VSS=0V)

Parameters	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Frame Frequency	fFR	56	80	104	Hz	fFR = 80Hz setting, 1/4 Duty setting

MPU interface Characteristics (Ta=-40 to +85°C, VDD=2.7V to 5.5V, VLCD=4.5 to 5.5V, VSS=0V)

Parameters	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input Rise Time	tr	-	-	80	ns	
Input Fall Time	tf	-	-	80	ns	
SCL Cycle Time	tSCYC	400	-	-	ns	
“H” SCL Pulse Width	tSHW	100	-	-	ns	
“L” SCL Pulse Width	tSLW	100	-	-	ns	
SD Setup Time	tSDS	20	-	-	ns	
SD Hold Time	tSDH	20	-	-	ns	
CSB Setup Time	tCSS	50	-	-	ns	
CSB Hold Time	tCSH	50	-	-	ns	
“H” CSB Pulse Time	tCHW	50	-	-	ns	

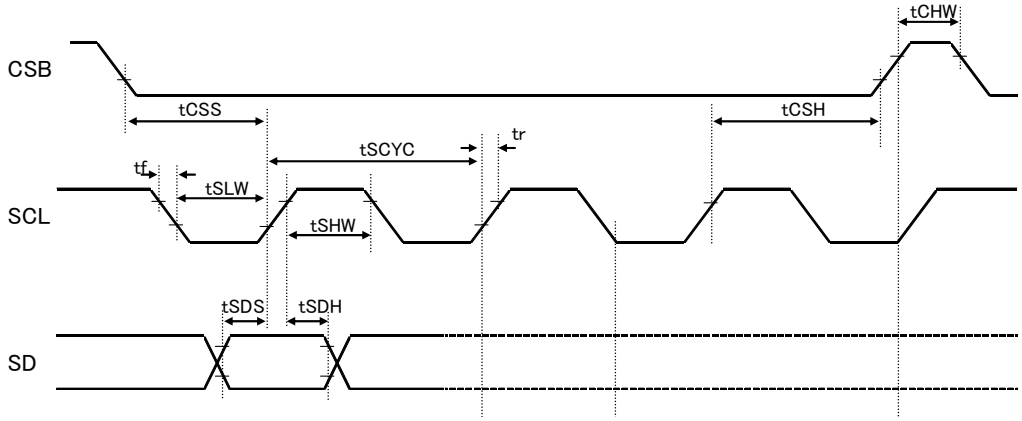


Figure 4. Serial interface Timing

Reset Timing characteristics (Ta=-40 to +85°C, VDD=2.7V to 5.5V, VLCD=4.5 to 5.5V, VSS=0V)

Item	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input Rise Time	tr	-	-	80	ns	
Input Fall Time	tf	-	-	80	ns	
Reset Pulse Width	tRW	3	-	-	us	
Reset Release Time	tRT	1	-	-	ms	

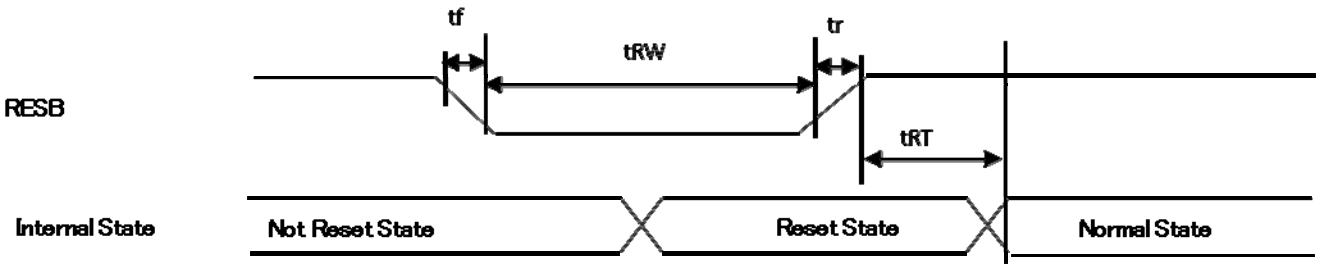


Figure 5. Reset Timing

●**I/O equivalent circuit**

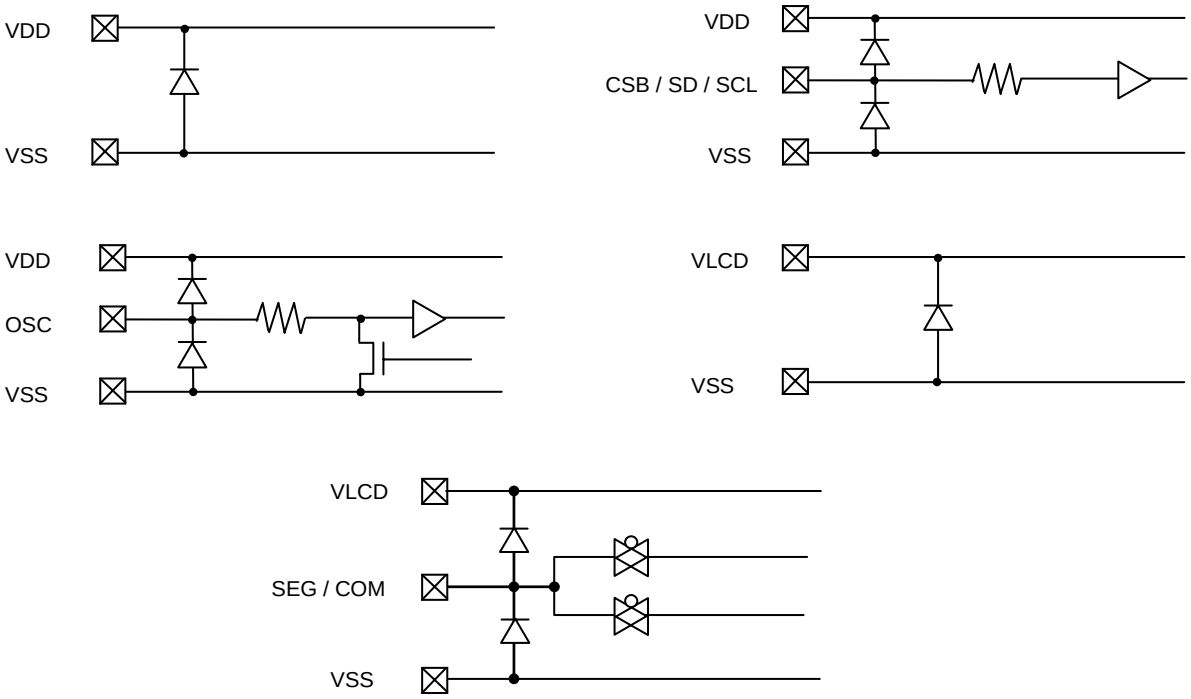
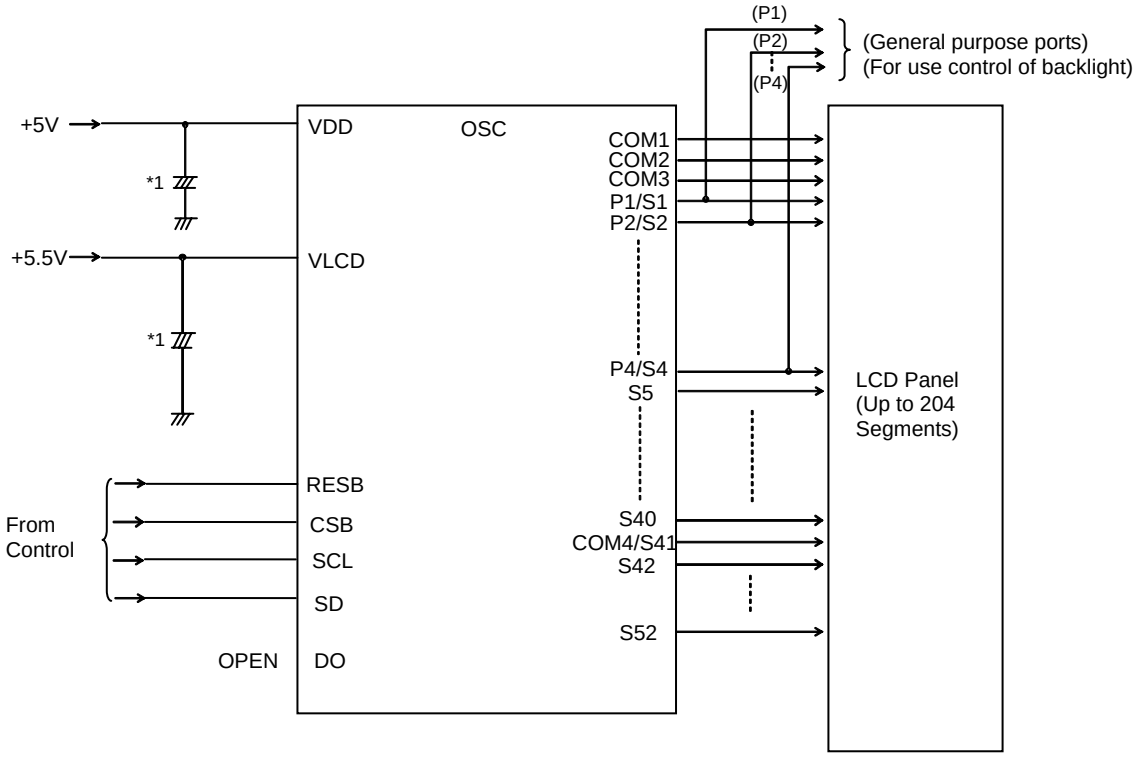


Figure 6. I/O equivalent circuit

●**Example of recommended circuit**



*1 Insert capacitors between VDD and VSS
C≥0.1uF

Figure 7. Example of recommended circuit

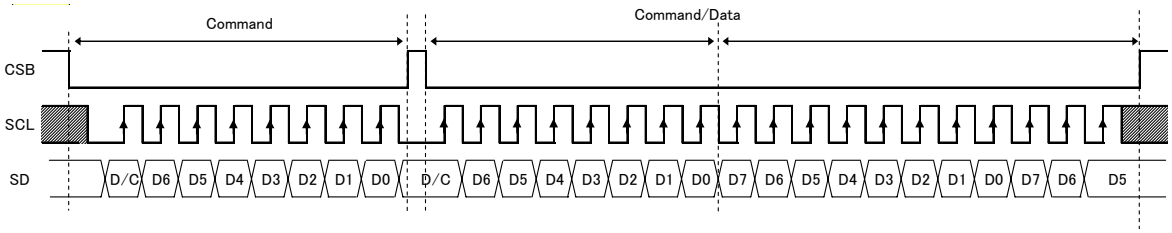
●Function descriptions

○Command and Data Transfer Method

○3-SPI (3-wire Serial Interface)

This device is controlled by a 3-wire signal (CSB, SCL, and SD).
First, Interface counter is initialized with CSB="H"
Setting CSB="L", enables SD and SCL inputs.
The protocol of 3-SPI transfer is shown as follows.
Each command starts with Command or Data judgment bit (D/C) as MSB data,
followed by D6 to D0 (this is while CSB ="L").
(Internal data is latched at the rising edge of SCL, then the data is converted to an 8-bit parallel data at the falling edge of the 8th CLK.)

<Write command/Data>



D/C = "H" : Command D/C = "L" : Data

Figure 8. 3-SPI Data Transfer Format

○Command Transfer Method

After CSB="H"→"L", the 1st byte shall be a command.
The MSB of the command input data will determine if the next byte data is either a command or display data.
This bit is called "command or data judgment bit".
When set "command or data judge bit"='1', the next byte will be (continuously) a command.
When set "command or data judge bit"='0', the following bytes will be display data bytes.

Command	Command	Command	Command	Display Data	…

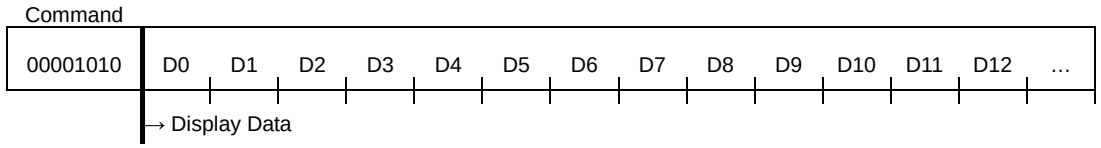
(DATAWR)

During display data transfer mode, setting D/C=1 will not revert it back to a command input mode..
To revert to a command input mode, set CSB="L"→"H"→"L".
(CSB "L"→"H" will cancel data transfer mode.)
Command transfer is done by 8bits unit, so if CSB="L"→"H" with less than 8bits data transfer, the command is cancelled.
It will be able to transfer command when CSB="L" .

○Display data transfer method

This LSI has Display Data RAM (DDRAM) of 51×4=204bit.

The relationship between data input and display data, DDRAM data and address are as follows.



The address to be written is the address specified by ADSET command, and the address is automatically incremented in every 4bit data if 1/4 Duty mode or in every 3 bit if 1/3 Duty mode respectively.

(1)1/3 Duty Mode

DDRAM Address/Segment Outputs

BIT	00h	01h	02h	03h	04h	····	31h	32h	33h	
0	D0	D3	D6	D9	D12		D148	D151	D154	COM1
1	D1	D4	D7	D10	D13		D149	D152	D155	COM2
2	D2	D5	D8	D11	D14		D150	D153	D156	COM3
	S1	S2	S3	S4	S5		S50	S51	S52	

Transferred data is written to the DDRAM by every 3bit. The write operation is cancelled if it changes CSB="L"→"H" before 3bits data transfer.

(2)1/4 Duty Mode

DDRAM Address/ Segment Outputs

BIT	00h	01h	02h	03h	04h	····	30h	31h	32h	
0	D0	D4	D8	D12	D16		D193	D197	D201	COM1
1	D1	D5	D9	D13	D17		D194	D198	D202	COM2
2	D2	D6	D10	D14	D18		D195	D199	D203	COM3
3	D3	D7	D11	D15	D19		D196	D200	D204	COM4
	S1	S2	S3	S4	S5		S50	S51	S52	

Transferred Data is written to the DDRAM by every 4bit. The write operation is cancelled if it changes CSB="L"→"H" before 4bits data transfer.

○Relationship between Display Data and Segment Output Pins

(1) 1/3 Duty Mode

output terminal	COM1	COM2	COM3	address
S1/P1	D1	D2	D3	00
S2/P2	D4	D5	D6	01
S3/P3	D7	D8	D9	02
S4/P4	D10	D11	D12	03
S5	D13	D14	D15	04
S6	D16	D17	D18	05
S7	D19	D20	D21	06
S8	D22	D23	D24	07
S9	D25	D26	D27	08
S10	D28	D29	D30	09
S11	D31	D32	D33	0A
S12	D34	D35	D36	0B
S13	D37	D38	D39	0C
S14	D40	D41	D42	0D
S15	D43	D44	D45	0E
S16	D46	D47	D48	0F
S17	D49	D50	D51	10
S18	D52	D53	D54	11
S19	D55	D56	D57	12
S20	D58	D59	D60	13
S21	D61	D62	D63	14
S22	D64	D65	D66	15
S23	D67	D68	D69	16
S24	D70	D71	D72	17
S25	D73	D74	D75	18
S26	D76	D77	D78	19

output terminal	COM1	COM2	COM3	address
S27	D79	D80	D81	1A
S28	D82	D83	D84	1B
S29	D85	D86	D87	1C
S30	D88	D89	D90	1D
S31	D91	D92	D93	1E
S32	D94	D95	D96	1F
S33	D97	D98	D99	20
S34	D100	D101	D102	21
S35	D103	D104	D105	22
S36	D106	D107	D108	23
S37	D109	D110	D111	24
S38	D112	D113	D114	25
S39	D115	D116	D117	26
S40	D118	D119	D120	27
COM4/S41	D121	D122	D123	28
S42	D124	D125	D126	29
S43	D127	D128	D129	2A
S44	D130	D131	D132	2B
S45	D133	D134	D135	2C
S46	D136	D137	D138	2D
S47	D139	D140	D141	2E
S48	D142	D143	D144	2F
S49	D145	D146	D147	30
S50	D148	D149	D150	31
S51	D151	D152	D153	32
S52	D154	D155	D156	33

NOTE: In case of S1/P1 to S4/P4 and COM4/S41 are selected for segment output.

For example, S11 output case

Bits in a DDRAM			Segment Output Pin (S11)
D31	D32	D33	
0	0	0	Off-state of the LCD elements corresponding to COM1,2 and 3
0	0	1	On-state of the LCD element corresponding to COM3
0	1	0	On-state of the LCD element corresponding to COM2
0	1	1	On-state of the LCD elements corresponding to COM2 and 3
1	0	0	On-state of the LCD element corresponding to COM1
1	0	1	On-state of the LCD elements corresponding to COM1 and 3
1	1	0	On-state of the LCD elements corresponding to COM1 and 2
1	1	1	On-state of the LCD elements corresponding to COM1,2 and 3

(2) 1/4 duty

output terminal	COM1	COM2	COM3	COM4	address
S1/P1	D1	D2	D3	D4	00
S2/P2	D5	D6	D7	D8	01
S3/P3	D9	D10	D11	D12	02
S4/P4	D13	D14	D15	D16	03
S5	D17	D18	D19	D20	04
S6	D21	D22	D23	D24	05
S7	D25	D26	D27	D28	06
S8	D29	D30	D31	D32	07
S9	D33	D34	D35	D36	08
S10	D37	D38	D39	D40	09
S11	D41	D42	D43	D44	0A
S12	D45	D46	D47	D48	0B
S13	D49	D50	D51	D52	0C
S14	D53	D54	D55	D56	0D
S15	D57	D58	D59	D60	0E
S16	D61	D62	D63	D64	0F
S17	D65	D66	D67	D68	10
S18	D69	D70	D71	D72	11
S19	D73	D74	D75	D76	12
S20	D77	D78	D79	D80	13
S21	D81	D82	D83	D84	14
S22	D85	D86	D87	D88	15
S23	D89	D90	D91	D92	16
S24	D93	D94	D95	D96	17
S25	D97	D98	D99	D100	18
S26	D101	D102	D103	D104	19

output terminal	COM1	COM2	COM3	COM4	address
S27	D105	D106	D107	D108	1A
S28	D109	D110	D111	D112	1B
S29	D113	D114	D115	D116	1C
S30	D117	D118	D119	D120	1D
S31	D121	D122	D123	D124	1E
S32	D125	D126	D127	D128	1F
S33	D129	D130	D131	D132	20
S34	D133	D134	D135	D136	21
S35	D137	D138	D139	D140	22
S36	D141	D142	D143	D144	23
S37	D145	D146	D147	D148	24
S38	D149	D150	D151	D152	25
S39	D153	D154	D155	D156	26
S40	D157	D158	D159	D160	27
S42	D161	D162	D163	D164	28
S43	D165	D166	D167	D168	29
S44	D169	D170	D171	D172	2A
S45	D173	D174	D175	D176	2B
S46	D177	D178	D179	D180	2C
S47	D181	D182	D183	D184	2D
S48	D185	D186	D187	D188	2E
S49	D189	D190	D191	D192	2F
S50	D193	D194	D195	D196	30
S51	D197	D198	D199	D200	31
S52	D201	D202	D203	D204	32

NOTE: In case of S1/P1 to S4/P4 are selected for segment output.

For example, S11 output case

Bits in the DDRAM				Segment Output Pin (S11)
D41	D42	D43	D44	
0	0	0	0	Off-state of the LCD elements corresponding to COM1,2 and 3
0	0	0	1	On-state of the LCD element corresponding to COM4
0	0	1	0	On-state of the LCD element corresponding to COM3
0	0	1	1	On-state of the LCD elements corresponding to COM3 and 4
0	1	0	0	On-state of the LCD element corresponding to COM2
0	1	0	1	On-state of the LCD elements corresponding to COM2 and 4
0	1	1	0	On-state of the LCD elements corresponding to COM2 and 3
0	1	1	1	On-state of the LCD elements corresponding to COM2,3 and 4
1	0	0	0	On-state of the LCD element corresponding to COM1
1	0	0	1	On-state of the LCD elements corresponding to COM1 and 4
1	0	1	0	On-state of the LCD elements corresponding to COM1 and 3
1	0	1	1	On-state of the LCD elements corresponding to COM1, 3 and 4
1	1	0	0	On-state of the LCD elements corresponding to COM1 and 2
1	1	0	1	On-state of the LCD elements corresponding to COM1,2 and 4
1	1	1	0	On-state of the LCD elements corresponding to COM1,2 and 3
1	1	1	1	On-state of the LCD elements corresponding to COM1,2 3 and 4

○OSCILLATOR

Several kinds of clock for logic and analog circuits are generated from internal oscillation circuit or external clock.
The OSC pins are open if the internal oscillator is used.

*To use external clock mode, please set in DRVCTRL1 command.

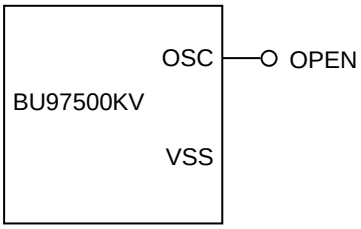


Figure 9. Internal clock mode

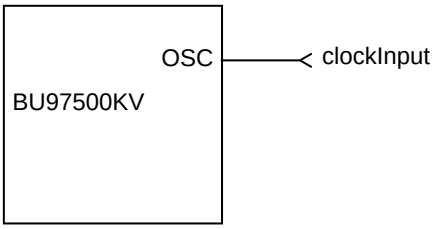


Figure 10. External clock mode

○LCD Driver Bias/Duty Circuit

This LSI generates LCD driving voltage with on-chip Buffer AMP.
And it can drive LCD at low power consumption.
* 1/3 or 1/2Bias and line or frame inversion mode can be selected by DRV CTRL2.
* 1/4 or 1/3Duty can be selected by DRV CTRL1 command.
Refer to “LCD waveform” about each LCD waveform.

○Reset initialize condition

Reset condition after execute Software Reset is as follows.
・Display is OFF.
・DDRAM address is initialized (DDRAM Data is not initialized).
Refer to “Detailed command description” about default value of each register.

●Command / Function List

Description List of Command / Function

NO	Command	Function
1	Sleep Control (SLP CTRL)	Select Normal mode / Sleep mode
2	Segment Control (SEG CTRL)	Select segment output / general purpose output
3	Drive Control1 (DRV CTRL1)	Duty setting, Frame frequency setting
4	Drive Control2 (DRV CTRL2)	Bias setting, LCD waveform setting
5	Drive Control3 (DRV CTRL3)	PIN setting
6	Software Reset (SWRST)	Software Reset
7	Display Control (DISCTRL)	Control display ON/OFF
8	Address Set (ADSET)	LCD display setting
9	Data Write (DATA WR)	Start RAM write

●Detailed command description

○Sleep Control (SLP CTRL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	P2	*	*

(* : Don't care)

P2: SLEEP CONTROL DATA
Normal Mode/Sleep Mode setting

Control bit	Mode	Internal Oscillator	Segment outputs Common outputs	Reset condition
P2				
0	Normal	enabled	L	
1	Sleep	disabled	L	○

○Segment Control (SEG CTRL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	P3	P2	P1	*

(* : Don't care)

P3 to P0: Segment Output / General purpose output mode selection

Control bits			Status of the pins				Reset condition
P3	P2	P1	S1/P1	S2/P2	S3/P3	S4/P4	
0	0	0	S1	S2	S3	S4	○
0	0	1	P1	S2	S3	S4	
0	1	0	P1	P2	S3	S4	
0	1	1	P1	P2	P3	S4	
1	0	0	P1	P2	P3	P4	

NOTE) Sn(n=1 to 4) : assigned as a Segment Output pin
Pn(n=1 to 4) : assigned as a General Purpose Output pin

Relationship of bit assignment between general purpose outputs pin and bit in DDRAM

Output Pin	Corresponding bit in DDRAM	
	1/3 Duty	1/4 Duty
S1/P1	D1	D1
S2/P2	D4	D5
S3/P3	D7	D9
S4/P4	D10	D13

In case of 1/4 Duty mode and S4/P4 is configured as a general purpose output pins,
S4/P4 is set to HIGH (VLCD level) if D13 is set to "1" in DDRAM.
S4/P4 is cleared to LOW (VSS level) if D13 is set to "0" in DDRAM.

○Drive Control (DRV CTRL1)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	P3	P2	P1	P0

P3: 1/3 Duty, 1/4 Duty selection

P3	Duty mode	Status of (COM4/ S41)	Reset condition
0	1/4	COM4	○
1	1/3	S41	

NOTE) COM4: COMMON output
S41: SEGMENT output

P2,P1 : Frame frequency setting

Setting	P2	P1	Reset condition
80Hz	0	0	○
100Hz	0	1	
120Hz	1	0	
External Clock input	1	1	

Relationships between Frame frequency (fFR), frequency (fosc) and Divide number

P2	P1	Divide number		fFR [Hz]	
		1/3 Duty	1/4 Duty	1/3 Duty	1/4 Duty
0	0	510	512	80	80
0	1	408	408	100	100
1	0	342	344	120	120
1	1	2040	2048	-	-

Formula to calculate Frame frequency from frequency and Divide number:
“Frame frequency = frequency / Divide number ”
Ex) In case, 1/4 Duty mode,(P2,P1) = (0,0)
fFR = 40.96[KHz] / 512 = 80[Hz]
NOTE: Built-in Oscillator circuit frequency = 40.96 KHz (typ).

P0 bit is reserved

P0	−	Reset condition
0	reserved	−

○Drive Control2 (DRV CTRL2)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	P3	P2	P1	P0

P2: 1/2 Bias, 1/3 Bias selection

P2	Bias mode	Reset condition
0	1/2	
1	1/3	○

P1: Inversion mode selection

P1	Inversion mode	Reset condition
0	Line	○
1	Frame	

P3, P0 bits are reserved

P3, P0	−	Reset condition
0	reserved	−

○Drive Control 3(DRV CTRL3)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	1	1	*	0

(* : Don't care)

Required to issue the command for pin configuration

○Display Control (DISCTRL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	P1	*

(* : Don't care)

P1: Display On/Off control

P1	Display status	Reset condition
1	ON	
0	OFF	○

○Software Reset (SWRST)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	0	0	1

This is the Software Reset command
After sending this command, each register and DDRAM address are initialized.

○Address Set (ADSET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
0	1	P5	P4	P3	P2	P1	P0

The value from 00(Hex) to the end of DDRAM address is valid and others will be set to 00(HEX).
The end of address is 33(HEX) if 1/3 Duty mode or 32(HEX) if 1/4 Duty mode respectively.
Refer to "Relationships between Display Data and Segment Output Pins"

○Data Write (DATAWR)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	0

Data transfer can be started by this command.
Set the CSB pin to High to terminate the data transfer
Refer to "Command/Data Transfer Method"

●LCD waveform

(1/4duty, 1/3bias)

Line inversion

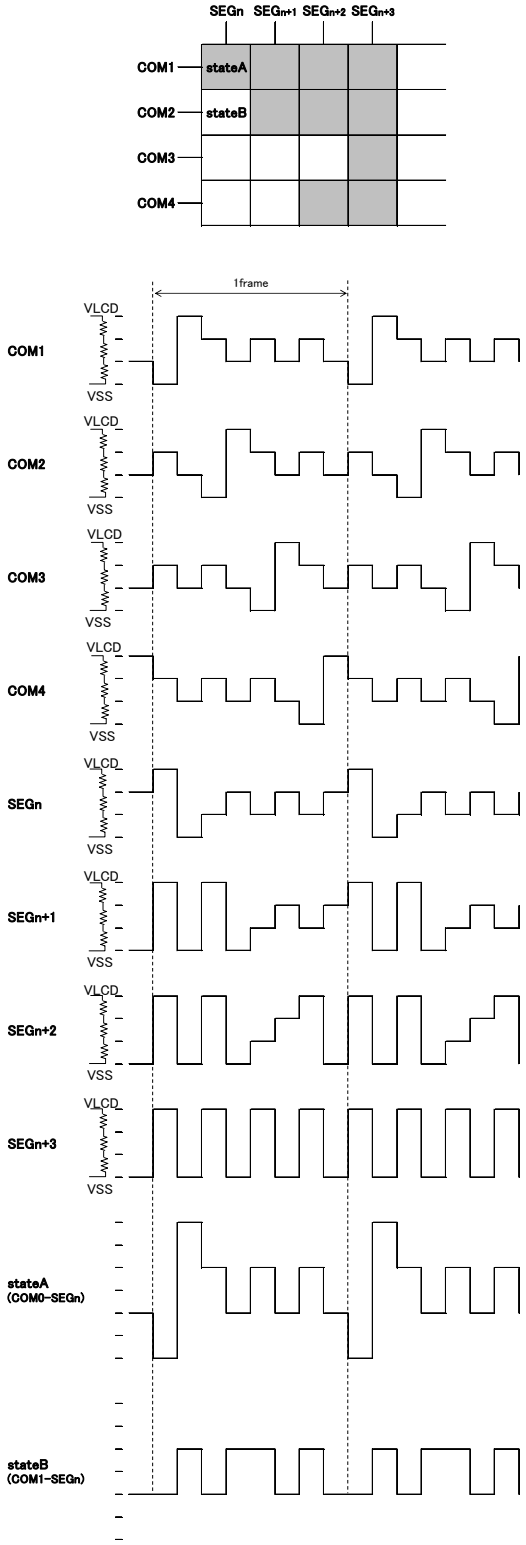


Figure 11. LCD waveform in line inversion

Frame inversion

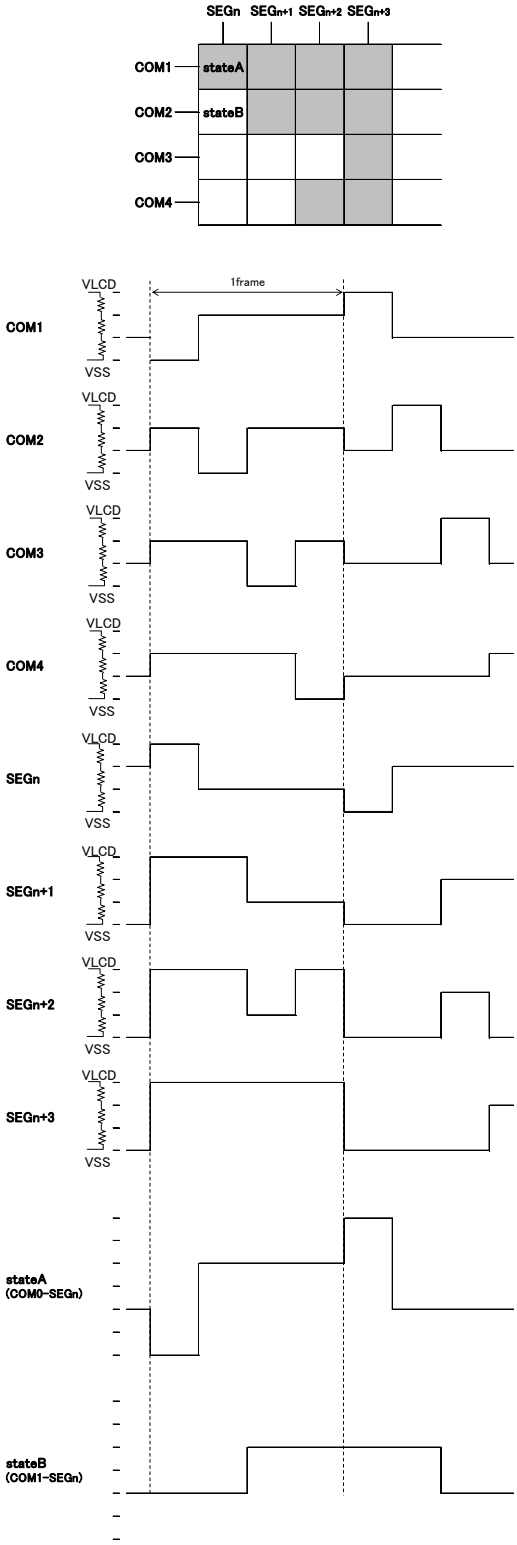


Figure 12. LCD waveform in frame inversion

(1/4duty, 1/2bias)

Line inversion

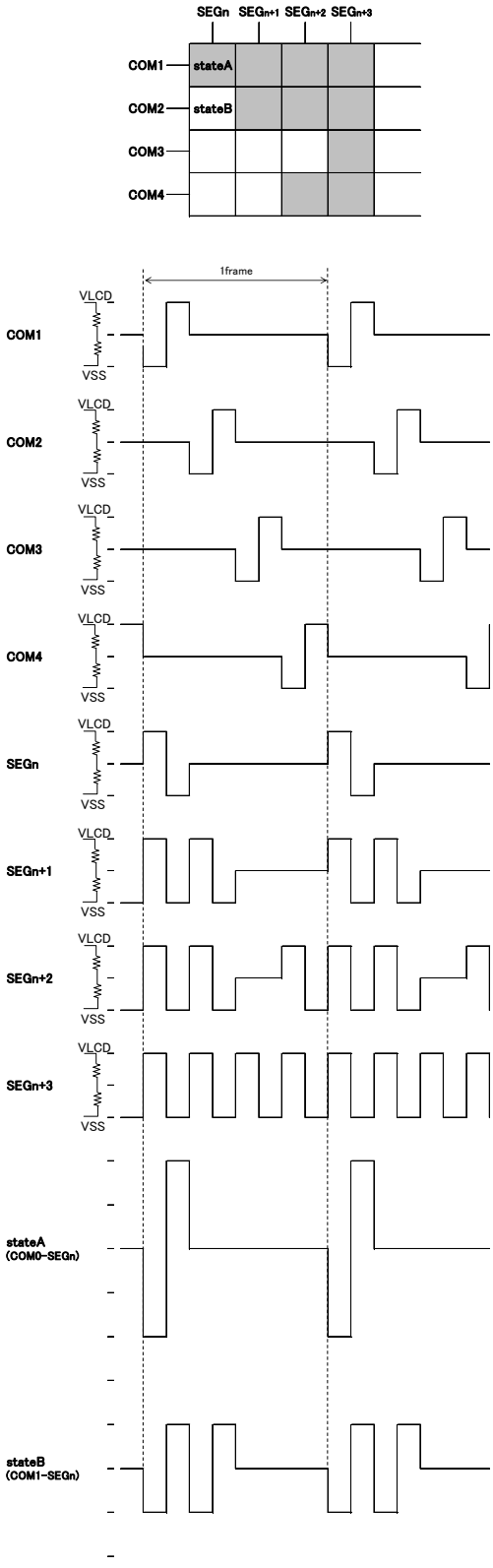


Figure 13. LCD waveform in line inversion

Frame inversion

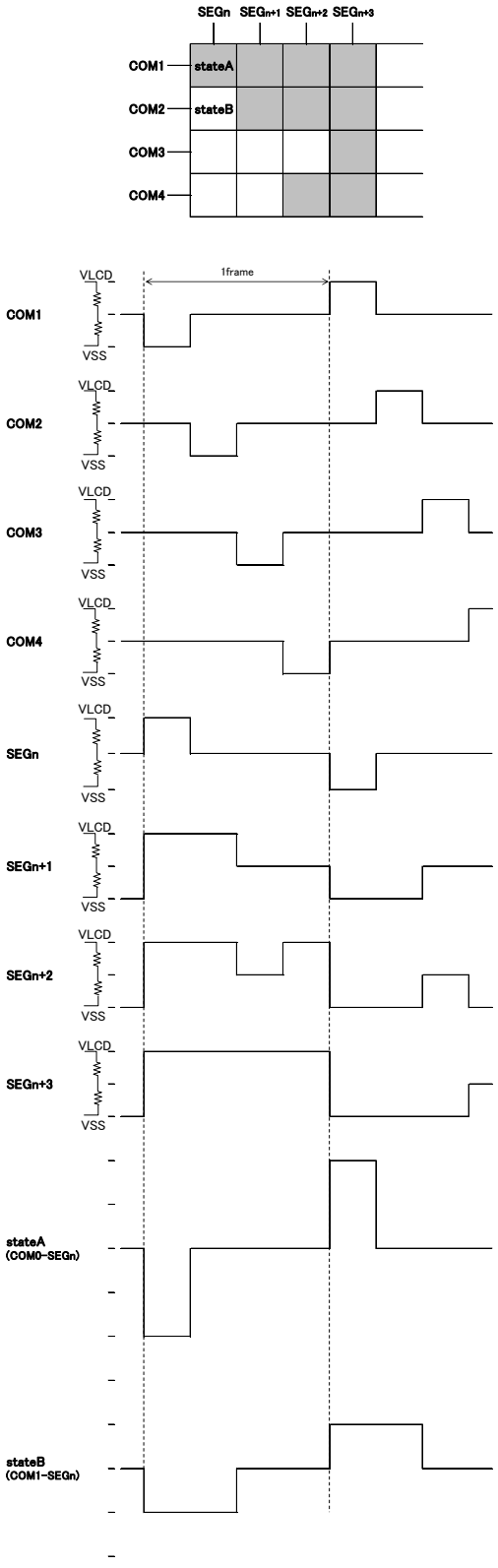


Figure 14. LCD waveform in frame inversion

(1/3duty, 1/3bias)

Line inversion

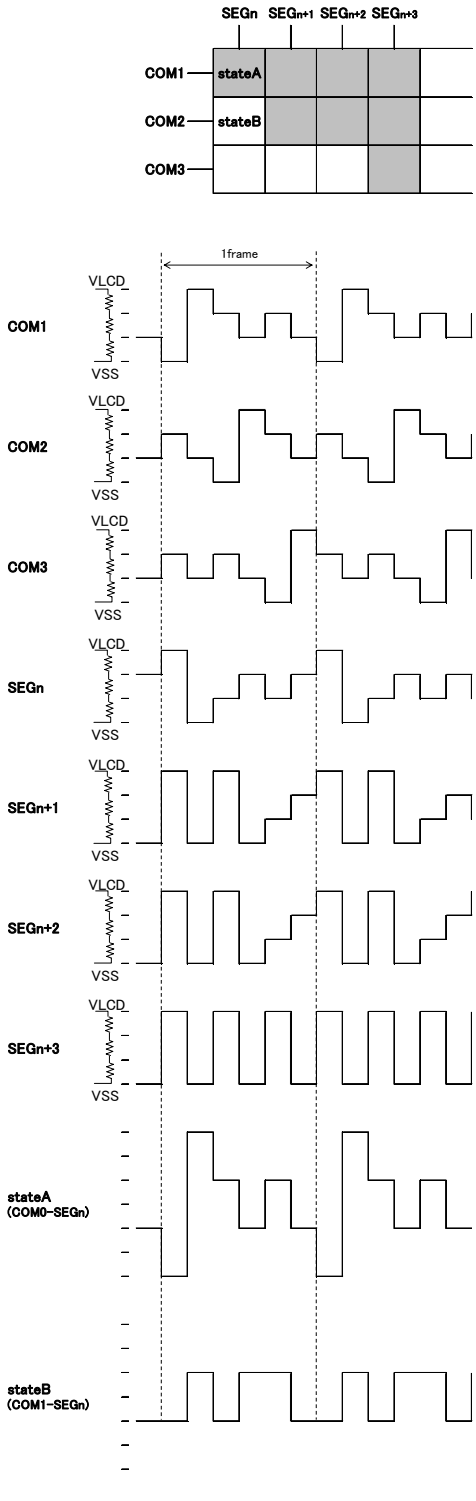


Figure 15. LCD waveform in line inversion

Frame inversion

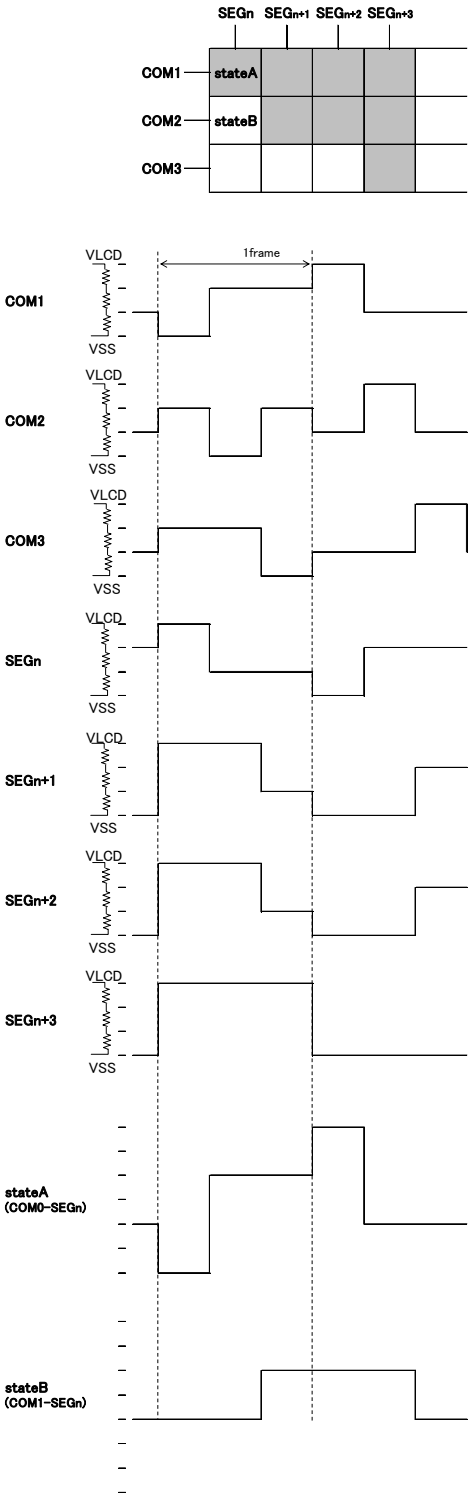


Figure 16. LCD waveform in frame inversion

(1/3duty, 1/2bias)

Line inversion

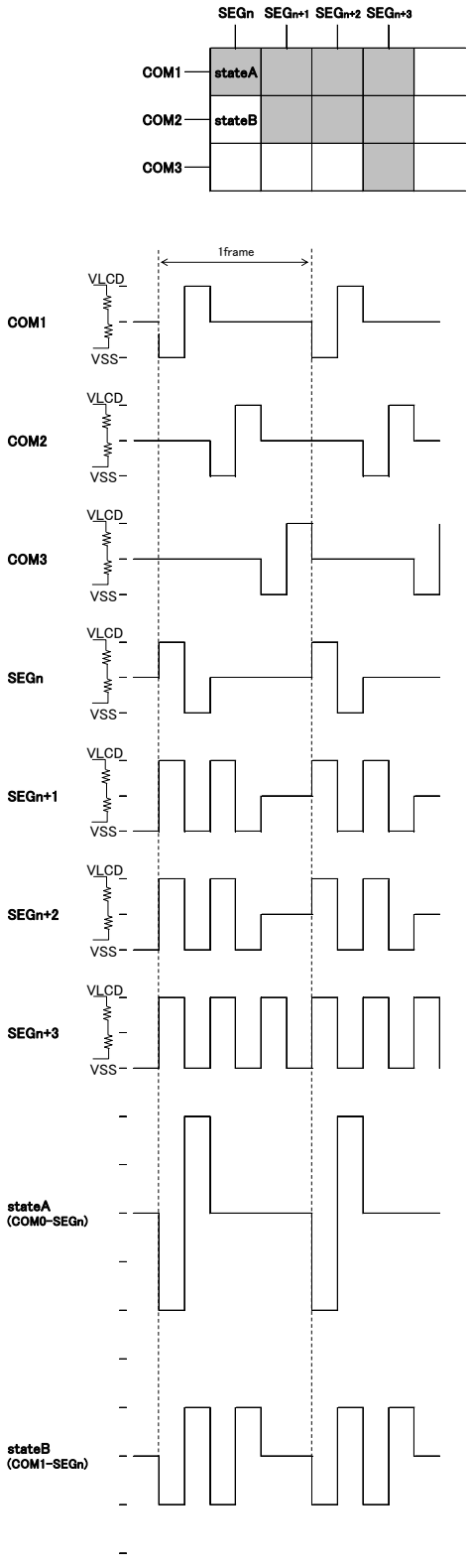


Figure 17. LCD waveform in line inversion

Frame inversion

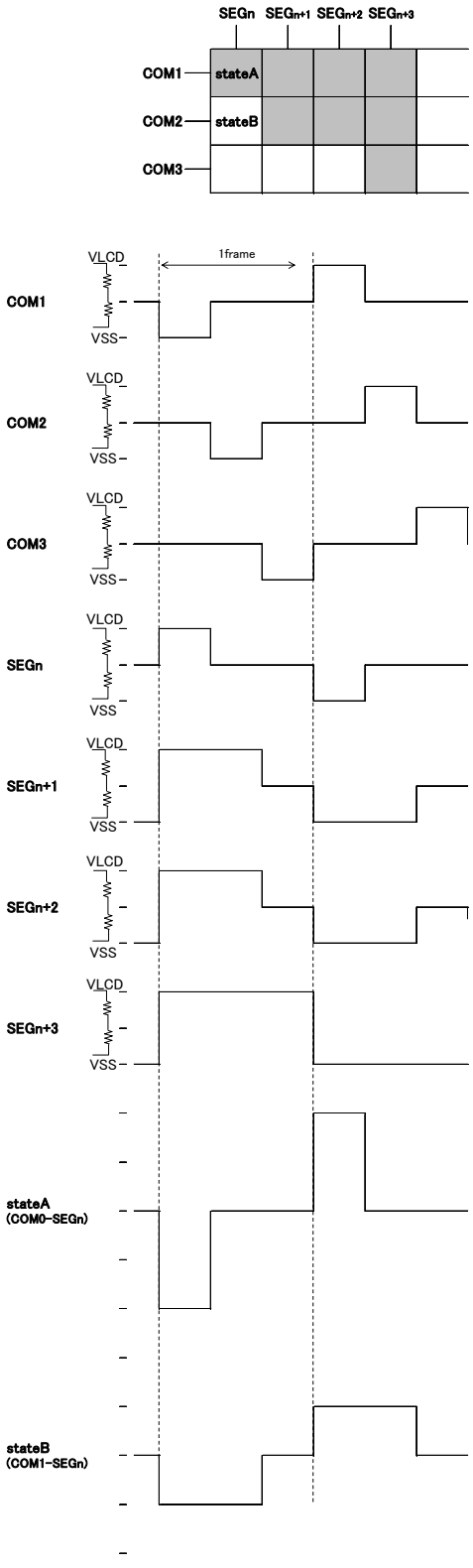


Figure 18. LCD waveform in frame inversion

●Initialize sequence

Recommended sequence after Power-On to set this device to initial condition.

(1) Software reset sequence

Power on
↓
CSB ‘H’ …Initialized I/F
↓
CSB ‘L’ …Start transferring I/F Data
↓
SWRST (execute Software Reset)
↓
DISCTRL (Display off)
↓
Set each Command
↓
DATA WR
↓
CSB ‘H’
↓
CSB ‘L’
↓
SLP CTRL
↓
DIS CTRL (Display on)
↓
Start display

(2) Hardware reset sequence

Power on
↓
RESB ‘L’
↓
RESB ‘H’
↓
CSB ‘H’ …Initialized I/F
↓
CSB ‘L’ …Start transferring I/F Data
↓
SWRST (execute Software Reset)
↓
DISCTRL (Display off)
↓
Set each Command
↓
DATA WR
↓
CSB ‘H’
↓
CSB ‘L’
↓
SLP CTRL
↓
DISCTRL (Display on)
↓
Start display

NOTE: Each register value and DDRAM address, DDRAM data are random condition after power on till initialize sequence is executed.

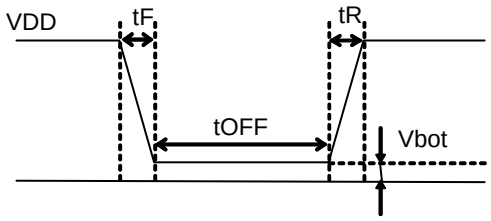
NOTE: Each register value and DDRAM address are reset by a hardware reset operation.
DDRAM cannot be reset by any resets.

●Cautions in Power-On Sequence

○Power-On Reset (POR) Circuit

This LSI has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Please follow the following recommended Power-On sequences to allow the reset action to complete.

1. Set the power up conditions to meet the recommended tR, tF, tOFF, and Vbot spec below in order to ensure P.O.R operation.



tR, tF, tOFF, Vbot recommended conditions

tR	tF	tOFF	Vbot
Less than 5ms	Less than 5ms	More than 150ms	Less than 0.1V

Figure 19. Power ON/OFF waveform

2. If it is difficult to meet above conditions, execute the following sequence after Power-On.
   (1) Set CSB to High
   (2) Clear CSB to Low and then issue a SWRST command.

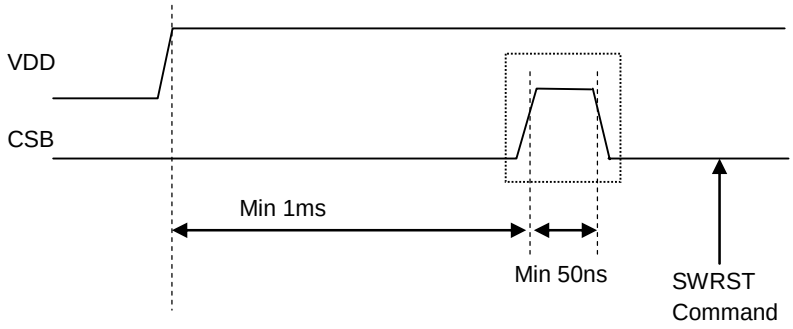


Figure 20. SWRST Command Sequence

○Power Up Sequence and Power Down Sequence
In power up sequence, VDD shall be turned on before VLCD.
In power down sequence, VDD shall be turned off after VLCD.

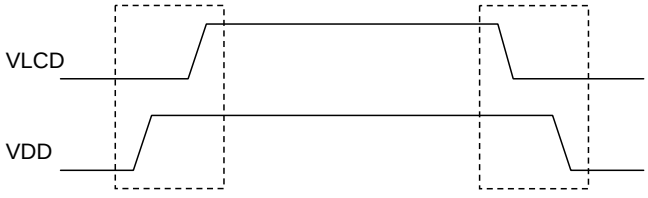


Figure 21. Power On/Off Sequence

●Operational Notes

(1) Absolute Maximum Ratings
Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

(2) Recommended Operating conditions
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse Connection of Power Supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

(4) Power Supply Lines
Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

(5) Ground Voltage
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

(6) Short between Pins and Mounting Errors
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

(7) Operation under Strong Electromagnetic Field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

(8) Testing on Application Boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(9) Regarding Input Pins of the IC
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the GND voltage should be avoided. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input terminals have voltages within the values specified in the electrical characteristics of this IC.

(10) GND Wiring Pattern
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

(11) External Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

(12) Unused Input Terminals
Input terminals of an IC are often connected to the gate of a CMOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or ground line.

(13) Rush current
When power is first supplied to the IC, rush current may flow instantaneously. It is possible that the charge current to the parasitic capacitance of internal photo diode or the internal logic may be unstable. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

●**Ordering Information**

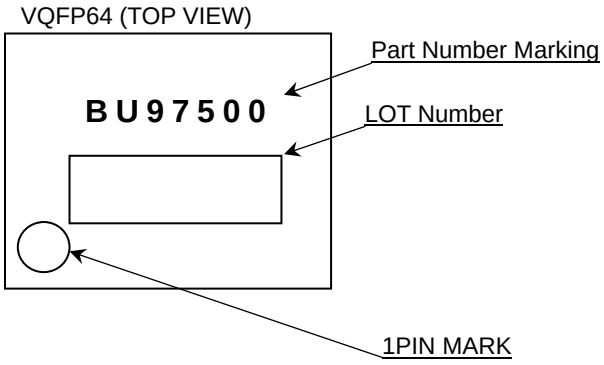
B U 9 7 5 0 0 K V	-	E 2

Part Number

Package
KV : VQFP64

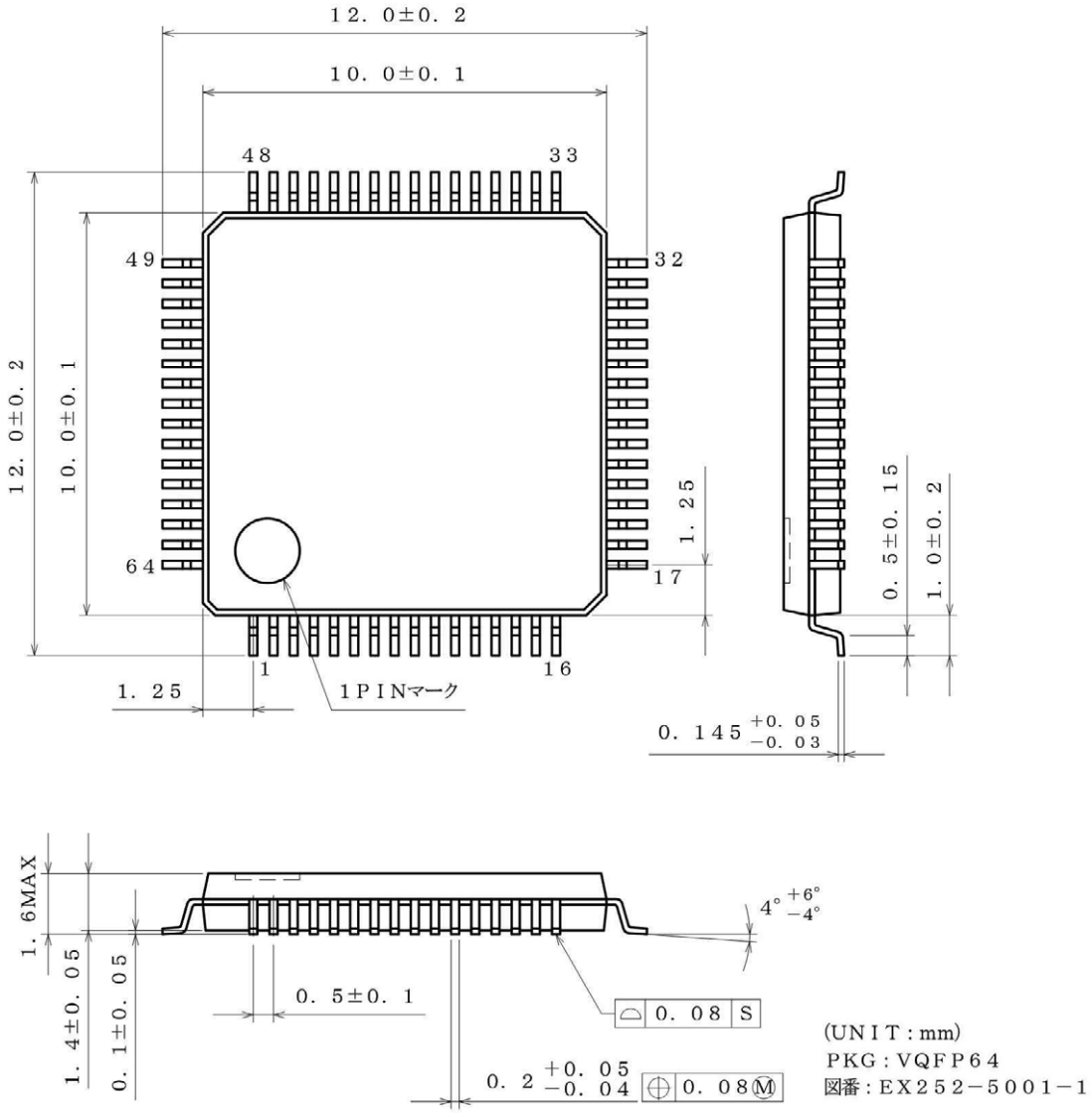
Packaging and forming specification
E2: Embossed tape and reel (VQFP64)

●**Marking Diagram**



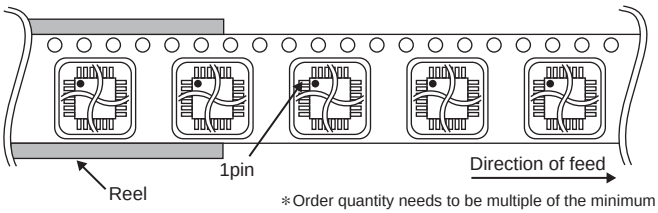
●**Physical Dimension, Tape and Reel Information**

Package Name	VQFP64



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●**Revision History**

Date	Revision	Changes
14.Mar.2012	001	New Release
8.Jan.2013	002	Improved the statement in all pages. Deleted “Status of this document” in page 21. Changed format of Physical Dimension, Tape and Reel Information

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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