Low Duty LCD Segment Drivers

BU97950AFUV MAX 280 segments (SEG35×COM8)

General Description

BU97950AFUV is a 1/8 or 1/4 duty general-purpose LCD driver that can be used for consumer / battery operated products and can drive up to 280 LCD Segments.
It has integrated display RAM for reducing CPU load. Also, it is designed with low power consumption and no external component needed.
It can support LCD contrast adjustment by its EVR function.

Key Specifications

- Supply Voltage Range: +2.5V to +6.0V
- LCD Drive Power Supply Range: +2.5V to +6.0V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 280 Segments
- Display Duty and Bias:
  1/4 Duty and 1/3 Bias,
  1/8 Duty and 1/4 Bias selectable
- Interface: 2wire serial interface

Features

- Integrated RAM for Display Data (DDRAM):
  35 x 8bit (Max 280 Segment)
- 1/8 or 1/4 Can be Selected with The Serial Control Data.
  1/8 duty drive: Up to 280 segments
  1/4 duty drive: Up to 156 segments
- Integrated Buffer AMP for LCD Driving
- Integrated Oscillator Circuit
- No External Components
- Low Power Consumption Design
- Independent Power Supply for LCD Driving
- Integrated Electrical Volume Register (EVR) function

Packages

W (Typ) x D (Typ) x H (Max)

TSSOP-C48V
8.1mm x 12.5mm x 1.0mm

Applications

- Metering
- Home Automation Goods
- White Goods, Small Appliances
- Healthcare Products
- Battery Operated Products

etc.

Typical Application Circuit

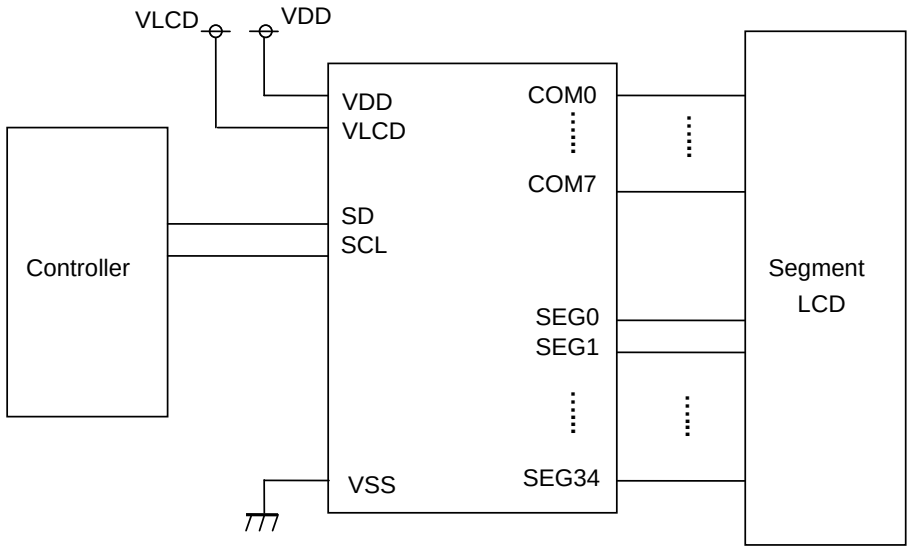


Figure 1. Typical Application Circuit

Block Diagram / Pin Configuration / Pin Description

BU97950AFUV (TSSOP-C48V)

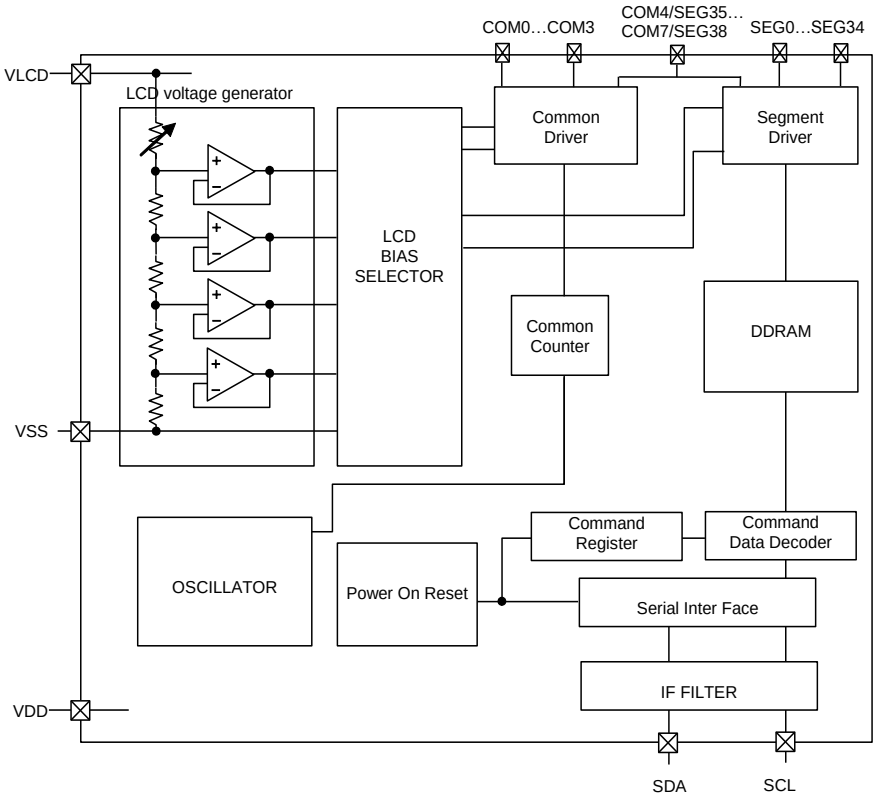


Figure 2. Block Diagram

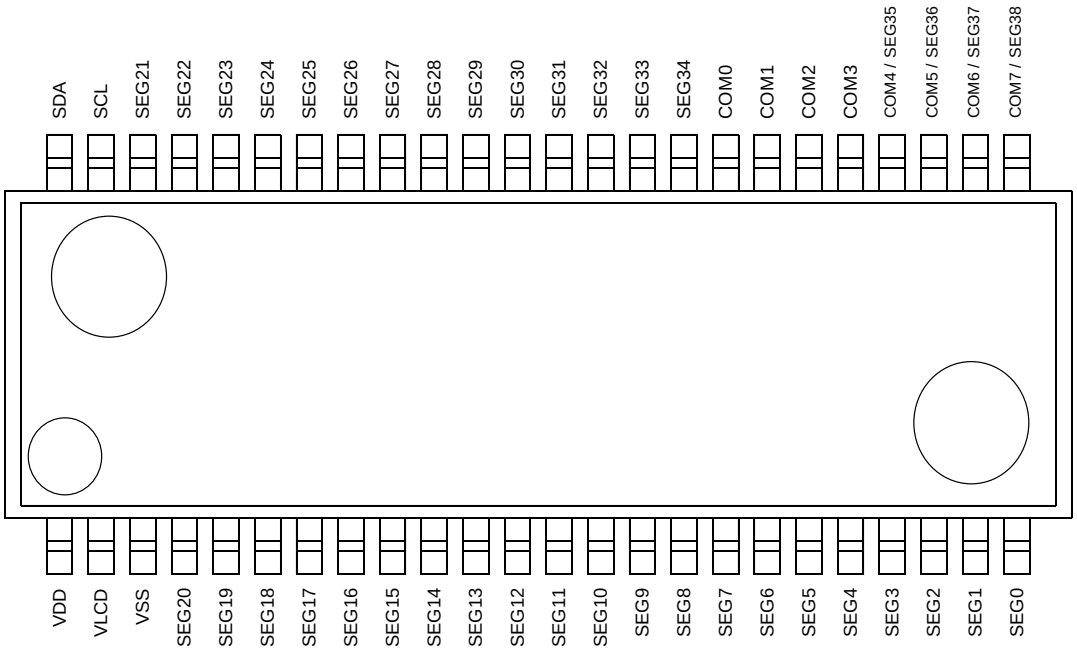


Figure 3. Pin Configuration (TOP VIEW)

Table 1. Pin Description

Terminal	Terminal No	I/O	Function	Handling when unused
SDA	48	I/O	Serial data input	-
SCL	47	I	Serial data transfer clock	-
VSS	3	I	Ground	-
VDD	1	I	Power supply	-
VLCD	2	I	Power supply for LCD drive	-
SEG0 to SEG34	4 to 24 33 to 46	O	SEGMENT output for LCD drive	OPEN
COM0 to COM3	29 to 32	O	COMMON output for LCD drive	OPEN
COM4/SEG35 to COM7/SEG38	25 to 28	O	COMMON / SEGMENT output for LCD drive	OPEN

Absolute Maximum Ratings (VSS=0V)

Parameter	Symbol	Ratings	Unit	Remarks
Power Supply Voltage1	VDD	-0.5 to +7.0	V	Power Supply
Power Supply Voltage2	VLCD	-0.5 to +7.0	V	LCD Drive Voltage
Allowable Loss	Pd	0.64*(Note)*	W	
Input voltage Range	V_{IN}	-0.5 to VDD+0.5	V	
Operational Temperature Range	Topr	-40 to +85	ºC	
Storage Temperature Range	Tstg	-55 to +125	ºC	

*(Note)*Derate by 6.40mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Ratings(Ta=-40°C to +85°C,VSS=0V)

Parameter	Symbol	Ratings			Unit	Remarks
		Min	Typ	Max		
Power Supply Voltage1	VDD	2.5	-	6.0	V	Power Supply
Power Supply Voltage2	VLCD	2.5	-	6.0	V	LCD Drive Voltage

Electrical Characteristics

DC Characteristics (VDD=2.5 to 6.0V, VLCD=2.5 to 6.0V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter		Symbol	Limits			Unit	Conditions
			Min	Typ	Max		
"H" Level Input Voltage		V_{IH}	0.7VDD	-	VDD	V	SDA,SCL
"L" Level Input Voltage		V_{IL}	VSS	-	0.3VDD	V	SDA,SCL
"H" Level Input Current		I_{IH}	-	-	1	µA	SDA,SCL
"L" Level Input Current		I_{IL}	-1	-	-	µA	SDA,SCL
LCD Driver on Resistance	SEG	R_{ON}	-	3.5	-	kΩ	Iload=±10µA
	COM	R_{ON}	-	3.5	-	kΩ	
Standby Current		I_{ST}	-	-	5	µA	Display off, Oscillation off
Power Consumption 1		I_{DD}	-	2.5	15	µA	VDD=3.3V, VLCD=5V, Ta=25°C Power Save Mode1, FR=80Hz 1/4 Bias, Frame Inversion
Power Consumption 2		I_{LCD}	-	10	20	µA	VDD=3.3V, VLCD=5V, Ta=25°C Power Save Mode1, FR=80Hz 1/4 Bias, Frame Inversion

Electrical Characteristics – continued

Oscillation Characteristics(VDD=2.5 to 6.0V, VLCD=2.5 to 6.0V, VSS=0V, Ta=-40°C to 85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Frame Frequency 1	f_{CLK1}	56	80	104	Hz	FR = 80Hz setting, VDD=2.5V to 6.0V, Ta=-40°C to +85°C
Frame Frequency 2	f_{CLK2}	72	80	88	Hz	FR = 80Hz setting, VDD=3.5V, Ta=-40°C to +85°C

[Reference Data]

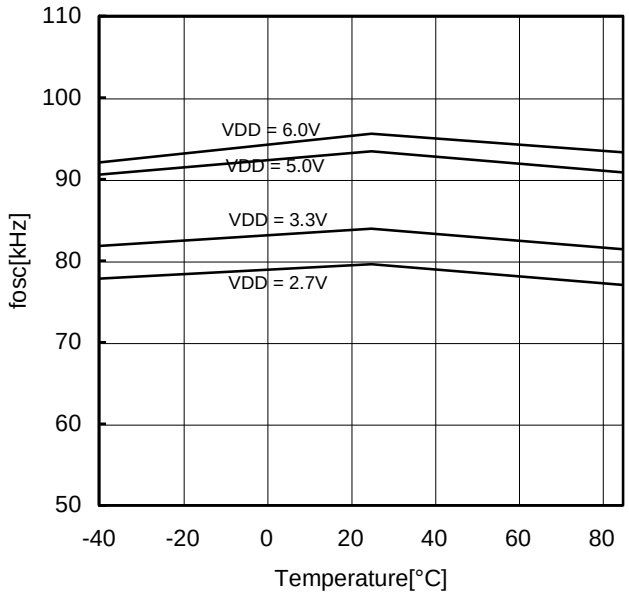


Figure 4. Frame Frequency Typical Temperature Characteristics

Electrical Characteristics – continued

MPU interface Characteristics (VDD=2.5 to 6.0V, VLCD=2.5 to 6.0V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input Rise Time	tr	-	-	0.3	µs	
Input Fall Time	tf	-	-	0.3	µs	
SCL Cycle Time	t_{SCYC}	2.5	-	-	µs	
“H” SCL Pulse Width	t_{SHW}	0.6	-	-	µs	
“L” SCL Pulse Width	t_{SLW}	1.3	-	-	µs	
SDA Setup Time	t_{SDS}	100	-	-	ns	
SDA Hold Time	t_{SDH}	100	-	-	ns	
Bus Free Time	t_{BUF}	1.3	-	-	µs	
START Condition Hold Time	$t_{HD;STA}$	0.6	-	-	µs	
START Condition Setup Time	$t_{SU;STA}$	0.6	-	-	µs	
STOP Condition Setup Time	$t_{SU;STO}$	0.6	-	-	µs	

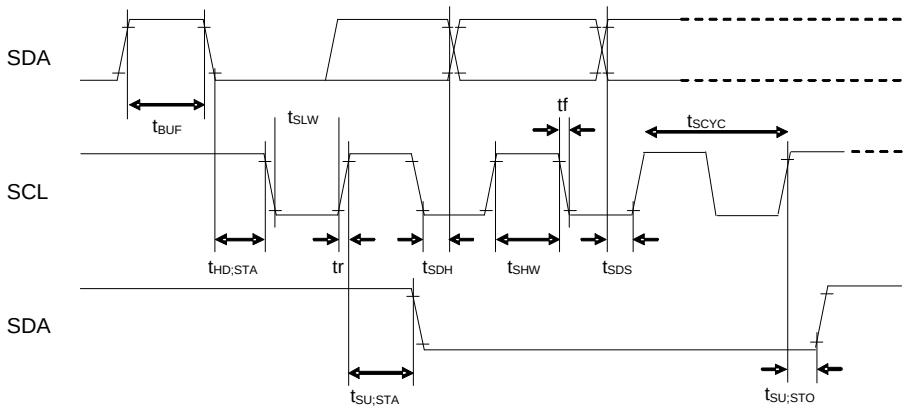


Figure 5. Serial Interface Timing

I/O Equivalent Circuit

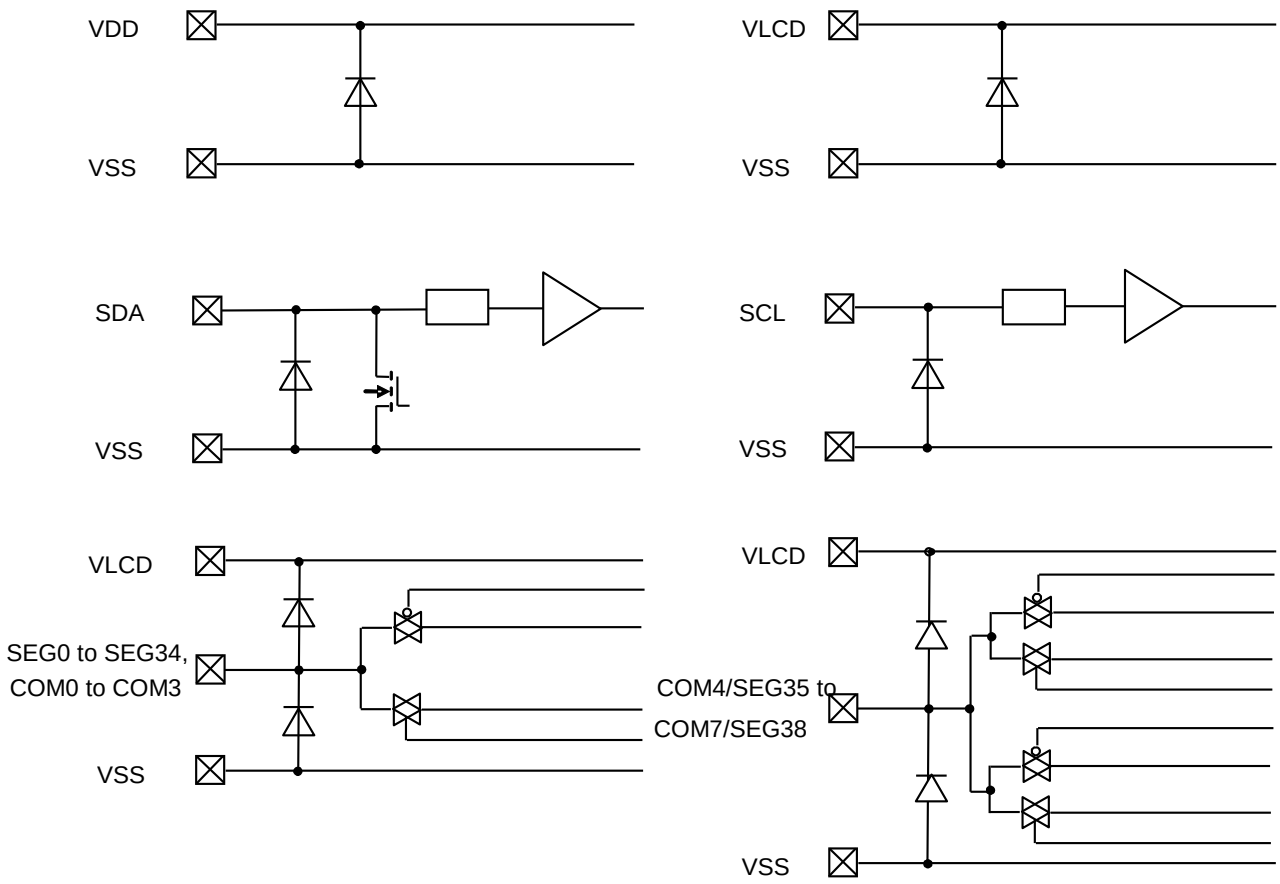


Figure 6. I/O Equivalent Circuit

Function Description

Command / Data Transfer Method

BU97950AFUV is controlled by 2-wire signal (SDA, SCL).

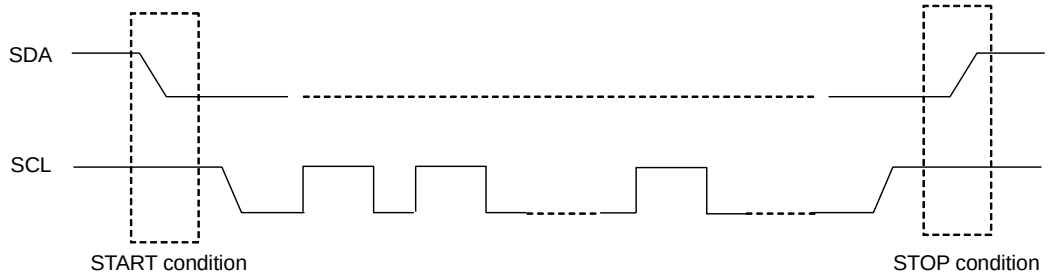


Figure 7. 2 wire Command/Data Transfer Format

It is necessary to generate START and STOP condition when sending Command or Display Data through this 2 wire serial interface.

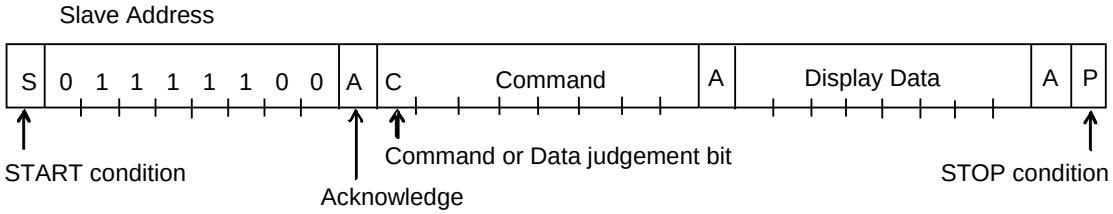


Figure 8. Interface Protocol

The following procedure shows how to transfer Command and Display Data.

(1) Generate “START condition”.
(2) Issue Slave Address.
(3) Transfer Command and Display Data.
(4) Generate “STOP condition

Acknowledge

Data format is comprised of 8 bits, Acknowledge bit is returned after sending 8-bit data.
After the transfer of 8-bit data (Slave Address, Command, Display Data), release the SDA line at the falling edge of the 8th clock. The SDA line is then pulled “Low” until the falling edge of the 9th clock SCL.
(Output cannot be pulled “High” because of open drain NMOS).
If acknowledge function is not required, keep SDA line at “Low” level from 8th falling edge to 9th falling edge of SCL.

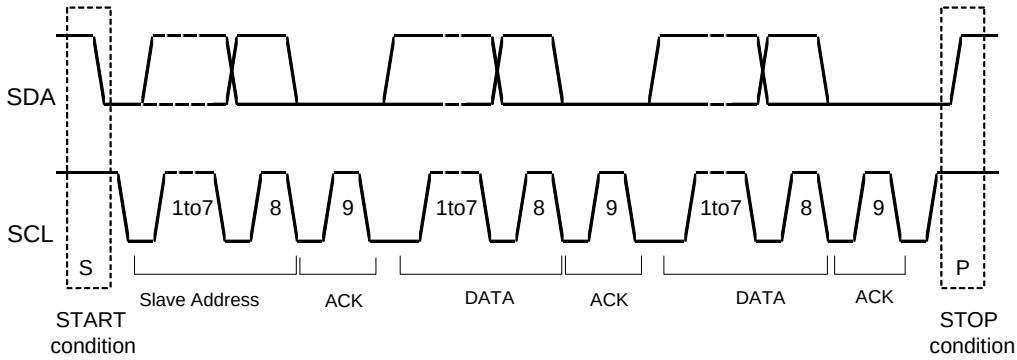
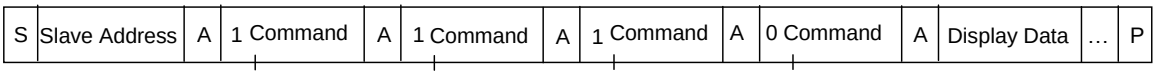


Figure 9. Acknowledge timing

Function Description – continued

Command Transfer Method

Issue Slave Address (“01111100”) after generate “START condition”.
The 1st byte after Slave Address always becomes command input.
MSB (“Command or Data judgement bit”) of command decide to next data is Command or Display Data.
When set “Command or Data judgement bit”=‘1’, next byte will be command.
When set “Command or Data judgement bit”=‘0’, next byte data is Display Data.

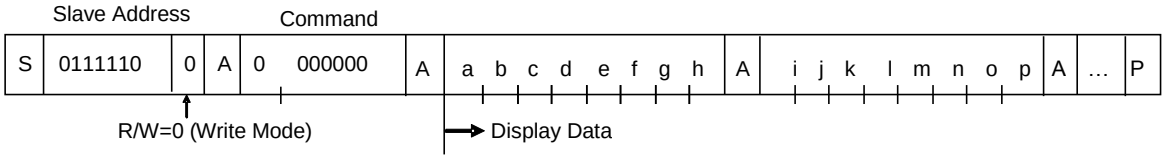


It cannot accept input command once it enters into Display Data transfer state.
In order to input command again it is necessary to generate “START condition”.
If “START condition” or “STOP condition” is sent in the middle of command transmission, command will be cancelled.
If Slave Address is continuously sent following “START condition”, it remains in command input state.
“Slave Address” must be sent right after the “START condition”.
When Slave Address cannot be recognized in the first data transmission, no Acknowledge bit is generated and next transmission will be invalid. When data is invalid status, if “START condition” is transmitted again, it will return to valid status.

Consider the MPU interface characteristic such as Input rise time and Setup/Hold time when transferring command and data (Refer to MPU Interface Characteristics).

Write Display and Transfer Method

BU97950AFUV enters “Write mode” when R/W bit of Slave address is ‘0’
BU97950AFUV has Display Data RAM (DDRAM) of 35×8=280bits.
The relationship between data input and Display Data, DDRAM data and address are as follows.



In 1/8 Duty Mode
8-bit data is stored in DDRAM. ADSET command specifies the address to be written, and address is automatically incremented in every 8-bit data.
Data can be continuously written in DDRAM by transmitting data continuously.

DDRAM Address

BIT	0h	1h	2h	3h	4h	5h	6h	7h	. . .	21h	22h	
0	a	i										COM0
1	b	j										COM1
2	c	k										COM2
3	d	l										COM3
4	e	m										COM4
5	f	n										COM5
6	g	o										COM6
7	h	p										COM7
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG33	SEG34	

Display data is written to DDRAM every 8-bit data.
No need to wait for ACK bit to complete data transfer.

Function Description – continued

In 1/4 Duty Mode

4-bit data is stored in DDRAM. ADSET command specifies the address to be written, and address is automatically incremented in every 8-bit data.

Data can be continuously written in DDRAM by transmitting data continuously.

DDRAM Address

BIT	0h	1h	2h	3h	. . .	12h	13h	
0	a	e	i	m				COM0
1	b	f	j	n				COM1
2	c	g	k	o				COM2
3	d	H	l	p				COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG36	SEG37	SEG38	

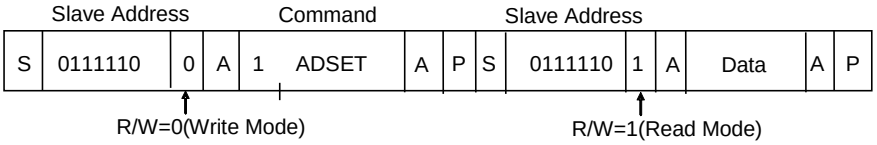
Display data is written to DDRAM every 4-bit data.

No need to wait for ACK bit to complete data transfer

Function Description – continued

Read Command Register and Transfer Method

BU97950AFUV enters “Read mode” when R/W bit of Slave Address is ‘1’
During Read mode the command registers can be read.
The sequence for the command register read is shown below.



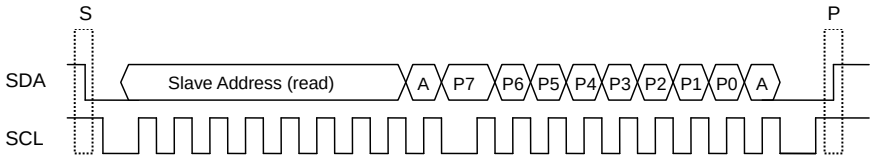
The following register settings can be read in this mode.
Only one register setting can be read at once, after reading register setting, BU97950 will exit from read mode and wait for slave Address. If all register setting needs to be read, please make sequence for “REG1” and “REG2”, respectively.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	P7	P6	P5	P4	P3	P2	P1	P0	23h
REG2	P7	P6	P5	P4	P3	P2	P1	P0	24h

REG1:P7 = Frame Frequency setting
P6 = Duty and Bias setting
P5 = Software Reset condition
P4 to P0 = EVR setting

REG2: P7 to P6 = Frame Frequency (FR) setting
P5 to P4 = Power Save Mode (SR) setting
P3 = LCD drive waveform setting
P2 = Display ON/OFF setting
P1 = APON setting
P0 = APOFF setting

An example of the command register read sequence is shown below.



LCD Driver Bias Circuit

BU97950AFUV generates LCD driving voltage with on-chip Buffer AMP.
And it can drive LCD at low power consumption.
1/4 or 1/3 Bias can be set by MODESET command.
Line or frame inversion can be set by DISCTL command.
Refer to the “LCD driving waveform” for each LCD Bias setting.

Reset Initialize Condition

Initial condition after executing Software Reset is as follows.
-Display is OFF.
-DDRAM address is initialized (DDRAM Data is not initialized).
Refer to Command Description for initialize value of registers.

Function Description – continued

Command / Function List

Description List of Command / Function

No.	Command	Function
1	Address Set (ADSET)	DDRAM Address setting (00h to 22h) Command register address setting (23h, 24h)
2	EVR Set (EVRSET)	EVR setting (0 to 31)
3	Display Control (DISCTL)	Frame Frequency, Power Save Mode setting
4	IC Operation Set (ICSET)	LCD drive mode, Software Reset, display on/off
5	All Pixel Control (APCTL)	All pixel control during display ON
6	Mode Set (MODESET)	Frame Frequency, Duty and Bias setting

Detailed command Description

D7 (MSB) is a Command or Data judgment bit.
Refer to Command / Data transfer method.

C: 0: Next byte is RAM write data.
1: Next byte is command.

Address Set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	P5	P4	P3	P2	P1	P0

Address data is specified in P[5:0].

The address range can be set as 00h(000000b) to 22h(100010b) for Write mode.
When the specified address is out of range, the address will be set to “0h(000000b)”.
The default value of the DDRAM Address is “0h(000000b)”

The address can be set 23h(100011b) and 24h(100100b) for Read mode.
It is prohibited to set other address.

P[5:0] = 23h（100011b）- REG1
Register address for Software Reset condition and EVR setting

P[5:0] = 24h（100100b）- REG2
Register address for the other settings
(For more detailed information, please refer to “Read Command Register and Transfer Method”)

EVR Set (EVRSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	P4	P3	P2	P1	P0

BU97950AFUV has 32-step Electrical Volume Register (EVR) that can set the best V0 voltage level (Maximum LCD driving voltage).
Electrical Volume Register (EVR) is set to “00000” in reset initialize condition.
In “0000” condition, V0 output voltage is equal to VLCD input voltage.
Keep Contrast Setting for V0 voltage more than 2.5V only.
Refer to the below table for V0 voltage.
And ensure “VLCD – V0 > 0.6” condition is satisfied.
Unstable IC output voltage may result if the above conditions are not satisfied.

Function Description – continued

The relationship of electrical volume register (EVR) setting and V0 voltage

EVR	Calculation formula	VLCD = 6.000	VLCD = 5.500	VLCD = 5.000	VLCD = 4.000	VLCD = 3.500	VLCD = 3.000	VLCD = 2.500	Unit
0	VLCD	V0= 6.000	V0= 5.500	V0= 5.000	V0= 4.000	V0= 3.500	V0= 3.000	V0= 2.500	V
1	0.967*VLCD	V0= 5.802	V0= 5.323	V0= 4.839	V0= 3.871	V0= 3.387	V0= 2.903	V0= 2.419	V
2	0.937*VLCD	V0= 5.622	V0= 5.156	V0= 4.688	V0= 3.750	V0= 3.281	V0= 2.813	V0= 2.344	V
3	0.909*VLCD	V0= 5.454	V0= 5.000	V0= 4.545	V0= 3.636	V0= 3.182	V0= 2.727	V0= 2.273	V
4	0.882*VLCD	V0= 5.292	V0= 4.853	V0= 4.412	V0= 3.529	V0= 3.088	V0= 2.647	V0= 2.206	V
5	0.857*VLCD	V0= 5.142	V0= 4.714	V0= 4.286	V0= 3.429	V0= 3.000	V0= 2.571	V0= 2.143	V
6	0.833*VLCD	V0= 4.998	V0= 4.583	V0= 4.167	V0= 3.333	V0= 2.917	V0= 2.500	V0= 2.083	V
7	0.810*VLCD	V0= 4.860	V0= 4.459	V0= 4.054	V0= 3.243	V0= 2.838	V0= 2.432	V0= 2.027	V
8	0.789*VLCD	V0= 4.734	V0= 4.342	V0= 3.947	V0= 3.158	V0= 2.763	V0= 2.368	V0= 1.974	V
9	0.769*VLCD	V0= 4.614	V0= 4.231	V0= 3.846	V0= 3.077	V0= 2.692	V0= 2.308	V0= 1.923	V
10	0.750*VLCD	V0= 4.500	V0= 4.125	V0= 3.750	V0= 3.000	V0= 2.625	V0= 2.250	V0= 1.875	V
11	0.731*VLCD	V0= 4.386	V0= 4.024	V0= 3.659	V0= 2.927	V0= 2.561	V0= 2.195	V0= 1.829	V
12	0.714*VLCD	V0= 4.284	V0= 3.929	V0= 3.571	V0= 2.857	V0= 2.500	V0= 2.143	V0= 1.786	V
13	0.697*VLCD	V0= 4.182	V0= 3.837	V0= 3.488	V0= 2.791	V0= 2.442	V0= 2.093	V0= 1.744	V
14	0.681*VLCD	V0= 4.086	V0= 3.750	V0= 3.409	V0= 2.727	V0= 2.386	V0= 2.045	V0= 1.705	V
15	0.666*VLCD	V0= 3.996	V0= 3.667	V0= 3.333	V0= 2.667	V0= 2.333	V0= 2.000	V0= 1.667	V
16	0.652*VLCD	V0= 3.912	V0= 3.587	V0= 3.261	V0= 2.609	V0= 2.283	V0= 1.957	V0= 1.630	V
17	0.638*VLCD	V0= 3.828	V0= 3.511	V0= 3.191	V0= 2.553	V0= 2.234	V0= 1.915	V0= 1.596	V
18	0.625*VLCD	V0= 3.750	V0= 3.438	V0= 3.125	V0= 2.500	V0= 2.188	V0= 1.875	V0= 1.563	V
19	0.612*VLCD	V0= 3.672	V0= 3.367	V0= 3.061	V0= 2.449	V0= 2.143	V0= 1.837	V0= 1.531	V
20	0.600*VLCD	V0= 3.600	V0= 3.300	V0= 3.000	V0= 2.400	V0= 2.100	V0= 1.800	V0= 1.500	V
21	0.588*VLCD	V0= 3.528	V0= 3.235	V0= 2.941	V0= 2.353	V0= 2.059	V0= 1.765	V0= 1.471	V
22	0.576*VLCD	V0= 3.456	V0= 3.173	V0= 2.885	V0= 2.308	V0= 2.019	V0= 1.731	V0= 1.442	V
23	0.566*VLCD	V0= 3.396	V0= 3.113	V0= 2.830	V0= 2.264	V0= 1.981	V0= 1.698	V0= 1.415	V
24	0.555*VLCD	V0= 3.330	V0= 3.056	V0= 2.778	V0= 2.222	V0= 1.944	V0= 1.667	V0= 1.389	V
25	0.545*VLCD	V0= 3.270	V0= 3.000	V0= 2.727	V0= 2.182	V0= 1.909	V0= 1.636	V0= 1.364	V
26	0.535*VLCD	V0= 3.210	V0= 2.946	V0= 2.679	V0= 2.143	V0= 1.875	V0= 1.607	V0= 1.339	V
27	0.526*VLCD	V0= 3.156	V0= 2.895	V0= 2.632	V0= 2.105	V0= 1.842	V0= 1.579	V0= 1.316	V
28	0.517*VLCD	V0= 3.102	V0= 2.845	V0= 2.586	V0= 2.069	V0= 1.810	V0= 1.552	V0= 1.293	V
29	0.508*VLCD	V0= 3.048	V0= 2.797	V0= 2.542	V0= 2.034	V0= 1.780	V0= 1.525	V0= 1.271	V
30	0.500*VLCD	V0= 3.000	V0= 2.750	V0= 2.500	V0= 2.000	V0= 1.750	V0= 1.500	V0= 1.250	V
31	0.491*VLCD	V0= 2.946	V0= 2.705	V0= 2.459	V0= 1.967	V0= 1.721	V0= 1.475	V0= 1.230	V

Prohibited setting

Function Description – continued

Display Control (DISCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	P3	P2	P1	P0

Set Frame Frequency

Setting(*Note 1*)	P3	P2	FRSEL(*Note 2*)	Reset initialize condition
80Hz	0	0	0	○
71Hz	0	1	0	
64Hz	1	0	0	
50Hz	1	1	0	
233Hz	0	0	1	
197Hz	0	1	1	
160Hz	1	0	1	
122Hz	1	1	1	

(*Note 1*) The frame frequency varies according to the characteristics of f_{CLK} when internal oscillation circuit is used. (Refer to oscillation characteristics for f_{CLK} properties).

(Note 2) Please refer to MODESET for FRSEL

Set Power Save Mode SR.

Setup	P1	P0	Reset initialize condition
Power Save Mode 1	0	0	
Power Save Mode 2	0	1	
Normal Mode	1	0	○
High Power Mode	1	1	

Function Description – continued

Set IC Operation (ICSET)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	1	1	1	0	P2	P1	P0

(* : Don't care)

Set LCD drive Waveform.

Setup	P2	Reset initialize condition
Line Inversion Mode	0	
Frame Inversion Mode	1	○

Power consumption is reduced in the following order:
Line Inversion > Frame Inversion
Typically, when driving large capacitance LCD, Line inversion is more susceptible to influence of crosstalk.
Regarding driving waveform, refer to LCD driving waveform.

Set Software Reset execution

Setup	P1	Reset initialize condition
Software Reset Not Execute	0	○
Software Reset Execute	1	

When "Software Reset" is executed, BU97950AFUV is reset to initial condition.
Don't set Software Reset (P1) with P2, P0 at the same time.

Set Display ON and OFF

Setup	P0	Reset initialize condition
Display off(DISPOFF)	0	○
Display on(DISPON)	1	

Display off : Regardless of DDRAM data, all SEGMENT and COMMON output will be stopped after 1frame of data write. Display OFF mode will be disabled after Display ON command.
Display on: SEGMENT and COMMON output will be active and start to read the display data from DDRAM.

All Pixel control (APCTL)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	1	1	1	1	0	P1	P0

All display set on, off

Setup	P1	Reset initialize condition
Normal	0	○
All pixel on	1	

Setup	P0	Reset initialize condition
Normal	0	○
All pixel off	1	

All pixels on: All pixels are on regardless of DDRAM data.
All pixels off: All pixels are off regardless of DDRAM data.

This command is valid in Display on status. The data of DDRAM is not changed by this command.
If set both P1 and P0 ="1", All Pixels OFF will be selected.

Function Description – continued

Mode Set (MODE SET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

(* : Don't care)

Set Frame Frequency Setting

Setup	P1	Reset initialize condition
Normal	0	○
200Hz Mode	1	

Set Duty and Bias Level

Setup	P0	Reset initialize condition
1/8 Duty and 1/4 Bias	0	○
1/4 Duty and 1/3 Bias	1	

Please refer to LCD drive waveform, for example of SEG and COM output waveform

LCD Driving Waveform

(1/4 Bias, 1/8 Duty) Line Inversion Mode

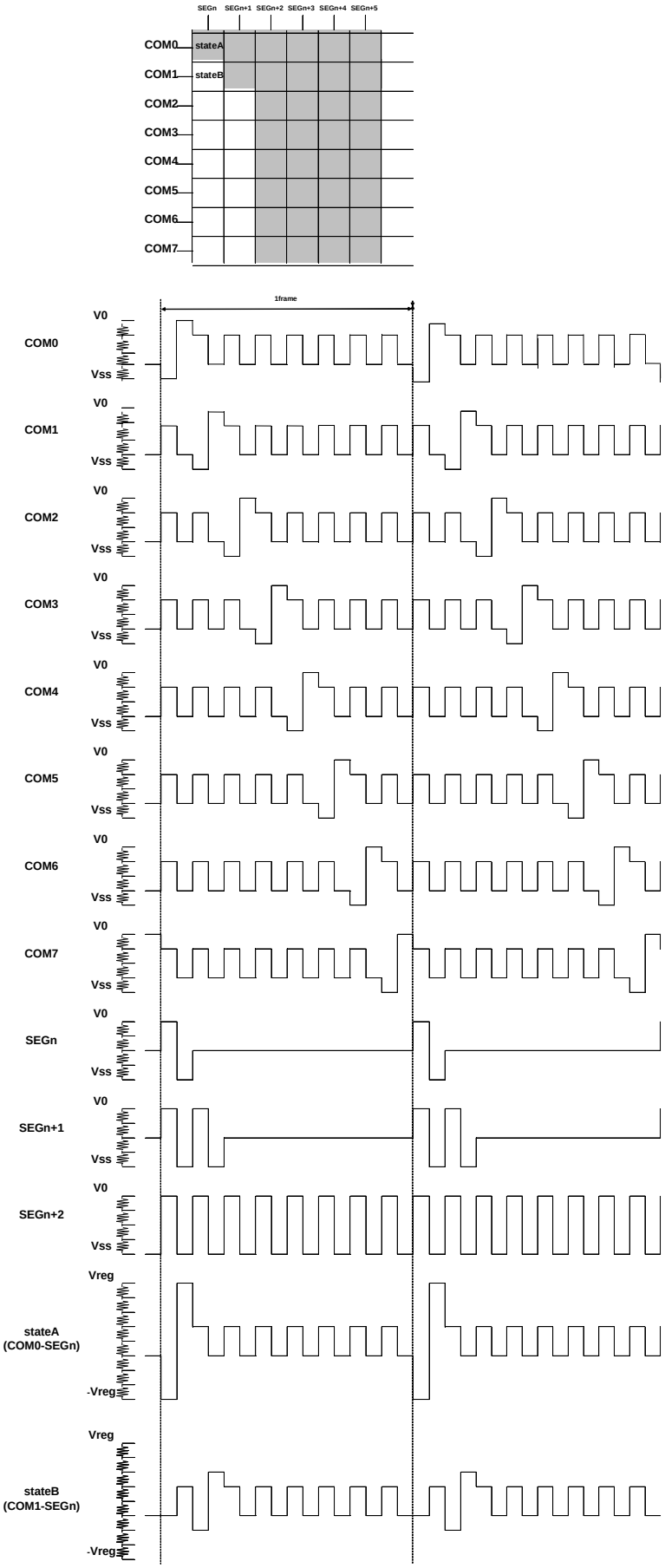


Figure 10. Wave form of line inversion

LCD Driving Waveform– continued

(1/4 Bias, 1/8 Duty)Frame Inversion Mode

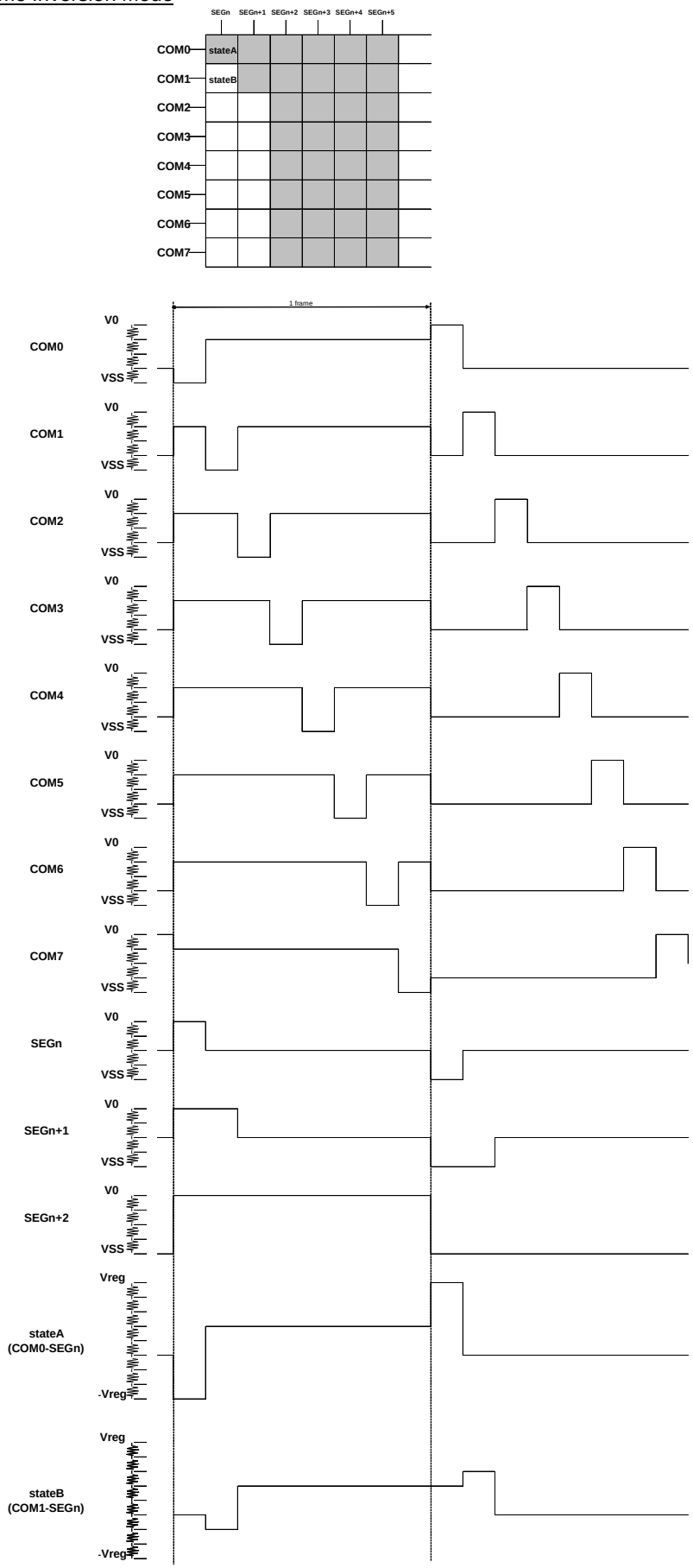


Figure 11. Wave form of frame inversion

LCD Driving Waveform– continued

(1/3 Bias, 1/4 Duty) Line Inversion Mode

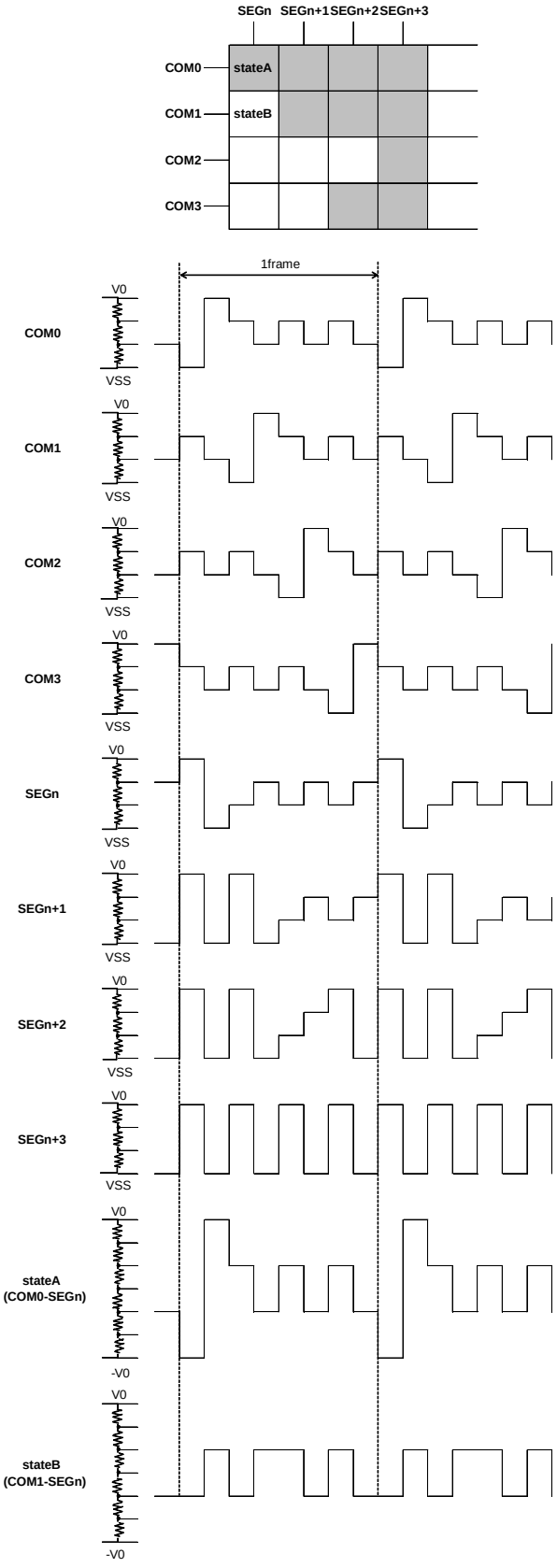


Figure 12. Wave form of frame inversion

LCD Driving Waveform– continued

(1/3 Bias, 1/4 Duty) Frame Inversion Mode

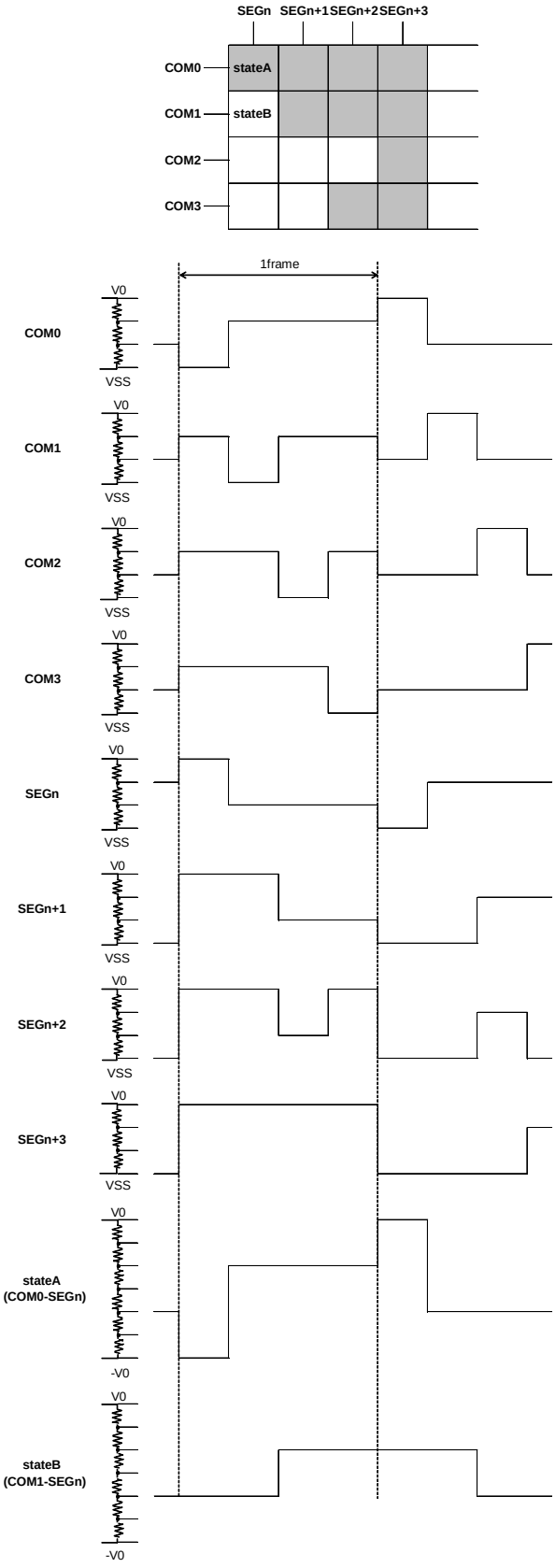


Figure 13. Wave form of Frame Inversion

Initialize sequence

Follow the Power-on sequence below to initialize condition.

Power on
↓
STOP condition
↓
START condition
↓
Issue Slave Address
↓
Execute Software Reset by ICSET command

After Power-on and before sending initialize sequence, each register value, DDRAM Address and DDRAM Data are random.

Start sequence

Start sequence example

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power on									VDD=0V to 5V (Tr=0.1ms)
	↓									
2	wait min 100µs									Initialize IC
	↓									
3	STOP									STOP condition
	↓									
4	START									START condition
5	Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
	↓									
6	ICSET	1	1	1	1	0	*	1	*	Execute Software Reset
	↓									
7	DISCTL	1	1	1	0	0	0	1	0	
	↓									
8	EVRSET	1	1	0	0	0	0	0	0	
	↓									
9	ADSET	0	0	0	0	0	0	0	0	DDRAM Address set
	↓									
10	Display Data	*	*	*	*	*	*	*	*	Address 00h
	⋮									⋮
	Display Data	*	*	*	*	*	*	*	*	Address 22h
	↓									
11	STOP									STOP condition
	↓									
12	START									START condition
13	Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
	↓									
14	ICSET	1	1	1	1	0	*	0	1	Display on

(*:Don't' care)

Cautions in Power ON/OFF

To prevent incorrect display, malfunction and abnormal current, follow Power On/Off sequence shown in waveform below.
VDD must be turned on before VLCD during power up sequence.
VDD must be turned off after VLCD during power down sequence.
Set VDD-2.4≥ VLCD, t1>0ns and t2>0ns.
To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

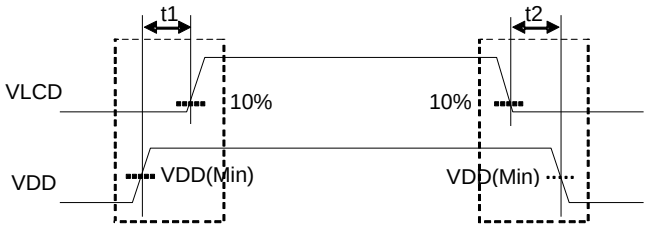


Figure 14. Recommended Power ON/OFF Sequence

Caution in P.O.R Circuit Use

BU97950AFUV has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Keep the following recommended Power-On conditions in order to power up properly.

Set power up conditions to meet the recommended t_R, t_F, t_{OFF}, and V_{BOT} specification below in order to ensure P.O.R operation.

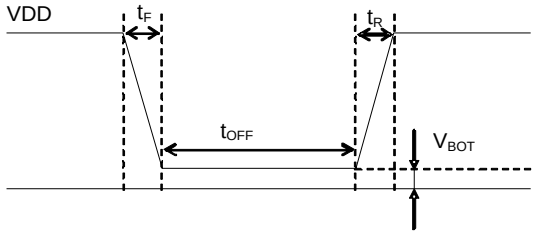


Figure 15. Power ON/OFF waveform

Recommended condition of t_R, t_F, t_{OFF}, V_{BOT} (Ta=25 ºC)

t_R	t_F	t_{OFF}	V_{BOT}
Less than 5ms	Less than 5ms	More than 20ms	Less than 0.3V

When it is difficult to keep above conditions, it is possibility to cause meaningless display due to no IC initialization.
Please execute the IC initialization as quickly as possible after Power-on to reduce such an affect.
See the IC initialization flow as below.
Setting TEST2="H" disables the POR circuit, in such case, execute the following sequence.
Note however that it cannot accept command while supply is unstable or below the minimum supply range.
Note also that Software Reset is not a complete alternative to POR function.

(1) Generate STOP condition

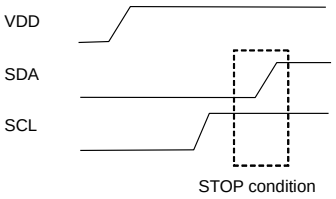


Figure 16. STOP condition

(2) Generate START condition.

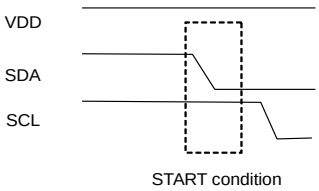


Figure 17. START condition

(3) Issue Slave Address.

(4) Execute Software Reset (ICSET) command.

Note on the Multiple Devices be Connected to 2 Wire Interface

Do not access the other device without power supply (VDD) to the BU97950AFUV.

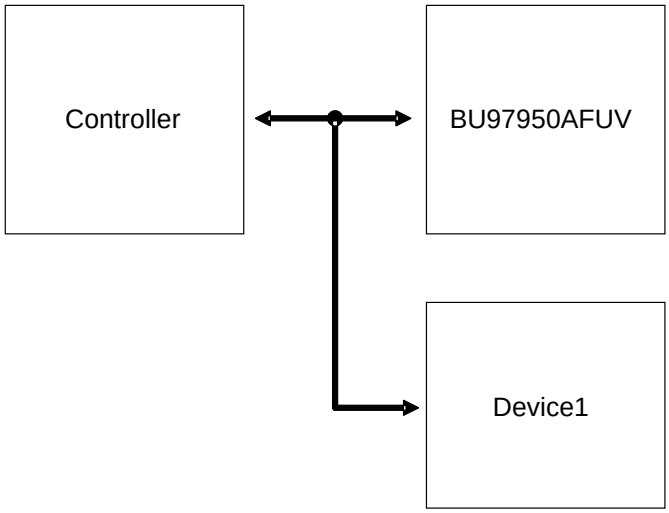


Figure 18. Example of BUS connection

To control the slope of the falling edge, a capacitor is connected between gate and drain of a NMOS transistor (Refer toFigure19).
The gate is in a high-impedance state if the power supply (VDD) is not supplied.

In this condition, the gate voltage is pulled up by the current flow through the capacitance as a result of the SDA signal's transition from LOW to HIGH.

The NMOS transistor turns on and draws some current (Ids) from the SDA port if the gate voltage (Vg) is higher than the threshold voltage (Vth).

An external resistor (R) is connected between the power line and SDA line to keep the SDA line as logic HIGH.
But the line cannot be kept as logic HGH if the voltage drop (R*Ids) is large.

Access the other LSIs with power supply to BU97950AFUV to control the gate voltage as logic level of 1 or 0 if the number of LSIs are connected to the same bus.

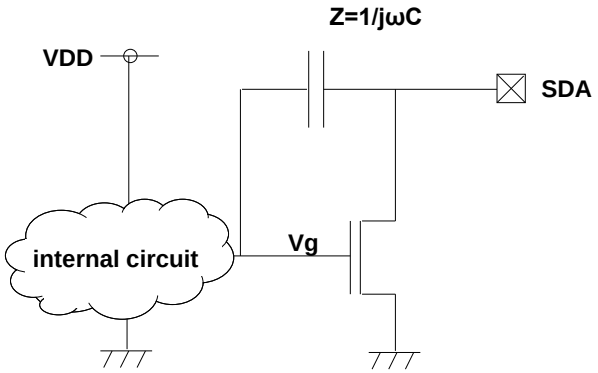


Figure 19. SDA output cell structure

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

Ordering Information

B U 9 7 9 5 0 A x x x - x x

Part Number

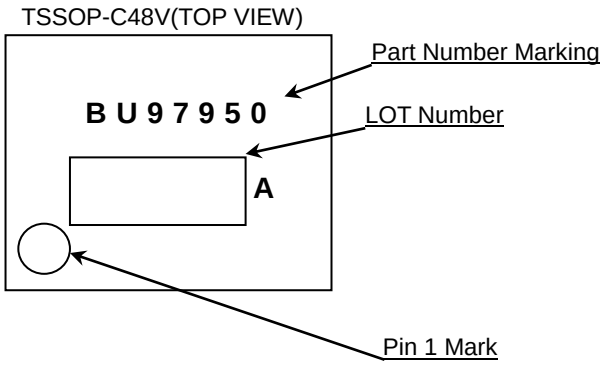
Package
FUV : TSSOP-C48V

Packaging and forming specification
E2: Embossed tape and reel

Lineup

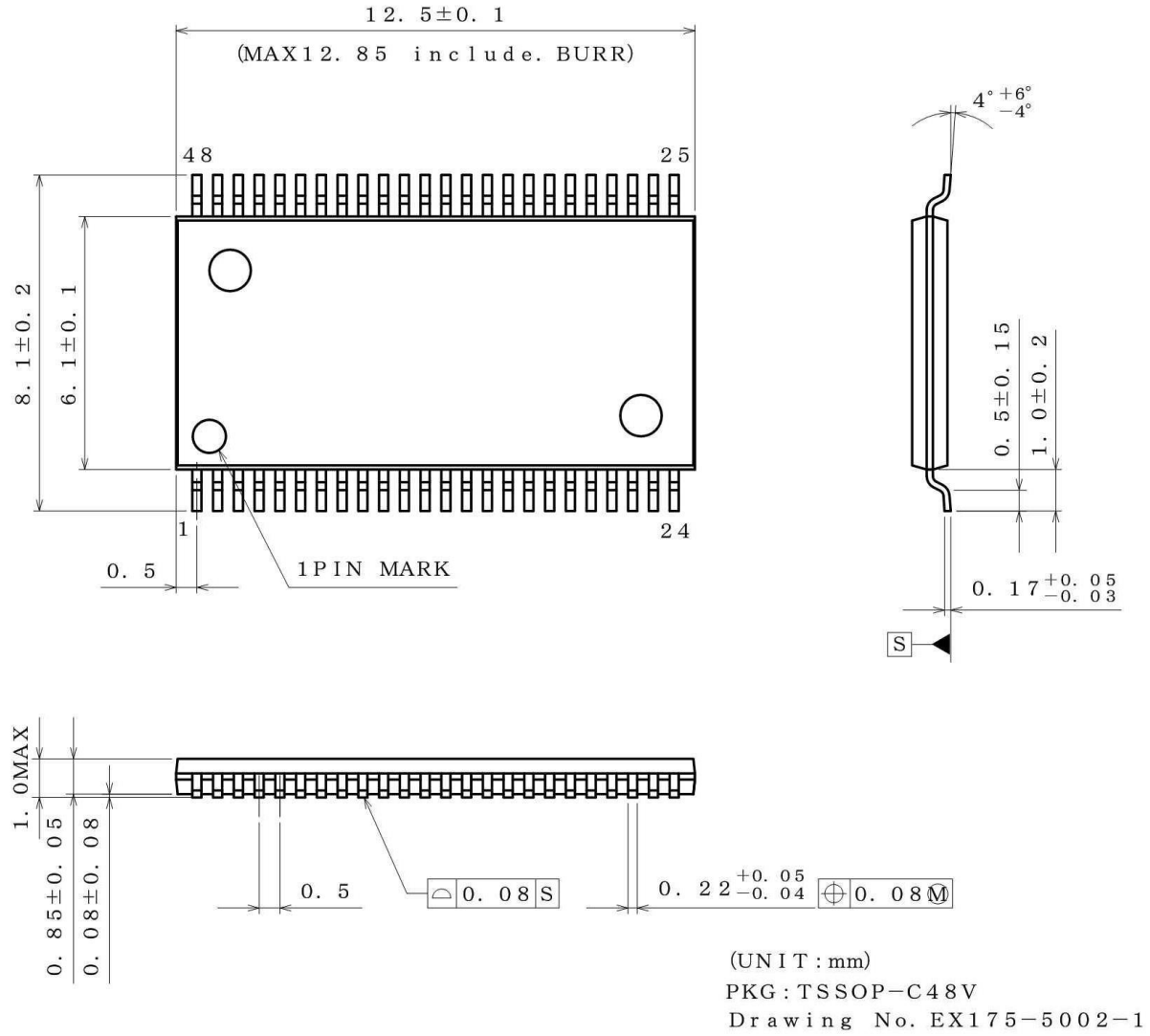
Package		Orderable Part Number
TSSOP-C48V	Reel of 2000	BU97950AFUV-E2

Marking Diagram



Physical Dimension, Tape and Reel Information

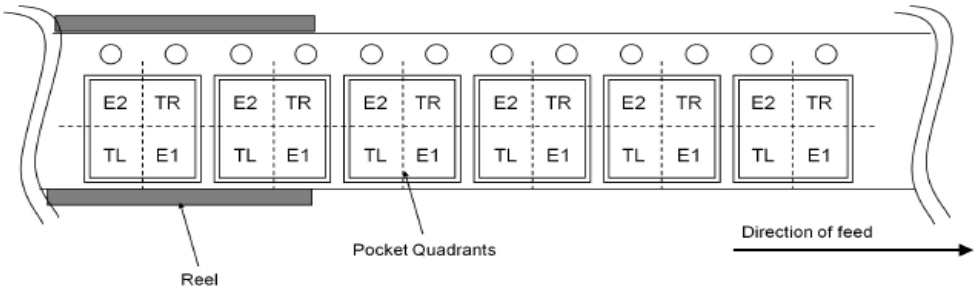
Package Name	TSSOP-C48V



(UNIT : mm)
PKG : TSSOP−C48V
Drawing No. EX175−5002−1

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
31.July.2017	001	New Release

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CLASSⅣ		CLASSⅢ	

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   [h] Use of the Products in places subject to dew condensation

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6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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