Standard LCD Segment Drivers

BU97950FUV MAX 280 segments (SEG35×COM8)

●Features

- Integrated RAM for display data (DDRAM): 35 x 8bit (Max 280 Segment)
- LCD drive output: 8 Common output, 35 Segment output
- Integrated Buffer AMP for LCD driving
- Integrated Oscillator circuit
- No external components
- Low power consumption design
- Independent power supply for LCD driving
- Integrated Electrical volume register (EVR) function

●Key Specifications

- Supply Voltage Range: +2.5V to +5.5V
- LCD drive power supply Range: +2.5V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 280 Segments
- Display Duty: 1/8
- Bias: 1/4
- Interface: 2wire serial interface

●Packages W (Typ.) x D (Typ.) x H (Max.)

TSSOP-C48V
8.1mm x 12.5mm x 1.0mm

●Applications

- Telephone
- FAX
- Portable equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car audio
- Home electrical appliance
- Meter equipment

etc.

●Typical Application Circuit

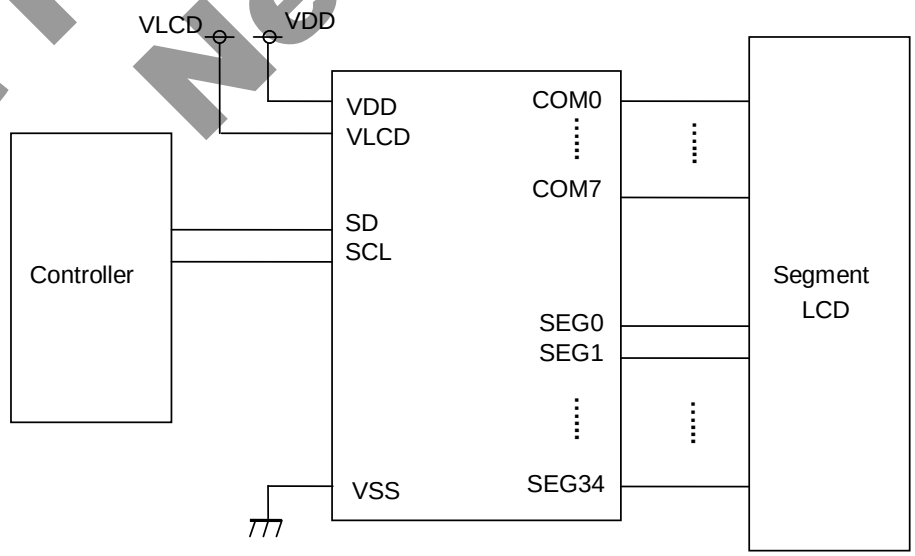


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays.

●Block Diagrams / Pin Configurations / Pin Descriptions

BU97950FUV (TSSOP-C48V)

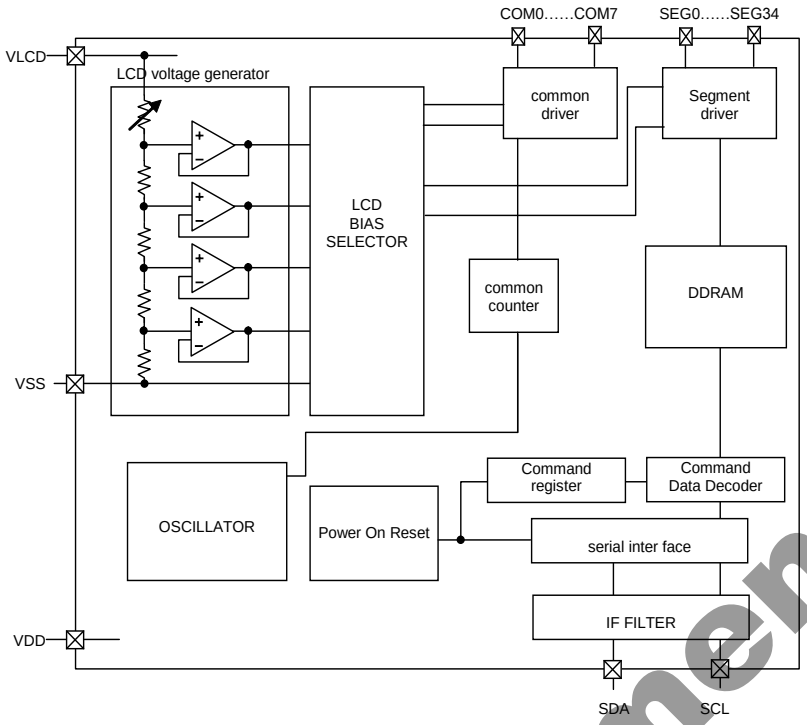


Figure 2. Block Diagram

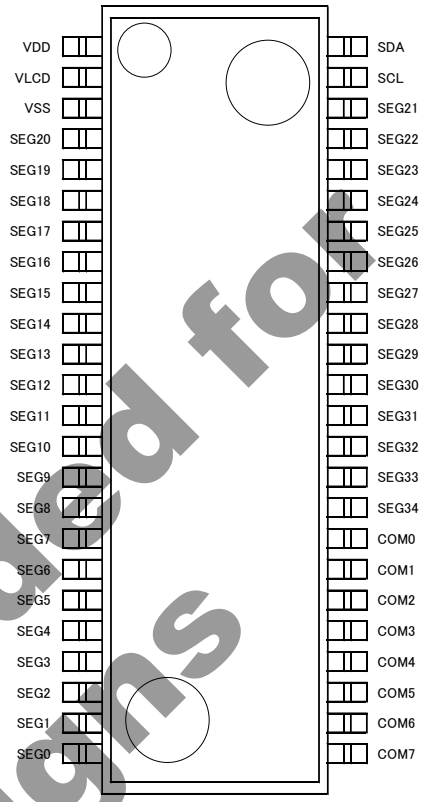


Figure 3. Pin Configuration (TOP VIEW)

Table 1 Pin Description

Terminal	Terminal No.	I/O	Function
SDA	48	I/O	Serial data input
SCL	47	I	Serial data transfer clock
VSS	3	I	GND
VDD	1	I	Power supply
VLCD	2	I	Power supply for LCD drive
SEG0 to 35	4 to 24 33 to 46	O	SEGMENT output for LCD drive
COM0 to 7	25 to 32	O	COMMON output for LCD drive

●Absolute Maximum Ratings (VSS=0V)

Parameter	Symbol	Ratings	Unit	Remarks
Power Supply Voltage1	VDD	-0.5 to +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.5 to +7.0	V	LCD drive voltage
Allowable loss	Pd	0.64	W	When used at more than Ta=25 ºC, subtract 6.4mW per degree. (BU97950FUV Package only)
Input voltage range	VIN	-0.5 to VDD+0.5	V	
Operational temperature range	Topr	-40 to +85	ºC	
Storage temperature range	Tstg	-55 to +125	ºC	

*1 This product is not designed against radioactive ray.

●Recommended Operating Ratings(Ta=-40°C to +85°C,VSS=0V)

Parameter	Symbol	Limits			Unit	Remarks
		MIN	TYP	MAX		
Power Supply Voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply Voltage2	VLCD	2.5	-	5.5	V	LCD drive voltage

●Electrical Characteristics

DC Characteristics (VDD=2.5 to 5.5V, VLCD=2.5 to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter		Symbol	Limits			Unit	Conditions
			MIN	TYP	MAX		
“H” level input voltage		VIH	0.7VDD	-	VDD	V	SDA,SCL
“L” level input voltage		VIL	VSS	-	0.3VDD	V	SDA,SCL
“H” level input current		IIH	-	-	1	µA	SDA,SCL
“L” level input current		IIL	-1	-	-	µA	SDA,SCL
LCD Driver on resistance	SEG	RON	-	3.5	-	kΩ	Iload=±10µA
	COM	RON	-	3.5	-	kΩ	
Standby current		Ist	-	-	5	µA	Display off, Oscillation off
Power consumption 1		IDD	-	2.5	15	µA	VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=80Hz 1/4 bias, Frame inversion
Power consumption 2		ILCD	-	10	20	µA	VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=80Hz 1/4 bias, Frame inversion

●**Electrical Characteristics – continued**

Oscillation Characteristics (VDD=2.5 to 5.5V, VLCD=2.5 to 5.5V, VSS=0V, Ta=-40°C to 85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Frame frequency	fCLK	56	80	104	Hz	FR = 80Hz setting, VDD=3.3V

MPU I/F Characteristics (VDD=2.5 to 5.5V, VLCD=2.5 to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Input rise time	tr	-	-	0.3	µs	
Input fall time	tf	-	-	0.3	µs	
SCL cycle time	tSCYC	2.5	-	-	µs	
“H” SCL pulse width	tSHW	0.6	-	-	µs	
“L” SCL pulse width	tSLW	1.3	-	-	µs	
SDA setup time	tSDS	200	-	-	ns	
SDA hold time	tSDH	0	-	-	ns	
Bus free time	tBUF	1.3	-	-	µs	
START condition hold time	tHD;STA	0.6	-	-	µs	
START condition setup time	tSU;STA	0.6	-	-	µs	
STOP condition setup time	tSU;STO	0.6	-	-	µs	

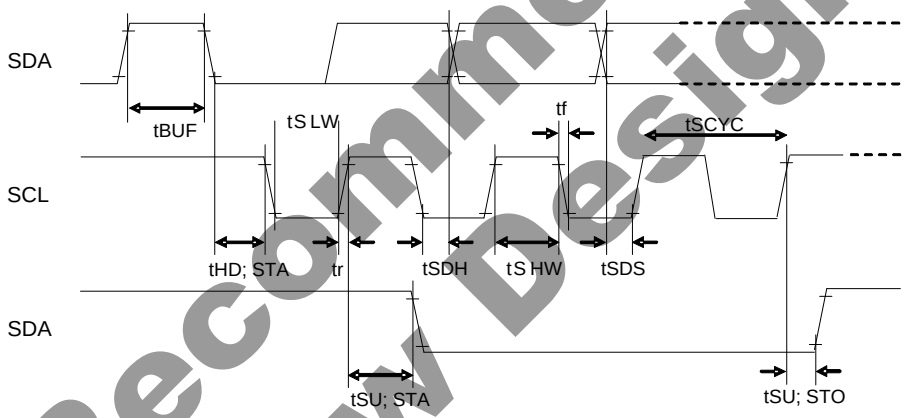


Figure 4. Serial Interface Timing

●**I/O equivalent circuit**

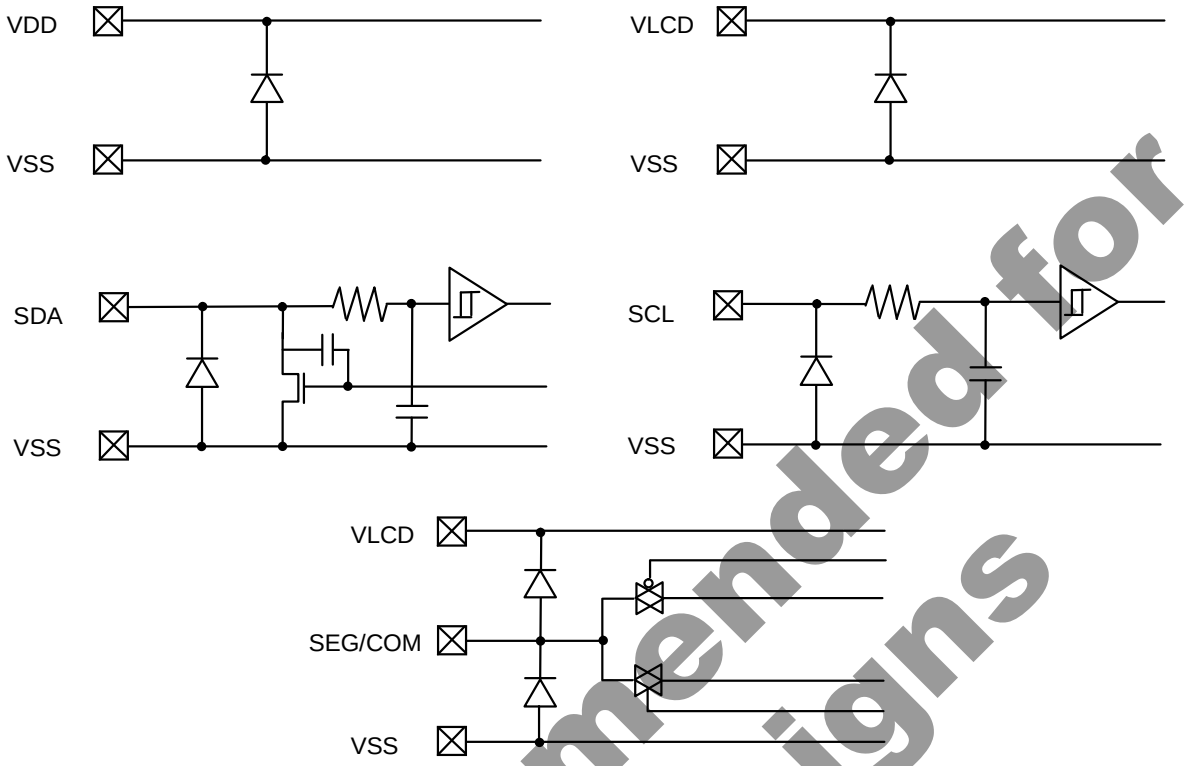


Figure 5. I/O Equivalent Circuit

●**Example of Recommended Circuit**

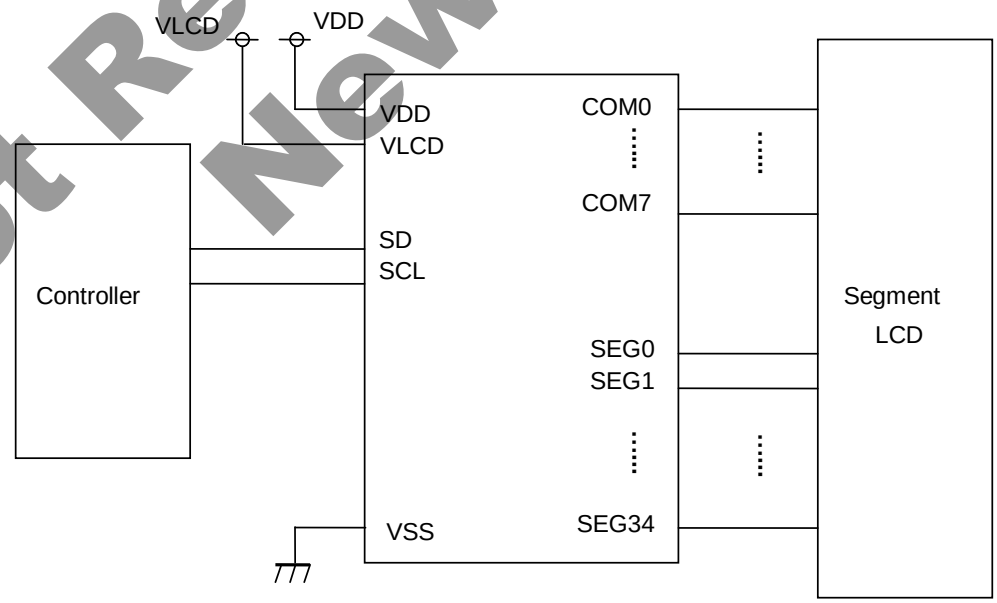


Figure 6. Example of Recommended Circuit

●Function Description

○Command /Data transfer method

This device is controlled by 2-wire serial signal (SDA, SCL).

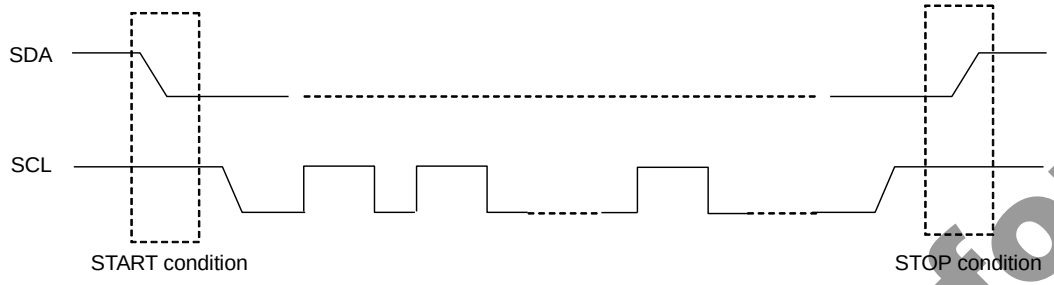


Figure 7. 2-wire Serial Command/Data Transfer Format

START and STOP conditions are required in 2-wire serial interface transfer method.

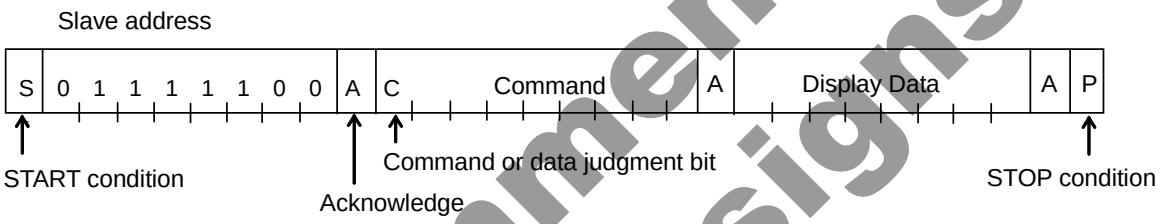


Figure 8. Interface Protocol

Method of transferring command and data is as follows:

1) Generate “START condition”.
2) Send Slave address.
3) Send command and display data.
4) Generate “STOP condition”.

○Acknowledge

Data format is 8-bit and an Acknowledge bit is returned after transfer of 8-bit data.
When SCL 8th=’L’ after transfer of 8-bit data (Slave Address, Command, Display Data), output ’L’ and open SDA line.
When SCL 9th=’L’, stop output function.
(As Output format is NMOS-Open-Drain, can’t output ‘H’ level.)
If there is no need for Acknowledge function, please input ‘L’ level from SCL 8th=’L’ to SCL 9th=’L’.

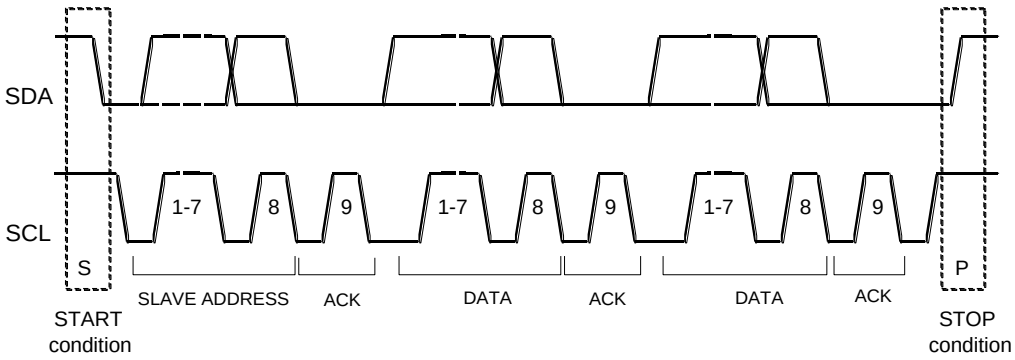


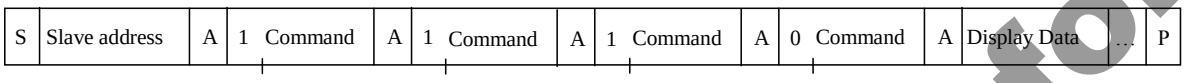
Figure 9. Acknowledge timing

○Command transfer method

Send the Slave Address (“0111110**0**” for Write Mode or “0111110**1**” for Read Mode) after the “START condition” is generated. Command input follows after the Slave Address. The least significant bit (LSB) of the Slave Address determines if the operation is Write or Read.

The MSB is the command/data judgment bit. This bit determines whether succeeding byte is a command or data.

When “command or data judgment bit”=‘1’, the next byte is a command.
When “command or data judgment bit”=‘0’, the next byte is display data.



Once the chip is in display data transfer condition, command can no longer be accepted.
To input another command, a “START condition” must be generated.

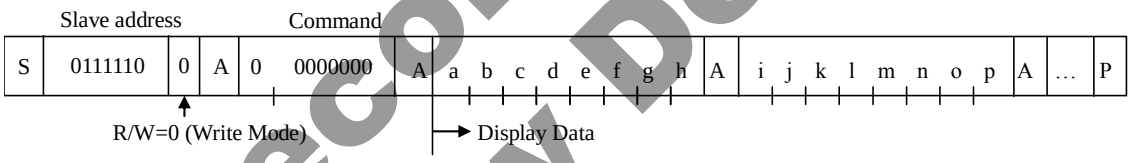
If “START condition” or “STOP condition” is inputted during command transmission, the current command will be cancelled.
If the Slave address is continuously inputted after the “START condition”, it will be in command input condition.

After “START condition” please input “Slave Address”. When Slave Address is not recognized, Acknowledge bit will not be returned and succeeding transmissions will be invalid. During an invalid state, sending the “START condition” will cause the device to return to a valid status.

∗When transferring command and data, please observe “MPU Interface characteristic” of input rise time, Setup time, and Hold time etc…（Refer to MPU Interface）.

○Write display and transfer method

BU97950 enters “Write mode” when R/W bit of Slave address is ‘0’
BU97950 has Display Data RAM (DDRAM) of 35×8=280bits.
The relationship between data input and display data, DDRAM data and address are as follows.



The 8-bit display data will be stored in the DDRAM. The address to be written is specified by Address Set command, and the address is automatically incremented after every 8-bit of data.

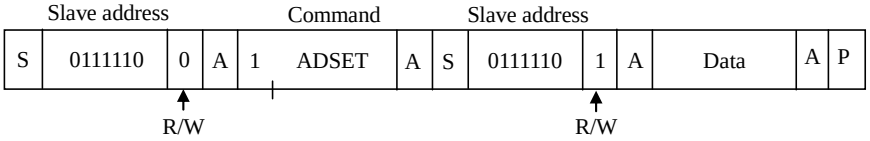
Data can be continuously written in the DDRAM by transmitting Data continuously.

BIT	0	1	2	3	4	5	6	7	·····	21h	22h	
0	a	i										COM0
1	b	j										COM1
2	c	k										COM2
3	d	l										COM3
4	e	m										COM4
5	f	n										COM5
6	g	o										COM6
7	h	p										COM7
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG33	SEG34	

DDRAM address

○Read Command Register and Transfer Method

BU97950 enters “Read mode” when R/W bit of Slave address is ‘1’
During Read mode the command registers can be read.
The sequence for the command register read is shown below.



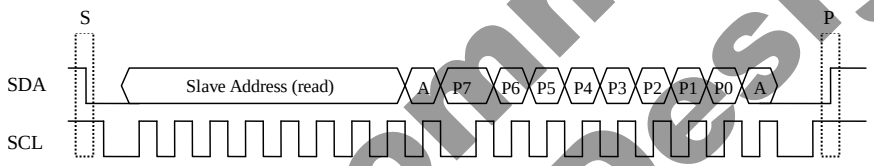
The following register settings can be read in this mode.
Only one register setting can be read at once, after reading register setting, BU97950 will exit from read mode and wait for slave address. If all register setting needs to be read, please make sequence for “REG1” and “REG2”, respectively.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	0	0	P5	P4	P3	P2	P1	P0	23h
REG2	P7	P6	P5	P4	P3	P2	P1	P0	24h

REG1: P5 = Software reset condition
P4 to P0 = EVR setting

REG2: P7 to P6 = Frame Frequency (FR) setting
P5 to P4 = Power Save Mode (SR) setting
P3 = LCD drive waveform setting
P2 = Display ON/OFF setting
P1 = APON setting
P0 = APOFF setting

An example of the command register read sequence is shown below.



○ LCD Driver Bias Circuit
This device generates LCD driving voltage with built in Buffer AMP.
And it can drive LCD at low power consumption.
*Line and frame inversion is set in DISCTL command.
Refer to the “LCD driving waveform” about each LCD driving waveform.

○ Reset initialize condition
Initial condition after Software Reset is as follows.
・Display is OFF.
・DDRAM address is initialized (DDRAM Data is not initialized).
Refer to Command Description about initialize value of register.

●Command / Function List
Description List of Command / Function

	Command	Function
1	Address set (ADSET)	DDRAM address setting (00h to 22h) Command register address setting (23h, 24h)
2	EVR set (EVRSET)	EVR setting (0 to 31)
3	Display Control (DISCTL)	Frame Frequency, Power save mode setting
4	IC operation set (ICSET)	LCD drive mode, software reset, display on/off
5	All pixel Control (APCTL)	All pixel control during display ON

●Detailed command description

D7 (MSB) is bit for command or data judgment.
For more detailed information, please refer to “Command and data transfer method”.

C: 0: Next byte is RAM write data.
1: Next byte is command.

○Address set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	P5	P4	P3	P2	P1	P0

Address data is specified in P[5:0].

The address range can be set as 000000 to 100010(bin) for Write mode.
When the specified address is out of range, the address will be set to “000000”.
The default value of the DDRAM address is “000000”

The address can be set 100011 (bin) and 100100 (bin) for Read mode.
It is prohibited to set other address.

P[5:0] = 23h（100011b）- REG1
Register address for Software reset condition and EVR setting

P[5:0] = 24h（100100b）- REG2
Register address for the other settings
(For more detailed information, please refer to “Read Command Register and Transfer Method”)

○EVR Set (EVRSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	P4	P3	P2	P1	P0

It is able to control a 32-step electrical volume register (EVR).
It is able to set V0 voltage level (the max level voltage of LCD driving voltage).

Electrical volume register (EVR) is set to “00000” upon initialization..
In “00000” condition, V0 voltage outputs VLCD voltage.

Avoid setting EVR V0 voltage under 2.5V.
And ensure “VLCD – V0 > 0.6” condition is satisfied.
Unstable IC output voltage may result if the above conditions are not satisfied.

○The relationship of electrical volume register (EVR) setting and V0 voltage

EVR	Calculation formula	VLCD= 5.500	VLCD= 5.000	VLCD= 4.000	VLCD= 3.500	VLCD= 3.000	VLCD= 2.500	[V]
0	VLCD	V0= 5.500	V0= 5.000	V0= 4.000	V0= 3.500	V0= 3.000	V0= 2.500	[V]
1	0.967*VLCD	V0= 5.323	V0= 4.839	V0= 3.871	V0= 3.387	V0= 2.903	V0= 2.419	[V]
2	0.937*VLCD	V0= 5.156	V0= 4.688	V0= 3.750	V0= 3.281	V0= 2.813	V0= 2.344	[V]
3	0.909*VLCD	V0= 5.000	V0= 4.545	V0= 3.636	V0= 3.182	V0= 2.727	V0= 2.273	[V]
4	0.882*VLCD	V0= 4.853	V0= 4.412	V0= 3.529	V0= 3.088	V0= 2.647	V0= 2.206	[V]
5	0.857*VLCD	V0= 4.714	V0= 4.286	V0= 3.429	V0= 3.000	V0= 2.571	V0= 2.143	[V]
6	0.833*VLCD	V0= 4.583	V0= 4.167	V0= 3.333	V0= 2.917	V0= 2.500	V0= 2.083	[V]
7	0.810*VLCD	V0= 4.459	V0= 4.054	V0= 3.243	V0= 2.838	V0= 2.432	V0= 2.027	[V]
8	0.789*VLCD	V0= 4.342	V0= 3.947	V0= 3.158	V0= 2.763	V0= 2.368	V0= 1.974	[V]
9	0.769*VLCD	V0= 4.231	V0= 3.846	V0= 3.077	V0= 2.692	V0= 2.308	V0= 1.923	[V]
10	0.750*VLCD	V0= 4.125	V0= 3.750	V0= 3.000	V0= 2.625	V0= 2.250	V0= 1.875	[V]
11	0.731*VLCD	V0= 4.024	V0= 3.659	V0= 2.927	V0= 2.561	V0= 2.195	V0= 1.829	[V]
12	0.714*VLCD	V0= 3.929	V0= 3.571	V0= 2.857	V0= 2.500	V0= 2.143	V0= 1.786	[V]
13	0.697*VLCD	V0= 3.837	V0= 3.488	V0= 2.791	V0= 2.442	V0= 2.093	V0= 1.744	[V]
14	0.681*VLCD	V0= 3.750	V0= 3.409	V0= 2.727	V0= 2.386	V0= 2.045	V0= 1.705	[V]
15	0.666*VLCD	V0= 3.667	V0= 3.333	V0= 2.667	V0= 2.333	V0= 2.000	V0= 1.667	[V]
16	0.652*VLCD	V0= 3.587	V0= 3.261	V0= 2.609	V0= 2.283	V0= 1.957	V0= 1.630	[V]
17	0.638*VLCD	V0= 3.511	V0= 3.191	V0= 2.553	V0= 2.234	V0= 1.915	V0= 1.596	[V]
18	0.625*VLCD	V0= 3.438	V0= 3.125	V0= 2.500	V0= 2.188	V0= 1.875	V0= 1.563	[V]
19	0.612*VLCD	V0= 3.367	V0= 3.061	V0= 2.449	V0= 2.143	V0= 1.837	V0= 1.531	[V]
20	0.600*VLCD	V0= 3.300	V0= 3.000	V0= 2.400	V0= 2.100	V0= 1.800	V0= 1.500	[V]
21	0.588*VLCD	V0= 3.235	V0= 2.941	V0= 2.353	V0= 2.059	V0= 1.765	V0= 1.471	[V]
22	0.576*VLCD	V0= 3.173	V0= 2.885	V0= 2.308	V0= 2.019	V0= 1.731	V0= 1.442	[V]
23	0.566*VLCD	V0= 3.113	V0= 2.830	V0= 2.264	V0= 1.981	V0= 1.698	V0= 1.415	[V]
24	0.555*VLCD	V0= 3.056	V0= 2.778	V0= 2.222	V0= 1.944	V0= 1.667	V0= 1.389	[V]
25	0.545*VLCD	V0= 3.000	V0= 2.727	V0= 2.182	V0= 1.909	V0= 1.636	V0= 1.364	[V]
26	0.535*VLCD	V0= 2.946	V0= 2.679	V0= 2.143	V0= 1.875	V0= 1.607	V0= 1.339	[V]
27	0.526*VLCD	V0= 2.895	V0= 2.632	V0= 2.105	V0= 1.842	V0= 1.579	V0= 1.316	[V]
28	0.517*VLCD	V0= 2.845	V0= 2.586	V0= 2.069	V0= 1.810	V0= 1.552	V0= 1.293	[V]
29	0.508*VLCD	V0= 2.797	V0= 2.542	V0= 2.034	V0= 1.780	V0= 1.525	V0= 1.271	[V]
30	0.500*VLCD	V0= 2.750	V0= 2.500	V0= 2.000	V0= 1.750	V0= 1.500	V0= 1.250	[V]
31	0.491*VLCD	V0= 2.705	V0= 2.459	V0= 1.967	V0= 1.721	V0= 1.475	V0= 1.230	[V]

Prohibited setting

*In case EVR is used, please satisfy VLCD-V0 >0.6 V condition.
If this condition cannot be satisfied, IC output will be unstable.
*Do not use V0 < 2.5V area. If EVR is set to this area, IC operation will be unstable.

○Display control (DISCTL)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	1	1	0	P3	P2	P1	P0

Set Power save mode FR.

Power save mode FR	P3	P2	Reset initialize condition
Normal mode (80Hz)	0	0	○
Power save mode1 (71Hz)	0	1	
Power save mode2 (64Hz)	1	0	
Power save mode3 (50Hz)	1	1	

∗ Operation current decrease in
Normal mode > Power save mode1 > Power save mode2 > Power save mode 3 order.

Set Power save mode SR.

Setup	P1	P0	Reset initialize condition
Power save mode 1	0	0	
Power save mode 2	0	1	
Normal mode	1	0	○
High power mode	1	1	

∗ Operation current increase in order of
Power save mode 1 < Power save mode 2 < Normal mode < High power mode order.

Note:
Power save mode FR / LCD drive waveform / Power save mode SR will affect the display image. Select the best value depending on the current consumption and display image using LCD panel (under real application).

Mode	Flicker	Display grade/Contrast
Power save mode FR	○	-
LCD drive waveform (ICSET)	○	○
Power save mode SR	-	○

○Set IC Operation (ICSET)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	1	1	1	0	P2	P1	P0

Set LCD drive waveform.

Setup	P2	Reset initialize condition
Line inversion mode	0	
Frame inversion mode	1	○

Operation current: Line inversion > Frame inversion
For drive mode of Line inversion and Frame inversion, refer to LCD waveform.

Set Software Reset condition.

Setup	P1	Reset initialize condition
No operation	0	○
Software reset	1	

When “Software Reset” is executed, this device is reset to initial condition.
(Refer to Reset initialize condition)
Software reset is asserted only once when P1 is set.
Other settings can be set after this.

Set Display ON and OFF

Setup	P0	Reset initialize condition
Display OFF (DISPOFF)	0	○
Display ON (DISPON)	1	

Display OFF : The DDRAM content is not affected. All SEGMENT and COMMON output stop after a frame.
Display OFF mode ends when Display ON is set.

Display ON : SEGMENT and COMMON outputs are active.
Start read operation to display data from the DDRAM.

○All Pixel control (APCTL)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	1	1	1	1	0	P1	P0

All display set ON

APON	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

All display set OFF

APOFF	P0	Reset initialize condition
Normal	0	○
All pixel OFF	1	

All pixels ON : All pixels are ON regardless of DDRAM data.
All pixels OFF : All pixels are OFF regardless of DDRAM data.

Note:
All pixels ON/OFF is effective only at the time of “Display ON” status.
The contents of DDRAM do not change at this time.
When P1 and P0=’1’, APOFF is selected. APOFF has higher priority than APON.

●LCD driving waveform

(1/4bias, 1/8duty)

Line inversion mode

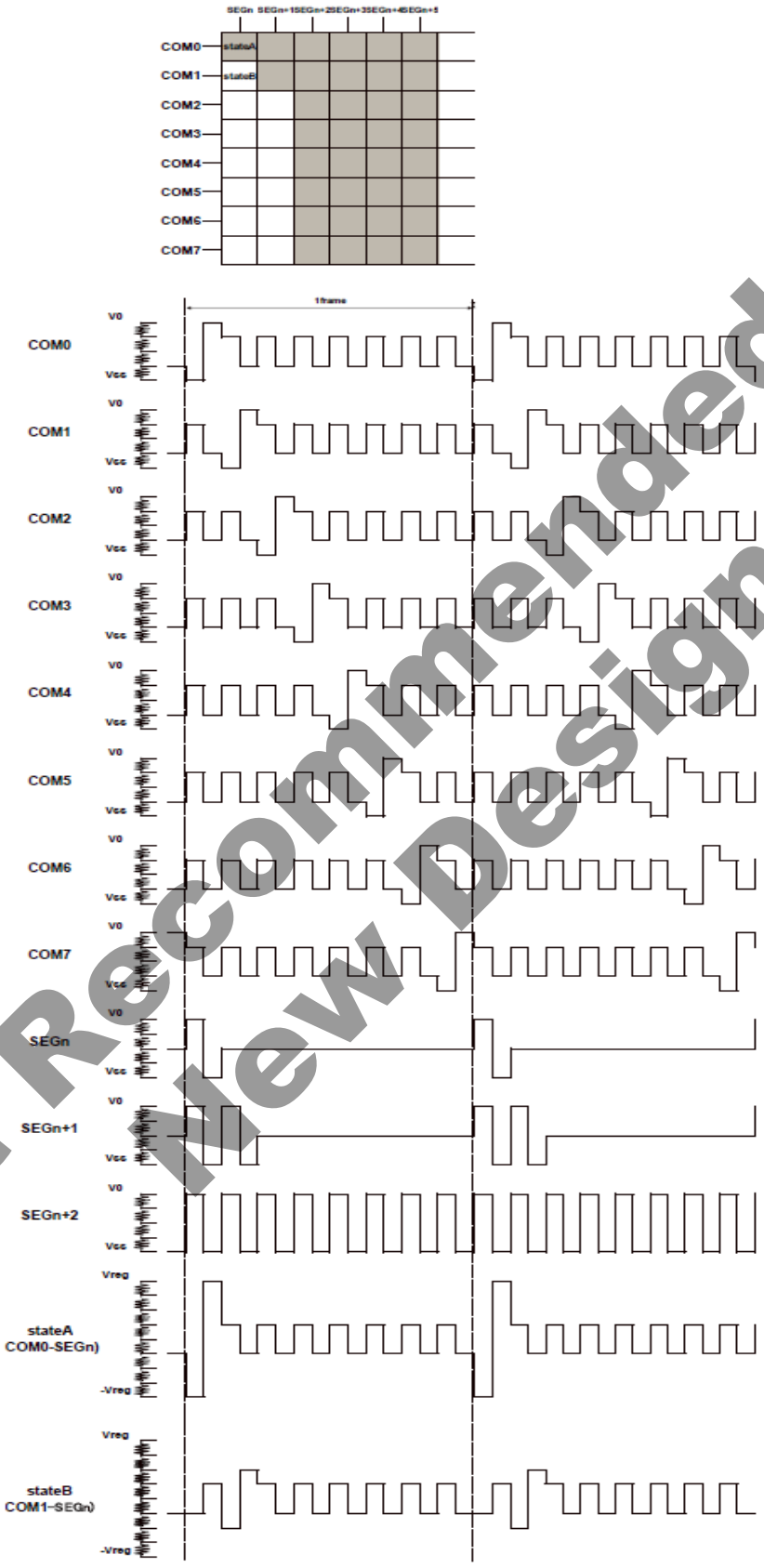


Figure 10. Wave form of line inversion

Frame inversion mode

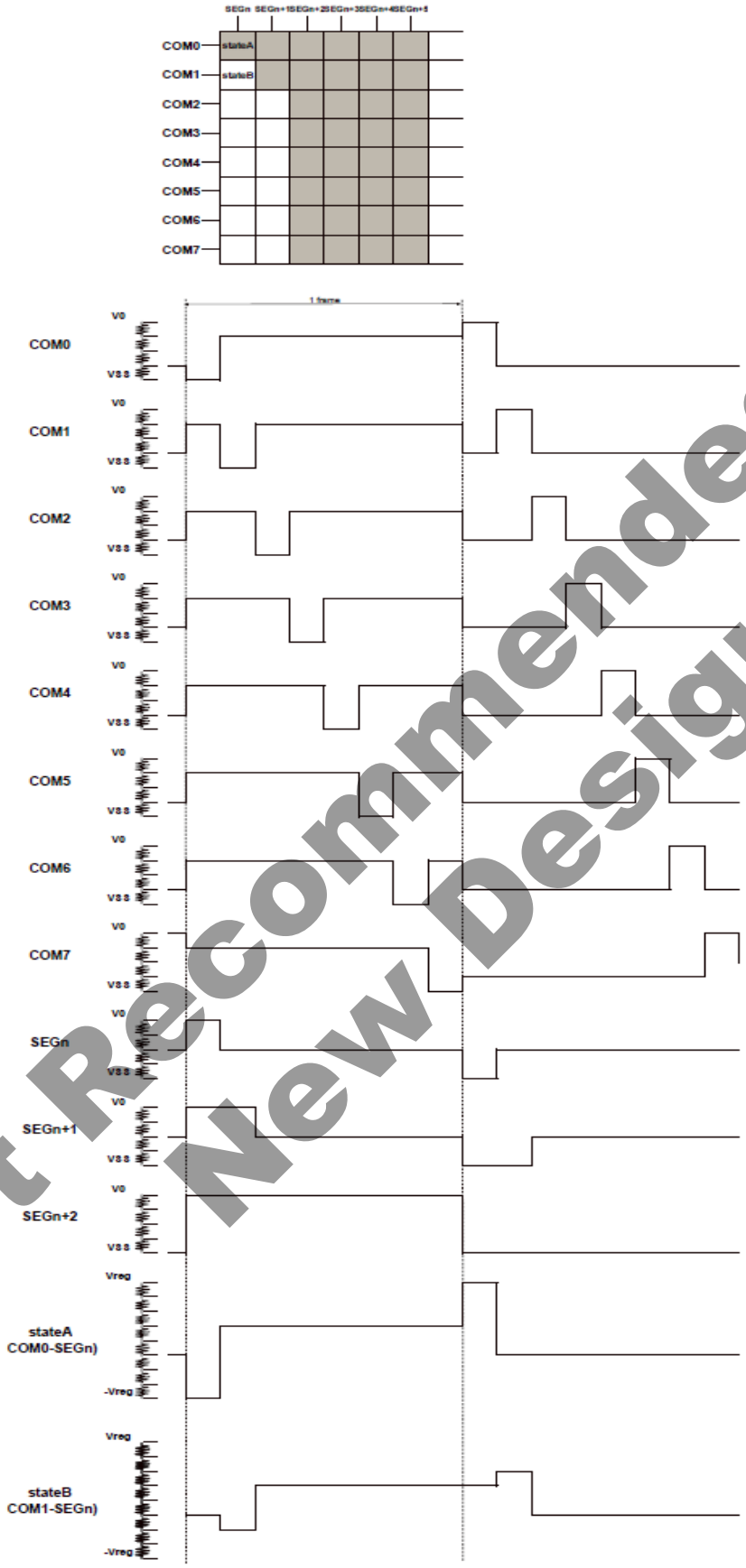


Figure 11. Wave form of frame inversion

●Initialize sequence

Please follow the sequence below after Power-On to set this device to initial condition.

Power on
↓
STOP condition
↓
START condition
↓
Issue Slave address
↓
Execute Software Reset by ICSET command
Each register value and DDRAM address is initialized to their default values.
DDRAM data is random after power on.

●Start sequence

○Start sequence example

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power on									VDD=0 to 5V (Tr=0.1ms)
	↓									
2	wait 100us									Initialize IC
	↓									
3	Stop									Stop condition
	↓									
4	Start									Start condition
5	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
6	ICSET	1	1	1	1	0	*	1	*	Software Reset
	↓									
7	DISCTL	1	1	1	0	0	0	1	0	Unnecessary when initial value setup
	↓									(If you need to change the condition)
8	EVRSET	1	1	0	0	0	0	0	0	Unnecessary when initial value setup
	↓									(If you need to change the condition)
9	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
10	Display Data	*	*	*	*	*	*	*	*	Address 00h
	⋮									⋮
	Display Data	*	*	*	*	*	*	*	*	Address 22h
	↓									
11	Stop									Stop condition
	↓									
12	Start									Start condition
13	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
14	ICSET	1	1	1	1	0	*	0	1	Display ON

●**Caution in P.O.R circuit use**

This device has “P.O.R.” (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.

Please set power up conditions to meet the recommended tR, tF, tOFF, and Vbot spec below in order to ensure P.O.R. operation

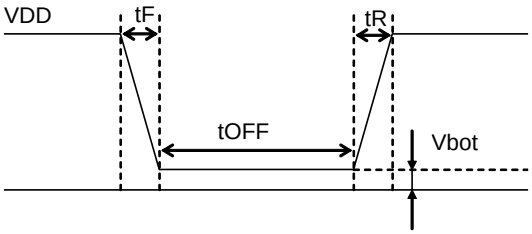


Figure 12. Power ON/OFF waveform

Recommended condition of tR, tF, tOFF, Vbot (Ta=25 ºC)

tR	tF	tOFF	Vbot
Less than 5ms	Less than 5ms	More than 20ms	Less than 0.3V

If it is difficult to meet above conditions, execute the following sequence after Power-On.

(1) STOP condition

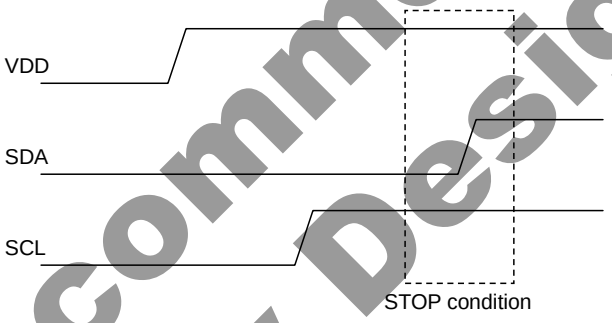


Figure 13. STOP condition

(2) START condition.
(3) Issue Slave address.
(4) Execute Software Reset (ICSET) command.

●Power Up Sequence and Power Down Sequence

To prevent incorrect display, malfunction and abnormal current,
VDD must be turned on before VLCD In power up sequence.
VDD must be turned off after VLCD In power down sequence.
Please satisfies VLCD≥VDD, t1>0ns, t2>0ns

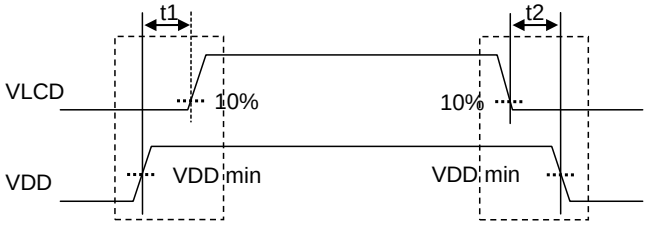


Figure 14. Power On/Off Sequence

●Note on the number of LSIs being connected to the same bus.

Do not access the other device without power supply (VDD) to the BU97950.

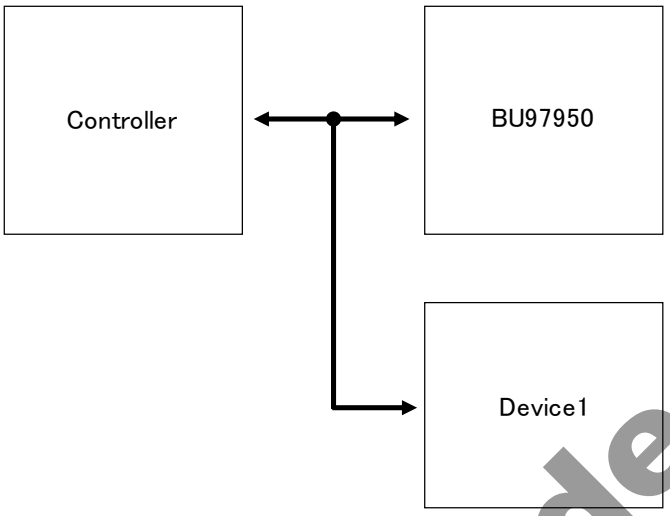


Figure 15. Example of BUS connection

To control the slope of the falling edge, a capacitor is connected between gate and drain of a NMOS transistor (Refer to Figure16).
The gate is in a high-impedance state if the power supply (VDD) is not supplied.

In this condition, the gate voltage is pulled up by the current flow through the capacitance as a result of the SDA signal's transition from LOW to HIGH.

The NMOS transistor turns on and draws some current (Ids) from the SDA port if the gate voltage (Vg) is higher than the threshold voltage (Vth).

An external resistor (R) is connected between the power line and SDA line to keep the SDA line as logic HIGH.
But the line cannot be kept as logic HGH if the voltage drop (R*Ids) is large.

Access the other LSIs with power supply to BU9792x to control the gate voltage as logic level of 1 or 0 if the number of LSIs are connected to the same bus.

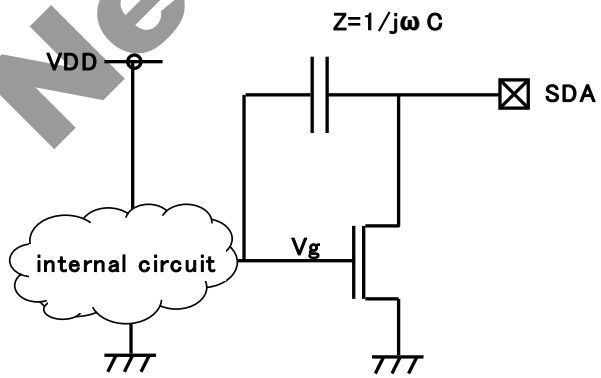


Figure 16. SDA output cell structure

●Operational Notes

(1) Absolute maximum ratings

Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

(2) Recommended operating conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

(4) Power supply lines

Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

(5) Ground Voltage

The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

(6) Short between pins and mounting errors

Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

(7) Operation under strong electromagnetic field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

(8) Testing on application boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(9) Regarding input pins of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the GND voltage should be avoided. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input terminals have voltages within the values specified in the electrical characteristics of this IC.

(10) GND wiring pattern

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

(11) External Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

(12) Unused input terminals

Input terminals of an IC are often connected to the gate of a CMOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or ground line.

(13) Rush current

When power is first supplied to the IC, rush current may flow instantaneously. It is possible that the charge current to the parasitic capacitance of internal photo diode or the internal logic may be unstable. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

●Ordering Information

B U 9 7 9 5 0 x x x - x x

Part Number

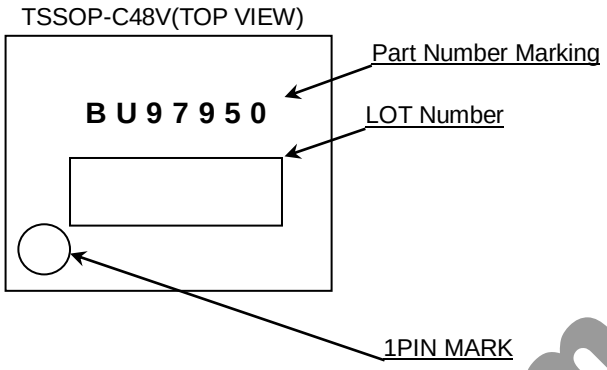
Package
FUV : TSSOP-C48V

Packaging and forming specification
E2: Embossed tape and reel
(TSSOP-C48V)

●**Lineup**

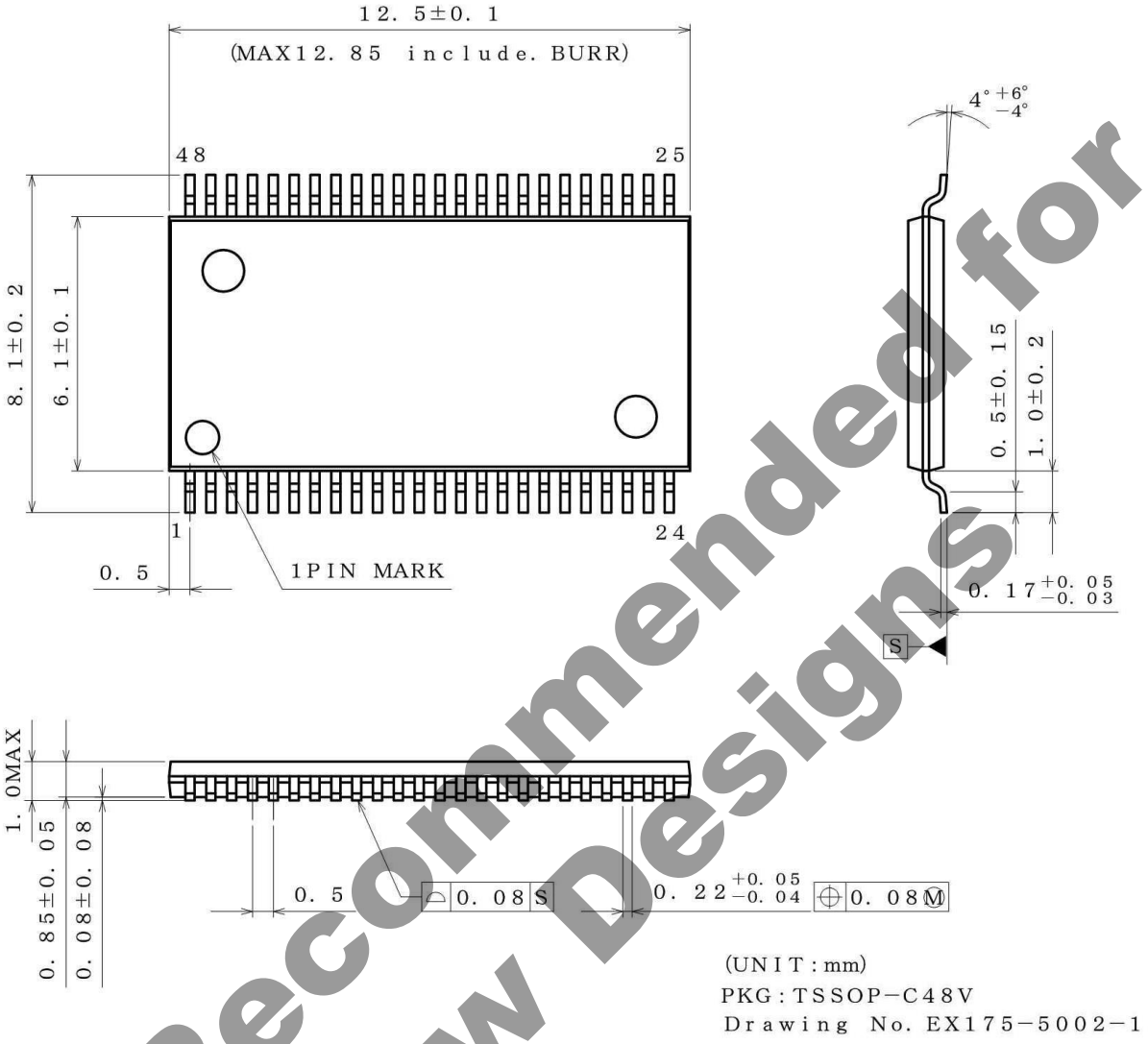
Package		Orderable Part Number
TSSOP-C48V	Reel of 2000	BU97950FUV-E2

●**Marking Diagrams**



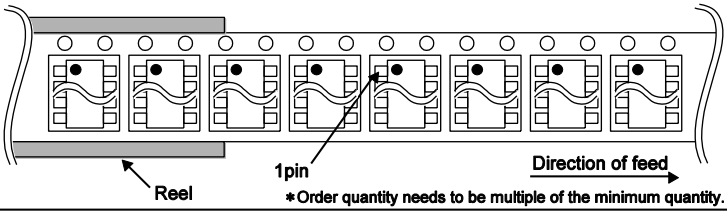
●**Physical Dimension, Tape and Reel Information**

Package Name	TSSOP-C48V



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

●**Revision History**

Date	Revision	Changes
14.Mar.2012	001	New Release
8.Jan.2013	002	Improved the statement in all pages. Deleted “Status of this document” in page 20. Changed format of Physical Dimension, Tape and Reel Information.
22.Apr.2013	003	Delete BU97950KS2
8.Sep.2015	004	Add Power Up Sequence and Power Down Sequence in page 16. Changed figure number of Example of BUS connection in page 17. Changed figure number of SDA output cell structure in page 17.
19.Apr.2018	005	Add the watermark of NRND due to the change to “Not recommended for new designs products”

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] the Products are exposed to high Electrostatic

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