LAPIS SEMICONDUCTOR

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ML5238

Preliminary Ver.7

16 series Li-ion secondary battery protection, Analog Front End IC

■ GENERAL DESCRIPTION

The ML5238 is analog front end IC for 16 series Lithium Ion secondary battery pack protection system. The ML5238 provides the function of cell voltage monitoring, charge/discharge current monitoring function, and it can detect over-charge/over-discharge of each battery cell charge/discharge over-current.
The ML5238 has short current detecting function which can turn off the external charge/discharge MOS-FET without external MCU.

■ FEATURES

- 16 cell highly accurate voltage monitoring function: output cell voltage by half from VMON pin
- built-in cell balancing switches for each cell
- charge/discharge current monitoring function :

  Select voltage gain of ISP-ISM and output from IMON pin.

  Voltage gain selection: x10 / x50
- short current detecting function: detecting threshold voltage is selectable,

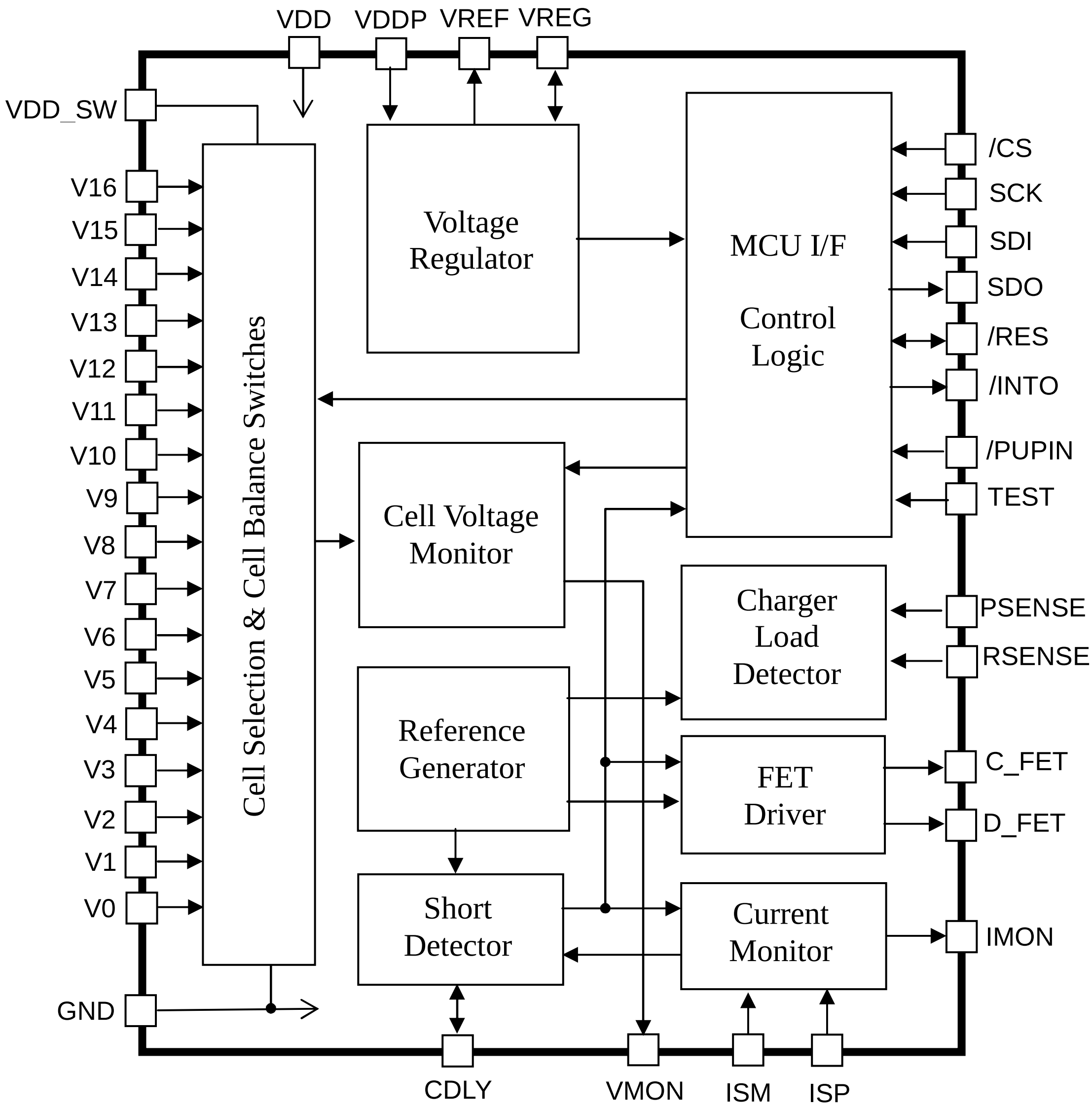
  ISP-ISM voltage = 0.1V/0.2V/0.3V/0.4V (typ),

  the detecting delay time is set by external capacitor
- external charge/discharge FET control: NMOS-FET driver built-in
- MCU interface: SPI serial interface (mode 0)
- 3.3V regulator for external MCU built-in: output current is 10mA (max)
- Reference voltage regulator for external ADC: 3.3V(typ), 3.28V(min),3.34V(max) @Ta=-10°C to +60°C
- Small power consumption

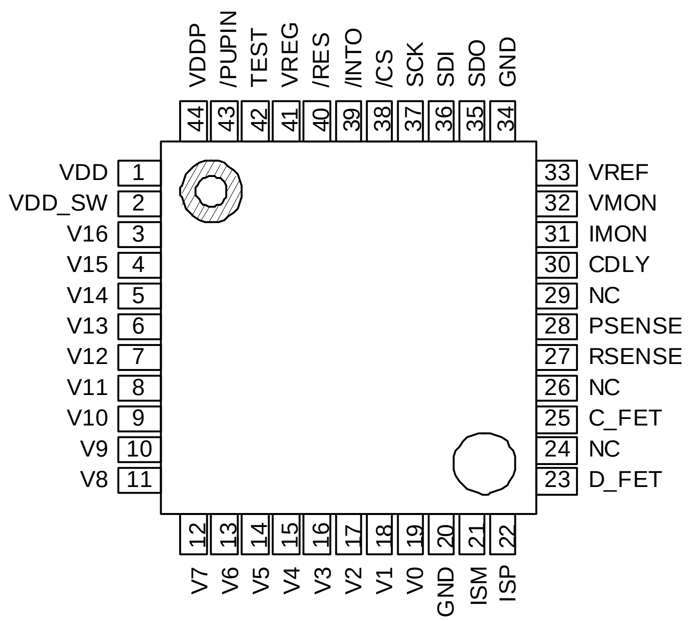
  Normal state : 50µA (typ), 100µA (max)
  Power save state : 25µA (typ), 50µA (max)
  Power down state : 0.1µA (typ), 1µA (max)
- power supply voltage : +7V to +80V
- operating temperature : -40°C to +85°C
- package : 44 pin plastic QFP (QFP44-P-910-0.80-2K)

Note: The ML5238 is forbidden to be used for automotive or any equipment, device or system which requires an extremely high level of reliability.

■ BLOCK DIAGRAM



■ PIN CONFIGURATION (TOP VIEW)



■ PIN DESCRIPTION

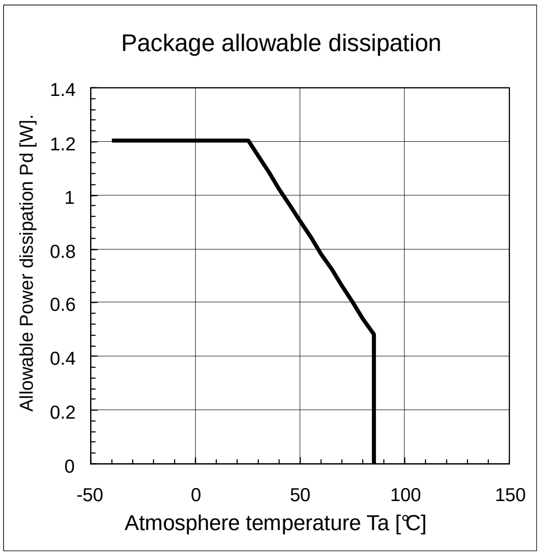
Pin No.	Pin name	I/O	Description
1	VDD	–	Power supply input pin. Connect CR filters for noise rejection.
2	VDD_SW	–	Power supply input pin for battery selection switches and cell balancing switched. Connect this pin to VDD via resistor.
3	V16	I	Battery cell 16 high voltage input pin If number of connected cell is 5 to 16, connect this pin to VDD_SW pin.
4	V15	I	Battery cell 16 low voltage input and Battery cell 15 high voltage input pin
5	V14	I	Battery cell 15 low voltage input and Battery cell 14 high voltage input pin
6	V13	I	Battery cell 14 low voltage input and Battery cell 13 high voltage input pin
7	V12	I	Battery cell 13 low voltage input and Battery cell 12 high voltage input pin
8	V11	I	Battery cell 12 low voltage input and Battery cell 11 high voltage input pin
9	V10	I	Battery cell 11 low voltage input and Battery cell 10 high voltage input pin
10	V9	I	Battery cell 10 low voltage input and Battery cell 9 high voltage input pin For the 5 cell series connected battery pack application, connect this pin to GND
11	V8	I	Battery cell 9 low voltage input and Battery cell 8 high voltage input pin For the 5 to 6 cell series connected battery pack application, connect this pin to GND
12	V7	I	Battery cell 8 low voltage input and Battery cell 7 high voltage input pin For the 5 to 7 cell series connected battery pack application, connect this pin to GND
13	V6	I	Battery cell 7 low voltage input and Battery cell 6 high voltage input pin For the 5 to 8 cell series connected battery pack application, connect this pin to GND
14	V5	I	Battery cell 6 low voltage input and Battery cell 5 high voltage input pin For the 5 to 9 cell series connected battery pack application, connect this pin to GND
15	V4	I	Battery cell 5 low voltage input and Battery cell 4 high voltage input pin For the 5 to 10 cell series connected battery pack application, connect this pin to GND
16	V3	I	Battery cell 4 low voltage input and Battery cell 3 high voltage input pin For the 5 to 11 cell series connected battery pack application, connect this pin to GND
17	V2	I	Battery cell 3 low voltage input and Battery cell 2 high voltage input pin For the 5 to 12 cell series connected battery pack application, connect this pin to GND
18	V1	I	Battery cell 2 low voltage input and Battery cell 1 high voltage input pin For the 5 to 13 cell series connected battery pack application, connect this pin to GND
19	V0	I	Battery cell 1 low voltage input pin For the 5 to 14 cell series connected battery pack application, connect this pin to GND
20, 34	GND	–	Ground pin.
21	ISM	I	Current sensing resistor connecting pin. Connect this pin to the low voltage terminal of the lowest level battery cell.
22	ISP	I	Current sensing resistor connecting pin. The voltage of this pin should be higher than the ISM pin in discharging state.
23	D_FET	O	Discharging NMOS-FET control signal pin. Connect this pin to the gate pin of the external NMOS FET. Output voltage is 14V (typ) for setting ON, output voltage is 0V for setting OFF.

Pin No.	Pin name	I/O	Description
25	C_FET	O	Charging NMOS-FET control signal output pin. Connect this pin to the gate pin of the external NMOS FET. Output voltage is 14V (typ) for setting ON, output is Hi-Z for setting OFF.
27	RSENSE	I	Input pin for detecting the load disconnection. Connect this pin to the negative side of the load.
28	PSENSE	I	Input pin for detecting the charger disconnection. Connect this pin to the negative side of the charger. If charger is connected to the same node as the load, connect this pin to the RSENSE pin.
30	CDLY	IO	Short current detection delay time setting pin. Connect a capacitor between GND and this pin.
31	IMON	O	Current monitor output pin. The voltage amplified the voltage between ISP-ISM by 10 or 50 is outputted. When current is not flowing, 1V (typ) is outputted.
32	VMON	O	Cell voltage monitor output pin. The voltage amplified a cell voltage by 0.5 is outputted.
33	VREF	O	Reference voltage output (3.3V) for external ADC. Connect a 4.7µF capacitor between this pin and the GND pin.
35	SDO	O	Serial interface data output pin. If /CS input is "H", output of this pin is Hi-Z state.
36	SDI	I	Serial interface data input pin.
37	SCK	I	Serial interface clock input pin. Capture the SDI input at the rising edge of the SCK clock. Output the data from the SDO pin at the falling edge of the SCK.
38	/CS	I	Serial interface chip select pin. The serial interface is active if the input is "L".
39	/INTO	O	Interrupt signal output to external MCU. This pin is a NMOS open drain output pin and output is "L" level if interrupted.
40	/RES	IO	Reset signal input and a reset signal output to external MCU. Since this pin is a NMOS open drain output pin, connect a 0.1µF capacitor between this pin and GND pin and pull-up resisitor. When recovered power-down state, "L" level reset pulse will be outputted and both ML5238 and external MCU will be initialized.
41	VREG	IO	Built-in 3.3V regulator output pin. Connect a 4.7µF capacitor between this pin and GND pin. It can be used as a power supply to the external MCU. And it is also used as a power supply to the MCU interface circuit in this IC.
42	TEST	I	Test input pin. Fix to GND level.
43	/PUPIN	IO	Power-up trigger input pin. If input is "L" level, the state of the ML5238 changes from power-down state to Initial state. A 100kΩ pull-up resistor is built-in between this pin and the VDD pin.
44	VDDP	–	Power supply input pin for internal regulator. Connect CR filters for noise rejection.
24, 26, 29	NC	–	No connection pin. Open this pin.

■ ABSOLUTE MAXIMUM RATINGS

(GND=0 V, Ta=25℃)

Parametor	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	VDD, VDDP , VDD_SW	-0.3 to +86.5	V
Input voltage	V_{IN1}	V16 ~ V0, Voltage difference between Vn+1 – Vn pin	-0.3 to +6.5	V
	V_{IN2}	RSENSE, PSENSE	V_{DD} - 86.5 to V_{DD}+0.3	V
	V_{IN3}	/PUPIN	-0.3 to V_{DD} + 0.3	V
	V_{IN4}	/CS, SCK, SDI, ISM, ISP	-0.3 to V_{REG} + 0.3	V
Output voltage	V_{OUT1}	D_FET	-0.3 to V_{DD} + 0.3	V
	V_{OUT2}	C_FET	V_{DD} - 86.5 to V_{DD} + 0.3	V
	V_{OUT3}	/RES, /INTO	-0.3 to + 6.5	V
Output short current	I_{OS}	VDD=50V, VREG, SDO, /RES, /INTO, C_FET, D_FET	20	mA
Cell balancing curren	I_{CB}	Per a cell balancing switch	200	mA
Allowable power Dissipation	P_D	Ta = 25℃	1.2	W
Junction temperature	Tj_{MAX}	–	125	℃
Package thermal resistance	θ ja	JEDEC 2 layer board	83	℃ /W
Storage tempetrature	T_{STG}	–	-55 to +150	℃



Package loss tolerant decreases as the atmosphere temperature (Ta) increase. If VREG pin output load current is large, make the power loss smaller than the value shown in this figure.

■ RECOMMENDED OPERATING CONDITIONS

(GND= 0 V)

Parameter	Symbol	Condition	Range	unit
Power supply voltage	V_{DD}	VDD, VDDP, VDD_SW	7 to 80	V
Opereating temperature	Ta	VREG no-loaded	-40 to +85	°C

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS

V_{DD}=7 to 80V, GND=0 V, Ta=-40 to +85℃, VREG output no-loaded

Parameter	Symbol	Condition	Min.	Typ.	Max.	unit
Digital "H" input voltage (note1)	V_{IH}	–	0.8×V_{REG}	–	V_{REG}	V
Digital "L" input voltage (note1)	V_{IL}	–	0	–	0.2×V_{REG}	V
/PUPIN-pin "H" input voltage	V_{IHP}	–	0.8×V_{DD}	–	V_{DD}	V
/PUPIN-pin "L" input voltage	V_{ILP}	–	0	–	0.2×V_{DD}	V
Digital "H" input current(note1)	I_{IH}	V_{IH} = V_{REG}	–	–	2	µA
Digital "L" input current (note1)	I_{IL}	V_{IL} = GND	-2	–	–	µA
/PUPIN-pin "H" input current	I_{IHP}	V_{IH} = V_{DD}	–	–	2	µA
/PUPIN-pin "L" input current	I_{ILP}	V_{DD}= 64V, V_{IL} = GND	-128	-64	-32	µA
Digital "H" output voltage (note2)	V_{OH}	I_{OH}= -100µA	V_{REG} - 0.2	–	V_{REG}	V
Digital "L" output voltage (note3)	V_{OL}	I_{OL}= 1mA	0	–	0.2	V
Digital output Leak current (note3)	I_{OLK}	V_{OH}=3V V_{OL}=0V	-2	–	2	µA
Cell monitoring pin Input current (note 4)	I_{INVC}	If measuring battery cell voltage	-5	–	15	µA
Cell monitoring pin Input leak current (note4)	I_{ILVC}	If not measuring battery cell voltage	-5	–	5	µA
FET "H" output voltage (note5)	V_{OH}	I_{OH}=-10µA V_{DD}=18V to 72V	10	14	18	V
FET "L" output voltage (note6)	V_{OL}	I_{OL} = 100µA	0	–	0.3	V
C_FET output leak current	I_{LVC}	V_{CFET}=0V to V_{DD}	-5	–	5	µA
VREG output voltage	V_{REG}	Output No-loaded	3.1	3.3	3.6	V
	V_{REG1}	10V<V_{DD}<64V Ta=-10 to 60℃ Load current < 10mA	3.1	3.3	3.5	V
	V_{REG2}	10V<V_{DD}<64V Ta=-40 to 70℃ Load current < 10mA	3.0	3.3	3.6	V
	V_{REG3}	7V<V_{DD}<10V Ta = -10 to 60℃ Load current < 5mA	3.1	3.3	3.5	V
	V_{REG4}	7V<V_{DD}<10V Ta = -40 to 85℃ Load current < 5mA	3.0	3.3	3.6	V
VREF output voltage	V_{REF1}	Ta = -10 to 60℃ Load current < 1mA	3.28	3.30	3.34	V
	V_{REF2}	Ta = -40 to 85℃ Load current < 1mA	3.25	3.30	3.35	V
Cell balancing switch ON resistance	R_{BL}	Internal balancing FET V_{DS} = 0.6V V_{DD} = 18V to 64V	3	6	12	Ω

Note 1: Applied to pins: /CS, SCK, SDI
Note2: Applied to SDO pin
Note3: Applied to pins: SDO, /RES, /INTO
Note4: Applied to pins V16 to V0
Note5: Applied to pins C_FET, D_FET
Note6: Applied to D_FET pin

- **SUPPLY CURRENT CHARACTERISTICS**

V_{DD}=7 to 64V, GND=0 V, Ta=-40 to +85℃, VREG, VREF output no noaded

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Normal operating Current	I_{DD1}	No-loaded	–	50	100	μA
Power save Current	I_{DD2}	No-loaded	–	25	50	μA
Power down Current	I_{DDS}	No-loaded	–	0.1	1.0	μA

(note) These power supply current is defined as the total current of VDD-pin and the VDDP-pin.
(note) The load current is added to these power supply current, using the load with VREG connector.

- **DETECTING VOLTAGE CHARACTERISTICS (TA=25°C)**

V_{DD}=48V, GND=0 V, Ta=25℃, VREG output no-loaded

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Short current detecting voltage	V_{SHRT0}	SC1,SC0 bit = (0,0)	0.05	0.1	0.15	V
	V_{SHRT1}	SC1,SC0 bit = (0,1)	0.1	0.2	0.3	V
	V_{SHRT2}	SC1,SC0 bit = (1,0)	0.2	0.3	0.4	V
	V_{SHRT3}	SC1,SC0 bit = (1,1)	0.3	0.4	0.5	V
Short current detecting delay time	t_{SHRT}	C_{DLY} = 1nF	50	100	200	µs
VREG low detecting voltage	V_{RD}	–	2.3	2.45	2.6	V
VREG recovery detecting voltage	V_{RR}	–	2.5	2.75	2.9	V

(note) Short detecting delay time tSC [μs]=CDLY[nF] x 100.

- **DETECTING VOLTAGE CHARACTERISTICS (TA= -10 ~ 60°C)**

V_{DD}=48V, GND=0 V, Ta=-10~+60℃, VREG output no-loaded

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Short current detecting voltage	V_{SHRT0}	SC1,SC0 bit = (0,0)	0.04	0.1	0.16	V
	V_{SHRT1}	SC1,SC0 bit = (0,1)	0.09	0.2	0.31	V
	V_{SHRT2}	SC1,SC0 bit = (1,0)	0.19	0.3	0.41	V
	V_{SHRT3}	SC1,SC0 bit = (1,1)	0.29	0.4	0.51	V
Short current detecting delay time	t_{SHRT}	C_{DLY} = 1nF	40	100	220	µs
VREG low detecting voltage	V_{RD}	–	2.20	2.45	2.70	V
VREG recovery detecting voltage	V_{RR}	–	2.40	2.75	3.00	V

(note) Short detecting delay time tSC [μs]=CDLY[nF] x 100.

• VOLTAGE AND CURRENT MONITORING CHARACTERISTICS (TA=25°C)

V_{DD}=48V, GND=0V, Ta=25℃, VREG output no-loaded

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VMON output voltage	V_{VMC1}	Cell voltage = 3.6V Output no-loaded	1.79	1.8	1.81	V
	V_{VMC2}	Cell voltage = 1V Output no-loaded	0.48	0.50	0.52	V
IMON output voltage	V_{IMON0}	ISP-ISM voltage difference = 0V GIM bit = "0"	0.9	1.0	1.1	V
	V_{IMON1}	ISP-ISM voltage difference = 0V GIM bit = "1"	0.5	1.0	1.5	V
IMON output voltage gain	G_{IM0}	GIM bit = "0"	9	10	11	V/V
	G_{IM1}	GIM bit = "1"	45	50	55	V/V

• VOLTAGE AND CURRENT MONITORING CHARACTERISTICS (TA=-10 ~60°C)

V_{DD}=48V, GND=0V, Ta=-10~+60℃, VREG output no-loaded

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VMON output voltage	V_{VMC1}	Cell voltage = 3.6V Output no-loaded	1.78	1.8	1.82	V
	V_{VMC2}	Cell voltage = 1V Output no-loaded	0.47	0.50	0.53	V
IMON output voltage	V_{IMON0}	ISP-ISM voltage difference = 0V GIM bit = "0"	0.85	1.0	1.15	V
	V_{IMON1}	ISP-ISM voltage difference = 0V GIM bit = "1"	0.4	1.0	1.6	V
IMON output voltage gain	G_{IM0}	GIM bit = "0"	8.5	10.0	11.5	V/V
	G_{IM1}	GIM bit = "1"	44	50	56	V/V

- **LOAD DISCONNECTION, CHARGER CONNECTION AND DISCONNECTION DETECTING VOLTAGE CHARACTERISTIC (TA=25°C)**

V_{DD}=48V, GND=0V, Ta=25℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detecting Charger connection PSENSE pin voltage	V_{PC}	At power up from power down state	V_{DD}× 0.2	V_{DD}×0.5	V_{DD}×0.8	V
Detecting charger disconnection PSENSE pin voltage	V_{PLU}	PSENSE register PSL bit threshold	0.1	0.2	0.3	V
	V_{PLD}	PSENSE register PSH bit threshold	V_{DD} × 0.7	V_{DD}×0.75	V_{DD}×0.8	V
Detecting load disconnection RSENSE pin voltage	V_{RL}	RSENSE register RRS bit threshold	2.2	2.4	2.6	V
PSENSE pull-up resistor	R_{PU}	PSENSE register EPSL、EPSH = "1"	300	500	850	kΩ
RSENSE pull-down resistor	R_{PD}	RSENSE register ERS = "1"	1	2	3	MΩ
PSENSE input leakage current	I_{LPS}	pull-up resistor is not connected	-2	–	2	µA
RSENSE input leakage current	I_{LRS}	Pull-down resistor is not connected	-2	–	2	µA

- **LOAD DISCONNECTION, CHARGER CONNECTION AND DISCONNECTION DETECTING VOLTAGE CHARACTERISTIC (TA=-10 ~60°C)**

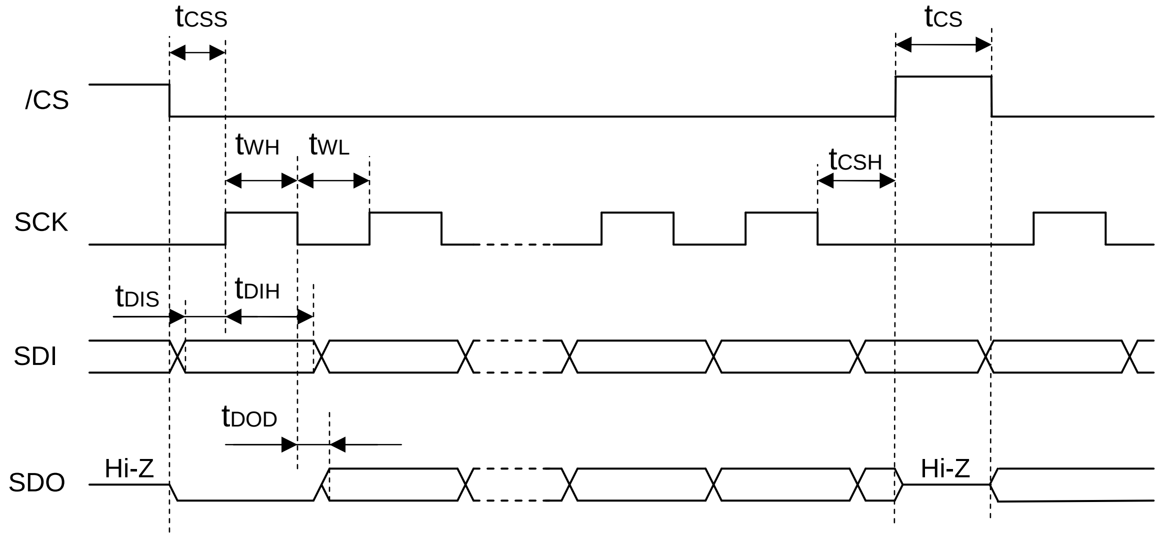
V_{DD}=48V, GND=0V, Ta=-10~60℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detecting Charger connection PSENSE pin voltage	V_{PC}	At power up from power down state	V_{DD}× 0.2	V_{DD}×0.5	V_{DD}×0.8	V
Detecting charger disconnection PSENSE pin voltage	V_{PLU}	PSENSE register PSL bit threshold	0	0.2	0.4	V
	V_{PLD}	PSENSE register PSH bit threshold	V_{DD} × 0.65	V_{DD}×0.75	V_{DD}×0.85	V
Detecting load disconnection RSENSE pin voltage	V_{RL}	RSENSE register RRS bit threshold	2.0	2.4	2.8	V
PSENSE pull-up resistor	R_{PU}	PSENSE register EPSL、EPSH = "1"	200	500	1000	kΩ
RSENSE pull-down resistor	R_{PD}	RSENSE register ERS = "1"	0.5	2	4	MΩ
PSENSE input leakage current	I_{LPS}	pull-up resistor is not connected	-2	–	2	µA
RSENSE input leakage current	I_{LRS}	Pull-down resistor is not connected	-2	–	2	µA

- **AC CHARACTERISTICS**

V_{DD}=7 to 80V, GND=0V, Ta=-40 to +85℃, VREG output no-loaded

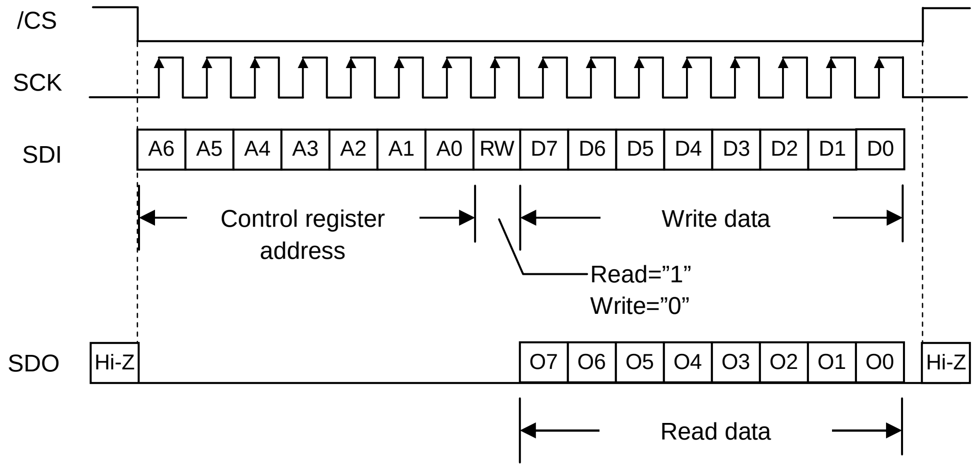
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
/CS-SCK setup time	t_{CSS}	–	100	–	–	ns
SCK-/CS hold time	t_{CSH}	–	100	–	–	ns
SCK "H" pulse width	t_{WH}	–	500	–	–	ns
SCK "L" pulse width	t_{WL}	–	500	–	–	ns
SCK-SDI setup time	t_{DIS}	–	50	–	–	ns
SCK-SDI hold time	t_{DIH}	–	50	–	–	ns
SCK-SDO output delay time	t_{DOD}	–	–	–	400	ns
/CS "H" pulse width	t_{CS}	–	500	–	–	ns



■ FUNCTIONAL DESCRIPTION

• MCU INTERFACE

SPI interface is built in the ML5238.
Setting and control is held by writing /reading control registers.



Set the RW bit "0" to write data, and set the RW bit "1" to read data.

• CONTROL REGISTER

Control register map is shown below.

Address	Register	R/W	Initial value	Register setting
00H	NOOP	R/W	00H	No function assigned
01H	VMON	R/W	00H	Battery cell voltage Measurement
02H	IMON	R/W	00H	Current measurement setting
03H	FET	R/W	00H	FET setting
04H	PSENSE	R/W	00H	PSENSE pin comparator setting
05H	RSENSE	R/W	00H	Short current detection setting RSENSE pin comparator setting
06H	POWER	R/W	00H	Power save, Power down control
07H	STATUS	R/W	00H	Internal Status
08H	CBALH	R/W	00H	Upper 8 cell balancing switch ON/OFF setting
09H	CBALL	R/W	00H	Lower 8 cell balancing switch ON/OFF setting
0AH	SETSC	R/W	00H	Short current detecting voltage setting
others	TEST	R/W	00H	TEST (Don't use)

1. NOOP register (Adrs = 00H)

	7	6	5	4	3	2	1	0
Bit name	NO7	NO6	NO5	NO4	NO3	NO2	NO1	NO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

No function is assigned to NOOP register, there is no status changes in the LSI even if this register is written or read. In the read operation written data is read

2. VMON register (Adrs = 01H)

	7	6	5	4	3	2	1	0
Bit name	–	–	–	OUT	CN3	CN2	CN1	CN0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

VMON register sets the battery cell outputted to the VMON pin.
Select the battery cell by CN0, CN1, CN2, CN3 bits, and OUT bit enable the output from VMON pin.

OUT	CN3	CN2	CN1	CN0	Battery cell selection
0	–	–	–	–	VMON pin = 0V (initial value)
1	0	0	0	0	V1 cell (lower most)
1	0	0	0	1	V2 cell
1	0	0	1	0	V3 cell
1	0	0	1	1	V4 cell
1	0	1	0	0	V5 cell
1	0	1	0	1	V6 cell
1	0	1	1	0	V7 cell
1	0	1	1	1	V8 cell
1	1	0	0	0	V9 cell
1	1	0	0	1	V10 cell
1	1	0	1	0	V11 cell
1	1	0	1	1	V12 cell
1	1	1	0	0	V13 cell
1	1	1	0	1	V14 cell
1	1	1	1	0	V15 cell
1	1	1	1	1	V16 cell (upper most)

3. IMON register (Adrs = 02H)

	7	6	5	4	3	2	1	0
Bit name	−	−	−	OUT	GCAL1	GCAL0	ZERO	GIM
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IMON register set the current measuring.
GIM bit set the voltage gain of current measuring amplifier.

GIM	Voltage gain G_{IM}
0	10 times (initial value)
1	50 times

ZERO bit set the zero-correction of current measuring amplifier.

ZERO	ISP input	ISM input
0	Pin input	Pin input
1	GND level	GND level

Voltage gain of current measuring amplifier is corrected by GCAL0, GCAL1 bits.
GCAL0 bit changes the ISP and ISM pin input to GND or internal reference voltage (20mV/100mV).
GCAL1 bit changes the IMON pin output to internal reference voltage output.

<table>
<tr><th>GCAL1</th><th>GCAL0</th><th colspan="2">ISP input</th><th>ISM input</th><th>IMON output</th></tr>
<tr><td>0</td><td>0</td><td colspan="2">Pin input</td><td>Pin input</td><td>Amplified output</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td>GIM=0</td><td>100mV</td><td>GND level</td><td>2V (typ)</td></tr>
<tr><td>GIM=1</td><td>20mV</td><td>GND level</td><td>2V (typ)</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">Pin input</td><td>Pin input</td><td>Amplified output</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">1</td><td>GIM=0</td><td>100mV</td><td>GND level</td><td>Reference voltage output 100mV (typ)</td></tr>
<tr><td>GIM=1</td><td>20mV</td><td>GND level</td><td>Reference voltage output 20mV (typ)</td></tr>
</table>

If the ZERO bit is set “1”, setting GCAL1 and GCAL0 bits are neglected.

OUT bit enables to output the current measuring amplifier from IMON pin. If zero correction and gain correction is held, OUT bit is set “1” too.

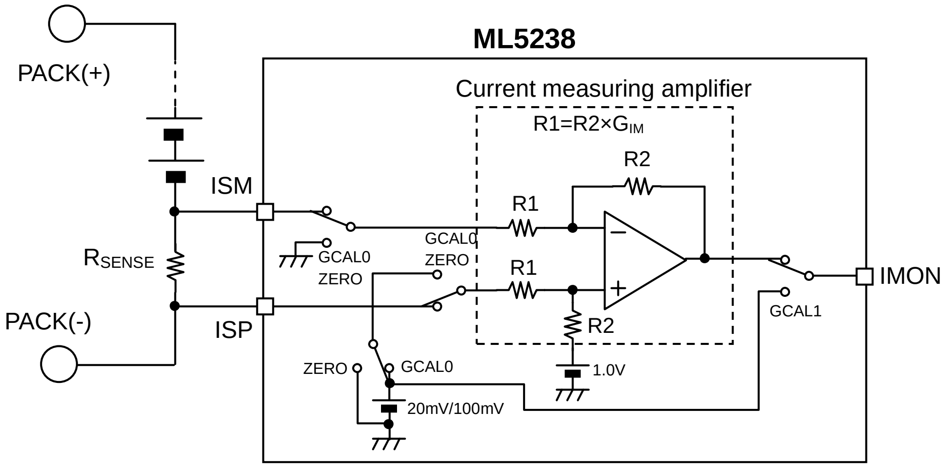
OUT	IMON pin output
0	0V (initial value)
1	Current measuring amplifier output

Current measurement is executed with current sensin resistor (R_{SENSE}) connected between ISP pin and ISM pin and by measuring input voltage difference between these pins.

Voltage difference between ISP and ISM is converted to voltage, its center is 1.0V (typ), and outputted from IMON pin. IMON pin output voltage V_{IMON} is given by the following equation with the current sensing resistor R_{SENSE} and its current I_{SENSE}.

$$V_{IMON} = (I_{SENSE} \times R_{SENSE}) \times G_{IM} + 1.0$$

The circuit of current measuring amplifier is shown below.



If the current is zero, V_{IMON} = 1.0V, in the discharging state, V_{IMON} > 1.0V, in the charging state, V_{IMON} < 1.0V.

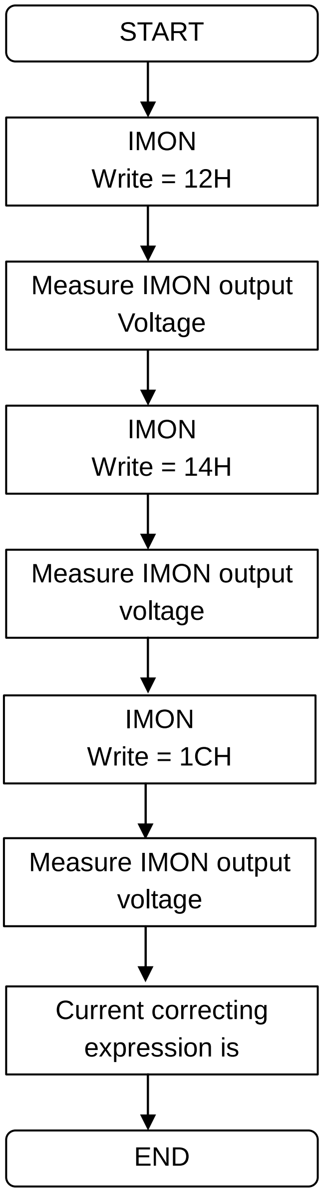
When the ZERO bit is set “1”, the input of ISM pin and ISM pin is switched to GND level in the LSI and set the input difference voltage of the current measuring amplifier to zero. The IMON pin output voltage in this state is set as the reference voltage of zero current, and internal 1.0V reference voltage and offset voltage of amplifier is corrected.

If the GCAL0 bit is set “1”; the ISM pin input is switched to GND level in the LSI; the ISP pin input is switched to 100mV (internal reference voltage) if the GIM bit is “0”, and else if GIM bit is “1” the ISP pin input is switched to 20mV (internal reference voltage). The gain error is corrected with the difference between the IMON output voltage at this state and it at current zero, and internal reference voltage.

Internal reference voltage is outputted from IMON pin by setting the GCAL1 bit “1”.

Short current detection characteristic is not depended on the IMON pin output setting.

The example flowchart of calibration for current measuring amplifier is shown below.
(Voltage gain is 10)



Write IMON register “12H” and set the current zero.

Measure the IMON pin output voltage when the current is zero with external ADC. Store its result in the variable VIM0.

Write IMON register “14H” and set the IMON output the amplified internal reference voltage.

Measure the IMON pin output voltage (amplified internal reference voltage) with external ADC. Store its result in the variable VIM1.

Write IMON register “1CH” and set the IMON output the internal reference voltage.

Measure the IMON pin output voltage (outputted internal reference voltage) with external ADC. Store its result in the variable VR.

Calculate the voltage gain and zero correcting value with VIM0, VIM1 and VR.

Voltage gain: G_{IM} = (VIM1-VIM0)/VR

Zero correcting value: V_{IMZ} = VIM0

Measured current I_{SENSE} is given with the following expression.

Current sensing resistor = R_{SENSE}

IMON voltage measured value = V_{IMON}

$I_{SENSE} = (V_{IMON} - V_{IMZ}) / G_{IM} / R_{SENSE}$

4. FET register (Adrs = 03H)

	7	6	5	4	3	2	1	0
Bit name	−	−	−	DRV	−	−	CF	DF
R/W	R	R	R	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FET register control the turn ON/OFF of the C_FET and D_FET pin, and read the state of its output.

DF bit sets the D_FET pin output state. If the short current is detected, the DF bit is automatically cleared to ”0”. Because the DF bit is not automatically set “1” even if the state is changed from short detection to normal state, external MCU must set this bit “1”.

DF	Discharge FET	D_FET pin output
0	OFF（initial value）	0V
1	ON	14V (typ)

CF bit set the C_FET pin output state. If the short current is detected, the CF bit is automatically cleared tot “0”. Because the CF bit is not automatically set “1” even if the state is changed from short detection to normal state, external MCU must set this bit “1”.

CF	Charge FET	C_FET pin output
0	OFF (initial value)	Hi-Z
1	ON	14V (typ)

DRV bit set the output current drive capacity of internal FET driver. If the DRV bit is set “1”, the rising time of D_FET, C_FET pins is short.
The duration to set the DRV bit “1” should be set depend on the capacitance load of the D_FET, C_FET pins. DRV bit should be cleared to “0”, after the D_FET, C_FET pin output level is fully risen to “H”.
If the DRV bit is left “1”, power consumption or the “H” output voltage of D_FET, C_FET might be higher than the level specified in the electrical characteristics.

DRV	FET driver output capacity
0	Normal (initial value)
1	enhanced

5. PSENSE register (Adrs = 04H)

	7	6	5	4	3	2	1	0
Bit name	EPSH	IPSH	RPSH	PSH	EPSL	IPSL	RPSL	PSL
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R
Initial value	0	0	0	0	0	0	0	0

PSENSE register set the parameters of comparators which detect charger connection/disconnection with PSENSE pin input.
Two comparators with difference threshold are connected to PSENSE pin to manage ON and OFF states of discharge FET.

For detecting charger disconnection in the state of discharge FET ON, low level threshold (0.2V (typ)) type comparator is selected, because PSENSE pin voltage is clamped by the body-diode of charge FET.
Low level threshold type comparator is selected mainly for detecting charger open in the state of charge over-current detected,

Parameters of the low level threshold type comparator for detecting the charger open is set in EPSL, IPSL, and RPSL bits. Comparator output is assigned to PSL bit.

EPSL bit set the run/stop of the comparator for detecting charger open. If EPSL bit is set running, 500kΩ pull-up resistor is connected to PSENSE pin in the LSI.

EPSL	State of comparator for detecting charger open	PSENSE pin status
0	Stop (initial value)	Hi-Z (initial value)
1	Run	500kΩ pull-up

IPSL bit enables asserting the interrupt from /INTO pin, if the output of comparator detecting charger open (PSL bit) is changed from “0” to “1”. IPSL bit should be set “1” more than 1 msec later from setting the EPSL bit “1”.

IPSL	Interrupt enable
0	Disable (initial value)
1	enable

RPSL bit indicates the interrupt assertion if the output of comparator detecting charger open (PSL bit) is changed from “0” to “1”. To clear this interrupt, write “0” in the RPSL bit. Writing “1” in the RPSL bit is neglected. If IPSL bit is “0”, RPSL bit is fixed to “0”.

RPSL	Interrupt occurred
0	No interrupt (initial value)
1	Interrupted

PSL bit indicates the state of charger connected. If the EPSL bit is “0”, PSL bit is fixed to “0”. Writing “1” in the PSL bit is neglected.

PSL	Charger connection	PSENSE pin voltage
0	Charger connected (initial value)	0.2V or less
1	Charger disconnected	Larger than 0.2V

For detecting charger disconnection in the state of discharge FET OFF, high level threshold (V_{DD}×0.75) type comparator is selected, because PSENSE pin voltage rise up to power supply voltage (V_{DD}).
High level threshold comparator is selected mainly for detecting charger open if the status changes to power down state.

Parameters of the high level threshold type comparator for detecting the charger open is set in EPSH, IPSH, and RPSH bits. Comparator output is assigned to PSH bit.

EPSH bit set the run/stop of the comparator for detecting charger open. If EPSH bit is set running, 500kΩ pull-up resistor is connected to PSENSE pin in the LSI.

EPSH	State of comparator for detecting charger open	PSENSE pin status
0	Stop（initial value）	Hi-Z (initial value)
1	Running	500kΩ pull-up

IPSH bit enables asserting the interrupt from /INTO pin, if the output of comparator detecting charger open (PSH bit) is changed from “0” to “1”. IPSH bit should be set “1” more than 1 msec later from setting the EPSH bit “1”.

IPSH	Interrupt enable
0	Disable (initial value)
1	enabled

RPSH bit indicates the interrupt assertion if the output of comparator detecting charger open (PSH bit) is changed from “0” to “1”. To clear this interrupt, write “0” in the RPSH bit. Writing “1” in the RPSH bit is neglected. If IPSH bit is “0”, RPSH bit is fixed to “0”.

RPSH	Interrupt occurred
0	No interrupt (initial value)
1	interrupted

PSH bit indicates the state of charger connected. If the EPSH bit is “0”, PSH bit is fixed to “0”. Writing “1” in the PSH bit is neglected.

PSH	Charger connection	PSENSE pin voltage
0	Charger connected (initial value)	V_{DD}×0.75 or less
1	Charger disconnected	Larger than V_{DD}×0.75

6. RSENSE register (Adrs = 05H)

	7	6	5	4	3	2	1	0
Bit name	ESC	ISC	RSC	SC	ERS	IRS	RRS	RS
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R
Initial value	0	0	0	0	0	0	0	0

RSENSE register set the parameters of detecting short current and the parameters of comparator which detect load connection/disconnection with RSENSE pin input.

ESC bit set the run/stop of the circuit detecting short current.

ESC	Status of the circuit detecting short current
0	Stop (initial value)
1	Run

ISC bit enables asserting the interrupt from /INTO pin, if the short current is detected.

ISC	Interrupt enable
0	Disable (initial value)
1	enable

RSC bit indicates the interrupt assertion if the short current is detected. To clear the interrupt, write "0" in the RSC bit. Writing "1" in the RSC bit is neglected. If ISC bit is "0", RSC bit is fiexed to "0".

RSC	Interrupt occurred
0	No interrupt (initial value)
1	interrupted

SC bit indicates the output from the comparator detecting short current.
If the SC bit is changed from "0" to "1", charging the capacitor connected to CDLY pin is started. If this charging is finished, the RSC bit is automatically changed to "1" and the DF bit and the CF bit in the FET register is automatically cleared to "0". If the short current status is cleared before charging the capacitor connected to CDLY pin is finished, charging the CDLY pin is stopped and the CDLY pin is fixed to GND level.
If the ESC bit is "0", SC bit is fixed to "0". Writing "1" in the SC bit is neglected.

SC	Status of the comparator output detecting short current	ISP-ISM voltage
0	Short current is not detected (initial value)	Short current detecting voltage or lower
1	Short current is detected	Higher than short current detecting voltage

Short current detecting delay time is set with the charging time of capacitor C_{DLY} which is connected to CDLY pin ; calculated with following formula.

Short current detecting delay time t_{sc} [μs] $= C_{DLY}$[nF] ×100

ERS bit set the run/stop of the comparator for detecting load open. If ERS bit is set running, 2MΩ pull-down resistor is connected to RSENSE pin in the LSI.

ERS	State of comparator for detecting load open	RSENSE pin status
0	Stop (initial value)	Hi-Z (initial value)
1	Running	2MΩ pull-down

IRS bit enables asserting the interrupt from /INTO pin, if the output of comparator detecting load open (RS bit) is changed from “0” to “1”. IRS bit should be set “1” more than 1 msec later from setting the ERP bit “1”.

IRS	Interrupt enable
0	Disable (initial value)
1	enabled

RRS bit indicates the interrupt assertion if he output of comparator detecting load open(RS bit) is changed from “0” to “1”. To clear this interrupt, write “0” in the RRS bit. Writing “1” in the RRS bit is neglected. If IRS bit is “0”, RRS bit is fixed to “0”.

RRS	Interrupt occurred
0	No interrupt (initial value)
1	interrupted

RS bit indicates the state of load connected. If the ERS bit is “0”, RS bit is fixed to “0”. Writing “1” in the RS bit is neglected.

RS	Load connection	RSENSE pin voltage
0	Load connected (initial value)	2.4V or higher
1	Load disconnected	Lower than 2.4V

7. POWER register (Adrs = 06H)

	7	6	5	4	3	2	1	0
Bit name	PUPIN	–	–	PDWN	–	–	–	PSV
R/W	R	R	R	R/W	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

Power register control the power save and the power down.

PSV bit set the state transition to power save.

PSV	Power save
0	Normal state (initial value)
1	Power save state

In the power save state, circuits for VREG output and VREF output is operating, cell voltage measuring and current measuring is stopped, and the power consumption is reduced. FET driving and short detecting circuit works in the power save state. Comparators in the PSENSE pin and the RSENSE pin are stopped.

Clearing the PSV bit to “0” and the status is recovered from power save state to normal state.

To set the comparators in the PSENSE pin and the RSENSE pin running, set these comparators to run after recovering from the power save state.

PDWN bit set the state transition to power down

PDWN	Power down
0	Normal state (initial value)
1	Power down state

If the PDWN bit is set “1”, 500kΩ pull-up resistor is automatically connected to PSENSE pin in the LSI and all the circuit is stopped, and the /RES pin output is “L”.

Before setting the PDWN bit “1”, C_FET and D_FET should be set OFF and charger disconnection should be confirmed with the PSENSE register. When the /PUPIN pin input is “L”, even if PDOWN bit is set to “1”, the state doesn’t get changed to power-down until the /PUPIN pin input rises to “H”. Before setting the PDWN bit “1”, it should be confirmed that /PUPIN pin is not “L” by reading the PUPIN bit.

PUPIN	/PUPIN pin state
0	“H” level
1	“L” level

If charger connection is detected with PSENSE pin or if /PUPIN pin is asserter “L” input, the LSI is recovered from power down state to normal state.

In the power down state, VREG output which is power supply for external micro-computer is set GND level. In recovering from power down state, every initial setting should be held after VREG is fully risen and after /RES pin output is fully changed from “L” level to “H” level.

8. STATUS register (Adrs = 07H)

	7	6	5	4	3	2	1	0
Bit name	RSC	RRS	RPSH	RPSL	INT	PSV	CF	DF
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

STATUS register indicates each status.

DF bit indicates the D_FET pin output status.

DF	D_FET pin status
0	OFF (initial value)
1	ON

CF bit indicates the C_FET pin output status.

CF	C_FET pin status
0	OFF (initial value)
1	ON

PSVbit indicates the power save state.

PSV	Power save state
0	Normal state (initial value)
1	Power save state

INT bit indicates the /INTO pin output status.

INT	/INTO pin output status
0	No interrupt (initial value)
1	Interrupted

RPSL bit indicates interrupt status of charger disconnecting interrupt if charge over-current detected.

RPSL	Status of charger disconnecting interrupt if charge over-current detected.
0	No interrupt (initial value)
1	Charger disconnecting interrupt

RPSH bit indicates interrupt status of charger disconnecting interrupt if the status is power down.

RPSH	Status of charger disconnecting interrupt if the status is power down
0	No interrupt (initial value)
1	Charger disconnecting interrupt

RRS bit indicates interrupt status of load disconnecting interrupt

RRS	Status of load disconnecting interrupt
0	No interrupt (initial value)
1	Load disconnecting interrupt

RSC bit indicates interrupt status of short current detecting interrupt.

RSC	Status of short current detecting interrupt
0	No interrupt (initial value)
1	Short current detecting interrupt.

9. CBALH register (Adrs = 08H)

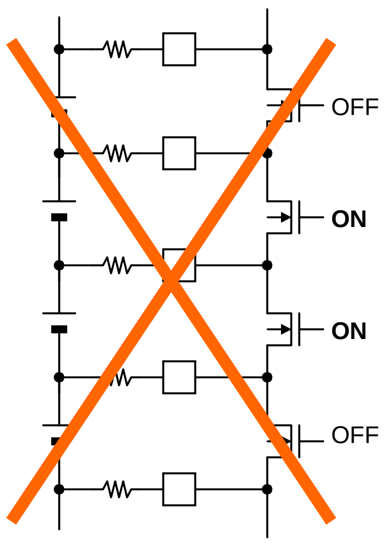
	7	6	5	4	3	2	1	0
Bit name	SW16	SW15	SW14	SW13	SW12	SW11	SW10	SW9
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

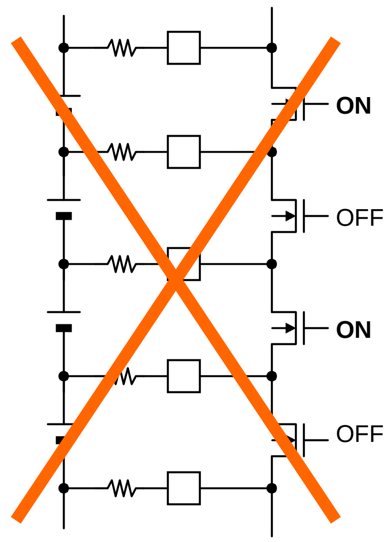
CBALH register set the cell balancing switches turning ON/OFF of upper 8 cells.
SW16~SW9 bit sets switches turning ON/OFF of each cell.

SW16	SW15	SW14	SW13	SW12	SW11	SW10	SW9	Switch ON/OFF
0	0	0	0	0	0	0	0	Upper 8 cells OFF (initial value)
0	0	0	0	0	0	0	1	V9-V8 pin switch ON
0	0	0	0	0	0	1	0	V10-V9 pin switch ON
0	0	0	0	0	1	0	0	V11-V10 pin switch ON
0	0	0	0	1	0	0	0	V12-V11 pin switch ON
0	0	0	1	0	0	0	0	V13-V12 pin switch ON
0	0	1	0	0	0	0	0	V14-V13 pin switch ON
0	1	0	0	0	0	0	0	V15-V14 pin switch ON
1	0	0	0	0	0	0	0	V16-V15 pin switch ON

More than one switch can be turned on in the same time, but following settings are inhibited because internal cell balancing switch might be broken.

(1) Side-by-side cell balancing switches are inhibited to be turned on in the same time.
(2) the cell balancing switches of both side of a cell balancing switch which is turned off is inhibited to be turned on in the same time.





IC heats by cell balancing current and cell balancing switch resistor, restrict the number of switches of ON and time of ON, in order to keep the power consumption of cell balancing switch less than allowable power dissipation,

If cell voltage is outputted from VMON pin, the voltage of a cell whose cell balancing switch is turned on is measured as the voltage difference between two ports of cell balancing switch.

10. CBALL register (Adrs = 09H)

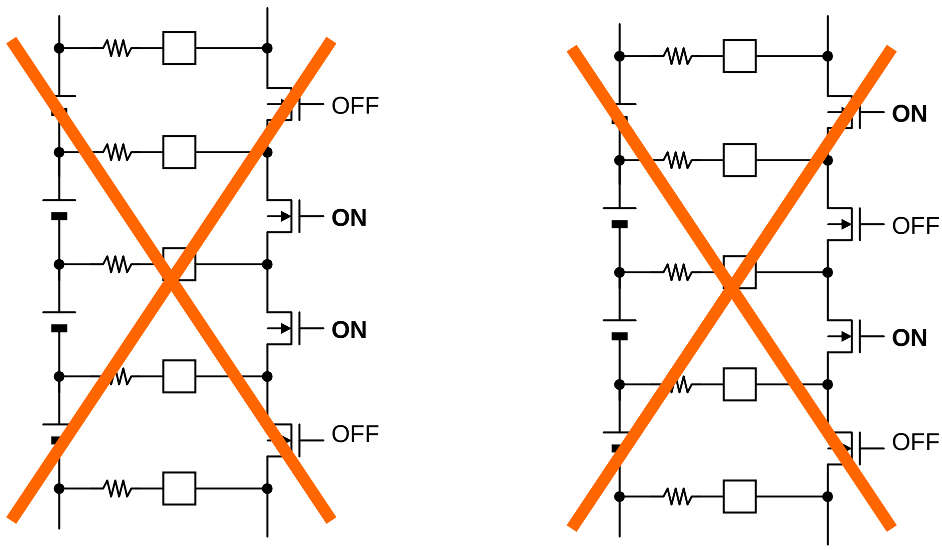
	7	6	5	4	3	2	1	0
Bit name	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CBALL register set the cell balancing switches turning ON/OFF of lower 8 cells.
SW8~SW1 bit sets switches turning ON/OFF of each cell.

SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	Switch ON/OFF
0	0	0	0	0	0	0	0	lower 8 cells OFF (initial value)
0	0	0	0	0	0	0	1	V1-V0 pin switch ON
0	0	0	0	0	0	1	0	V2-V1 pin switch ON
0	0	0	0	0	1	0	0	V3-V2 pin switch ON
0	0	0	0	1	0	0	0	V4-V3 pin switch ON
0	0	0	1	0	0	0	0	V5-V4 pin switch ON
0	0	1	0	0	0	0	0	V6-V5 pin switch ON
0	1	0	0	0	0	0	0	V7-V6 pin switch ON
1	0	0	0	0	0	0	0	V8-V7 pin switch ON

More than one switch can be turned on in the same time, but following settings are inhibited because internal cell balancing switch might be broken.

(1) Side-by-side cell balancing switches are inhibited to be turned on in the same time.
(2) the cell balancing switches of both side of a cell balancing switch which is turned off is inhibited to be turned on in the same time.



IC heats by cell balancing current and cell balancing switch resistor, restrict the number of switches of ON and time of ON, in order to keep the power consumption of cell balancing switch less than allowable power dissipation,

If cell voltage is outputted from VMON pin, the voltage of a cell whose cell balancing switch is turned on is measured as the voltage difference between two ports of cell balancing switch.

11. SETSC register (Adrs = 0AH)

	7	6	5	4	3	2	1	0
Bit name	–	–	–	–	–	–	SC1	SC0
R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SETSC register sets the short current detecting voltage.
Short current detecting voltage is selected with SC0 and SC1 bit depend on current sensing resistor value.

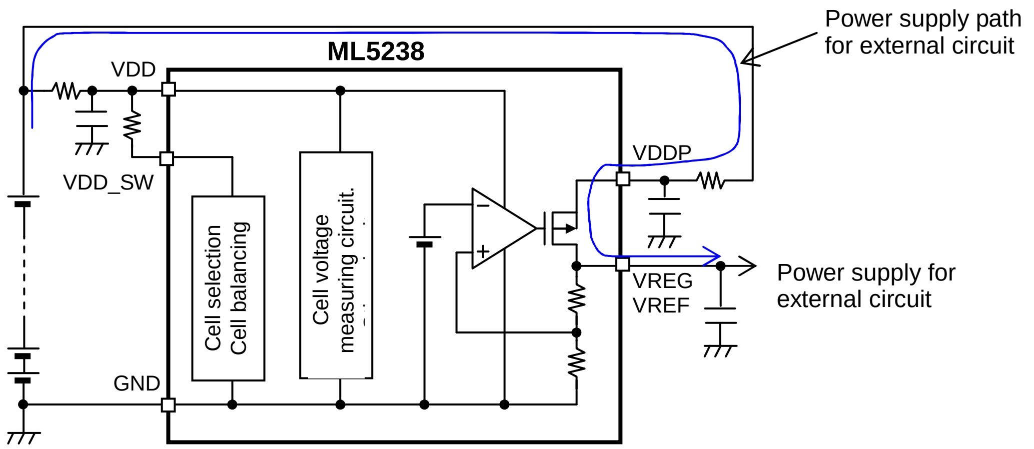
SC1	SC0	Short current detecting voltage	Short current detecting current if Current sensing resistor value = 3mΩ
0	0	0.1V (initial value)	33.3A
0	1	0.2V	66.6A
1	0	0.3V	100A
1	1	0.4V	133.3A

- **CONNECTING POWER SUPPLY (VDDP, VDD, VDD_SW)**

VDDP pin is the power supply pin only for internal 3.3V regulator (VREG pin, VREF pin). If the output current of 3.3V regulator is large, it is recommended to make the voltage drop of RC filter resistor (for removing noise at the VDDP pin) smaller than 1V.

VDD_SW pin is the power supply pin only for cell selection switches and cell balancing switches. Connect this pin to VDD via 51Ω resistor.

VDD pin is the power supply pin for all the circuit other than internal 3.3V regulator and cell selection switches and cell balancing switches.



- **POWER-ON / POWER-OFF SEQUENCE**

Recommended connecting order is; connect the GND first, after that connect the VDD, VDDP, VDD_SW, and after that connect each cells from lower level. Power supply voltage rising time of power-on, power off order, power supply voltage falling time of power-off is not defined.

Following the power-on, the ML5238 normally enter into normal state. ML5238 may rarely enter into the Power down state by the chattering or another reason during the connection of the battery cells. In this case, input the voltage lower than or equal to the Detecting charger connection PSENSE pin voltage (V_{PC}) to PSENSE pins, or input the "L" level to the /PUPIN pin, in order to power-up.

Else after the power-on or after the power-up, cell voltage measurement and current measurement should be done after the internal analog circuit is settled. To get the settling time of analog circuit, confirm the output settling time of VREF pin, VMON pin, and IMON pin in the application system.

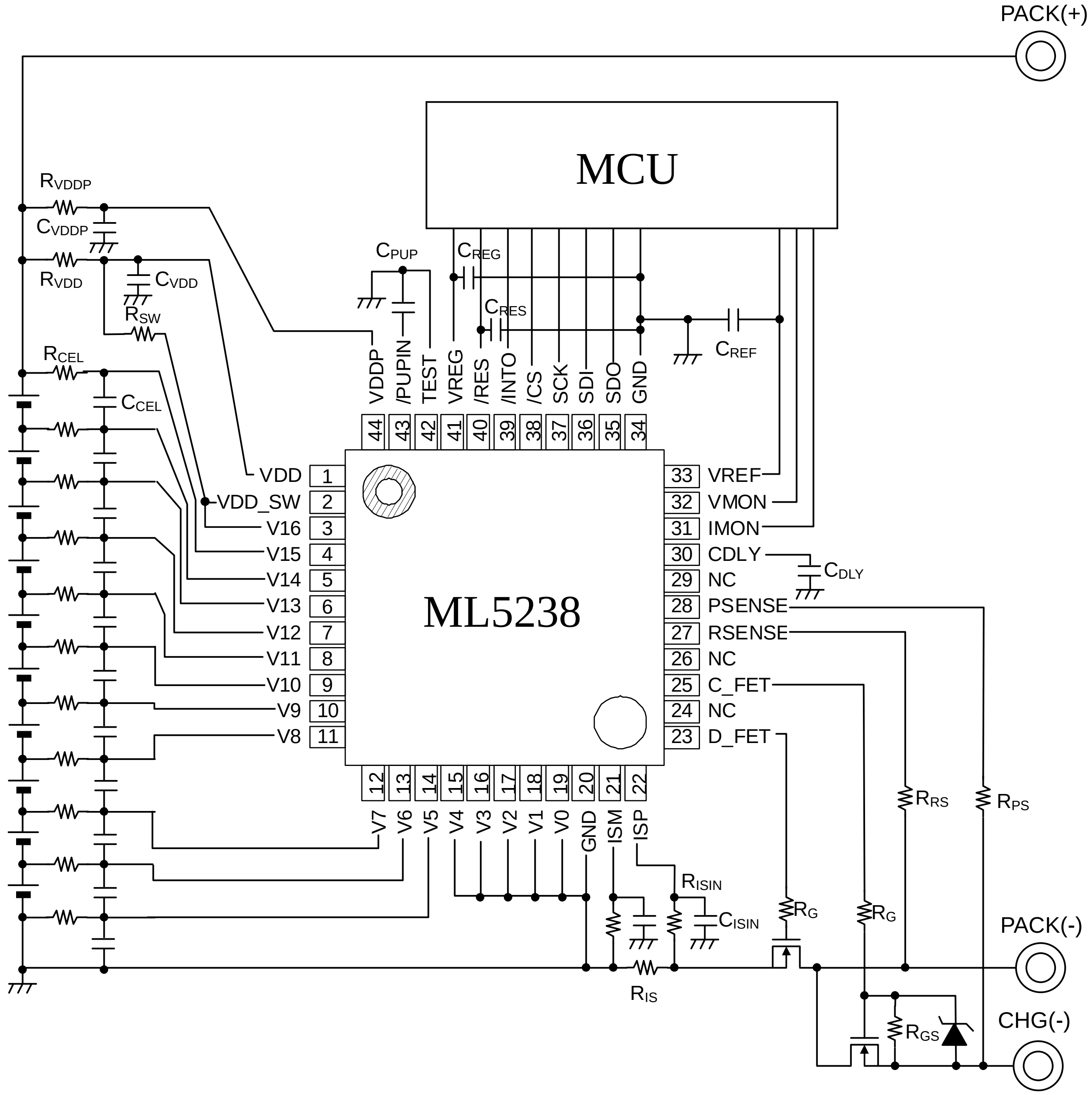
- **CELL CONNECTING**

If the number of connected cells is less than 16, connecting order in following table is recommended.

Number of Connected cells	V16	V15 to V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0
15	VDD_SW	cell	cell	cell	cell	cell	cell	cell	cell	cell	cell	cell
14	VDD_SW	cell	cell	cell	cell	cell	cell	cell	cell	cell	cell	GND
13	VDD_SW	cell	cell	cell	cell	cell	cell	cell	cell	cell	GND	GND
12	VDD_SW	cell	cell	cell	cell	cell	cell	cell	cell	GND	GND	GND
11	VDD_SW	cell	cell	cell	cell	cell	cell	cell	GND	GND	GND	GND
10	VDD_SW	cell	cell	cell	cell	cell	cell	GND	GND	GND	GND	GND
9	VDD_SW	cell	cell	cell	cell	cell	GND	GND	GND	GND	GND	GND
8	VDD_SW	cell	cell	cell	cell	GND	GND	GND	GND	GND	GND	GND
7	VDD_SW	cell	cell	cell	GND	GND	GND	GND	GND	GND	GND	GND
6	VDD_SW	cell	cell	GND	GND	GND	GND	GND	GND	GND	GND	GND
5	VDD_SW	cell	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

■ EXAMPLE OF APPLICATION CIRCUIT

(10 cells, charge/discharge path is isolated)



■ PARTS LIST

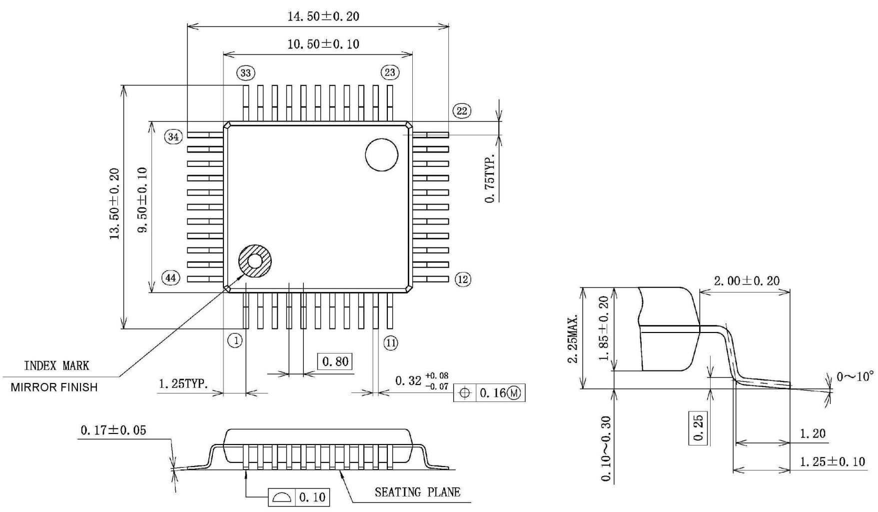
Symbol	Value
R_{VDD}	510Ω
C_{VDD}	10µF or more
R_{VDDP}	100Ω
C_{VDDP}	10µF or more
R_{SW}	51Ω
R_{CEL}	18Ω or more
C_{CEL}	0.1µF or more
R_{IS}	3mΩ

Symbol	Value
R_{ISIN}	1kΩ
C_{ISIN}, C_{RES}	0.1µF
C_{REG}, C_{REF}	4.7µF
C_{DLY}	1nF to 10nF
C_{PUP}	1µF
R_G	10kΩ
R_{GS}	1MΩ
R_{RS}	10kΩ
R_{PS}	1kΩ

■ PACKAGE DIMENSIONS

(Unit: mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.41 TYP.
Rev. No./Last Revised	2/Nov. 12, 2008

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

■ REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL5238-01	2012.05.18	–	–	First Edition
PEDL5238-02	2012.07.23	1	1	Note is added
		19	19	POWER register; PUPIN bit is added
		25	25	R_{PS} is revised to 1kΩ. Higher side PACK(-) is revised to PACK(+)
PEDL5238-03	2012.11.29	1	1	“switch ON resistance = 6 Ω (typ)” is deleted.
		6	6	$V_{REF1/2}$ 3.3 → 3.30 V
		7	7	“(note) The load current is …VREG connector.” Is added.
				“(note) Short detecting delay time tSC [μs]=CDLY[nF] x 100” is added.
		14	14	CF → CCF, DF → CDF
PEDL5238-04	2013.02.01	3	3	Cell connecting order modified Add D_FET, C_FET comment.
		6	6	Add VREG output voltage: no-loaded state condition VREF output voltage @Ta=-10 to 60°C modified.
		7	8	Detecting voltage characteristic (Ta=^10 to 60°C) is added.
		8	9	Load disconnection, charger connection / disconnection detecting voltage characteristics (Ta=-10 to 60°C) is added.
		14	16	CCF→CF, CDF→CF
		14	16	FET register: D_FET, C_FET pin output state is added.
		17	19	RSENSE register: ISC bit mistyping is corrected.
		21,22	23,24	CBALH,CBALL register: because of cell balancing current, allowable power dissipation exceeds its limit.
		-	26	Cell connection reference added.
		25	27	Application diagram: cell connection is modified.
PEDL5238-05	2013.03.04	1	1	Reference voltage regulator for external ADC: 25℃ is deleted
		6	6	VREF output voltage: V_{REF1} =3.27V(min), 3.33V(max) →3.28V(min), 3.34V(max)
PEDL5238-06	2013.03.19	26	26	GND pin is connected first.
PEDL5238-07	2013.04.03	6	6	Cell monitoring pin Input current: -0.5μA → 5μA(min) Cell monitoring pin Input leak current: -0.5μA (add) FET “H” output voltage : V_{DD}=18V to 50V →18V to 72V VREG output voltage, Output No-loaded : 3.5V → 3.6V(max)

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