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Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

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LAPIS Technology Co., Ltd.
October 1, 2020

ML62Q1500/1800 Group

16-bit micro controller

GENERAL DESCRIPTION

ML62Q1500/1800 Group is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with program memory(Flash memory), data memory(RAM), data Flash and rich peripheral functions such as the multiplier/divider, CRC generator, DMA controller, Clock generator, Simplified RTC, Timer, General Purpose Ports, UART, Synchronous serial port, I²C bus interface unit (Master, Slave), Buzzer, Voltage Level Supervisor(VLS), Successive approximation type A/D converter, D/A converter, Analog comparator, Safety function(IEC60730/60335 Class B) and so on. The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipeline architecture parallel processing.

The built-in on-chip debug function enables debugging and programming the software. Also, ISP(In-System Programming) function supports the Flash programming in production line.

The ML62Q1500/1800 Group has seven packages (48pin - 100pin) and ten kinds of memory sizes(32Kbyte - 512Kbyte).

Table 1 ML62Q1500/1800 Group Product List

| Program memory | Data memory (RAM) | Data Flash | 48pin TQFP48 | 52pin TQFP52 | 64pin QFP64 TQFP64 | 80pin QFP80 | 100pin QFP100 TQFP100 |
|----------------|-------------------|------------|--------------|--------------|--------------------|-------------|-----------------------|
| 512Kbyte | 32Kbyte | 8Kbyte | — | — | ML62Q1859 | ML62Q1869 | ML62Q1879 |
| 384Kbyte | | | — | — | ML62Q1858 | ML62Q1868 | ML62Q1878 |
| 256Kbyte | 16Kbyte | 4Kbyte | — | — | ML62Q1557 | ML62Q1567 | ML62Q1577 |
| 192Kbyte | | | — | — | ML62Q1556 | ML62Q1566 | ML62Q1576 |
| 160Kbyte | | | — | — | ML62Q1555 | ML62Q1565 | ML62Q1575 |
| 128Kbyte | 16Kbyte | | — | — | — | ML62Q1564 | ML62Q1574 |
| | 8Kbyte | | ML62Q1534 | ML62Q1544 | ML62Q1554 | — | — |
| 96Kbyte | 16Kbyte | | — | — | — | ML62Q1563 | ML62Q1573 |
| | 8Kbyte | | ML62Q1533 | ML62Q1543 | ML62Q1553 | — | — |
| 64Kbyte | 8Kbyte | | ML62Q1532 | ML62Q1542 | ML62Q1552 | — | — |
| 48Kbyte | | | ML62Q1531 | ML62Q1541 | ML62Q1551 | — | — |
| 32Kbyte | | | ML62Q1530 | ML62Q1540 | ML62Q1550 | — | — |
| | | — | — | — | — | — | |

FEATURES

- CPU
 - 16-bit RISC CPU: nX-U16/100(A35 core)
 - Instruction system: 16-bit length instructions
 - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - Built-in On-chip debug function
 - Built-in ISP (In-System Programming) function
 - Minimum instruction execution time
Approximately 30.5 μs (at 32.768 kHz system clock)
Approximately 62.5ns/41.6ns (at 16 MHz/24MHz system clock)

- Coprocessor for multiplication and division
 - Multiplication : 16bit × 16bit (operation time : 4 cycles)
 - Division : 32bit ÷ 16bit (operation time : 8 cycles)
 - Division : 32bit ÷ 32bit (operation time : 16 cycles)
 - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time : 4 cycles)
 - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time : 4 cycles)
 - Signed or Unsigned is selectable
- Operating voltage and temperature
 - Operating voltage: $V_{DD} = 1.6$ to 5.5 V (V_{DD} should be 1.8V or over at Power-on)
 - Operating temperature: -40 °C to $+105$ °C
- Internal memory
 - Program memory area
 - Rewrite count: 100 cycles
 - Write unit: 32bit(4byte)
 - Erase unit: 16Kbyte/1Kbyte
 - Erase/Write temperature: 0 °C to $+40$ °C
 - Data Flash memory area
 - Rewrite count 10,000 cycles
 - Write unit: 8bit(1byte)
 - Erase unit: all area/128byte
 - Erase/Write temperature: -40 °C to $+85$ °C
 - Back Ground Operation(CPU can work while erasing and rewriting)

This product uses Super Flash® technology licensed from Silicon Storage Technology, Inc.
Super Flash® is a registered trademark of Silicon Storage Technology, Inc.
 - Data RAM area
 - Rewrite unit: 8bit/16bit (1byte/2byte)
 - Parity check function is available (interrupt / reset are generatable at Parity error)
- Clock Generation Circuit
 - Low-speed clock (LSCLK)
 - Internal low-speed RC oscillation: Approximately 32.768 kHz
 - External low-speed clock input: Approximately 32.768 kHz
 - External low-speed crystal oscillation: 32.768 kHz crystal resonator is connectable
 - 3 selectable crystal oscillation mode (Tough, Normal, and Low current consumption)
 - Tough mode: Largest oscillation allowance to make highest resistance against leakage between the pins
 - Normal mode: Normal oscillation allowance and current consumption
 - Low current consumption mode: Smallest oscillation allowance to make lower current consumption
 - High-speed clock (HSCLK)
 - PLL oscillation: 2 selectable oscillation frequency (24MHz and 16MHz) by code option
 - Watch Dog Timer (WDT): built-in independent clock for WDT (RC1K: Approximately 1kHz)
- Reset
 - Reset by reset input pin
 - Reset by Power-On Reset
 - Reset by WDT overflow
 - Reset by WDT invalid clear
 - Reset by RAM parity error
 - Reset by unused ROM area access (instruction access)
 - Reset by voltage level supervisor (VLS)
 - Software reset by BRK instruction (reset CPU only)
 - Reset the peripherals individually
 - Collective reset to the all control pins and peripheral circuits

- Power management
 - HALT mode: CPU stops executing instruction, peripheral circuits continue working
 - HALT-H mode: CPU stops executing instruction, high-speed clock oscillation stops and peripheral circuits continue working with low-speed clock
 - STOP mode: CPU and peripheral circuits stops executing instruction, both high-speed oscillation and low-speed oscillation stop.
 - STOP-D mode: CPU and peripheral circuits stops executing instruction, both high-speed oscillation and low-speed oscillation stop. The internal logic voltage (V_{DDL}) goes down to reduce the current consumption (RAM data is retained).
 - Clock gear: High-speed system clock frequency can be changed (1/1, 1/2, 1/4, 1/8, 1/16 or 1/32 of HSCLK)
 - Block Control Function: Powers down the unused function blocks (reset the block or stop supplying the clock)
- Interrupt controller
 - External interrupt ports : max 12
 - Non-maskable interrupt source: 1 (Internal source: WDT)
 - Maskable interrupt sources: max.51
 - Four step interrupt levels
- Watchdog timer(WDT)
 - Selectable Operating clock : select RC1K or LSCLK by code option
 - Overflow period: 8selectable (7.8ms, 15.6ms, 31.3ms, 62.5ms, 125ms, 500ms, 2s and 8s)
 - Selectable window function (enable or disable): configurable clear enable period (50% or 75% of overflow period)
 - Selectable WDT operation : select Enable or Disable by code option
 - Readable WDT counter : WDT counter monitor function
- DMA(Direct Memory Access) controller
 - Channel: 2channel
 - Transfer unit: 8bit/16bit
 - Transfer count: 1 to 1024
 - Transfer cycle: 2 cycle transfer
 - Transfer address: Fixed addressing mode, increment addressing mode , and decrement addressing mode
 - Transfer target: Special Function Register (SFR)/RAM → SFR/RAM (Transfer from/to Flash is not supported)
 - Transfer request: External pins, Serial communication unit, Successive approximation type A/D converter, 16bit timer, and Functional timer
- Low-speed Time base counter
 - Generate 8 frequency (128Hz to 1Hz) internal pulse signals by dividing the Low-speed clock (LSCLK)
 - Selectable 3 interrupts from eight frequency internal pulse signals
 - 1Hz or 2Hz output from general purpose port
 - Built-in Frequency adjust function : Adjust range: Approximately -488ppm to +488ppm, adjust resolution: Approximately 0.119ppm
- Simplified RTC
 - Channel: 1channel
 - Count by a unit for one second from "00 min. 00 sec" to "59 min. 59 sec"
 - Selectable Periodical interrupt request from four periods (0.5s, 1s, 30s or 60s)
 - Built-in minute and second writing error protraction function

- Functional timer
 - Channel: Max. 8 channel
 - Built-in timer, capture, and PWM function by 16 bit counter
 - Built-in Repeat mode, One shot mode is available
 - Two types of PWM output with the same period and different duties, and complementary PWM output with the dead time
 - Monitor input signal duty and the period by capture function
 - Generate periodical interrupts, duty interrupts, and interrupts coincided with set value
 - Counter Start, Stop, Counter clear triggered by an external inputs or Timer
 - Generate Emergency stop and emergency stop interrupt triggered by an external input
 - Same start/stop among different channels of the functional timer
 - Selectable counter clock(external clock or divided by 1 to 128 of LSCLK or HSCLK) for each channels

- 16-bit General timers
 - Channel: Max. 8channel
 - 8 bits timer mode and 16-bit timer mode
 - Same start/stop among different channels of 16bit (8bit) timer
 - Timer output (toggled by overflow)
 - Selectable counter clock (external clock or divided by 1 to 128 of LSCLK or HSCLK) for each channels

- Serial communication unit
 - Synchronous Serial Port (SSIO) mode or UART mode is selectable
 - Channel: Max. 6channel
 - < Synchronous Serial Port mode>
 - Selectable from Master and Slave
 - Selectable from LSB first or MSB first
 - Selectable 8-bit length or 16-bit length
 - < UART mode>
 - Full-duplex communication mode and half-duplex communication mode
 - 5 to 8 bit length, parity or no parity, odd parity or even parity, 1 stop bit or 2 stop bits
 - Selectable from Positive logic or Negative logic
 - Selectable from LSB first or MSB first
 - Configurable wide range communication speed
 - 32.768kHz operation clock : 1 bit/s to 4,800 bit/s
 - 24MHz operation clock : 600 bit/s to 3 Mbit/s
 - 16MHz operation clock : 300 bit/s to 2 Mbit/s
 - Built-in baud rate generator

- I²C bus unit (Master / Slave)
 - Selectable from Master mode or Slave mode
 - Channel: 1 channel
 - < Master function >
 - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
 - Handshake (Clock synchronization)
 - 7bit address format (10bit address format is supported)
 - < Slave function >
 - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
 - Clock stretch function
 - 7bit address format

- I²C bus Master
 - Channel: 2channel
 - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
 - Handshake (Clock synchronization)
 - 7bit address format (10bit address format is supported)

- General-purpose ports (GPIO)
 - I/O port: Max. 92 (Including one pin for on-chip debug and pins for other shared functions)
 - Input port: Max. 2(Including a shared function)
 - External interrupt port: Max. 12
 - LED driver port : Max. 91
 - Carrier frequency output function (used for IR communication)
- Successive approximation type A/D converter (SA-ADC)
 - Channel: Max.16channel
 - Resolution: 10bit
 - Conversion time: Min. 2.25 μ s /channel (When the conversion clock speed is 8MHz)
 - Reference voltages are selectable
(V_{DD} pin / Internal reference voltage(V_{REFI} = Approximately 1.55V) / External reference voltage (V_{REF} pin))
 - Selected channel repeat conversion
 - Dedicated result register for each channel
 - Interrupt determining by upper limit or lower limit threshold of conversion result
- Voltage Level Supervisor (VLS)
 - Accuracy: $\pm 4\%$
 - Threshold voltage: 12 selectable (from 1.85V to 4.00V)
 - Functional Voltage level detection reset (VLS reset)
 - Functional Voltage level detection interrupt (VLS0 interrupt)
- Analog comparator
 - Channel: Max. 2 channel
 - Selectable interrupt from the comparator output (rising edge or falling edge)
 - Selectable from sampling or without sampling
 - Comparable with external 2 inputs
 - Comparable with external input and internal reference voltage (0.8V)
- D/A converter
 - Channel: Max. 2 channel
 - Resolution: 8bit
 - Output impedance: 6k ohm (Typ.)
 - R-2R ladder type
- Buzzer
 - 4 buzzer mode (Continuous sound, Single sound, Intermittent sound 1 and Intermittent sound 2)
 - 8frequencies (4.096kHz to 293Hz)
 - 15 step duty (1/16 to 15/16)
 - Selectable from positive logic buzzer output or negative logic buzzer output
- CRC(Cyclic Redundancy Check) generator
 - Generation equation: $X^{16}+X^{12}+X^5+1$
 - Selectable from LSB first or MSB first
 - Built-in Automatic program memory CRC calculation mode in HALT mode

- Safety Function (IEC60730/60335 Class B)
 - Automatic switching to the internal low-speed RC oscillation in case the low-speed crystal oscillation stopped
 - RAM/SFR guard
 - Automatic program memory CRC calculation
 - RAM parity error detection
 - ROM unused area access reset (instruction access)
 - Clock mutual monitoring
 - WDT counter monitoring
 - SA-ADC test
 - UART test
 - Synchronous serial I/O test
 - I²C bus test
 - GPIO test

- Shipping package
 - 48 pin plastic TQFP
ML62Q1530/1531/1532/1533/1534 - xxxTB
(Blank part: ML62Q1530/1531/1532/1533/1534-NNNTB)
 - 52 pin plastic TQFP
ML62Q1540/1541/1542/1543/1544 - xxxTB
(Blank part: ML62Q1540/1541/1542/1543/1544-NNNTB)
 - 64 pin plastic TQFP
ML62Q1550/1551/1552/1553/1554/1555/1556/1557/1858/1859 - xxxTB
(Blank part: ML62Q1550/1551/1552/1553/1554/1555/1556/1557/1858/1859-NNNTB)
 - 64 pin plastic QFP
ML62Q1550/1551/1552/1553/1554/1555/1556/1557/1858/1859 - xxxGA
(Blank part: ML62Q1550/1551/1552/1553/1554/1555/1556/1557/1858/1859-NNNGA)
 - 80 pin plastic QFP
ML62Q1563/1564/1565/1566/1567 /1868/1869- xxxGA
(Blank part: ML62Q1563/1564/1565/1566/1567/1868/1869-NNNGA)
 - 100 pin plastic TQFP
ML62Q1573/1574/1575/1576/1577/1878/1879 - xxxTB
(Blank part: ML62Q1573/1574/1575/1576/1577/1878/1879-NNNTB)
 - 100 pin plastic QFP
ML62Q1573/1574/1575/1576/1577/1878/1879 - xxxGA
(Blank part: ML62Q1573/1574/1575/1576/1577/1878/1879-NNNGA)

xxx: ROM code number

ML62Q1500/1800 Group how to read the part number

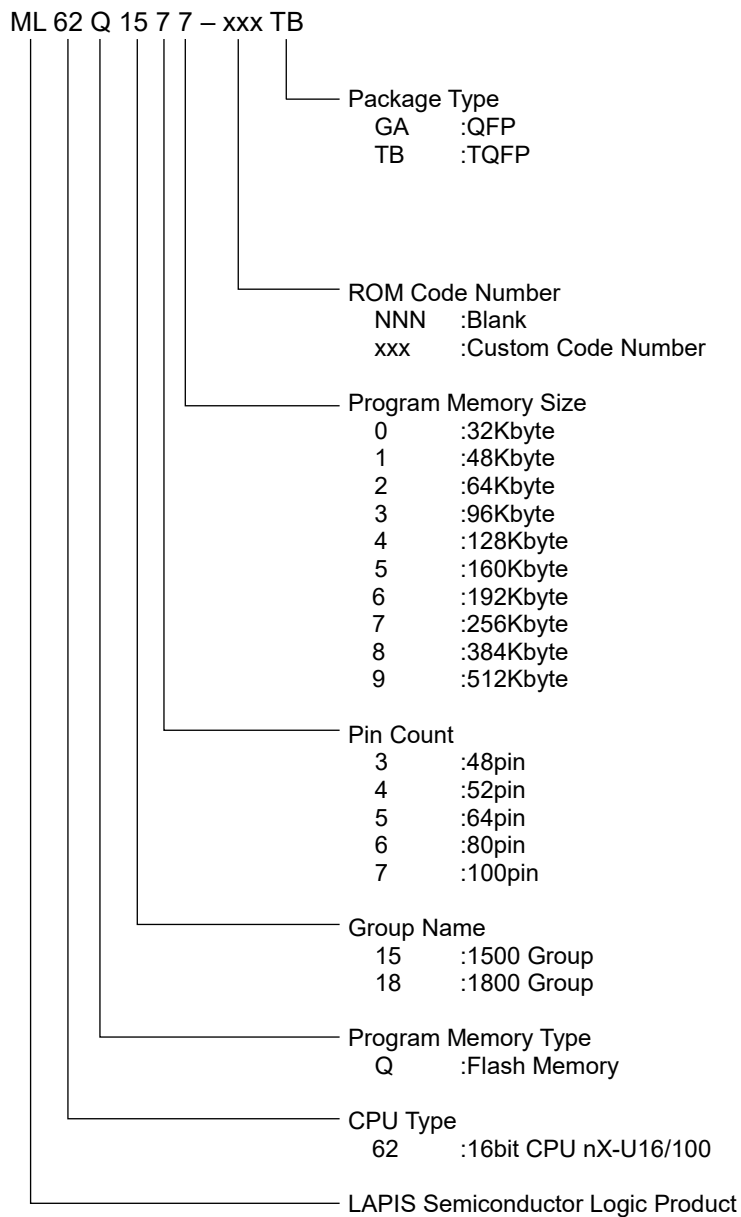


Figure 1 ML62Q1500/1800 Group Part Number

ML62Q1500/1800 Group Main Function List

Table 2 ML62Q1500/1800 Group Main Function List

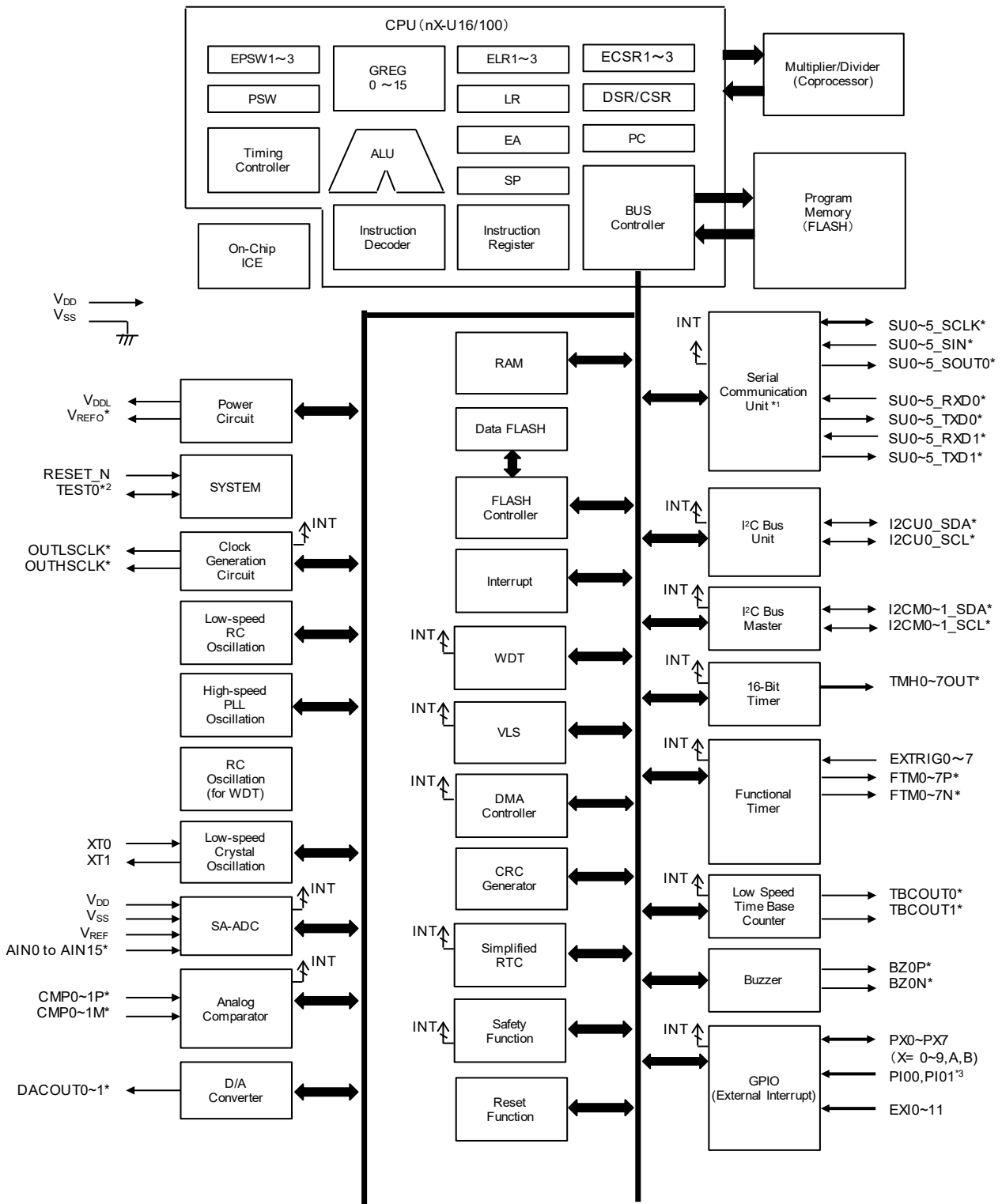
| Part number | Pin | | | | Interrupt | Timer | | | Serial | | | Analog | | | | | | | |
|-------------|-----------------|-----------------|-----------------------|-------------------------------|-----------|---------------|---|-----------------------------|---------------------------|----------------------------|---|--------------------------|--|--|--|---|-----------------------------|-------------------------------|-------------------------|
| | Total pin-count | Power pin count | Reset Input pin count | Input pin count* ³ | | I/O pin count | LED drive port (shared with the I/O port) | Internal interrupt [source] | External interrupt [port] | Functional Timer [channel] | 16bit General I Timer [channel]* ¹ | Simplified RTC [channel] | Serial communication unit (Full-duplex UART or Synchronous serial) [channel]* ² | I ² C bus unit (Master/Slave) [channel] | I ² C bus interface (Master only) [channel] | Successive type A/D converter [channel] | Analog comparator [channel] | Analog comparator [input pin] | D/A converter [channel] |
| ML62Q1530 | 48 | | | | 42 | 41 | | | | | | | | | | | | | |
| ML62Q1531 | | | | | | | | | | | | | | | | | | | |
| ML62Q1532 | | | | | | | | | | | | | | | | | | | |
| ML62Q1533 | | | | | | | | | | | | | | | | | | | |
| ML62Q1534 | | | | | | | | | | | | | | | | | | | |
| ML62Q1540 | 52 | | | | 46 | 45 | | | | | | | | | | | | | |
| ML62Q1541 | | | | | | | | | | | | | | | | | | | |
| ML62Q1542 | | | | | | | | | | | | | | | | | | | |
| ML62Q1543 | | | | | | | | | | | | | | | | | | | |
| ML62Q1544 | | | | | | | | | | | | | | | | | | | |
| ML62Q1550 | 64 | 3 | | | | | 31 | 10 | 6 | 6 | 2 | | | | | | | | |
| ML62Q1551 | | | | | | | | | | | | | | | | | | | |
| ML62Q1552 | | | | | | | | | | | | | | | | | | | |
| ML62Q1553 | | | | | | | | | | | | | | | | | | | |
| ML62Q1554 | | | | | | | | | | | | | | | | | | | |
| ML62Q1555 | 64 | 1 | 2 | | 58 | 57 | | | | | | 1 | 1 | 2 | | 2 | 4 | | |
| ML62Q1556 | | | | | | | | | | | | | | | | | | | |
| ML62Q1557 | | | | | | | | | | | | | | | | | | | |
| ML62Q1858 | | | | | | | | | | | | | | | | | | | |
| ML62Q1859 | | | | | | | | | | | | | | | | | | | |
| ML62Q1563 | 80 | | | | | | | | | | | | | | | | | | |
| ML62Q1564 | | | | | | | | | | | | | | | | | | | |
| ML62Q1565 | | | | | | | | | | | | | | | | | | | |
| ML62Q1566 | | | | | | | | | | | | | | | | | | | |
| ML62Q1567 | | | | | | | | | | | | | | | | | | | |
| ML62Q1868 | 100 | 4 | | | 72 | 71 | | | | | | | | | | | | | |
| ML62Q1869 | | | | | | | | | | | | | | | | | | | |
| ML62Q1573 | | | | | | | | | | | | | | | | | | | |
| ML62Q1574 | | | | | | | | | | | | | | | | | | | |
| ML62Q1575 | | | | | | | | | | | | | | | | | | | |
| ML62Q1576 | | | | | | | | | | | | | | | | | | | |
| ML62Q1577 | | | | | | | | | | | | | | | | | | | |
| ML62Q1878 | | | | | | | | | | | | | | | | | | | |
| ML62Q1879 | | | | | | | | | | | | | | | | | | | |

*¹ : One 16bit timer is configurable as two 8bit timers

*² : Synchronous Communication unit includes UART and Synchronous Serial Port. UART mode and Synchronous Serial Port can not be used at the same time in the same channel.

*³ : Shared with pins for crystal oscillation

BLOCK DIAGRAM



* : Indicates the shared function of general ports.

*1 : Shared UART and Synchronous Serial Port.

*2 : Not available as the input port when connecting to the on-chip debug emulator.

*3 : Not available as the input port when connecting to the crystal resonator.

Figure 2 ML62Q1500/1800 Group Block Diagram

PIN CONFIGURATION

The port names in the pin-layout indicate 1st-function. Refer to Table-3 or Table-4 about other functions.

Pin Layout of 48pin TQFP Package

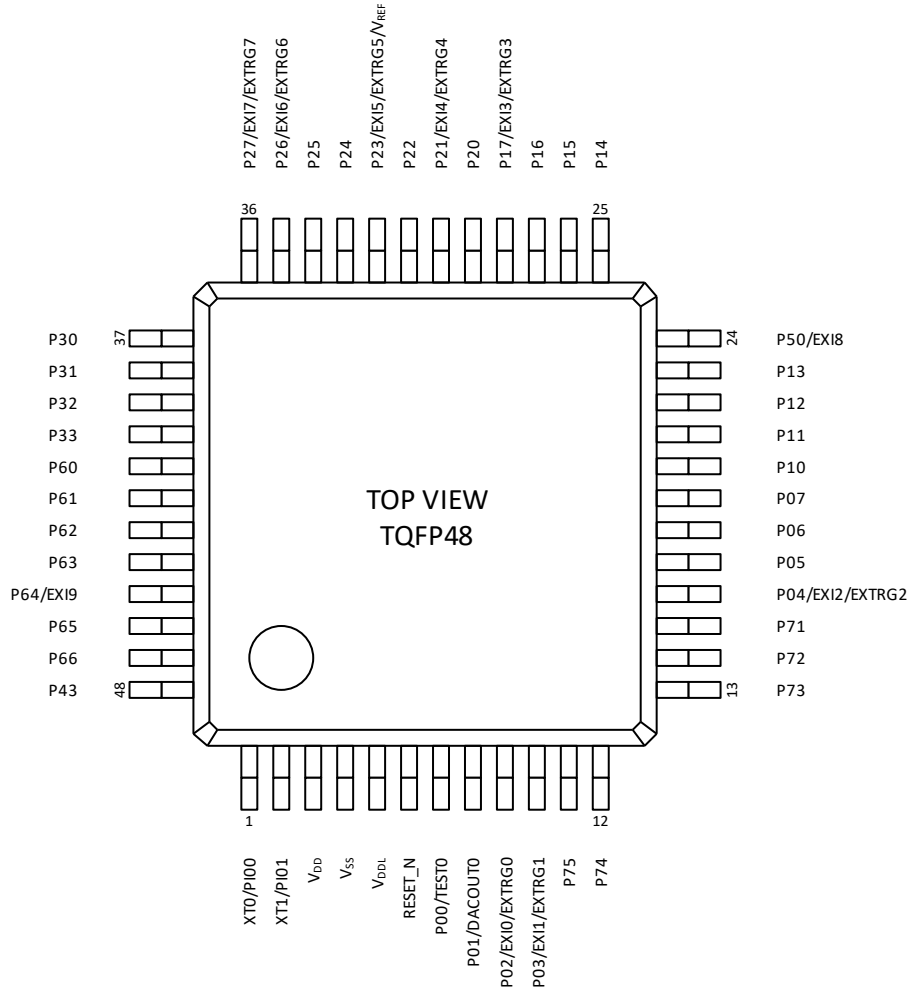


Figure 3 Pin Layout of 48pin TQFP Package

Pin Layout of 52pin TQFP Package

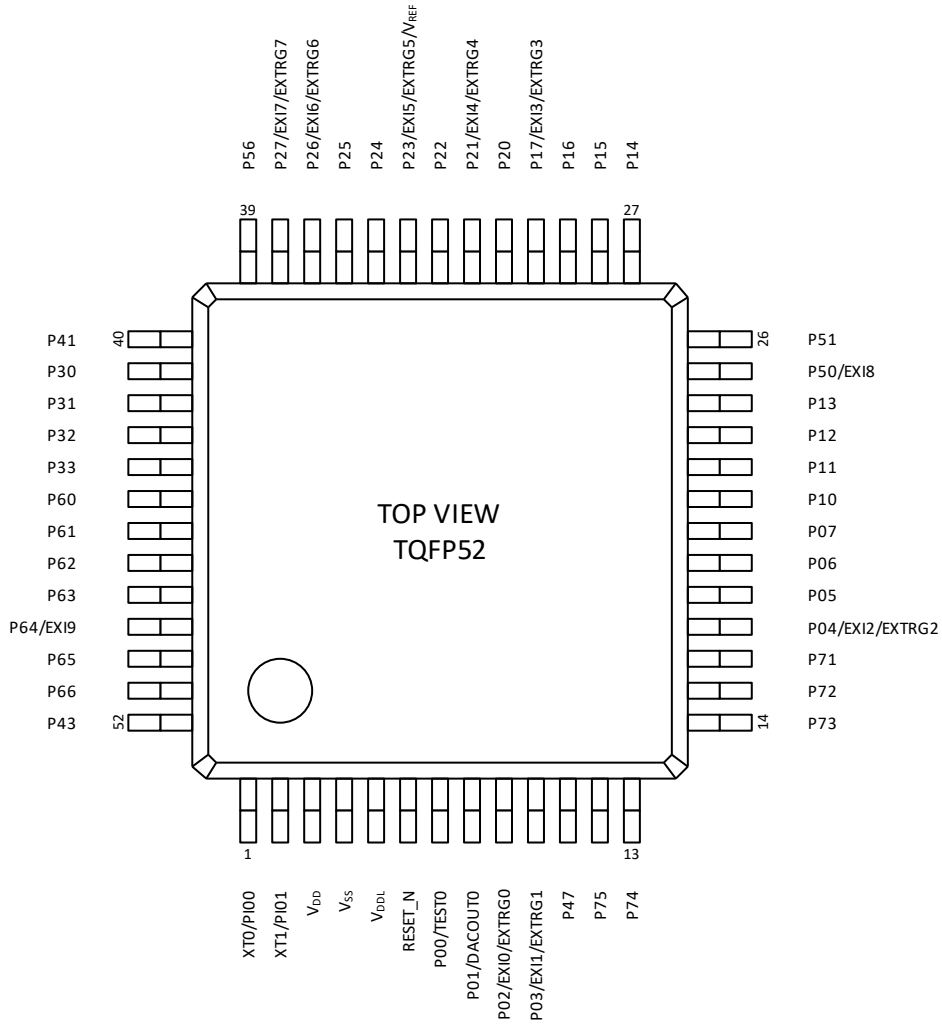


Figure 4 Pin Layout of 52pin TQFP52 Package

Pin Layout of 64pin TQFP/QFP Package

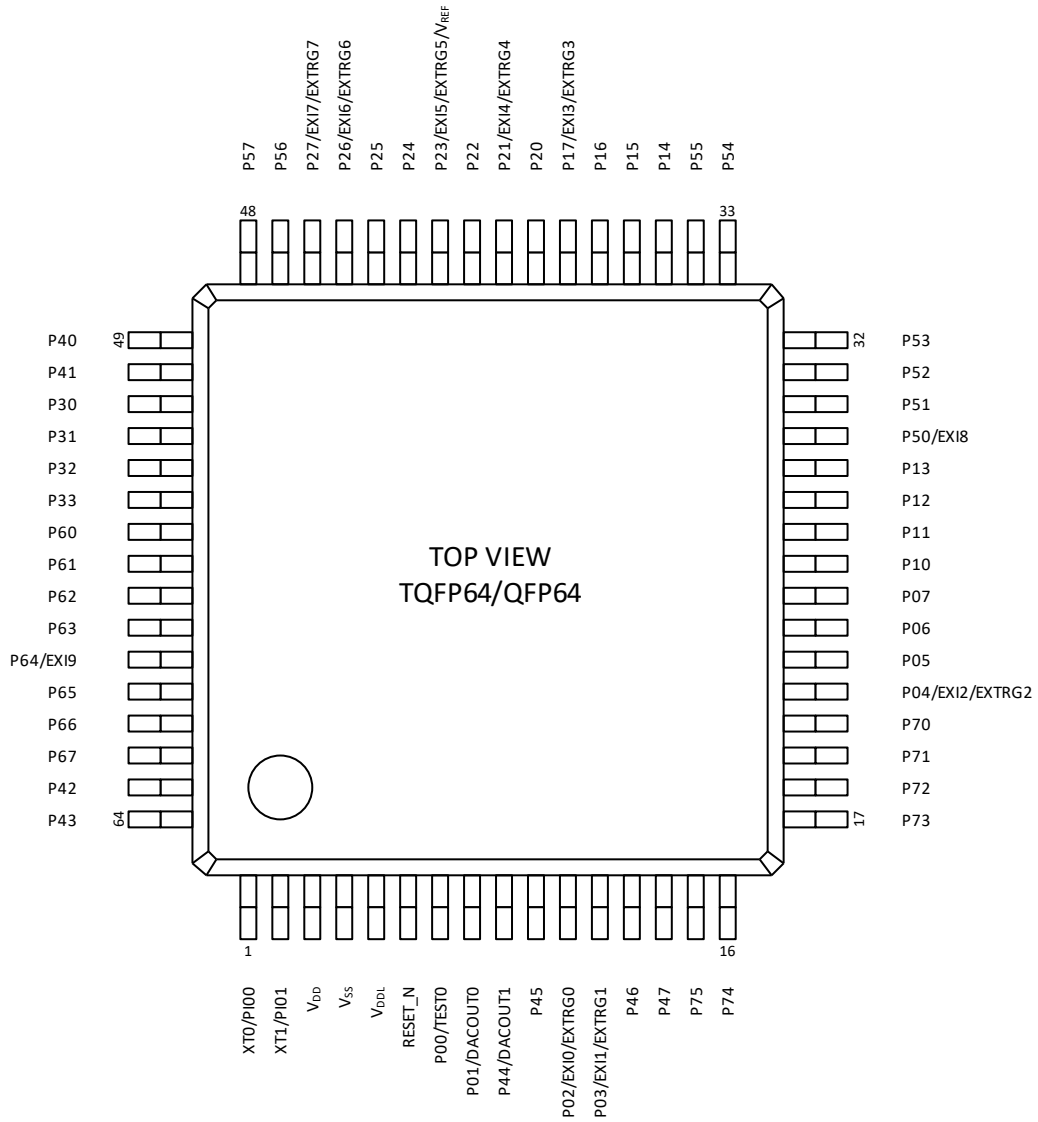


Figure 5 Pin Layout of 64pin TQFP/QFP Package

Pin Layout of 100pin TQFP Package

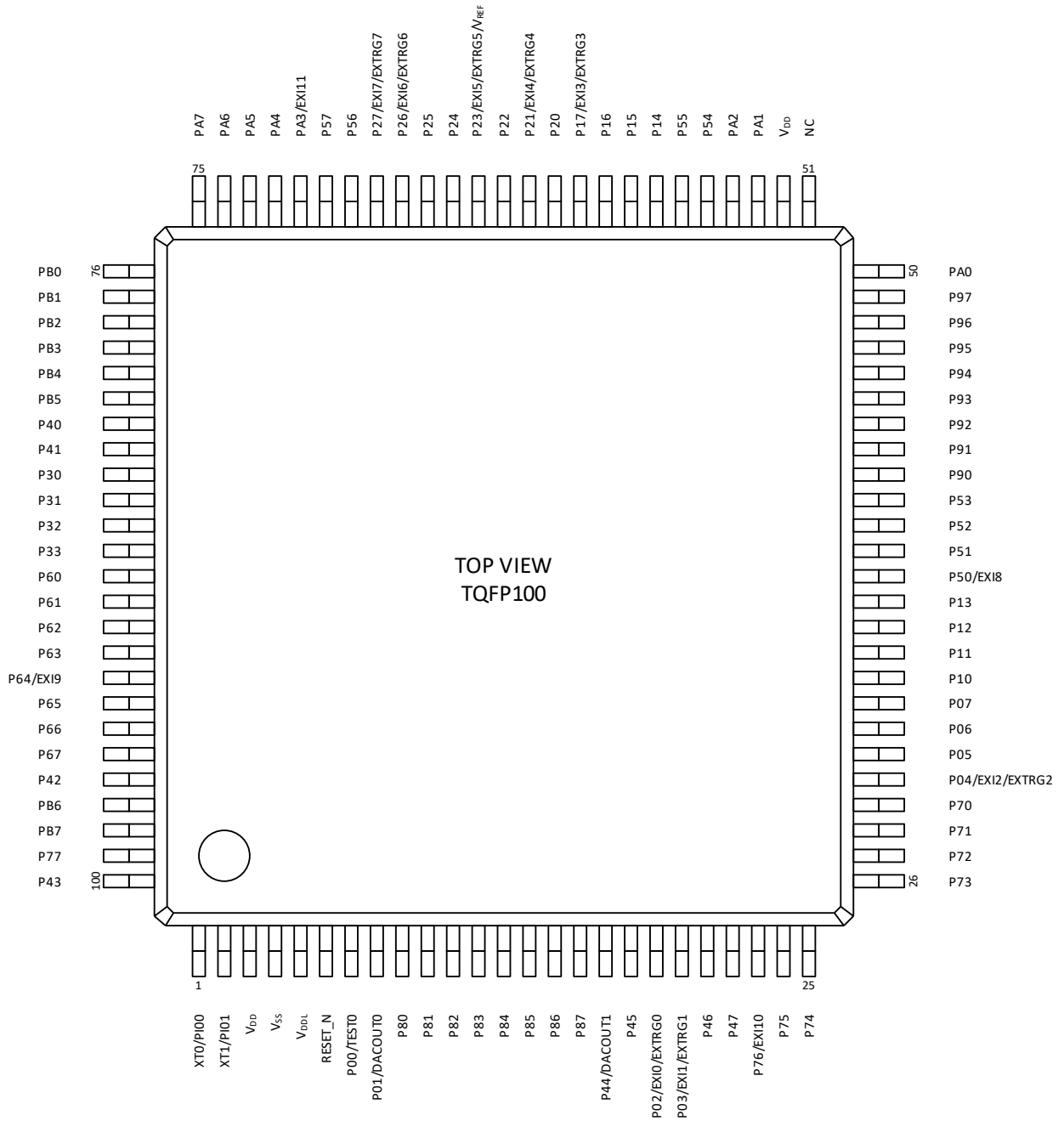


Figure 7 Pin Layout of 100pin TQFP Package

Pin Layout of 100pin QFP Package

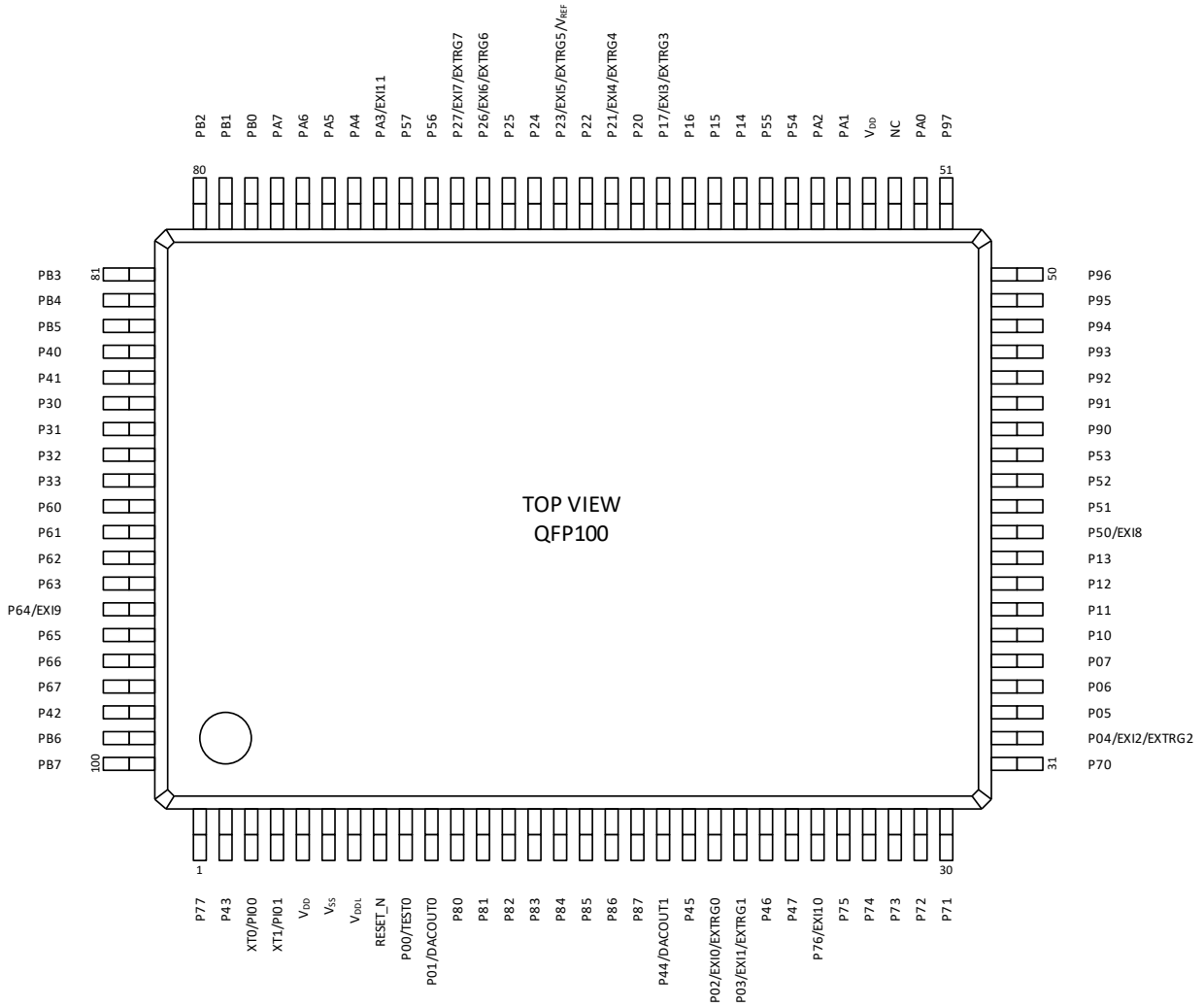


Figure 8 Pin Layout of 100pin QFP Package

PIN LIST

Table 3 Pin List (1/3)

| Pin No. | | | | | | Pin name (Primary func.) | Primary func. Others | 2 nd func. communica tions | 3 rd func. communica tions | 4 th func. communica tions | 5 th func. Timer | 6 th func. Others | 7 th func. Others | 8 th func. ADC |
|---------|-------|-------|-------|---------|--------|--------------------------------|------------------------------------|---|---|---|--------------------------------|---------------------------------|---------------------------------|------------------------------|
| 48Pin | 52Pin | 64Pin | 80Pin | TQFP100 | QFP100 | | | | | | | | | |
| 3 | 3 | 3 | 3 | 3 | 5 | V _{DD} | - | - | - | - | - | - | - | - |
| - | - | - | 42 | 52 | 54 | V _{DD} | - | - | - | - | - | - | - | - |
| 4 | 4 | 4 | 4 | 4 | 6 | V _{SS} | - | - | - | - | - | - | - | - |
| - | - | - | 41 | 51 | 53 | NC | - | - | - | - | - | - | - | - |
| 5 | 5 | 5 | 5 | 5 | 7 | V _{DDL} | - | - | - | - | - | - | - | - |
| 1 | 1 | 1 | 1 | 1 | 3 | XT0 | PI00 | - | - | - | - | - | - | - |
| 2 | 2 | 2 | 2 | 2 | 4 | XT1 | PI01 | - | - | - | - | - | - | - |
| 6 | 6 | 6 | 6 | 6 | 8 | RESET_N | - | - | - | - | - | - | - | - |
| 7 | 7 | 7 | 7 | 7 | 9 | P00 | TEST0 | - | - | - | - | - | - | - |
| 8 | 8 | 8 | 8 | 8 | 10 | P01 | DACOUT0 | - | - | - | - | TBCOUT0 | TBCOUT1 | - |
| 9 | 9 | 11 | 14 | 19 | 21 | P02 | EXI0 EXTRG0 | SU0_RXD0 SU0_SIN | - | - | FTM0P | OUTLSCLK | CMP0M | - |
| 10 | 10 | 12 | 15 | 20 | 22 | P03 | EXI1 EXTRG1 | SU0_TXD0 SU0_SOUT | SU0_TXD1 | I2CU0_SDA | FTM0N | OUTHCLK | CMP0P | AIN11 |
| 16 | 17 | 21 | 25 | 30 | 32 | P04 | EXI2 EXTRG2 | SU0_SCLK | - | I2CU0_SCL | TMH0OUT | - | - | - |
| 17 | 18 | 22 | 26 | 31 | 33 | P05 | - | - | - | - | - | - | - | - |
| 18 | 19 | 23 | 27 | 32 | 34 | P06 | - | - | - | I2CM0_SDA | - | - | - | - |
| 19 | 20 | 24 | 28 | 33 | 35 | P07 | - | SU0_RXD1 | SU0_RXD0 | I2CM0_SCL | - | - | - | - |
| 20 | 21 | 25 | 29 | 34 | 36 | P10 | - | SU0_TXD1 | - | - | - | - | - | - |
| 21 | 22 | 26 | 30 | 35 | 37 | P11 | - | SU0_SCLK | - | - | - | - | - | - |
| 22 | 23 | 27 | 31 | 36 | 38 | P12 | - | SU0_RXD0 SU0_SIN | - | - | TMH4OUT | - | - | - |
| 23 | 24 | 28 | 32 | 37 | 39 | P13 | - | SU0_TXD0 SU0_SOUT | SU0_TXD1 | - | TMH1OUT | - | TMH3OUT | - |
| 25 | 27 | 35 | 45 | 57 | 59 | P14 | - | - | - | - | - | - | - | - |
| 26 | 28 | 36 | 46 | 58 | 60 | P15 | - | - | - | I2CU0_SDA | - | - | - | - |
| 27 | 29 | 37 | 47 | 59 | 61 | P16 | - | SU1_SCLK | - | I2CU0_SCL | TMH5OUT | - | - | - |
| 28 | 30 | 38 | 48 | 60 | 62 | P17 | EXI3 EXTRG3 | SU0_RXD1 | SU0_RXD0 | - | FTM1P | TBCOUT0 | BZ0P | AIN0 |
| 29 | 31 | 39 | 49 | 61 | 63 | P20 | - | SU0_TXD1 | - | - | FTM1N | TBCOUT1 | BZ0N | AIN1 |
| 30 | 32 | 40 | 50 | 62 | 64 | P21 | EXI4 EXTRG4 | SU1_RXD0 SU1_SIN | - | - | FTM2P | OUTLSCLK | - | AIN2 |
| 31 | 33 | 41 | 51 | 63 | 65 | P22 | - | SU1_TXD0 SU1_SOUT | SU1_TXD1 | I2CM0_SDA | FTM2N | OUTHCLK | - | AIN3 |
| 32 | 34 | 42 | 52 | 64 | 66 | P23 | EXI5 EXTRG5 V _{REF} | SU1_SCLK | - | I2CM0_SCL | TMH2OUT | - | - | V _{REF0} |
| 33 | 35 | 43 | 53 | 65 | 67 | P24 | - | SU1_RXD0 SU1_SIN | - | - | - | - | - | AIN4 |
| 34 | 36 | 44 | 54 | 66 | 68 | P25 | - | SU1_TXD0 SU1_SOUT | SU1_TXD1 | - | - | - | - | AIN5 |
| 35 | 37 | 45 | 55 | 67 | 69 | P26 | EXI6 EXTRG6 | SU1_RXD1 | SU1_RXD0 | I2CU0_SDA | FTM3P | TBCOUT0 | BZ0P | AIN6 |
| 36 | 38 | 46 | 56 | 68 | 70 | P27 | EXI7 EXTRG7 | SU1_TXD1 | - | I2CU0_SCL | FTM3N | TBCOUT1 | BZ0N | AIN7 |

Table 3 Pin List (2/3)

| Pin No. | | | | | | Pin name (Primary func) | Primary func. Others *1 | 2 nd func. communica tions *1 | 3 rd func. communica tions *1 | 4 th func. communica tions | 5 th func. Timer *1 | 6 th func. Others | 7 th func. Others | 8 th func. ADC *1 |
|---------|-------|-------|-------|---------|--------|-------------------------------|----------------------------------|---|---|---|--------------------------------------|---------------------------------|---------------------------------|------------------------------------|
| 48Pin | 52Pin | 64Pin | 80Pin | TQFP100 | QFP100 | | | | | | | | | |
| 37 | 41 | 51 | 67 | 84 | 86 | P30 | - | - | - | - | - | - | - | |
| 38 | 42 | 52 | 68 | 85 | 87 | P31 | - | - | - | - | TBCOUT0 | TBCOUT1 | - | |
| 39 | 43 | 53 | 69 | 86 | 88 | P32 | - | SU1_RXD1 | SU1_RXD0 | - | - | - | - | |
| 40 | 44 | 54 | 70 | 87 | 89 | P33 | - | SU1_TXD1 | - | - | TMH3OUT | - | - | |
| - | - | 49 | 65 | 82 | 84 | P40 | - | SU5_TXD1 | - | - | - | - | - | |
| - | 40 | 50 | 66 | 83 | 85 | P41 | - | - | - | - | - | - | - | |
| - | - | 63 | 79 | 96 | 98 | P42 | - | SU3_TXD1 | - | - | - | - | - | |
| 48 | 52 | 64 | 80 | 100 | 2 | P43 | - | - | - | - | TBCOUT0 | TBCOUT1 | AIN10 | |
| - | - | 9 | 12 | 17 | 19 | P44 | DACOUT1 | SU4_RXD1 | SU4_RXD0 | - | - | - | - | |
| - | - | 10 | 13 | 18 | 20 | P45 | - | SU4_TXD1 | - | - | - | - | - | |
| - | - | 13 | 16 | 21 | 23 | P46 | - | - | - | - | - | - | - | |
| - | 11 | 14 | 17 | 22 | 24 | P47 | - | - | - | - | - | - | - | |
| 24 | 25 | 29 | 33 | 38 | 40 | P50 | EXI8 | - | - | - | - | - | - | |
| - | 26 | 30 | 34 | 39 | 41 | P51 | - | - | - | - | - | - | - | |
| - | - | 31 | 35 | 40 | 42 | P52 | - | SU4_RXD1 | SU4_RXD0 | - | - | - | - | |
| - | - | 32 | 36 | 41 | 43 | P53 | - | SU4_TXD1 | - | - | - | - | - | |
| - | - | 33 | 43 | 55 | 57 | P54 | - | SU2_RXD1 | SU2_RXD0 | - | TMH7OUT | - | - | |
| - | - | 34 | 44 | 56 | 58 | P55 | - | SU2_TXD1 | - | - | - | - | - | |
| - | 39 | 47 | 57 | 69 | 71 | P56 | - | SU2_RXD0 SU2_SIN | - | - | - | - | AIN12 | |
| - | - | 48 | 58 | 70 | 72 | P57 | - | SU2_TXD0 SU2_SOUT | SU2_TXD1 | - | - | - | AIN13 | |
| 41 | 45 | 55 | 71 | 88 | 90 | P60 | - | - | - | I2CM1_SCL | - | - | - | |
| 42 | 46 | 56 | 72 | 89 | 91 | P61 | - | - | - | I2CM1_SDA | - | - | - | |
| 43 | 47 | 57 | 73 | 90 | 92 | P62 | - | - | - | - | FTM4N | - | CMP1P | |
| 44 | 48 | 58 | 74 | 91 | 93 | P63 | - | - | - | - | FTM4P | - | CMP1M | |
| 45 | 49 | 59 | 75 | 92 | 94 | P64 | EXI9 | SU3_RXD0 SU3_SIN | - | - | FTM5P | - | - | |
| 46 | 50 | 60 | 76 | 93 | 95 | P65 | - | SU3_TXD0 SU3_SOUT | SU3_TXD1 | - | FTM5N | - | AIN8 | |
| 47 | 51 | 61 | 77 | 94 | 96 | P66 | - | SU3_SCLK | - | - | - | - | AIN9 | |
| - | - | 62 | 78 | 95 | 97 | P67 | - | SU3_RXD1 | SU3_RXD0 | - | - | - | - | |
| - | - | 20 | 24 | 29 | 31 | P70 | - | - | - | - | TMH6OUT | - | - | |
| 15 | 16 | 19 | 23 | 28 | 30 | P71 | - | - | - | - | - | - | - | |
| 14 | 15 | 18 | 22 | 27 | 29 | P72 | - | - | - | - | - | - | - | |
| 13 | 14 | 17 | 21 | 26 | 28 | P73 | - | - | - | - | - | - | - | |
| 12 | 13 | 16 | 20 | 25 | 27 | P74 | - | - | - | - | - | - | - | |
| 11 | 12 | 15 | 19 | 24 | 26 | P75 | - | - | - | - | - | - | - | |
| - | - | - | 18 | 23 | 25 | P76 | EXI10 | - | - | - | - | - | - | |
| - | - | - | - | 99 | 1 | P77 | - | - | - | - | - | - | - | |
| - | - | - | 9 | 9 | 11 | P80 | - | SU4_RXD0 SU4_SIN | - | - | - | - | - | |
| - | - | - | 10 | 10 | 12 | P81 | - | SU4_TXD0 SU4_SOUT | SU4_TXD1 | - | - | - | - | |
| - | - | - | 11 | 11 | 13 | P82 | - | SU4_SCLK | - | - | - | - | - | |
| - | - | - | - | 12 | 14 | P83 | - | - | - | - | - | - | - | |
| - | - | - | - | 13 | 15 | P84 | - | - | - | - | - | - | - | |
| - | - | - | - | 14 | 16 | P85 | - | - | - | - | - | - | - | |
| - | - | - | - | 15 | 17 | P86 | - | - | - | - | - | - | - | |
| - | - | - | - | 16 | 18 | P87 | - | - | - | - | - | - | - | |

*1: The pins of name with DACOUT1, SU2, SU3, SU4, SU5, TMH6, TMH7, AIN12 or AIN13 are not assigned to products of 48/52/64 PIN-packages.

Table 3 Pin List (3/3)

| Pin No. | | | | | | Pin name (Primary func) | Primary func. Others | 2 nd func. communica tions | 3 rd func. communica tions | 4 th func. communica tions | 5 th func. Timers | 6 th func. Others | 7 th func. Others | 8 th func. ADC |
|---------|-------|-------|-------|--------|--------|-------------------------------|----------------------------|---|---|---|---------------------------------|---------------------------------|---------------------------------|------------------------------|
| 48Pin | 52Pin | 64Pin | 80Pin | 104Pin | QFP100 | | | | | | | | | |
| - | - | - | - | 42 | 44 | P90 | - | - | - | - | - | - | - | - |
| - | - | - | - | 43 | 45 | P91 | - | - | - | - | - | - | - | - |
| - | - | - | - | 44 | 46 | P92 | - | - | - | - | - | - | - | - |
| - | - | - | 37 | 45 | 47 | P93 | - | SU4_RXD0 SU4_SIN | - | - | FTM6P | - | - | - |
| - | - | - | 38 | 46 | 48 | P94 | - | SU4_TXD0 SU4_SOUT | SU4_TXD1 | - | FTM6N | - | - | - |
| - | - | - | 39 | 47 | 49 | P95 | - | SU4_SCLK | - | - | - | - | - | - |
| - | - | - | 40 | 48 | 50 | P96 | - | - | - | - | - | - | - | - |
| - | - | - | - | 49 | 51 | P97 | - | - | - | - | - | - | - | - |
| - | - | - | - | 50 | 52 | PA0 | - | - | - | - | - | - | - | - |
| - | - | - | - | 53 | 55 | PA1 | - | - | - | - | - | - | - | - |
| - | - | - | - | 54 | 56 | PA2 | - | - | - | - | - | - | - | - |
| - | - | - | 59 | 71 | 73 | PA3 | EXI11 | SU2_SCLK | - | - | FTM7P | - | - | AIN14 |
| - | - | - | 60 | 72 | 74 | PA4 | - | - | - | - | FTM7N | - | - | AIN15 |
| - | - | - | - | 73 | 75 | PA5 | - | - | - | - | - | - | - | - |
| - | - | - | - | 74 | 76 | PA6 | - | - | - | - | - | - | - | - |
| - | - | - | - | 75 | 77 | PA7 | - | - | - | - | - | - | - | - |
| - | - | - | - | 76 | 78 | PB0 | - | - | - | - | - | - | - | - |
| - | - | - | - | 77 | 79 | PB1 | - | - | - | - | - | - | - | - |
| - | - | - | 61 | 78 | 80 | PB2 | - | SU5_RXD0 SU5_SIN | - | - | - | - | - | - |
| - | - | - | 62 | 79 | 81 | PB3 | - | SU5_TXD0 SU5_SOUT | SU5_TXD1 | - | - | - | - | - |
| - | - | - | 63 | 80 | 82 | PB4 | - | SU5_SCLK | - | - | - | - | - | - |
| - | - | - | 64 | 81 | 83 | PB5 | - | SU5_RXD1 | SU5_RXD0 | - | - | - | - | - |
| - | - | - | - | 97 | 99 | PB6 | - | - | - | - | - | - | - | - |
| - | - | - | - | 98 | 100 | PB7 | - | - | - | - | - | - | - | - |

PIN DESCRIPTION

Table 4 Pin Description (1/5)

| Function | Signal name | Pin name | I/O | Description | Logic |
|----------------------|-------------------|------------------|-----|--|----------|
| Power | - | V _{SS} | - | Negative power supply pin (-) | - |
| | - | V _{DD} | - | Positive power supply pin (+). Connect a capacitor C _v between this pin and V _{SS} . | - |
| | - | V _{DDL} | - | Power supply pin for internal logic (internal regulator's output). Connect a capacitor C _L (1μF) between this pin and V _{SS} . | - |
| Test | TEST0 | P00 | I/O | Input for testing, is used as on-chip debug interface and ISP function. P00 is initialized as pull-up input mode by the system reset. | - |
| Un used | NC | NC | - | Connect to V _{SS} . | - |
| System | V _{REF0} | P23 | - | Reference voltage output | - |
| | RESET_N | RESET_N | I | Reset input. Applying "L" level shifts the MCU in system reset mode. Applying "H" level shifts the CPU in program running mode. Used for on-chip debug interface and ISP function. No pull-up resistor is installed. | Negative |
| | XT0 | XT0 | I | Low speed crystal oscillation pins Connect 32.768kHz crystal resonator and Connect capacitors between the pin and V _{SS} . | - |
| | XT1 | XT1 | O | | - |
| | OUTLSCLK | P02 P21 | O | Low-speed clock output. | - |
| | OUTHCLK | P03 P22 | O | High-speed clock output. | - |
| General purpose port | PI00,PI01 | XT0,XT1 | I | General purpose input. Not available as general inputs when using the crystal resonator. | Positive |
| | P00 | P00 | I/O | General purpose I/O port - High-impedance - Input with Pull-UP (initial value) - Input without Pull-UP - CMOS output - N-channel open drain output Not available to use as I/O pin when using for on-chip debug interface or ISP function. | Positive |
| | P01 to P07 | P01 to P07 | I/O | General purpose I/O - High-impedance (initial value) - Input with Pull-UP - Input without Pull-UP - CMOS output - N-channel open drain output | Positive |
| | P10 to P17 | P10 to P17 | I/O | | Positive |
| | P20 to P27 | P20 to P27 | I/O | | Positive |
| | P30 to P33 | P30 to P33 | I/O | | Positive |
| | P40 to P47 | P40 to P47 | I/O | | Positive |
| | P50 to P57 | P50 to P57 | I/O | | Positive |
| | P60 to P67 | P60 to P67 | I/O | | Positive |
| | P70 to P77 | P70 to P77 | I/O | | Positive |
| | P80 to P87 | P80 to P87 | I/O | | Positive |
| | P90 to P97 | P90 to P97 | I/O | | Positive |
| | PA0 to PA7 | PA0 to PA7 | I/O | | Positive |
| | PB0 to PB7 | PB0 to PB7 | I/O | | Positive |

Table 4 Pin Description (2/5)

| Function | Signal name | Pin name | I/O | Description | Logic |
|----------|-------------|----------|---|--|----------|
| UART | SU0_TXD0 | P03 | O | Serial communication unit0 UART0 data output | Positive |
| | | P13 | | | |
| | SU0_RXD0 | P02 | I | Serial communication unit0 Full-duplex data input Serial communication unit0 UART0 data input | Positive |
| | | P07 | | | |
| | | P12 | | | |
| | | P17 | | | |
| | SU0_TXD1 | P03 | O | Serial communication unit0 Full-duplex data output Serial communication unit0 UART1 data output | Positive |
| | | P10 | | | |
| | | P13 | | | |
| | SU0_RXD1 | P07 | I | Serial communication unit0 UART1 data input | Positive |
| | | P17 | | | |
| | SU1_TXD0 | P22 | O | Serial communication unit1 UART0 data output | Positive |
| | | P25 | | | |
| | SU1_RXD0 | P21 | I | Serial communication unit1 Full-duplex data input Serial communication unit1 UART0 data input | Positive |
| | | P24 | | | |
| | | P26 | | | |
| | | P32 | | | |
| | SU1_TXD1 | P22 | O | Serial communication unit1 Full-duplex data output Serial communication unit1 UART1 data output | Positive |
| | | P25 | | | |
| | | P27 | | | |
| | | P33 | | | |
| | SU1_RXD1 | P26 | I | Serial communication unit1 UART1 data input | Positive |
| | | P32 | | | |
| | SU2_TXD0 | P57 | O | Serial communication unit2 UART0 data output | Positive |
| | SU2_RXD0 | P54 | I | Serial communication unit2 Full-duplex data input Serial communication unit2 UART0 data input | Positive |
| | | P56 | | | |
| | SU2_TXD1 | P55 | O | Serial communication unit2 Full-duplex data output Serial communication unit2 UART1 data output | Positive |
| | | P57 | | | |
| SU2_RXD1 | P54 | I | Serial communication unit2 UART1 data input | Positive | |
| SU3_TXD0 | P65 | O | Serial communication unit3 UART0 data output | Positive | |
| SU3_RXD0 | P64 | I | Serial communication unit3 Full-duplex data input Serial communication unit3 UART0 data input | Positive | |
| | P67 | | | | |
| SU3_TXD1 | P42 | O | Serial communication unit3 Full-duplex data output Serial communication unit3 UART1 data output | Positive | |
| | P65 | | | | |
| SU3_RXD1 | P67 | I | Serial communication unit3 UART1 data input | Positive | |
| SU4_TXD0 | P81 | O | Serial communication unit4 UART0 data output | Positive | |
| | P94 | | | | |
| SU4_RXD0 | P44 | I | Serial communication unit4 Full-duplex data input Serial communication unit4 UART0 data input | Positive | |
| | P52 | | | | |
| | P80 | | | | |
| | P93 | | | | |
| SU4_TXD1 | P45 | O | Serial communication unit4 Full-duplex data output Serial communication unit4 UART1 data output. | Positive | |
| | P53 | | | | |
| | P81 | | | | |
| | P94 | | | | |
| SU4_RXD1 | P44 | I | Serial communication unit4 UART1 data input | Positive | |
| | P52 | | | | |
| SU5_TXD0 | P84 | O | Serial communication unit5 UART0 data output | Positive | |
| | PB3 | | | | |

Table 4 Pin Description (3/5)

| Function | Signal name | Pin name | I/O | Description | Logic |
|----------------------------|-------------|----------|---|---|----------|
| UART | SU5_RXD0 | P83 | I | Serial communication unit5 Full-duplex data input Serial communication unit5 UART0 data input | Positive |
| | | PB2 | | | |
| | | PB5 | | | |
| | SU5_TXD1 | P40 | O | Serial communication unit5 Full-duplex data output Serial communication unit5 UART1 data output. | Positive |
| | | P84 | | | |
| | | PB3 | | | |
| SU5_RXD1 | PB5 | I | Serial communication unit5 UART1 data input | Positive | |
| Synchronous Serial Port | SU0_SIN | P02 | I | Serial communication unit0 Synchronous serial data input | Positive |
| | | P12 | | | |
| | SU0_SCLK | P04 | I/O | Serial communication unit0 Synchronous serial clock I/O | Positive |
| | | P11 | | | |
| | | P47 | | | |
| | SU0_SOUT | P03 | O | Serial communication unit0 Synchronous serial data output | Positive |
| | | P13 | | | |
| | SU1_SIN | P21 | I | Serial communication unit1 Synchronous serial data input | Positive |
| | | P24 | | | |
| | SU1_SCLK | P16 | I/O | Serial communication unit1 Synchronous serial clock I/O | Positive |
| | | P23 | | | |
| | SU1_SOUT | P22 | O | Serial communication unit1 Synchronous serial data output | Positive |
| | | P25 | | | |
| | SU2_SIN | P56 | I | Serial communication unit2 Synchronous serial data | Positive |
| | SU2_SCLK | PA3 | I/O | Serial communication unit2 Synchronous serial clock I/O | Positive |
| | SU2_SOUT | P57 | O | Serial communication unit2 Synchronous serial data output | Positive |
| | SU3_SIN | P64 | I | Serial communication unit3 Synchronous serial data input | Positive |
| | SU3_SCLK | P66 | I/O | Serial communication unit3 Synchronous serial clock I/O | Positive |
| SU3_SOUT | P65 | O | Serial communication unit3 Synchronous serial data output | Positive | |
| SU4_SIN | P80 | I | Serial communication unit4 Synchronous serial data input | Positive | |
| | P93 | | | | |
| SU4_SCLK | P95 | I/O | Serial communication unit4 Synchronous serial clock I/O | Positive | |
| | P82 | | | | |
| SU4_SOUT | P81 | O | Serial communication unit4 Synchronous serial data output | Positive | |
| | P94 | | | | |
| SU5_SIN | PB2 | I | Serial communication unit5 Synchronous serial data input | Positive | |
| SU5_SCLK | PB4 | I/O | Serial communication unit5 Synchronous serial clock I/O | Positive | |
| SU5_SOUT | PB3 | O | Serial communication unit5 Synchronous serial data output | Positive | |
| I ² C Bus | I2CU0_SDA | P03 | I/O | I ² C Unit0 (Master and Salve) Data I/O N-channel open drain Connect a pull-up resistor externally | Positive |
| | | P15 | | | |
| | | P26 | | | |
| | | P46 | | | |
| | I2CU0_SCL | P02 | I/O | I ² C Unit0 (Master and Salve) Clock I/O N-channel open drain output Connect a pull-up resistor externally | Positive |
| | | P04 | | | |
| | | P16 | | | |
| | | P27 | | | |
| | I2CM0_SDA | P06 | I/O | I ² C Master0 Data I/O pin N-channel open drain output Connect a pull-up resistor externally | Positive |
| P22 | | | | | |

Table 4 Pin Description (4/5)

| Function | Signal name | Pin name | I/O | Description | Logic |
|------------------------|-------------|----------|--------------------------------------|--|----------|
| I ² C Bus | I2CM0_SCL | P07 | I/O | I ² C Master0 Clock I/O N-channel open drain output Connect a pull-up resistor externally | Positive |
| | | P23 | | | |
| | I2CM1_SDA | P61 | I/O | I ² C Master1 Data I/O N-channel open drain output Connect a pull-up resistor externally | Positive |
| | I2CM1_SCL | P60 | I/O | I ² C Master1 Clock I/O N-channel open drain output Connect a pull-up resistor externally | Positive |
| Functional Timer (FTM) | FTM0P | P02 | O | Functional Timer0 P output | Positive |
| | FTM0N | P03 | O | Functional Timer0 N output | Negative |
| | FTM1P | P17 | O | Functional Timer1 P output | Positive |
| | | P47 | | | |
| | FTM1N | P20 | O | Functional Timer1 N output | Negative |
| | | P46 | | | |
| | FTM2P | P21 | O | Functional Timer2 P output | Positive |
| | FTM2N | P22 | O | Functional Timer2 N output | Negative |
| | FTM3P | P01 | O | Functional Timer3 P output | Positive |
| | | P26 | | | |
| | FTM3N | P27 | O | Functional Timer3 N output | Negative |
| | | P44 | | | |
| | FTM4P | P63 | O | Functional Timer4 P output | Positive |
| | FTM4N | P62 | O | Functional Timer4 N output | Negative |
| | FTM5P | P64 | O | Functional Timer5 P output | Positive |
| | FTM5N | P65 | O | Functional Timer5 N output | Negative |
| | FTM6P | P93 | O | Functional Timer6 P output | Positive |
| | FTM6N | P94 | O | Functional Timer6 N output | Negative |
| | FTM7P | P86 | O | Functional Timer7 P output | Positive |
| | | PA3 | | | |
| | FTM7N | P87 | O | Functional Timer7 N output | Negative |
| | | PA4 | | | |
| | EXTRG0 | P02 | I | Functional Timer event trigger input | - |
| EXTRG1 | P03 | I | Functional Timer event trigger input | - | |
| EXTRG2 | P04 | I | Functional Timer event trigger input | - | |
| EXTRG3 | P17 | I | Functional Timer event trigger input | - | |
| EXTRG4 | P21 | I | Functional Timer event trigger input | - | |
| EXTRG5 | P23 | I | Functional Timer event trigger input | - | |
| EXTRG6 | P26 | I | Functional Timer event trigger input | - | |
| EXTRG7 | P27 | I | Functional Timer event trigger input | - | |
| 16 bit Timer | TMH0OUT | P04 | O | 16bit General Timer 0 output | Positive |
| | TMH1OUT | P13 | O | 16bit General Timer 1 output | Positive |
| | TMH2OUT | P23 | O | 16bit General Timer 2 output | Positive |
| | TMH3OUT | P13 | O | 16bit General Timer 3 output | Positive |
| | | P33 | | | |
| | TMH4OUT | P12 | O | 16bit General Timer 4 output | Positive |
| | TMH5OUT | P16 | O | 16bit General Timer 5 output | Positive |
| | TMH6OUT | P70 | O | 16bit General Timer 6 output | Positive |
| | TMH7OUT | P54 | O | 16bit General Timer 7 output | Positive |
| | EXTRG0 | P02 | I | 16bit Timer trigger input | - |
| EXTRG1 | P03 | I | 16bit Timer trigger input | - | |

Table 4 Pin Description (5/5)

| Function | Signal name | Pin name | I/O | Description | Logic |
|--|------------------|----------|-----------------------------|--|----------|
| Low-speed Time Base Counter | TBCOUT0 | P01 | O | The virtual frequency adjustment signal output | Positive |
| | | P17 | | | |
| | | P26 | | | |
| | | P31 | | | |
| | | P43 | | | |
| | TBCOUT1 | P01 | O | Low-speed Time Base Counter 1Hz/2Hz output | Positive |
| | | P20 | | | |
| | | P27 | | | |
| | | P31 | | | |
| Buzzer | BZ0P | P17 | O | Buzzer output (positive phase) | Positive |
| | | P26 | | | |
| | BZ0N | P20 | O | Buzzer output (negative phase) | Negative |
| | | P27 | | | |
| External Interrupt | EXI0 | P02 | I | External Interrupt 0 Input | - |
| | EXI1 | P03 | I | External Interrupt 1 Input | - |
| | EXI2 | P04 | I | External Interrupt 2 Input | - |
| | EXI3 | P17 | I | External Interrupt 3 Input | - |
| | EXI4 | P21 | I | External Interrupt 4 Input | - |
| | EXI5 | P23 | I | External Interrupt 5 Input | - |
| | EXI6 | P26 | I | External Interrupt 6 Input | - |
| | EXI7 | P27 | I | External Interrupt 7 Input | - |
| | EXI8 | P50 | I | External Interrupt 8 Input | - |
| | EXI9 | P64 | I | External Interrupt 9 Input | - |
| | EXI10 | P76 | I | External Interrupt 10 Input | - |
| EXI11 | PA3 | I | External Interrupt 11 Input | - | |
| Successive approximation type A/D converter (SA-ADC) | V _{REF} | P23 | - | SA-ADC external reference voltage input | - |
| | AIN0 | P17 | I | SA-ADC channel 0 input | - |
| | AIN1 | P20 | I | SA-ADC channel 1 input | - |
| | AIN2 | P21 | I | SA-ADC channel 2 input | - |
| | AIN3 | P22 | I | SA-ADC channel 3 input | - |
| | AIN4 | P24 | I | SA-ADC channel 4 input | - |
| | AIN5 | P25 | I | SA-ADC channel 5 input | - |
| | AIN6 | P26 | I | SA-ADC channel 6 input | - |
| | AIN7 | P27 | I | SA-ADC channel 7 input | - |
| | AIN8 | P65 | I | SA-ADC channel 8 input | - |
| | AIN9 | P66 | I | SA-ADC channel 9 input | - |
| | AIN10 | P43 | I | SA-ADC channel 10 input | - |
| | AIN11 | P03 | I | SA-ADC channel 11 input | - |
| | AIN12 | P56 | I | SA-ADC channel 12 input | - |
| | AIN13 | P57 | I | SA-ADC channel 13 input | - |
| AIN14 | PA3 | I | SA-ADC channel 14 input | - | |
| AIN15 | PA4 | I | SA-ADC channel 15 input | - | |
| Analog comparator | CMP0P | P03 | I | Comparator input 0 (noninverting input) | - |
| | CMP0M | P02 | I | Comparator input 0 (inverting input) | - |
| | CMP1P | P62 | I | Comparator input 1 (noninverting input) | - |
| | CMP1M | P63 | I | Comparator input 1 (inverting input) | - |
| D/A converter | DACOUT0 | P01 | O | D/A converter 0 output | - |
| | DACOUT1 | P44 | O | D/A converter 1 output | - |

TERMINATION OF UNUSED PINS

Table 5 Termination of unused pins

| Pin | pin termination |
|--------------------|---|
| NC | Connect to V_{SS} . |
| RESET_N | Connect to V_{DD} |
| P00/TEST0 | Connect to V_{DD} with initial state (pulled-up input mode) |
| XT0/PI00, XT1/PI01 | Open with initial state(Hi-impedance) |
| P01 to P07 | |
| P10 to P17 | |
| P20 to P27 | |
| P30 to P33 | |
| P40 to P47 | |
| P50 to P57 | |
| P60 to P67 | |
| P70 to P77 | |
| P80 to P87 | |
| P90 to P97 | |
| PA0 to PA7 | |
| PB0 to PB7 | |

Note:

- Terminate unused input pins according to the table 5 in order to avoid unexpected through-current in the pins.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

| Parameter | Symbol | Condition | Rating | Unit | |
|--------------------------|-------------------|------------|--|--------------------|----|
| Power supply voltage 1 | V _{DD} | Ta = +25°C | -0.3 to +6.5 | V | |
| Power supply voltage 2 | V _{DDL} | Ta = +25°C | -0.3 to +2.0 | V | |
| Input voltage | V _{IN} | Ta = +25°C | -0.3 to V _{DD} +0.3* ¹ | V | |
| Output voltage | V _{OUT} | Ta = +25°C | -0.3 to V _{DD} +0.3* ¹ | V | |
| “H” level output current | I _{OUTH} | Ta = +25°C | 1pin | -40* ² | mA |
| | | | Total | -180* ² | |
| “L” level output current | I _{OUTL} | Ta = +25°C | 1pin | +40 | mA |
| | | | Total | +180 | |
| Power dissipation | PD | Ta = +25°C | 1 | W | |
| Storage temperature | T _{STG} | — | -55 to +150 | °C | |

*¹ 6.5V or lower*² The current flowing out the LSI through the pin is described in the negative number.

The applicable maximum current is the absolute value.

For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

[Note]

Stresses above the absolute maximum ratings listed in the above table may cause permanent damage to the device.

These are stress ratings only and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

(V_{SS} = 0V)

| Parameter | Symbol | Condition | Range | Unit |
|---|-----------------|-------------------------------|-------------|------|
| Operating temperature (Ambient) | Ta | — | -40 to +105 | °C |
| Operating temperature (Chip-Junction) | Tj | — | -40 to +115 | °C |
| Operating voltage | V _{DD} | — | 1.6 to 5.5 | V |
| Operating frequency (CPU) | f _{OP} | V _{DD} = 1.6 to 5.5V | 30k to 4M | Hz |
| | | V _{DD} = 1.8 to 5.5V | 30k to 25M | |
| V _{DDL} pin external capacitance | C _L | — | 1.0 ±30% | μF |

Thermal characteristics

The maximum chip-junction temperature, T_{jmax} , may be calculated using the following equation.

$$T_{jmax} = T_{amax} + P_{Dmax} \times \theta_{ja}$$

T_{amax} : maximum ambient temperature

P_{Dmax} : LSI maximum power dissipation

θ_{ja} : Package junction to ambient thermal resistance

Design a Mounting board by considering heat radiation such as power dissipation and ambient temperature to satisfy the recommended conditions.

The following table shows the each package's thermal resistance for thermal design reference estimated by simulation based on the PCB (printed circuit board) conditions define as a below.

| Parameter | Symbol | Package type | Value | | Unit |
|--------------------|---------------|--------------|-------|-------|------|
| | | | L1 | L2 | |
| Thermal resistance | θ_{ja} | TQFP48 | 63.6 | 57.8 | °C/W |
| | | TQFP52 | 61.7 | 56.7 | |
| | | TQFP64 | 63.2 | 58.2 | |
| | | QFP64 | 47.2 | 43.3 | |
| | | QFP80 | 55.5 | 51.6 | |
| | | TQFP100 | 48.0 | 43.3 | |
| | | QFP100 | 104.7 | 101.3 | |

PCB conditions:

| PCB name | L1 | L2 | Unit |
|----------------------|--------------------|---------------------------|-------|
| PCB size (L / W / T) | 114.3 / 76.2 / 1.6 | 114.3 / 76.2 / 1.6 | mm |
| Number of layer | 1 | 2 | layer |
| Wiring density | 60% (top layer) | 60%(top and bottom layer) | — |
| Wind condition | No wind (0m/s) | | — |

Current Consumption 1

Product: ML62Q1530, ML62Q1531, ML62Q1532, ML62Q1533, ML62Q1534, ML62Q1540,
ML62Q1541, ML62Q1542, ML62Q1543, ML62Q1544, ML62Q1550, ML62Q1551,
ML62Q1552, ML62Q1553, ML62Q1554

($V_{DD}=1.6$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ.* ³ | Max. | Unit | Measuring circuit |
|--------------------|--------|---|--------------------------------|--------------------|------|------|-------------------|
| Supply current 0 | IDD0 | CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped. | $T_a = -40$ to $+85^{\circ}C$ | — | 0.8 | 23 | μA |
| | | | $T_a = -40$ to $+105^{\circ}C$ | — | | 75 | |
| Supply current 1 | IDD1 | CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped. | $T_a = -40$ to $+85^{\circ}C$ | — | 1.0 | 26 | μA |
| | | | $T_a = -40$ to $+105^{\circ}C$ | — | | 80 | |
| Supply current 2-1 | IDD2-1 | Low-speed RC32K Oscillating. CPU is in HALT state (LTBC and WDT are operating* ¹). PLL oscillation is stopped. | $T_a = -40$ to $+85^{\circ}C$ | — | 4.7 | 35 | μA |
| | | | $T_a = -40$ to $+105^{\circ}C$ | — | | 85 | |
| Supply current 2-2 | IDD2-2 | Low-speed Crystal Oscillating.* ⁴ CPU is in HALT state (LTBC and WDT are operating* ¹). PLL oscillation is stopped. | $T_a = -40$ to $+85^{\circ}C$ | — | 3.0 | 32 | μA |
| | | | $T_a = -40$ to $+105^{\circ}C$ | — | | 85 | |
| Supply current 3 | IDD3 | CPU: Running with low-speed RC32K oscillation clock* ^{1*2} PLL oscillation is stopped. | $T_a = -40$ to $+105^{\circ}C$ | — | 17 | 105 | μA |
| Supply current 4 | IDD4 | CPU: Running with 16MHz PLL oscillating clock* ^{1*2} PLL 16MHz is oscillating. $V_{DD}=1.8\sim 5.5V$ | $T_a = -40$ to $+105^{\circ}C$ | — | 3.3 | 4.5 | mA |
| Supply current 5 | IDD5 | CPU: Running with 24MHz PLL oscillating clock* ^{1*2} PLL 24MHz is oscillating. $V_{DD}=1.8\sim 5.5V$ | $T_a = -40$ to $+105^{\circ}C$ | — | 4.7 | 6.0 | |

*¹ LTBC and WDT is operating, Significant bits of BLKCON0-3 and BRECON0-3 registers are all "1"

*² CPU running in wait mode

*³ On the condition of $V_{DD}=3.0V$, $T_a=+25^{\circ}C$

*⁴ When the noise filter is not used in the low power consumption mode

Current Consumption 2

Product: ML62Q1555, ML62Q1556, ML62Q1557, ML62Q1563, ML62Q1564, ML62Q1565, ML62Q1566,
ML62Q1567, ML62Q1573, ML62Q1574, ML62Q1575, ML62Q1576, ML62Q1577

($V_{DD}=1.6$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ.* ³ | Max. | Unit | Measuring circuit |
|--------------------|--------|---|--------------------------------|--------------------|------|------|-------------------|
| Supply current 0 | IDD0 | CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped. | $T_a = -40$ to $+85^{\circ}C$ | — | 1.0 | 55 | μA |
| | | | $T_a = -40$ to $+105^{\circ}C$ | — | | 110 | |
| Supply current 1 | IDD1 | CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped. | $T_a = -40$ to $+85^{\circ}C$ | — | 1.3 | 60 | μA |
| | | | $T_a = -40$ to $+105^{\circ}C$ | — | | 120 | |
| Supply current 2-1 | IDD2-1 | Low-speed RC32K Oscillating. CPU is in HALT state (LTBC and WDT are operating ^{*1}). PLL oscillation is stopped. | $T_a = -40$ to $+85^{\circ}C$ | — | 5.5 | 76 | μA |
| | | | $T_a = -40$ to $+105^{\circ}C$ | — | | 135 | |
| Supply current 2-2 | IDD2-2 | Low-speed Crystal Oscillating. ^{*4} CPU is in HALT state (LTBC and WDT are operating ^{*1}). PLL oscillation is stopped. | $T_a = -40$ to $+85^{\circ}C$ | — | 4.5 | 76 | μA |
| | | | $T_a = -40$ to $+105^{\circ}C$ | — | | 135 | |
| Supply current 3 | IDD3 | CPU: Running with low-speed RC32K oscillation clock ^{*1*2} PLL oscillation is stopped. | $T_a = -40$ to $+105^{\circ}C$ | — | 20 | 150 | μA |
| Supply current 4 | IDD4 | CPU: Running with 16MHz PLL oscillating clock ^{*1*2} PLL 16MHz is oscillating. $V_{DD}=1.8\sim 5.5V$ | $T_a = -40$ to $+105^{\circ}C$ | — | 5.0 | 6.2 | mA |
| Supply current 5 | IDD5 | CPU: Running with 24MHz PLL oscillating clock ^{*1*2} PLL 24MHz is oscillating. $V_{DD}=1.8\sim 5.5V$ | $T_a = -40$ to $+105^{\circ}C$ | — | 6.8 | 8.5 | |

*¹ LTBC and WDT is operating, Significant bits of BLKCON0-3 and BRECON0-3 registers are all "1"

*² CPU running in wait mode

*³ On the condition of $V_{DD}=3.0V$, $T_a=+25^{\circ}C$

*⁴ When the noise filter is not used in the low power consumption mode

Current Consumption 3

Product: ML62Q1858, ML62Q1859, ML62Q1868, ML62Q1869, ML62Q1878, ML62Q1879

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ.* ³ | Max. | Unit | Measuring circuit |
|--------------------|--------|--|---------------------|--------------------|------|------|-------------------|
| Supply current 0 | IDD0 | CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped. | Ta = -40 to +85 °C | — | 1.2 | 57 | μA |
| | | | Ta = -40 to +105 °C | — | | 140 | |
| Supply current 1 | IDD1 | CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped. | Ta = -40 to +85 °C | — | 1.8 | 62 | μA |
| | | | Ta = -40 to +105 °C | — | | 150 | |
| Supply current 2-1 | IDD2-1 | Low-speed RC32K Oscillating. CPU is in HALT state (LTBC and WDT are operating ^{*1}). PLL oscillation is stopped. | Ta = -40 to +85 °C | — | 6.0 | 78 | μA |
| | | | Ta = -40 to +105 °C | — | | 165 | |
| Supply current 2-2 | IDD2-2 | Low-speed Crystal Oscillating. ^{*4} CPU is in HALT state (LTBC and WDT are operating ^{*1}). PLL oscillation is stopped. | Ta = -40 to +85 °C | — | 4.5 | 78 | μA |
| | | | Ta = -40 to +105 °C | — | | 165 | |
| Supply current 3 | IDD3 | CPU: Running with low-speed RC32K oscillation clock ^{*1*2} PLL oscillation is stopped. | Ta = -40 to +105 °C | — | 20 | 190 | μA |
| Supply current 4 | IDD4 | CPU: Running with 16MHz PLL oscillating clock ^{*1*2} PLL 16MHz is oscillating. V _{DD} =1.8~5.5V | Ta = -40 to +105 °C | — | 4.0 | 5.0 | mA |
| Supply current 5 | IDD5 | CPU: Running with 24MHz PLL oscillating clock ^{*1*2} PLL 24MHz is oscillating. V _{DD} =1.8~5.5V | Ta = -40 to +105 °C | — | 5.7 | 7.0 | |

1

*1 LTBC and WDT is operating, Significant bits of BLKCON0-3 and BRECON0-3 registers are all "1"

*2 CPU running in wait mode

*3 On the condition of V_{DD}=3.0V, Ta=+25°C

*4 When the noise filter is not used in the low power consumption mode

Low speed Crystal Oscillation

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

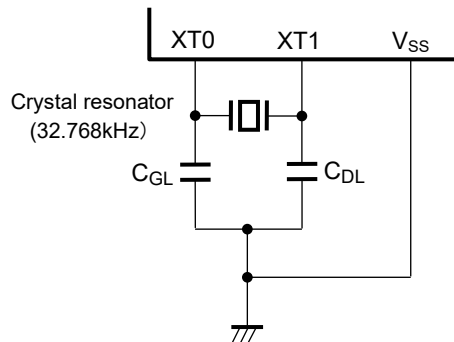
| Parameter | Symbol | Condition | Range | | | Unit |
|-------------------------------------|------------------|-----------|-------|--------|------|------|
| | | | Min. | Typ. | Max. | |
| Crystal oscillation frequency *1 *2 | f _{XTL} | — | — | 32.768 | — | kHz |
| Crystal oscillation start time | T _{XTL} | — | — | — | 2 | s |

*1: The oscillation frequency is determined by the oscillation circuit, crystal resonator and the external capacitance (C_{GL}/C_{DL}). As those parameters changes depending the crystal resonator, it requires evaluation on the actual PCB circuit for matching. Ask crystal resonator makers for matching and confirm the oscillation characteristics.

*2: The quality of oscillation characteristics might be lost, depending on material of PCB, condition of wiring capacitance or parasitic capacitance on the external circuits. Note for designing the external circuit.

- Make the wires on the external circuit as short as possible.
- Place the crystal resonator and oscillation circuit as close to the MCU as possible and make the wires between the external capacitance and crystal resonator as short as possible.
- Ensure no signal line flowing big current runs near the oscillation circuit.
- Ensure no signal line runs under and near the oscillation circuit.
- Make ground of external capacitance the same as MCU ground V_{SS} pin and connect them to the ground that has low variation of current and voltage.
- The quality of oscillation characteristics might be lost depending on operating environment due to moisture absorption of PCB and condensation of PCB surface, recommended to have measures such as covering the oscillation circuit with resin.

Low speed Crystal Oscillation external circuit example



External Clock Input

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Range | | | Unit |
|-------------------|--------------------|-----------|---------------------------|--------|---------------------------|------|
| | | | Min. | Typ. | Max. | |
| Input Frequency | f _{EXCK} | — | Typ. -1.0% | 32.768 | Typ. +1.0% | kHz |
| Input pulse width | t _{EXCKW} | — | 1/f _{EXCK} x 0.4 | — | 1/f _{EXCK} x 0.6 | s |

On-chip Oscillator

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring circuit |
|---|-------------------|--|---------------|--------|---------------|------|-------------------|
| Low-speed RC oscillator frequency accuracy 1 Without software adjustment | f _{RCL1} | Ta= +25°C V _{DD} = 1.8 to 5.5V | Typ. -1.0% | 32.768 | Typ. +1.0% | kHz | 1 |
| | | Ta= -40 to +85°C V _{DD} = 1.8 to 5.5V | Typ. -2.5% | 32.768 | Typ. +2.5% | | |
| | | Ta= -40 to +105°C V _{DD} = 1.8 to 5.5V | Typ. -3.0% | 32.768 | Typ. +3.0% | | |
| | | V _{DD} = 1.6 to 1.8V | Typ. -3.5% | 32.768 | Typ. -3.5% | | |
| Low-speed RC oscillator frequency accuracy 2 With software adjustment | f _{RCL2} | Ta= -40 to +85°C V _{DD} = 1.8 to 5.5V | Typ. -1.0% | 32.768 | Typ. +1.0% | | |
| | | Ta= -40 to +105°C V _{DD} = 1.8 to 5.5V | Typ. -1.5% | 32.768 | Typ. +1.5% | | |
| PLL oscillation frequency accuracy 1 Without software adjustment | f _{PLL1} | Ta= -40 to +85°C V _{DD} = 1.8 to 5.5V | Typ. -2.5% | 16/24 | Typ. +2.5% | MHz | |
| | | Ta= -40 to +105°C V _{DD} = 1.8 to 5.5V | Typ. -3.0% | 16/24 | Typ. +3.0% | | |
| | | V _{DD} = 1.6 to 1.8V | Typ. -3.5% | 16/24 | Typ. +3.5% | | |
| PLL oscillation frequency accuracy 2 With software adjustment | f _{PLL2} | Ta= -40 to +85°C V _{DD} = 1.8 to 5.5V | Typ. -1.0% | 16/24 | Typ. +1.0% | | |
| | | Ta= -40 to +105°C V _{DD} = 1.8 to 5.5V | Typ. -1.5% | 16/24 | Typ. +1.5% | | |
| PLL oscillation start time | T _{PLL} | V _{DD} = 1.6 to 5.5V | — | — | 2 | ms | |
| 1kHz Low-speed RC oscillator (for WDT) frequency accuracy | f _{RC1K} | Ta= -40 to +105°C V _{DD} = 1.6 to 5.5V | 0.5 | 1 | 2.5 | kHz | |

Input / Output pin 1

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring circuit |
|--|--------|---|-------------------------------------|------|------|------|-------------------|
| Output voltage1 “H”/“L” level (P00-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7) | VOH1 | IOH1=-10mA V _{DD} ≥4.5V | V _{DD} -1.5 | — | — | V | 2 |
| | | IOH1=-1mA V _{DD} ≥1.6V | V _{DD} -0.5 | — | — | | |
| | VOL1 | IOL1=+10mA V _{DD} ≥4.5V | — | — | 1.5 | | |
| | | IOL1=+1mA V _{DD} ≥1.6V | — | — | 0.5 | | |
| Output voltage2 “L” level (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7) | VOL2 | When Nch open drain output mode is selected | IOL2=+15mA V _{DD} ≥4.5V | — | — | 0.7 | |
| | | | IOL2=+8mA V _{DD} ≥3.0V | — | — | 0.5 | |
| | | | IOL2=+3mA V _{DD} ≥2.0V | — | — | 0.4 | |
| | | | IOL2=+2mA V _{DD} ≥1.6V | — | — | 0.4 | |

Input / Output pin 2

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring circuit |
|---|--------|---|-----------------------|---------|------|------|-------------------|
| “H” level output current1 *6 | IOH1 | 1pin | V _{DD} ≥4.5V | -10*3*5 | — | — | mA |
| | | | V _{DD} ≥1.6V | -1*3*5 | — | — | |
| “H” level output total current *1*4 | IOH3 | Total of ‘P00-P07, P10-P13, P44-P47, P50-P53, P70-P76, P80-P87, P90-P97, PA0’ or ‘P14-P17, P20-P27, P30-P33, P40-P43, P54-P57 P60-P67,P77, PA1-PA7, PB0-PB7’ (duty≤50%) | V _{DD} ≥4.5V | -90*5 | — | — | |
| | | | V _{DD} ≥1.6V | -20*5 | — | — | |
| | | All pin total (duty≤50%) | V _{DD} ≥4.5V | -180*5 | — | — | |
| | | | V _{DD} ≥1.6V | -40*5 | — | — | |
| “L” level output current1 *6 | IOL1 | 1pin (CMOS output mode) | V _{DD} ≥4.5V | — | — | 10*3 | |
| | | | V _{DD} ≥1.6V | — | — | 1*3 | |
| “L” level output current2 *6 | IOL2 | 1pin (Nch open drain output mode) | V _{DD} ≥4.5V | — | — | 15*3 | |
| | | | V _{DD} ≥3.0V | — | — | 8*3 | |
| | | | V _{DD} ≥2.0V | — | — | 3*3 | |
| | | | V _{DD} ≥1.6V | — | — | 2*3 | |
| “L” level output total current *2*4 | IOL3 | Total of P00-P07, P10-P13, P44-P47, P50-P53, P70-P76, P80-P87, P90-P97, PA0’ or ‘P14~P17, P20-P27, P30-P33, P40-P43, P54-P57 P60-P67,P77, PA1-PA7, PB0-PB7’ (Nch open drain output mode,duty≤50%) | V _{DD} ≥4.5V | — | — | 90 | |
| | | | V _{DD} ≥3.0V | — | — | 40 | |
| | | | V _{DD} ≥2.0V | — | — | 15 | |
| | | | V _{DD} ≥1.6V | — | — | 10 | |
| | | All pin total (Nch open drain output mode,duty≤50%) | V _{DD} ≥4.5V | — | — | 180 | |
| | | | V _{DD} ≥1.6V | — | — | 20 | |
| Output leak (P00-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7) | IOOH | VOH=V _{DD} (High impedance mode) | — | — | +1 | μA | |
| | IOL | VOL=V _{SS} (High impedance mode) | -1*5 | — | — | | |

3

- *¹ Sink-out current from V_{DD} to the output pin, which can guarantee the device operation.
- *² Sink-in current from the output pin to V_{SS} , which can guarantee the device operation.
- *³ Do not beyond total current.
- *⁴ The total current is on the condition of Duty \leq 50%(same applies to IOH1).
When the duty $>$ 50% the total current is calculated by following formula.
Total current = $IOL3 \times 50/n$ (When the duty is n%)
<For an example> When $IOL3=100mA$ and $n=80\%$,
Total current = $IOL3 \times 50/80 = 62.5mA$
Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.
Do not apply current larger than Absolute Maximum Ratings.
- *⁵ The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
- *⁶ These values are satisfied with VOH1, VOL1 and VOL2.

Input / Output pin 3

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring circuit |
|--|-------------------------------|--|--------------------------|--------------------------|---------------------------|-----------------|-------------------|
| Input current1 (RESET_N) | I _{IH1} | V _{IH1} =V _{DD} | — | — | 1 | μA | 4 |
| | I _{IL1} | V _{IL1} =V _{SS} | -1 ^{*1} | — | — | | |
| Input current2 (P00/TEST0) | I _{IL2} | V _{IL2} =V _{SS} (pull-up mode) ^{*2} | -1500 ^{*1} | -300 ^{*1} | -20 ^{*1} | kΩ | |
| | V/I _{IL2} | V _{IL2} =V _{SS} (pull-up mode) ^{*2} | 3.7 | 10 | 80 | μA | |
| | I _{IH2Z} | V _{IH2} =V _{DD} (High impedance mode) | — | — | 1 | | |
| Input current3 (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7) | I _{IL2Z} | V _{IL2} =V _{SS} (High impedance mode) | -1 ^{*1} | — | — | μA | |
| | I _{IL3} | V _{IL1} =V _{SS} (pull-up mode) ^{*2} | -250 ^{*1} | -30 ^{*1} | -2 ^{*1} | | |
| | V/I _{IL3} | V _{IL1} =V _{SS} (pull-up mode) ^{*2} | 22 | 100 | 800 | kΩ | |
| | I _{IH3Z} | V _{IH1} =V _{DD} (High impedance mode) | — | — | 1 | μA | |
| Input current4 (PI00-PI01) | I _{IL3Z} | V _{IL1} =V _{SS} (High impedance mode) | -1 ^{*1} | — | — | | |
| | I _{IH4} | V _{IH1} =V _{DD} | — | — | 1 | V | |
| Input voltage1 (RESET_N) (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7) (PI00-PI01) | I _{IL4} | V _{IL1} =V _{SS} | -1 ^{*1} | — | — | | |
| | Input voltage2 (P00/TEST0) | V _{IH1} | — | 0.7 x V _{DD} | — | V _{DD} | 5 |
| V _{IL1} | | — | 0 | — | 0.3 x V _{DD} | | |
| Pin capacitance (RESET_N) (P00/TEST0) (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7) (PI00-PI01) | V _{IH2} | — | 0.7 x V _{DD} | — | V _{DD} | pF | |
| | V _{IL2} | — | 0 | — | 0.25 x V _{DD} | | |
| CPIN | CPIN | f = 10kHz Ta = +25°C | — | — | 10 | — | |

^{*1} The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value. For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

^{*2} Measurement conditions: Typ. : V_{DD} = 3.0V, Max. : V_{DD} = 1.6V, Min. : V_{DD} = 5.5V

Synchronous Serial Port

Slave mode

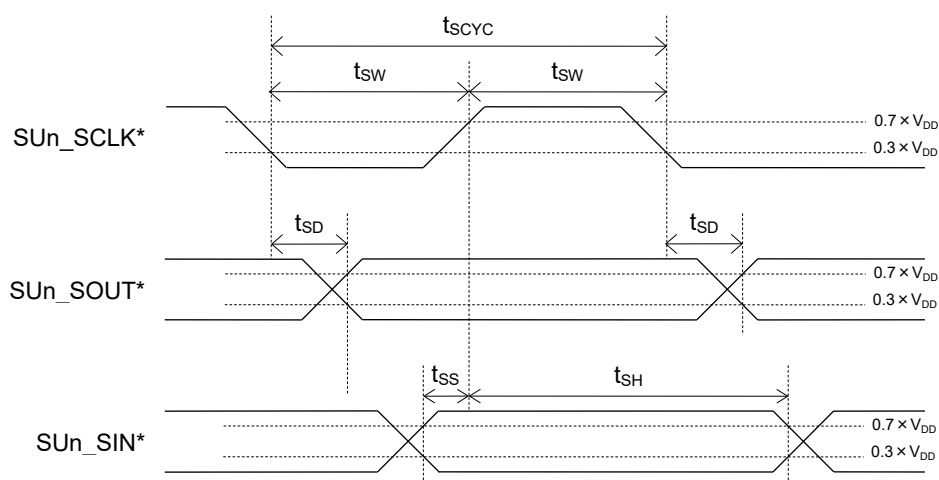
($V_{DD}=1.8$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------------|------------|------------------------|--------------------------|------|---------------------------|---------|
| SCK input cycle | t_{SCYC} | — | 1 ^{*2} | — | — | μs |
| SCK input pulse width | t_{SW} | — | 0.5 ^{*3} | — | — | μs |
| SOUT output delay time | t_{SD} | $V_{DD}=2.4$ to $5.5V$ | — | — | $100+HSCLK^{*1} \times 3$ | ns |
| | | $V_{DD}=1.8$ to $5.5V$ | — | — | $200+HSCLK^{*1} \times 3$ | ns |
| SIN input setup time | t_{SS} | — | $HSCLK^{*1} \times 1$ | — | — | ns |
| SIN input hold time | t_{SH} | — | $80+HSCLK^{*1} \times 3$ | — | — | ns |

*1 Cycle of high speed clock

*2 Need input cycles of HSLCK x8 or longer

*3 Need input cycles of HSLCK x4 or longer



* 2nd to 8th function of port, n=0 to 5

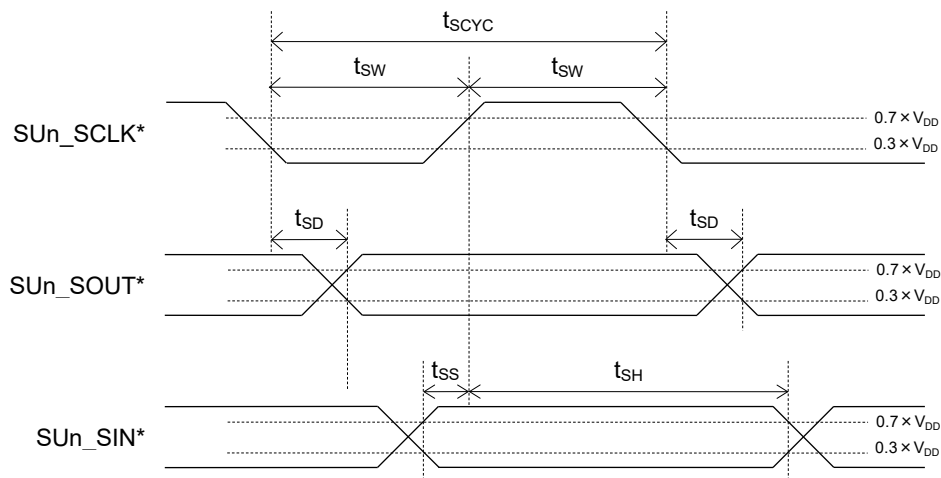
Master mode

($V_{DD}=1.8$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------------|------------|------------------------|------------------------|------------------------|------------------------|------|
| SCK output cycle | t_{SCYC} | — | — | $SCLK^{*1}$ | — | ns |
| SCK output pulse width | t_{SW} | — | $SCLK^{*1} \times 0.4$ | $SCLK^{*1} \times 0.5$ | $SCLK^{*1} \times 0.6$ | ns |
| SOUT output delay time | t_{SD} | $V_{DD}=2.4$ to $5.5V$ | — | — | 100 | ns |
| | | $V_{DD}=1.8$ to $5.5V$ | — | — | 160 | ns |
| SIN input setup time | t_{SS} | $V_{DD}=2.4$ to $5.5V$ | 120 | — | — | ns |
| | | $V_{DD}=1.8$ to $5.5V$ | 180 | — | — | ns |
| SIN input hold time | t_{SH} | $V_{DD}=2.4$ to $5.5V$ | 80 | — | — | ns |
| | | $V_{DD}=1.8$ to $5.5V$ | 100 | — | — | ns |

*1 Clock cycle selected by bit12~8(SnCK4~0) of the serial port n mode register (SIO nMOD)

$V_{DD} \geq 2.4V$: min250ns , $V_{DD} \geq 1.8V$: min500ns



* 2nd to 8th function of port, n=0 to 5

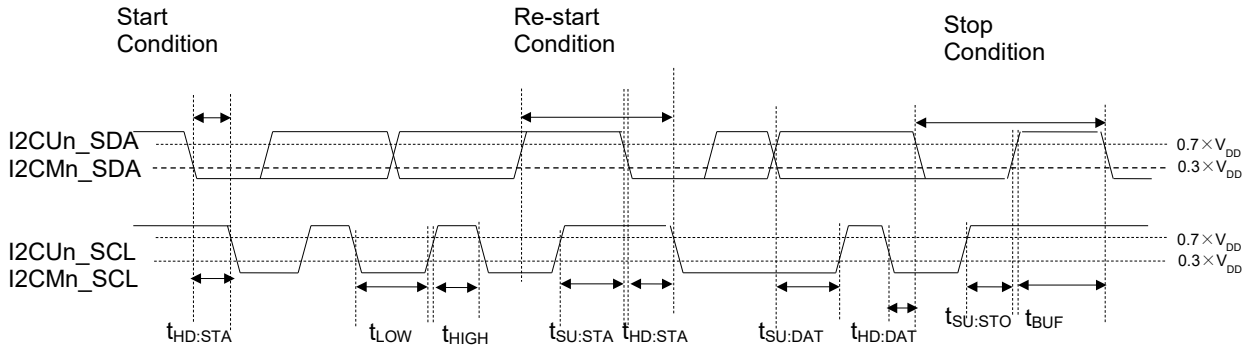
I²C Bus Interface

Standard Mode (100kbit/s)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--|---------------------|-----------|------|------|------|------|
| SCL clock frequency | f _{SCL} | — | 0 | — | 100 | kHz |
| SCL hold time (start/restart condition) | t _{HD:STA} | — | 4.0 | — | — | μs |
| SCL "L" level time | t _{LOW} | — | 4.7 | — | — | μs |
| SCL "H" level time | t _{HIGH} | — | 4.0 | — | — | μs |
| SCL setup time (restart condition) | t _{SU:STA} | — | 4.7 | — | — | μs |
| SDA hold time | t _{HD:DAT} | — | 0 | — | — | μs |
| SDA setup time | t _{SU:DAT} | — | 0.25 | — | — | μs |
| SDA setup time (stop condition) | t _{SU:STO} | — | 4.0 | — | — | μs |
| Bus-free time | t _{BUF} | — | 4.7 | — | — | μs |

When using the I²C as the master, configure the I²C master n mode register(I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



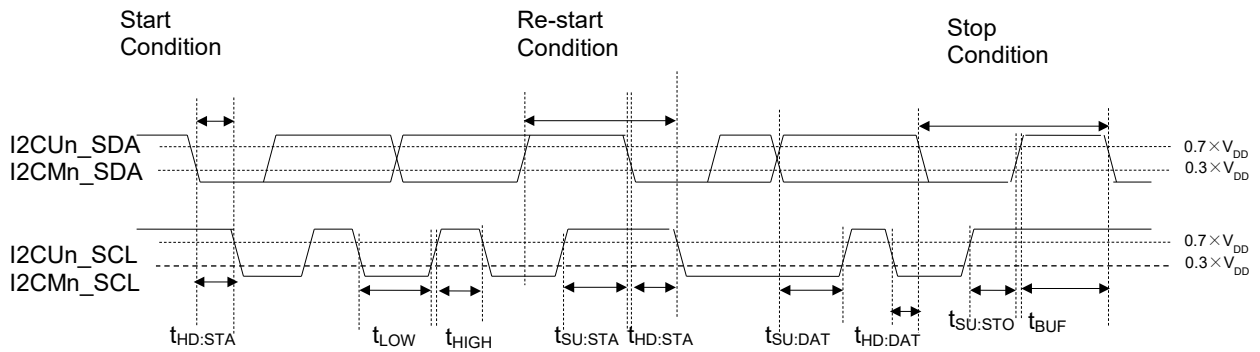
n: 0 to 1

Fast Mode (400 kbit/s)

($V_{DD}=1.8$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|--------------|-----------|------|------|------|---------|
| SCL clock frequency | f_{SCL} | — | 0 | — | 400 | kHz |
| SCL hold time (start/restart condition) | $t_{HD:STA}$ | — | 0.6 | — | — | μs |
| SCL "L" level time | t_{LOW} | — | 1.3 | — | — | μs |
| SCL "H" level time | t_{HIGH} | — | 0.6 | — | — | μs |
| SCL setup time (restart condition) | $t_{SU:STA}$ | — | 0.6 | — | — | μs |
| SDA hold time | $t_{HD:DAT}$ | — | 0 | — | — | μs |
| SDA setup time | $t_{SU:DAT}$ | — | 0.1 | — | — | μs |
| SDA setup time (stop condition) | $t_{SU:STO}$ | — | 0.6 | — | — | μs |
| Bus-free time | t_{BUF} | — | 1.3 | — | — | μs |

When using the I²C as the master, configure the I²C master n mode register(I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



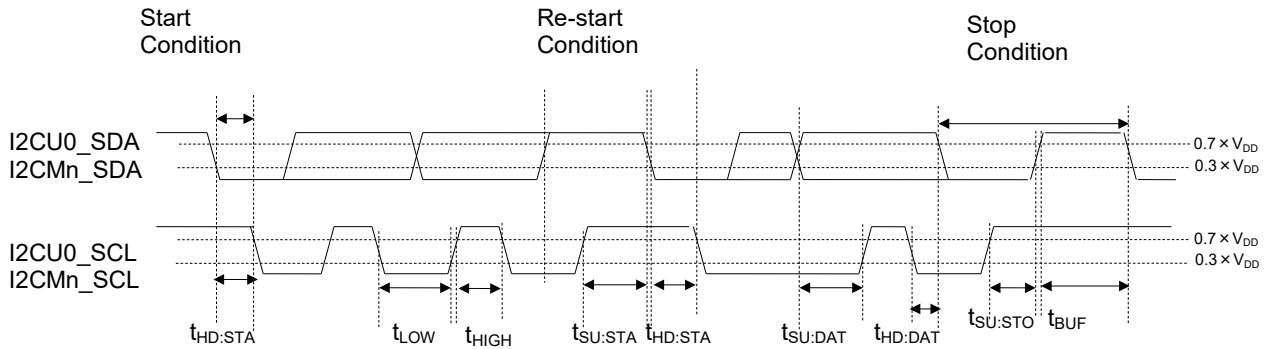
n:0 to 1

1Mbps Mode (1M bit/s)

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--|--------------|-----------|------|------|------|---------|
| SCL clock frequency | f_{SCL} | — | 0 | — | 1000 | kHz |
| SCL hold time (start/restart condition) | $t_{HD:STA}$ | — | 0.26 | — | — | μs |
| SCL "L" level time | t_{LOW} | — | 0.5 | — | — | μs |
| SCL "H" level time | t_{HIGH} | — | 0.26 | — | — | μs |
| SCL setup time (restart condition) | $t_{SU:STA}$ | — | 0.26 | — | — | μs |
| SDA hold time | $t_{HD:DAT}$ | — | 0 | — | — | μs |
| SDA setup time | $t_{SU:DAT}$ | — | 0.1 | — | — | μs |
| SDA setup time (stop condition) | $t_{SU:STO}$ | — | 0.26 | — | — | μs |
| Bus-free time | t_{BUF} | — | 0.5 | — | — | μs |

When using the I²C as the master, configure the I²C master n mode register(I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



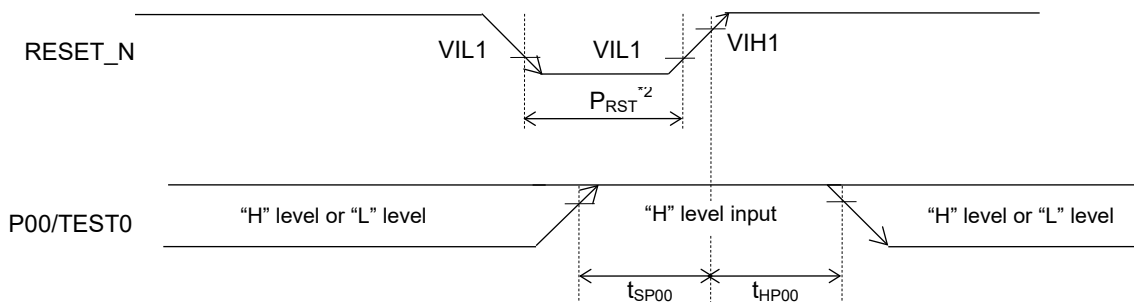
n: 0 to 1

Reset

($V_{DD}=1.6$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring circuit |
|---------------------------------------|-----------------|-----------|------|------|------|------|-------------------|
| Reset pulse width | P_{RST} | — | 2 | — | — | ms | 1 |
| P00 "H" level setup time | t_{SP00} | — | 1 | — | — | ms | |
| P00 "H" level hold time ^{*1} | t_{HP00}^{*1} | — | 1 | — | — | ms | |

^{*1}: except ISP mode. Refer to the User's manual "25.4 In-System Programming Function" for the timing in ISP mode.



^{*2}: $V_{DD}=1.6V$ or over at power on.

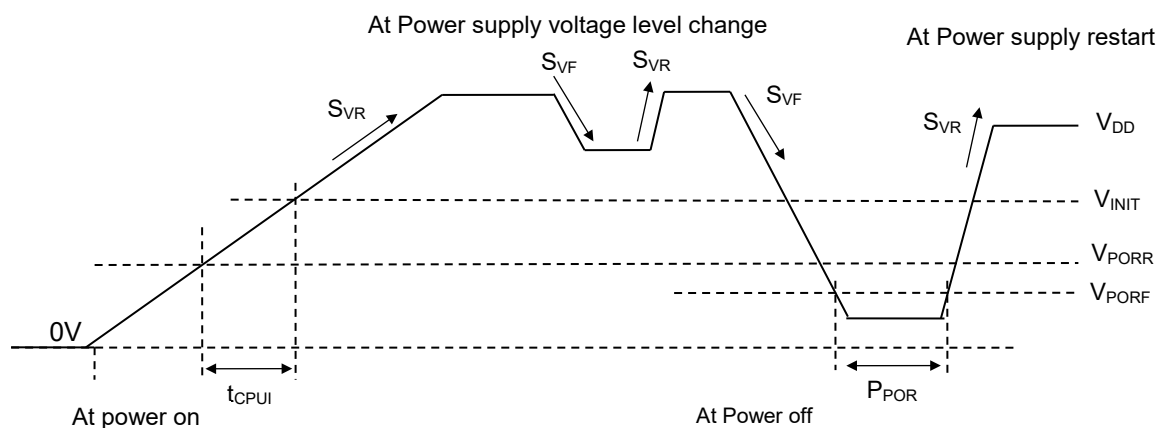
Note:

- RESET_N input shorter pulse than the Reset pulse width (P_{RST}) valid time should be avoided. The shorter pulse input may cause unexpected behavior.

Slope of Power supply and Power On Reset

($V_{SS} = 0V$, $T_a = -40$ to $+105^\circ C$, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring circuit |
|---|------------|-------------------------|------|------|------|---------|-------------------|
| Power on rising slope | S_{VR} | — | — | — | 60 | V/ms | 1 |
| Power on falling slope | S_{VF} | — | — | — | 2 | V/ms | |
| Power on reset detection voltage | V_{PORR} | At Power up (rising) | 1.47 | 1.57 | 1.80 | V | |
| | V_{PORF} | At Power down (falling) | 1.33 | 1.49 | 1.58 | V | |
| Power on reset minimum pulse width | P_{POR} | — | 200 | — | — | μs | |
| Power on voltage | V_{INIT} | At power on | 1.8 | — | — | V | |
| CPU operation start time (from the release of reset to the CPU starts to run) | t_{CPU} | — | 11 | 16 | — | ms | — |



Note:

- If a pulse shorter than the Power on reset minimum pulse width is asserted to V_{DD} , it may cause the MCU malfunction. Apply prevent measurement such as bypass capacitors or external reset input, and so on.
- Start the high-speed clock when the V_{DD} is within the operating voltage.

VLS

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit | Measuring circuit |
|--------------------------------------|-------------------|-----------------------|---------|------|------|------|------|-------------------|
| | | VLS0LV * ¹ | | | | | | |
| VLS threshold voltage * ² | V _{VLSR} | 00H | Rising | 3.86 | 4.06 | 4.26 | V | 1 |
| | V _{VLSF} | | Falling | 3.84 | 4.00 | 4.16 | | |
| | V _{VLSR} | 01H | Rising | 3.57 | 3.76 | 3.95 | | |
| | V _{VLSF} | | Falling | 3.55 | 3.70 | 3.85 | | |
| | V _{VLSR} | 02H | Rising | 2.94 | 3.11 | 3.28 | | |
| | V _{VLSF} | | Falling | 2.92 | 3.05 | 3.18 | | |
| | V _{VLSR} | 03H | Rising | 2.85 | 3.01 | 3.17 | | |
| | V _{VLSF} | | Falling | 2.83 | 2.95 | 3.07 | | |
| | V _{VLSR} | 04H | Rising | 2.75 | 2.91 | 3.07 | | |
| | V _{VLSF} | | Falling | 2.73 | 2.85 | 2.97 | | |
| | V _{VLSR} | 05H | Rising | 2.66 | 2.81 | 2.96 | | |
| | V _{VLSF} | | Falling | 2.64 | 2.75 | 2.86 | | |
| | V _{VLSR} | 06H | Rising | 2.56 | 2.71 | 2.86 | | |
| | V _{VLSF} | | Falling | 2.54 | 2.65 | 2.76 | | |
| | V _{VLSR} | 07H | Rising | 2.46 | 2.61 | 2.76 | | |
| | V _{VLSF} | | Falling | 2.44 | 2.55 | 2.66 | | |
| | V _{VLSR} | 08H | Rising | 2.37 | 2.51 | 2.65 | | |
| | V _{VLSF} | | Falling | 2.35 | 2.45 | 2.55 | | |
| | V _{VLSR} | 09H | Rising | 1.98 | 2.11 | 2.24 | | |
| | V _{VLSF} | | Falling | 1.96 | 2.05 | 2.14 | | |
| V _{VLSR} | 0AH | Rising | 1.89 | 2.01 | 2.13 | | | |
| V _{VLSF} | | Falling | 1.87 | 1.95 | 2.03 | | | |
| V _{VLSR} | 0BH | Rising | 1.79 | 1.91 | 2.03 | | | |
| V _{VLSF} | | Falling | 1.77 | 1.85 | 1.93 | | | |
| VLS Current | I _{VLS} | — | | — | 50 | — | nA | |

*¹ Bit3~Bit0 of voltage level detection circuit 0 level register (VLS0LV).*² The Data VLS0LV = 0CH~0FH is not available to use, if the data is specified it will the same spec as that 0BH is specified.

Analog Comparator

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring circuit |
|---|--------------------|---------------------------------|------|------|-------------------------|------|-------------------|
| Comparator same phase input voltage range | V _{CMR} | — | 0.1 | — | V _{DD} -1.5 | V | 1 |
| Comparator0 input offset | V _{CMOF} | Ta=+25°C, V _{DD} =5.0V | — | 5 | — | mV | |
| Comparator Reference Voltage | V _{CMREF} | — | 0.75 | 0.8 | 0.85 | V | |

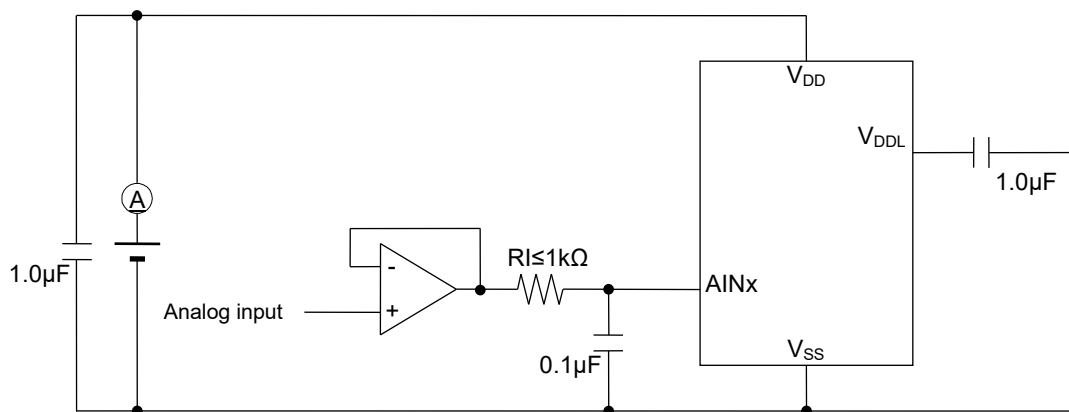
Successive Approximation Type A/D Converter

($V_{DD}=1.8$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|------------|---|------|------|----------|---------|
| Resolution | n_{AD} | — | — | — | 10 | bit |
| Overall error | — | $4.5V \leq \text{Reference voltage}^{*1} \leq 5.5V$ | -3.5 | 1.2 | 3.5 | LSB |
| Integral non-linearity error | INL_{AD} | $2.7V \leq \text{Reference voltage}^{*1} \leq 5.5V$ | -4 | — | 4 | |
| | | $2.2V \leq \text{Reference voltage}^{*1} < 2.7V$ | -6 | — | 6 | |
| | | $1.8V \leq \text{Reference voltage}^{*1} < 2.2V$ | -10 | — | 10 | |
| | | Reference voltage = Internal reference voltage (V_{REFI}) | -15 | — | 15 | |
| Differential non-linearity error | DNL_{AD} | $2.7V \leq \text{Reference voltage}^{*1} \leq 5.5V$ | -3 | — | 3 | |
| | | $2.2V \leq \text{Reference voltage}^{*1} < 2.7V$ | -5 | — | 5 | |
| | | $1.8V \leq \text{Reference voltage}^{*1} < 2.2V$ | -9 | — | 9 | |
| | | Reference voltage = Internal reference voltage (V_{REFI}) | -14 | — | 14 | |
| Zero-scale error | ZSE | $R_I \leq 1k\Omega$ | -6 | — | 6 | |
| Full-scale error | FSE | $R_I \leq 1k\Omega$ | -6 | — | 6 | |
| A/D reference voltage | V_{REF} | — | 1.8 | — | V_{DD} | V |
| Internal reference voltage | V_{REFI} | — | 1.5 | 1.55 | 1.6 | |
| Conversion time | t_{CONV} | $4.5V \leq V_{DD} \leq 5.5V$ | 2.25 | — | 427 | μs |
| | | $2.2V \leq V_{DD} \leq 5.5V$ | 4.5 | — | 427 | |
| | | $1.8V \leq V_{DD} \leq 5.5V$ | 18 | — | 427 | |

*1 : V_{DD} or P23/ V_{REF} is selected for the reference voltage of Successive Approximation Type A/D Converter by setting bit5(V_{REFP1}) and bit4(V_{REFP0}) of Reference voltage control register(V_{REFCON}).

The current flows during the ADC sampling as it takes charging. Make the output impedance of the analog signal source $1k\Omega$ or smaller. Also, putting $0.1\mu F$ capacitor on the ADC input pin is recommended to reduce the noise.



D/A Converter

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|-------------------|---|------|------|------|------|
| Resolution | n _{DA} | — | — | — | 8 | bit |
| Conversion cycle | tc | — | 10 | — | — | μs |
| Integral non-linearity error | INL _{DA} | RL=4MΩ | -2 | — | 2 | LSB |
| Differential non-linearity error | DNL _{DA} | RL=4MΩ | -1 | — | 1 | |
| Output impedance | R _o | DACEN bit of D/A converter enable register =1 | 3 | 6 | 9 | kΩ |

Reference Voltage Output

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

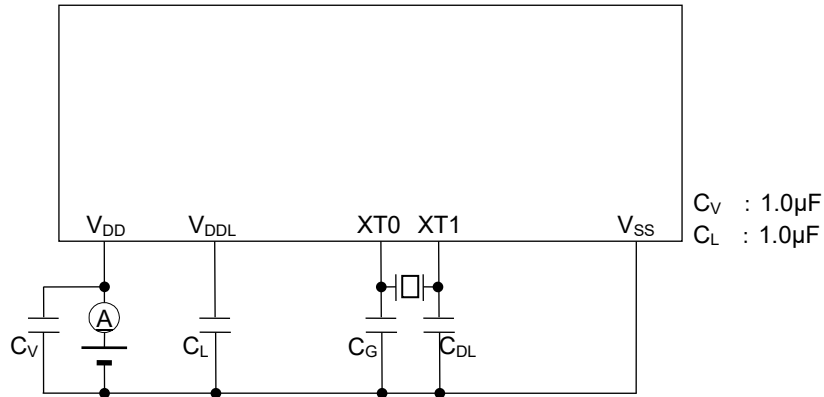
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------|--------------------|-----------|------|------|------|------|
| Output voltage | V _{REFO} | — | — | 1.55 | — | V |
| Output impedance | R _{VREFO} | — | — | — | 500 | kΩ |

Flash Memory

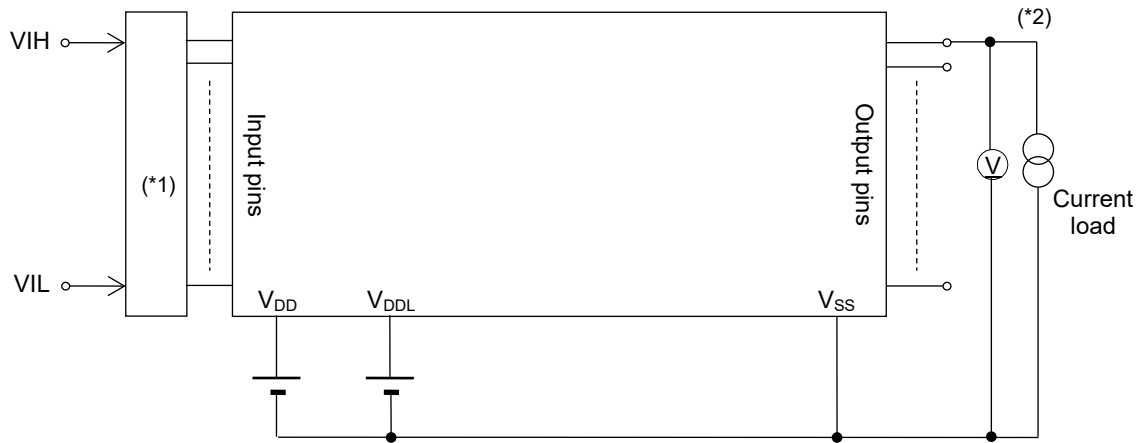
(V_{SS}= 0V)

| Parameter | Symbol | Condition | Range | Unit | |
|-----------------------|-----------------|-----------------------------------|---------------|----------|---|
| Operating temperature | T _{OP} | Data flash memory, At write/erase | -40 to +85 | °C | |
| | | Flash ROM, At write/erase | 0 to +40 | | |
| Operating voltage | V _{DD} | At write/erase | +1.8 to +5.5 | V | |
| Maximum rewrite count | CEPD | Data Flash | 10000 | times | |
| | CEPP | Program Flash | 100 | | |
| Erase unit | — | Block erase | Program Flash | 16K | B |
| | | | Data Flash | all area | |
| | — | Sector erase | Program Flash | 1K | B |
| | | | Data Flash | 128 | |
| Erase time (Max.) | — | Block erase / Sector erase | 50 | ms | |
| Write unit | — | Program Flash | 4 | B | |
| | | Data Flash | 1 | | |
| Write time (Max.) | — | Program Flash | 80 | μs | |
| | — | Data Flash | 40 | | |
| Data retention period | YDR | — | 15 | years | |

Measuring circuit
Measuring circuit 1

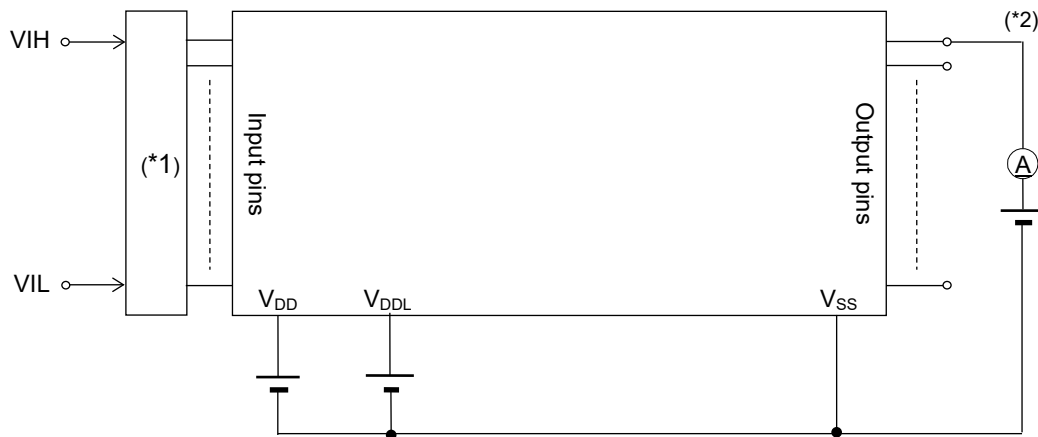


Measuring circuit 2



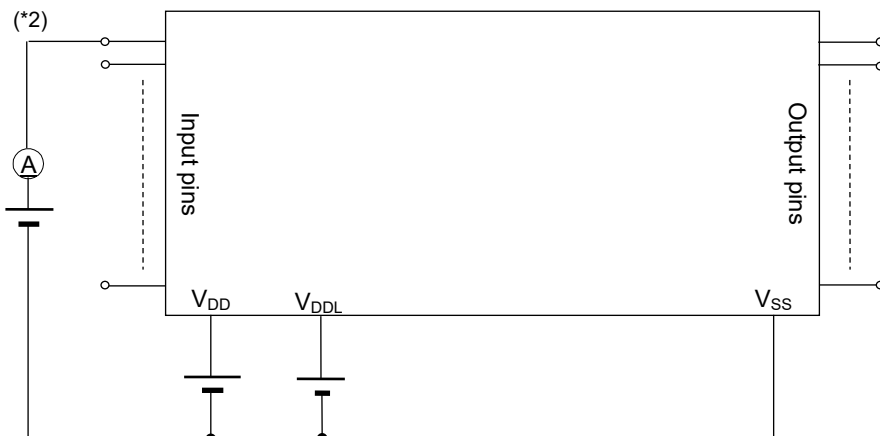
(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

Measuring circuit 3



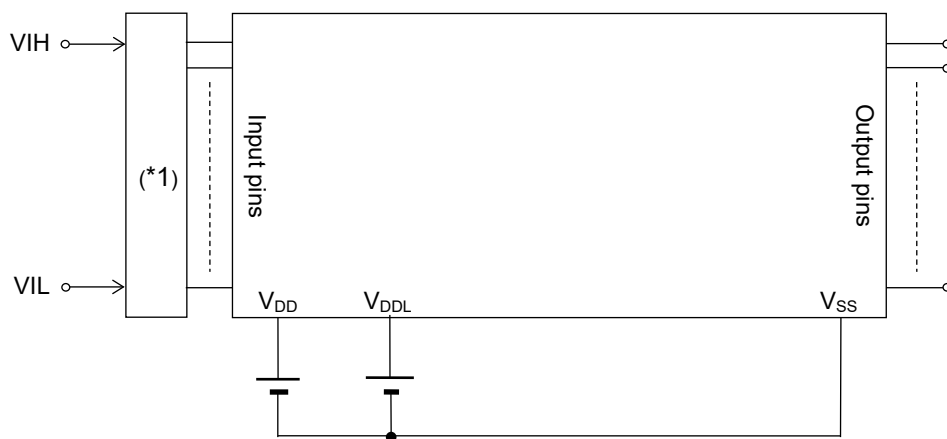
(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

Measuring circuit 4



(*)2 Measured connecting specified pins

Measuring circuit 5

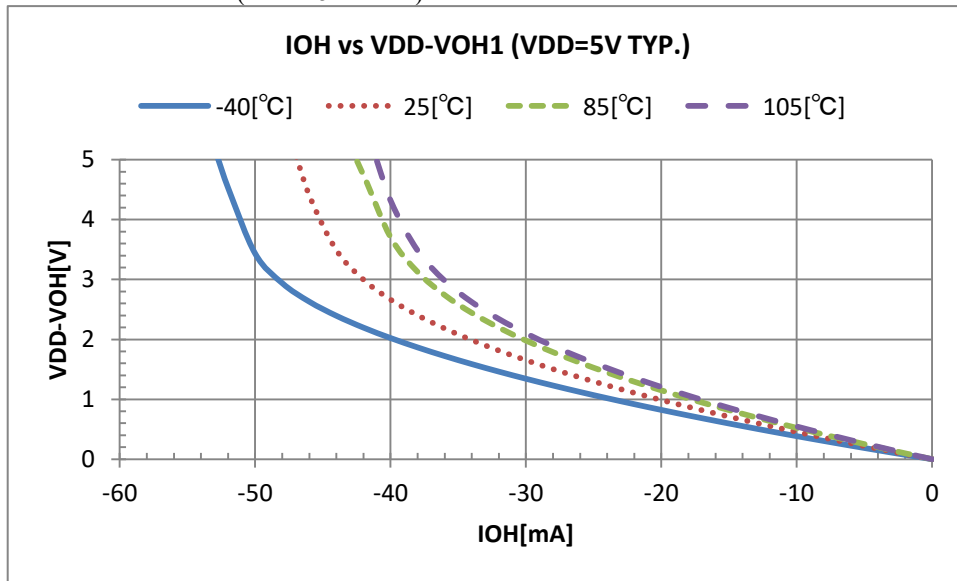


(*)1 Input logic circuit to determine the specified measuring conditions

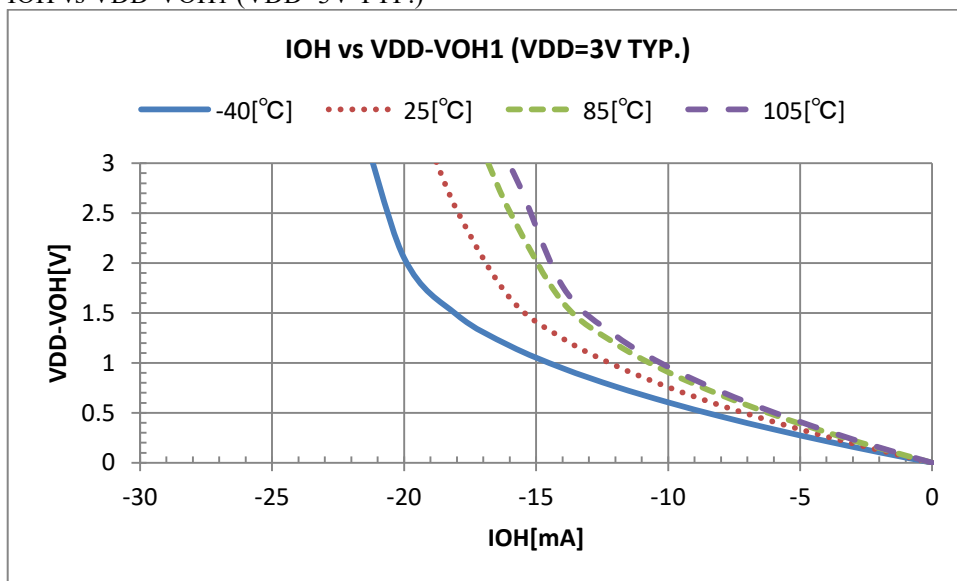
Characteristics graphs

These Graphs on the following pages are references for designing an application.

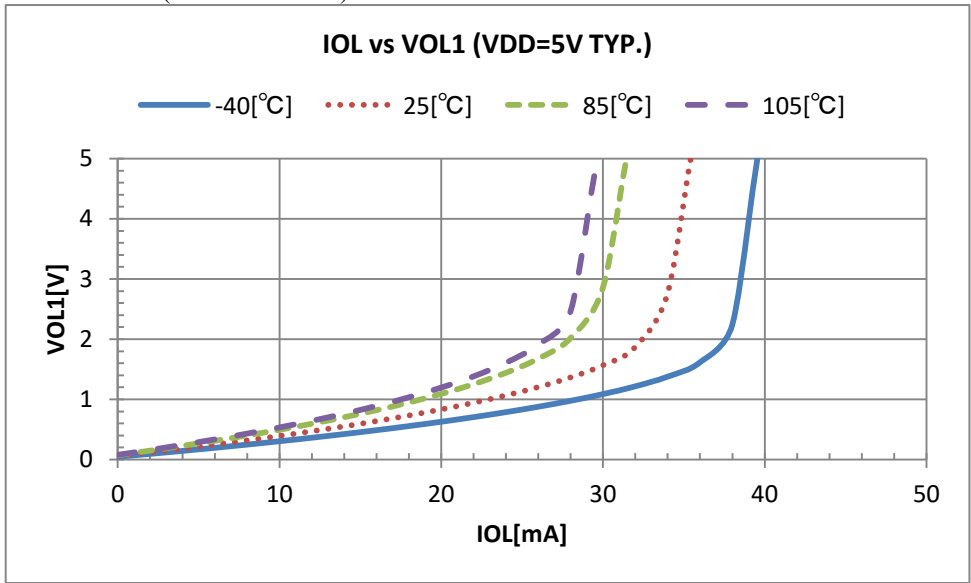
IOH vs VDD-VOH1 (VDD=5V TYP.)



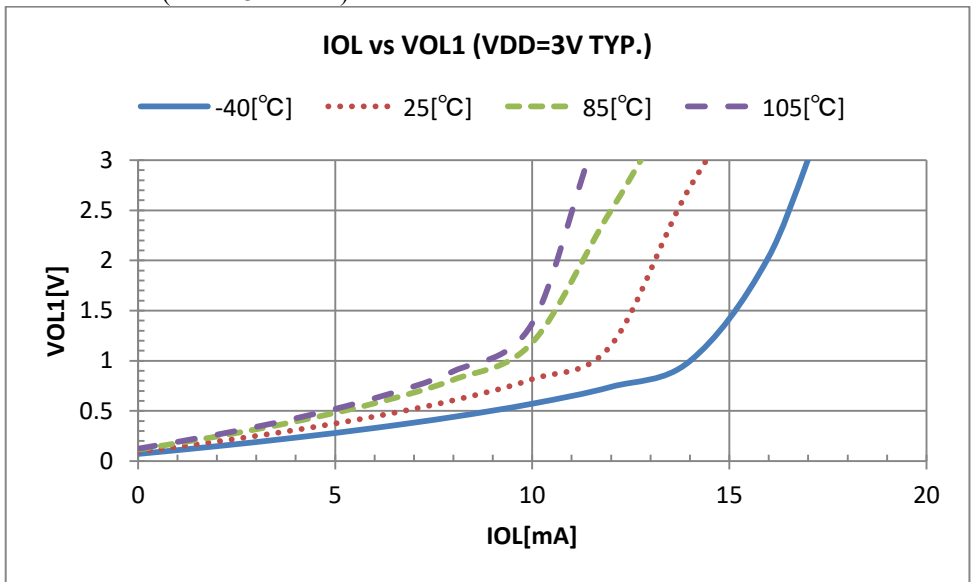
IOH vs VDD-VOH1 (VDD=3V TYP.)



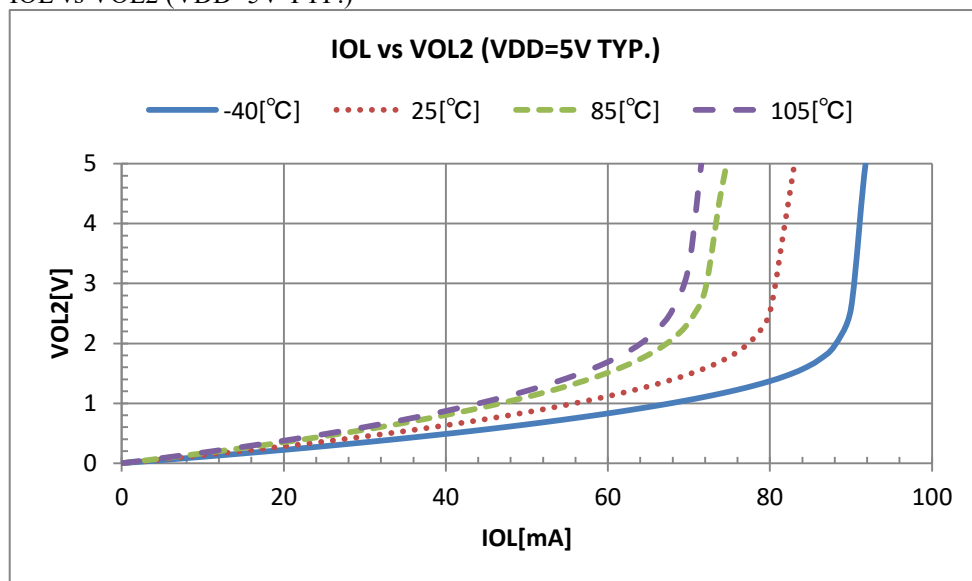
IOL vs VOL1 (VDD=5V TYP.)



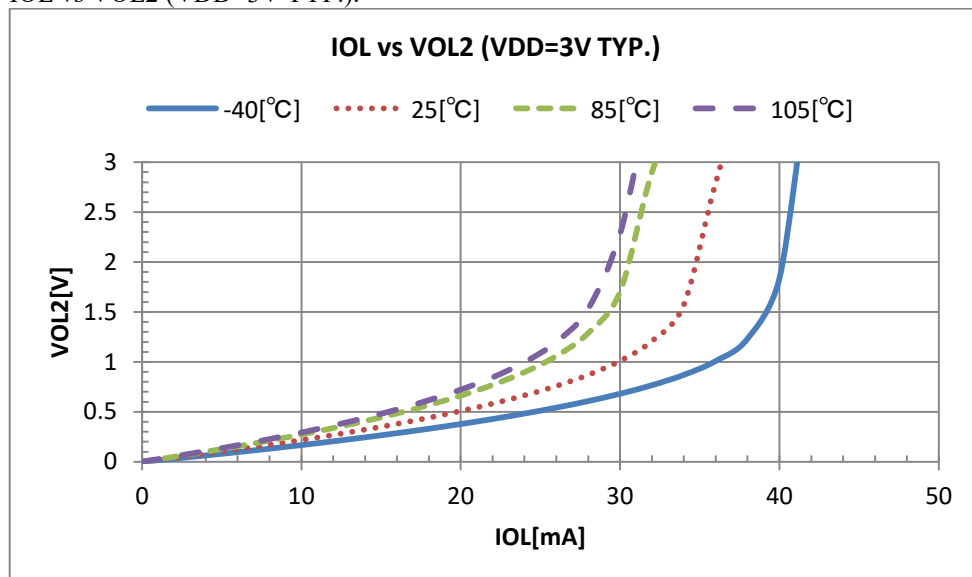
IOL vs VOL1 (VDD=3V TYP.)



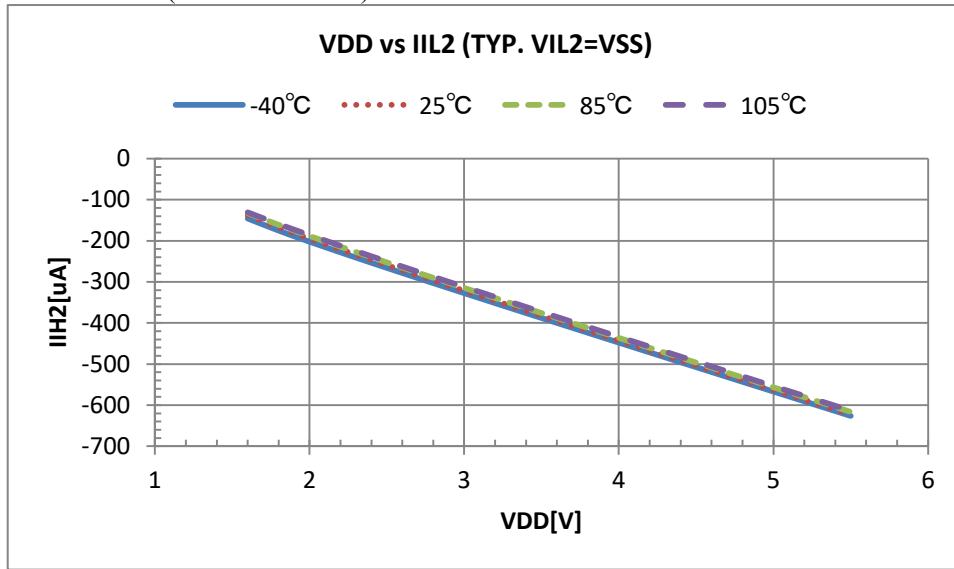
IOL vs VOL2 (VDD=5V TYP.)



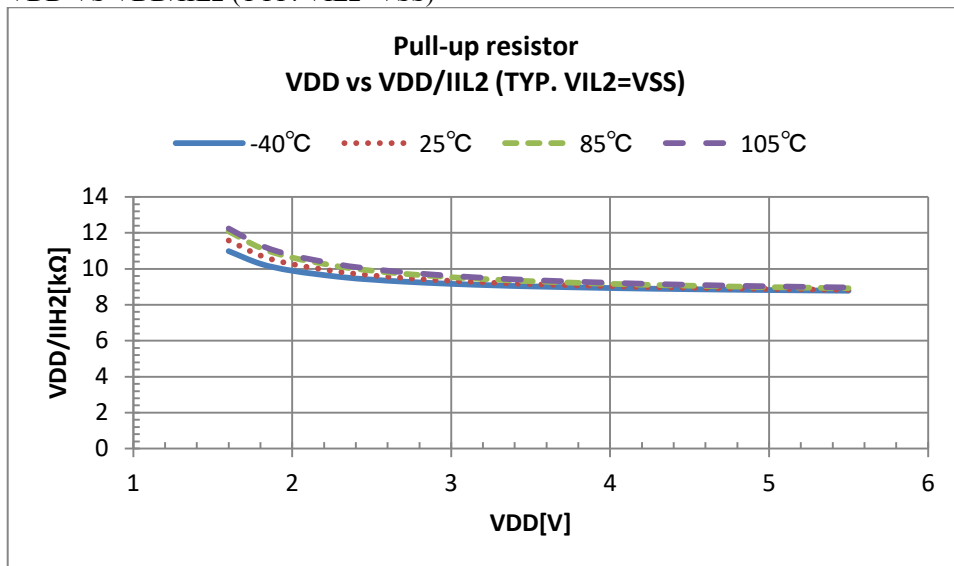
IOL vs VOL2 (VDD=3V TYP.).



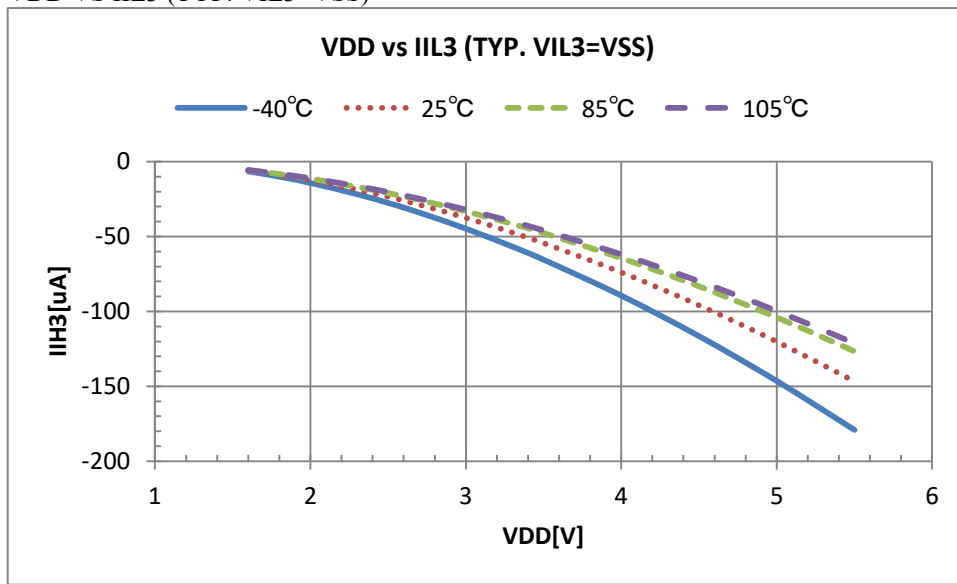
VDD VS IIL2 (TYP. VIL2=VSS)



Pull-up resistor
VDD VS VDD/IIL2 (TYP. VIL2=VSS)

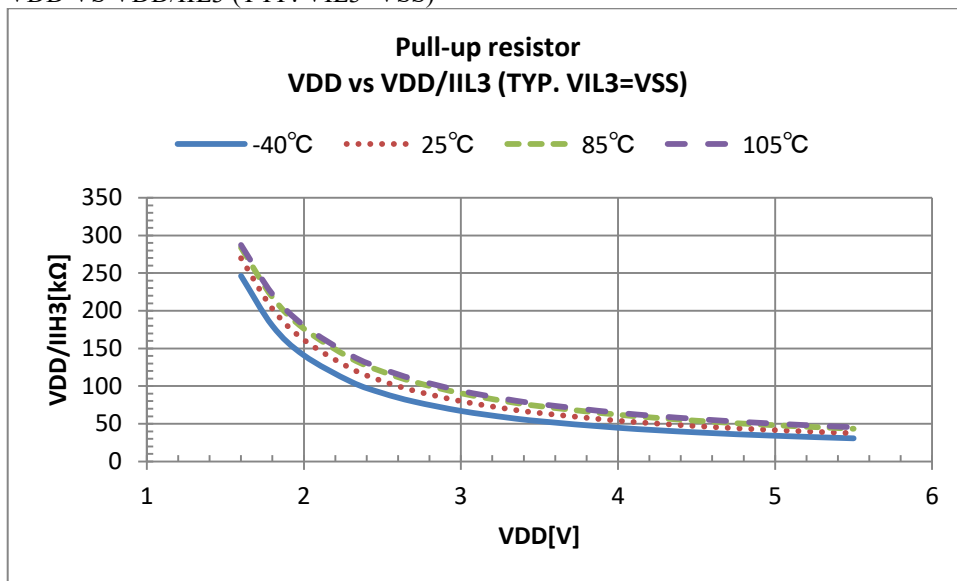


VDD VS IIL3 (TYP. VIL3=VSS)



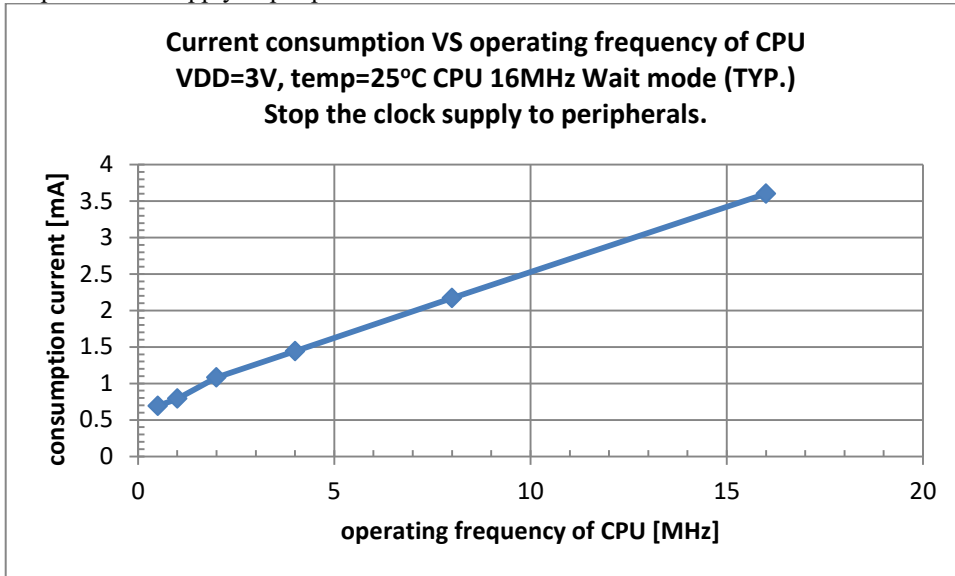
Pull-up resistor

VDD VS VDD/IIL3 (TYP. VIL3=VSS)

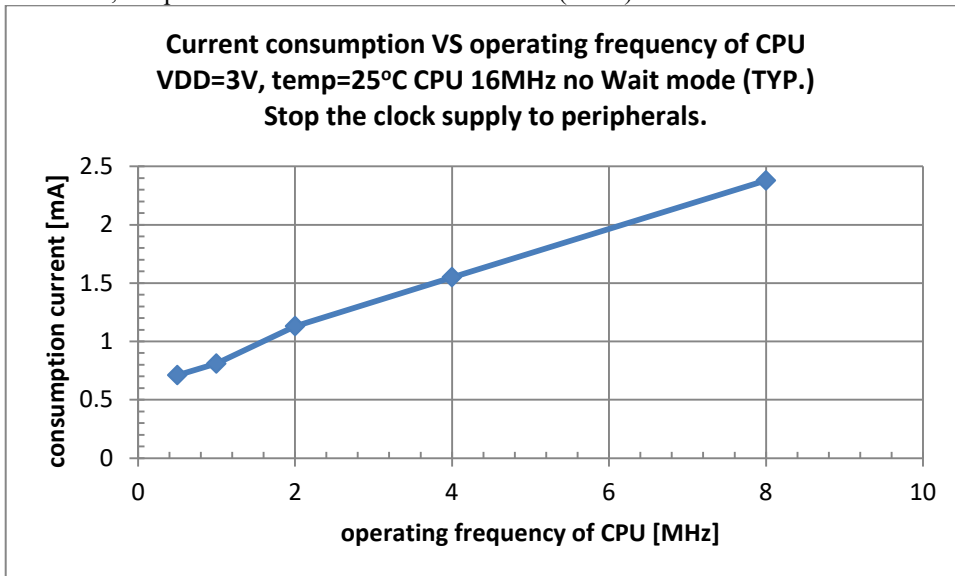


Product: ML62Q1530, ML62Q1531, ML62Q1532, ML62Q1533, ML62Q1534, ML62Q1540, ML62Q1541, ML62Q1542, ML62Q1543, ML62Q1544, ML62Q1550, ML62Q1551, ML62Q1552, ML62Q1553, ML62Q1554

Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 16MHz Wait mode (TYP.)
Stop the clock supply to peripherals.

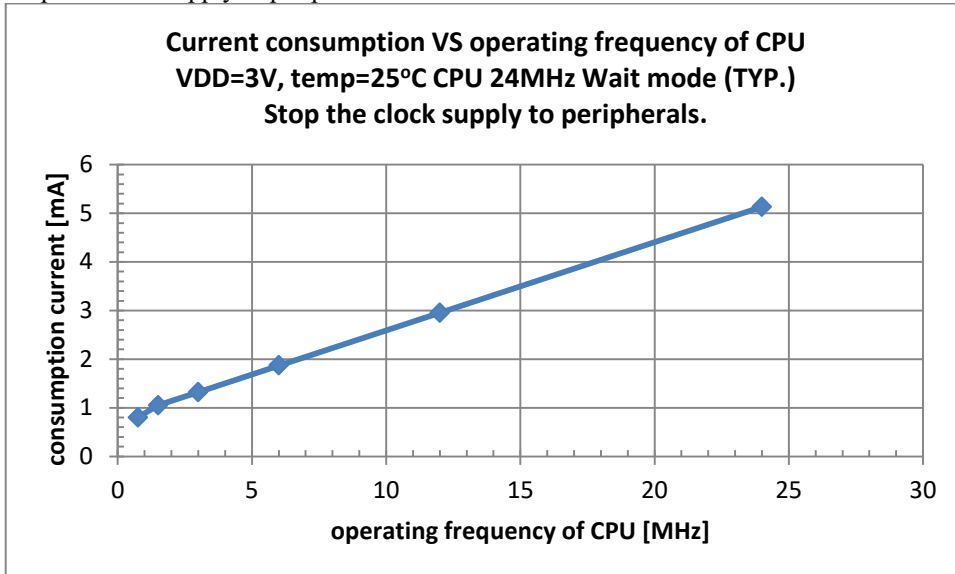


VDD=3V, temp=25°C CPU 16MHz no Wait mode (TYP.)

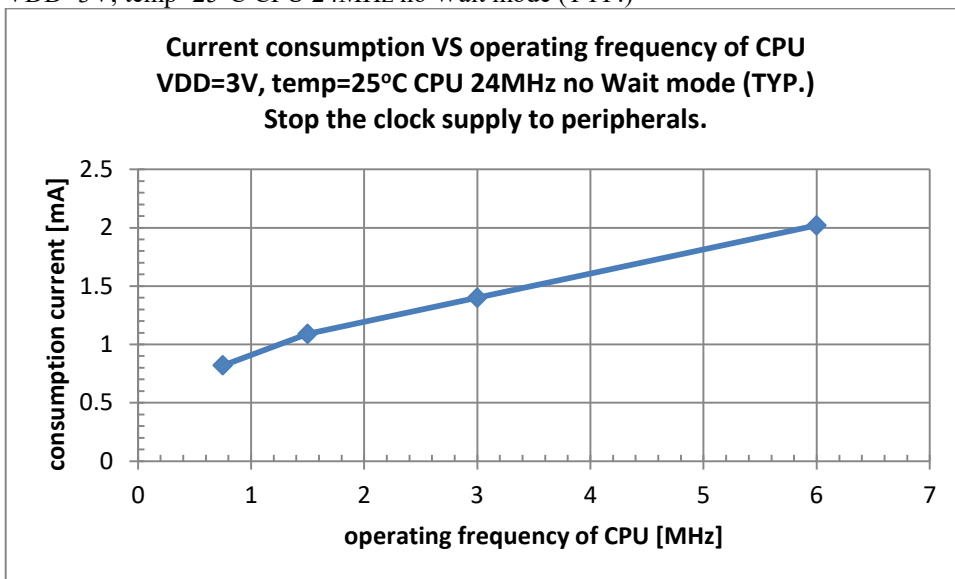


Product: ML62Q1530, ML62Q1531, ML62Q1532, ML62Q1533, ML62Q1534, ML62Q1540, ML62Q1541, ML62Q1542, ML62Q1543, ML62Q1544, ML62Q1550, ML62Q1551, ML62Q1552, ML62Q1553, ML62Q1554

Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 24MHz Wait mode (TYP.)
Stop the clock supply to peripherals.

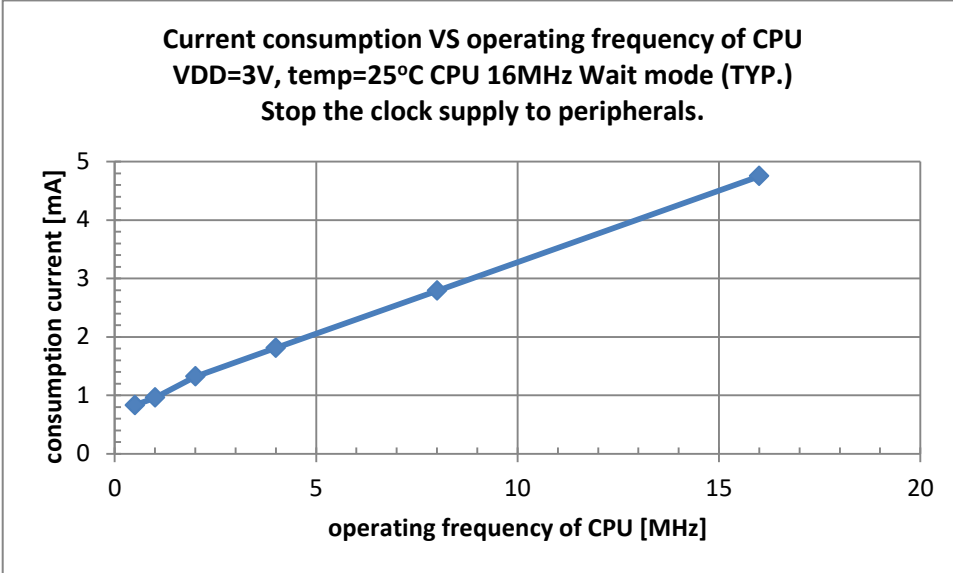


VDD=3V, temp=25°C CPU 24MHz no Wait mode (TYP.)

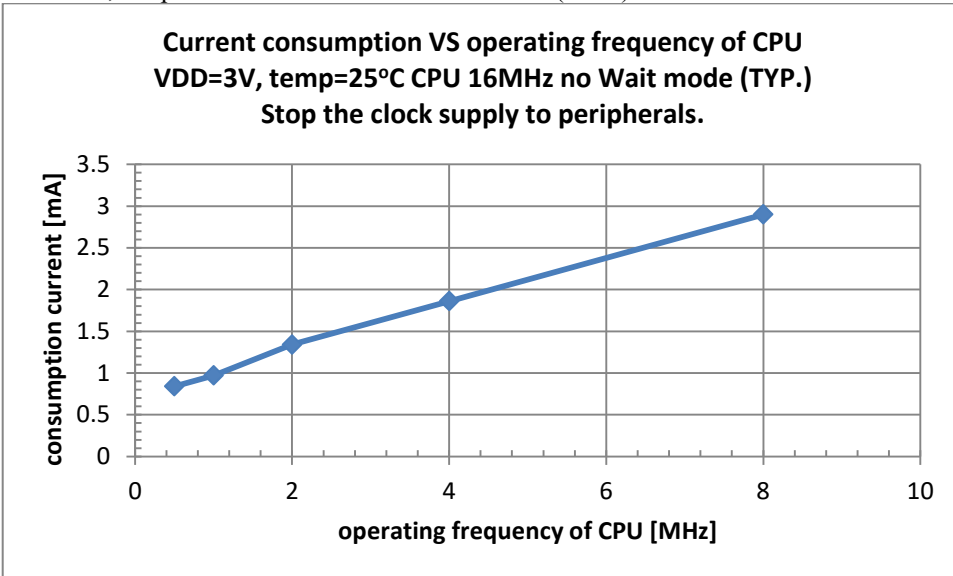


Product: ML62Q1555, ML62Q1556, ML62Q1557, ML62Q1563, ML62Q1564, ML62Q1565, ML62Q1566, ML62Q1567, ML62Q1573, ML62Q1574, ML62Q1575, ML62Q1576, ML62Q1577

Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 16MHz Wait mode (TYP.)
Stop the clock supply to peripherals.

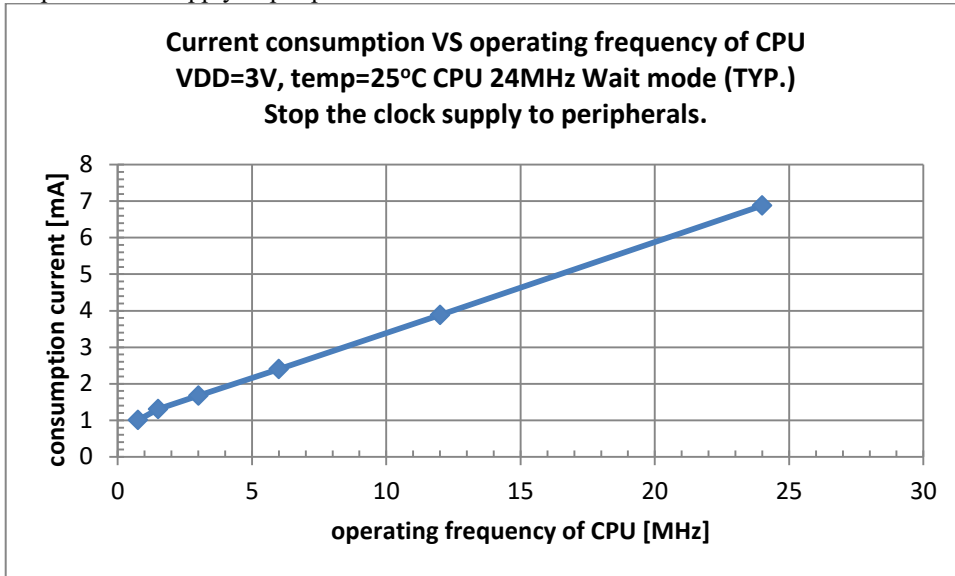


VDD=3V, temp=25°C CPU 16MHz no Wait mode (TYP.)

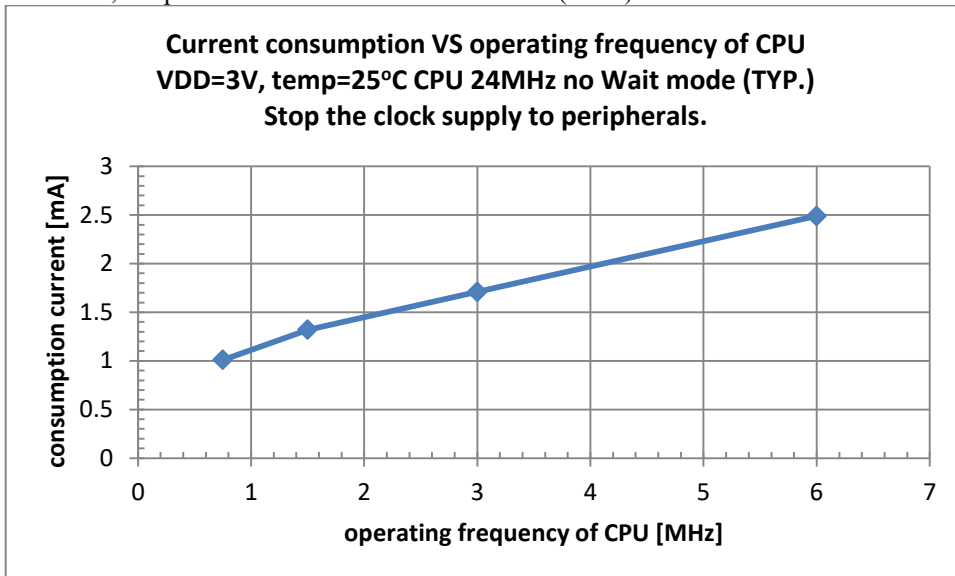


Product: ML62Q1555, ML62Q1556, ML62Q1557, ML62Q1563, ML62Q1564, ML62Q1565, ML62Q1566, ML62Q1567, ML62Q1573, ML62Q1574, ML62Q1575, ML62Q1576, ML62Q1577

Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 24MHz Wait mode (TYP.)
Stop the clock supply to peripherals.

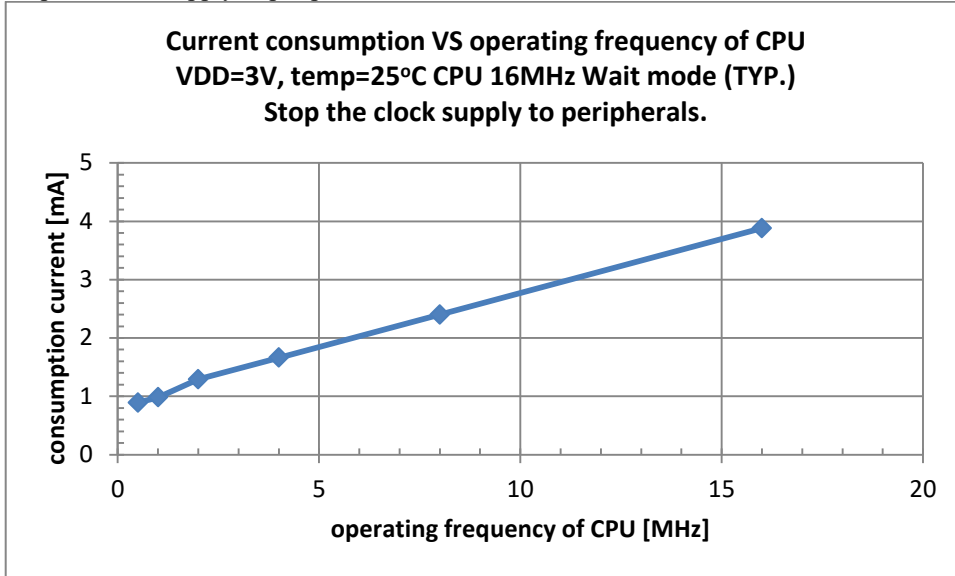


VDD=3V, temp=25°C CPU 24MHz no Wait mode (TYP.)

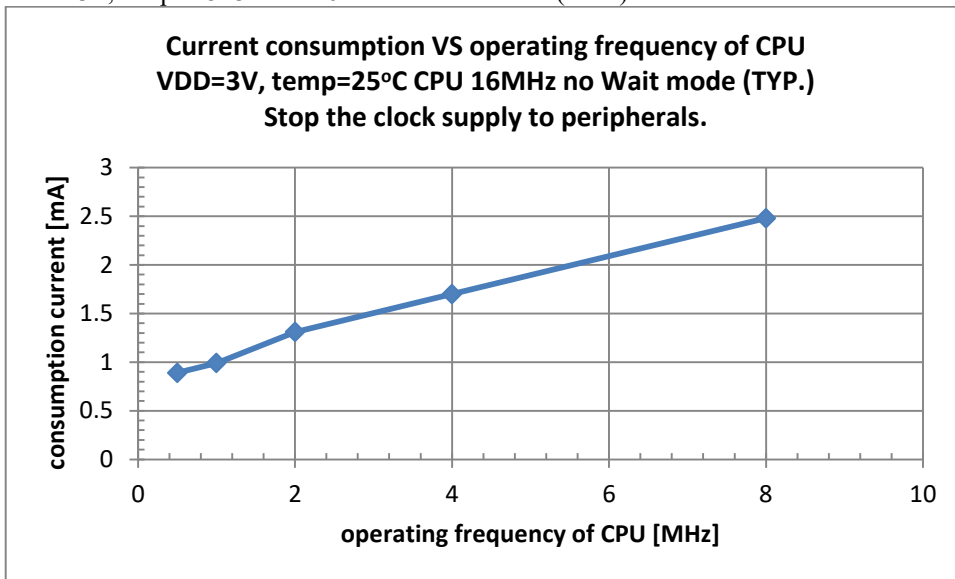


Product: ML62Q1858, ML62Q1859, ML62Q1868, ML62Q1869, ML62Q1878, ML62Q1879

Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 16MHz Wait mode (TYP.)
Stop the clock supply to peripherals.

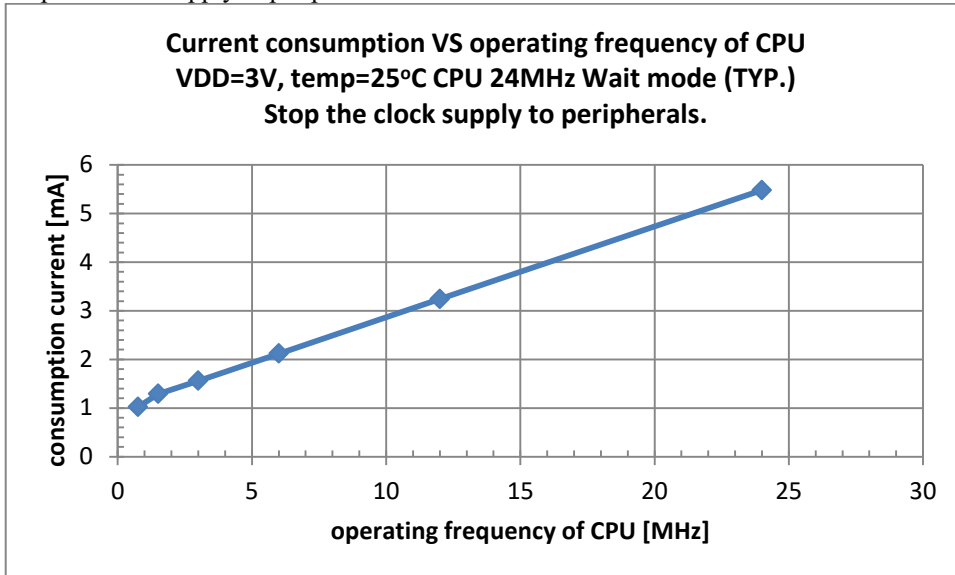


VDD=3V, temp=25°C CPU 16MHz no Wait mode (TYP.)

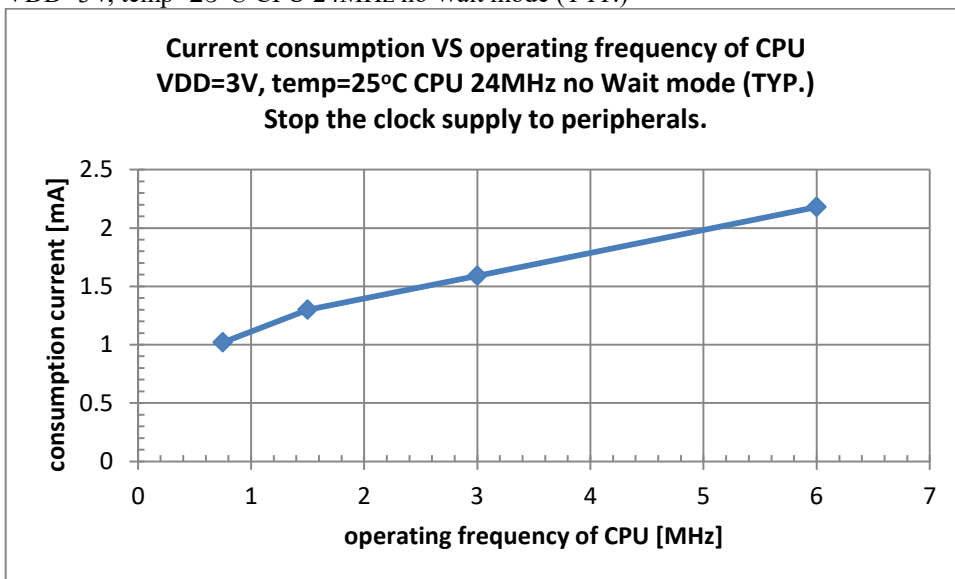


Product: ML62Q1858, ML62Q1859, ML62Q1868, ML62Q1869, ML62Q1878, ML62Q1879

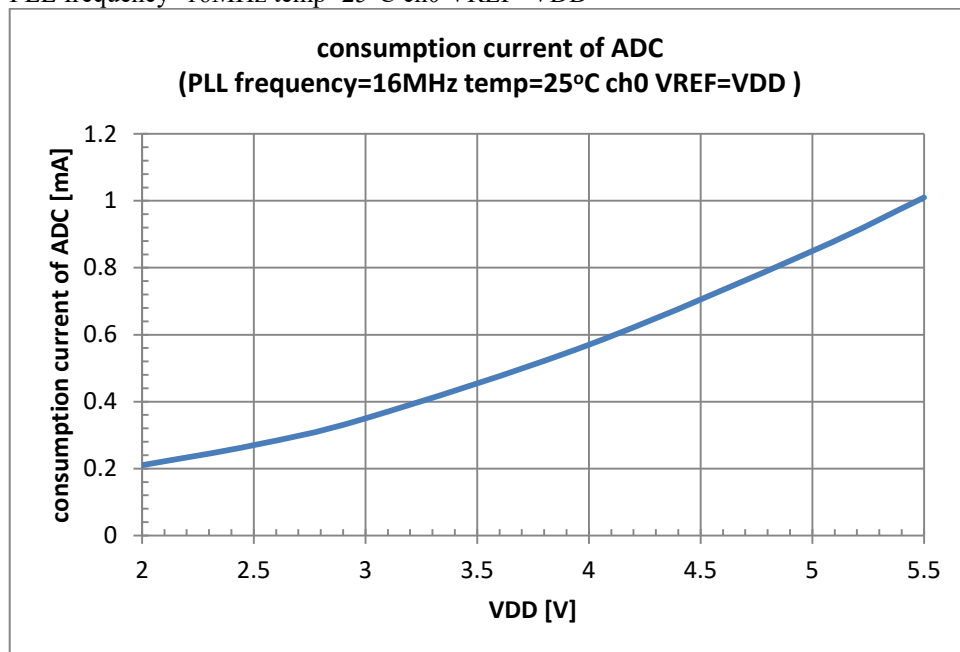
Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 24MHz Wait mode (TYP.)
Stop the clock supply to peripherals.



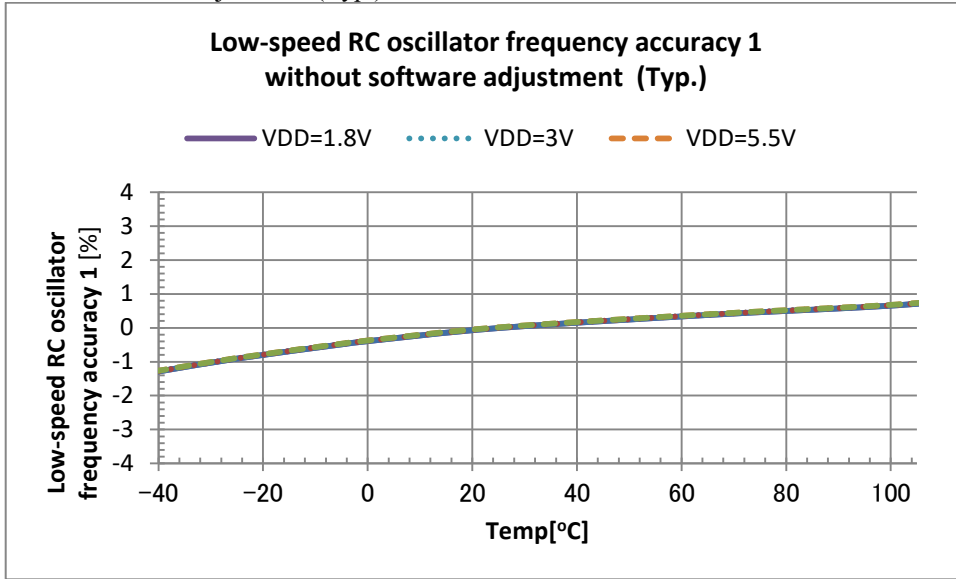
VDD=3V, temp=25°C CPU 24MHz no Wait mode (TYP.)



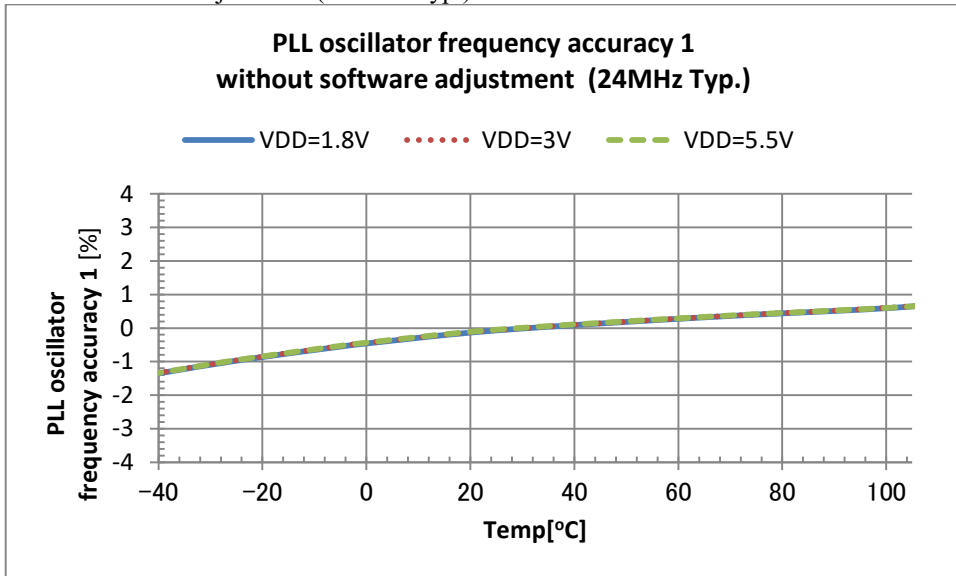
Consumption current of ADC VS operating voltage
PLL frequency=16MHz temp=25°C ch0 VREF=VDD



TEMP VS Low-speed RC oscillator frequency accuracy 1 without software adjustment (Typ.)

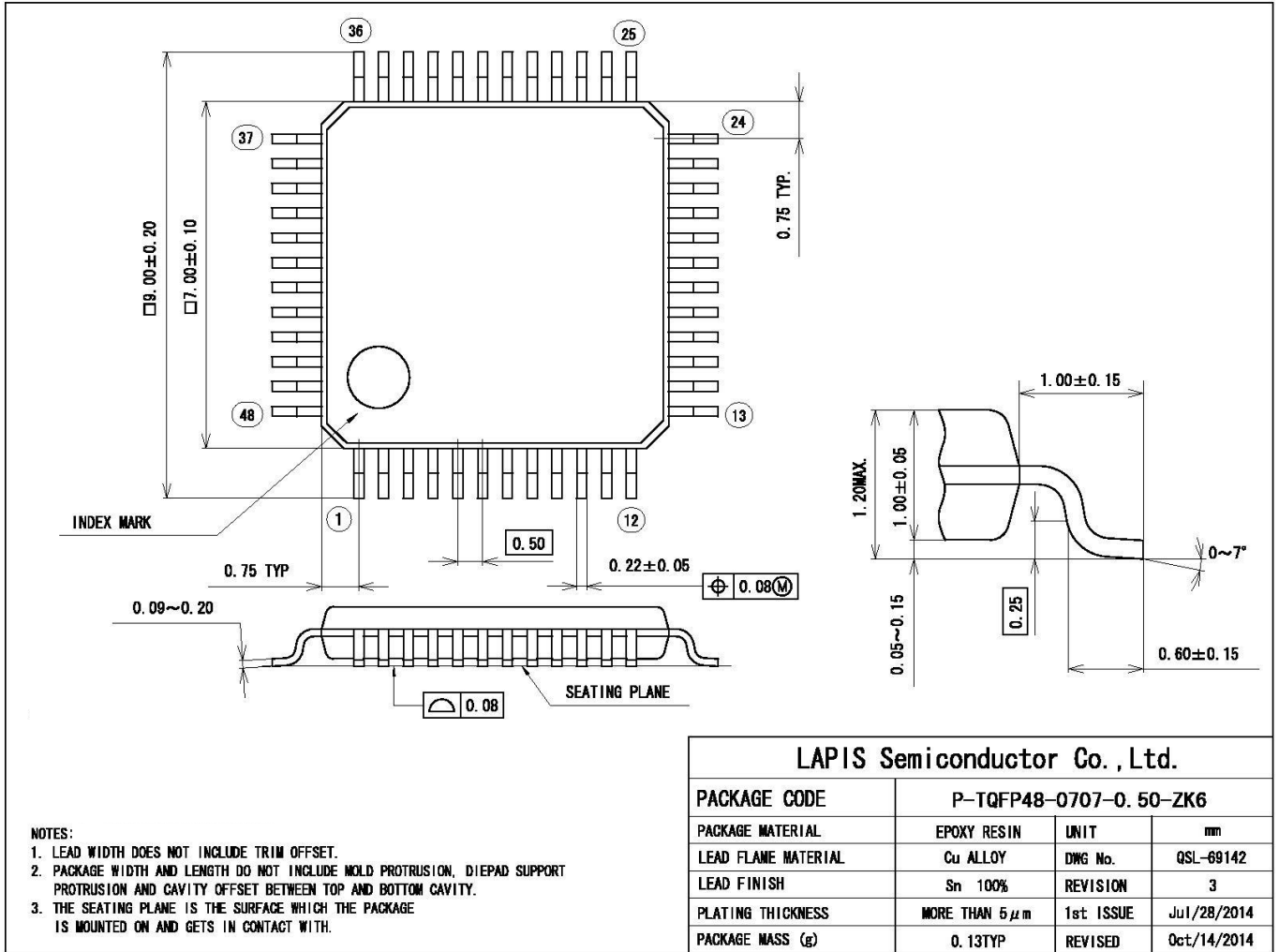


TEMP VS PLL oscillator frequency accuracy 1 without software adjustment (24MHz Typ.)



PACKAGE DIMENSIONS

48pin TQFP Package

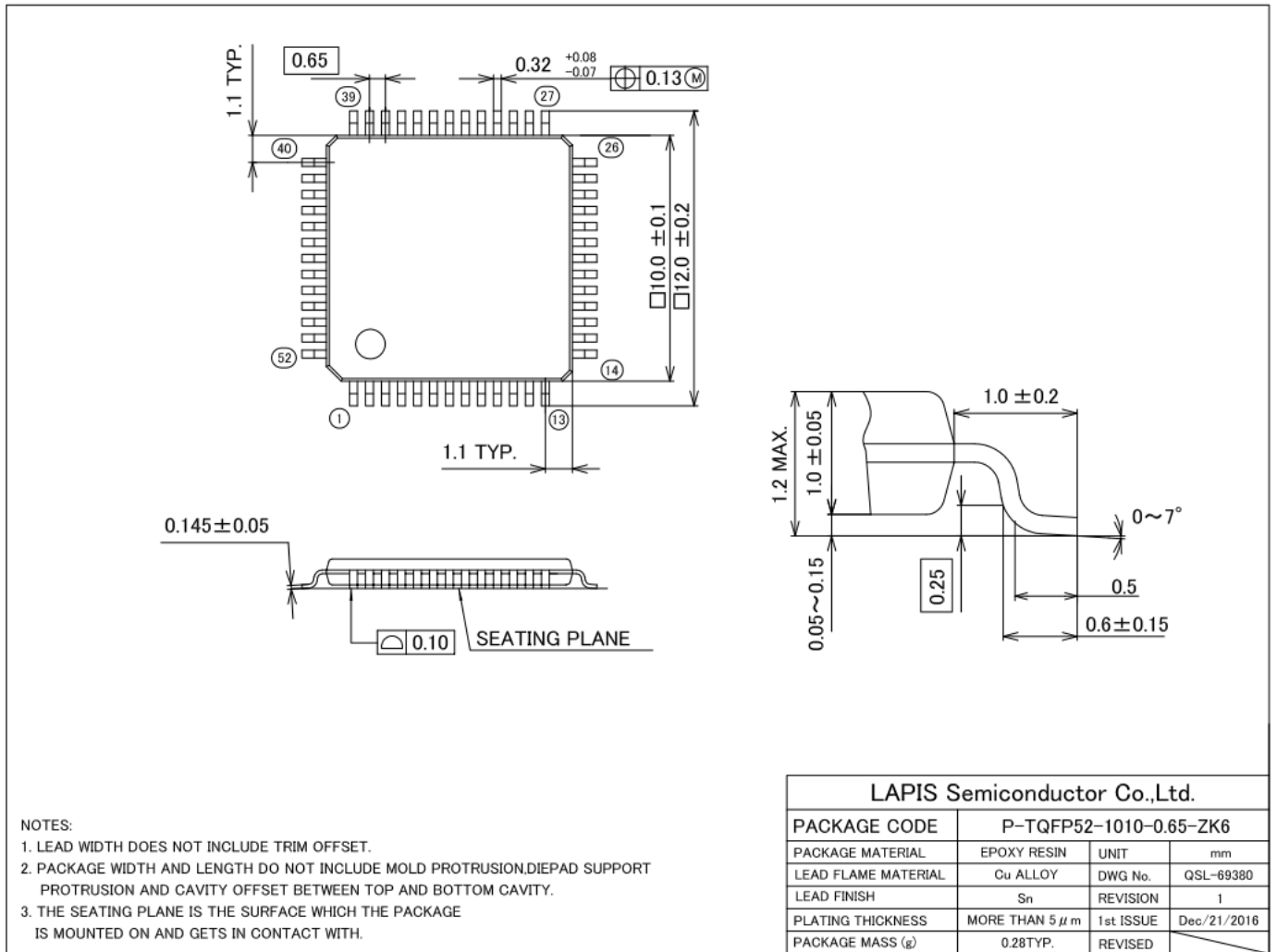


(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

52pin TQFP Package

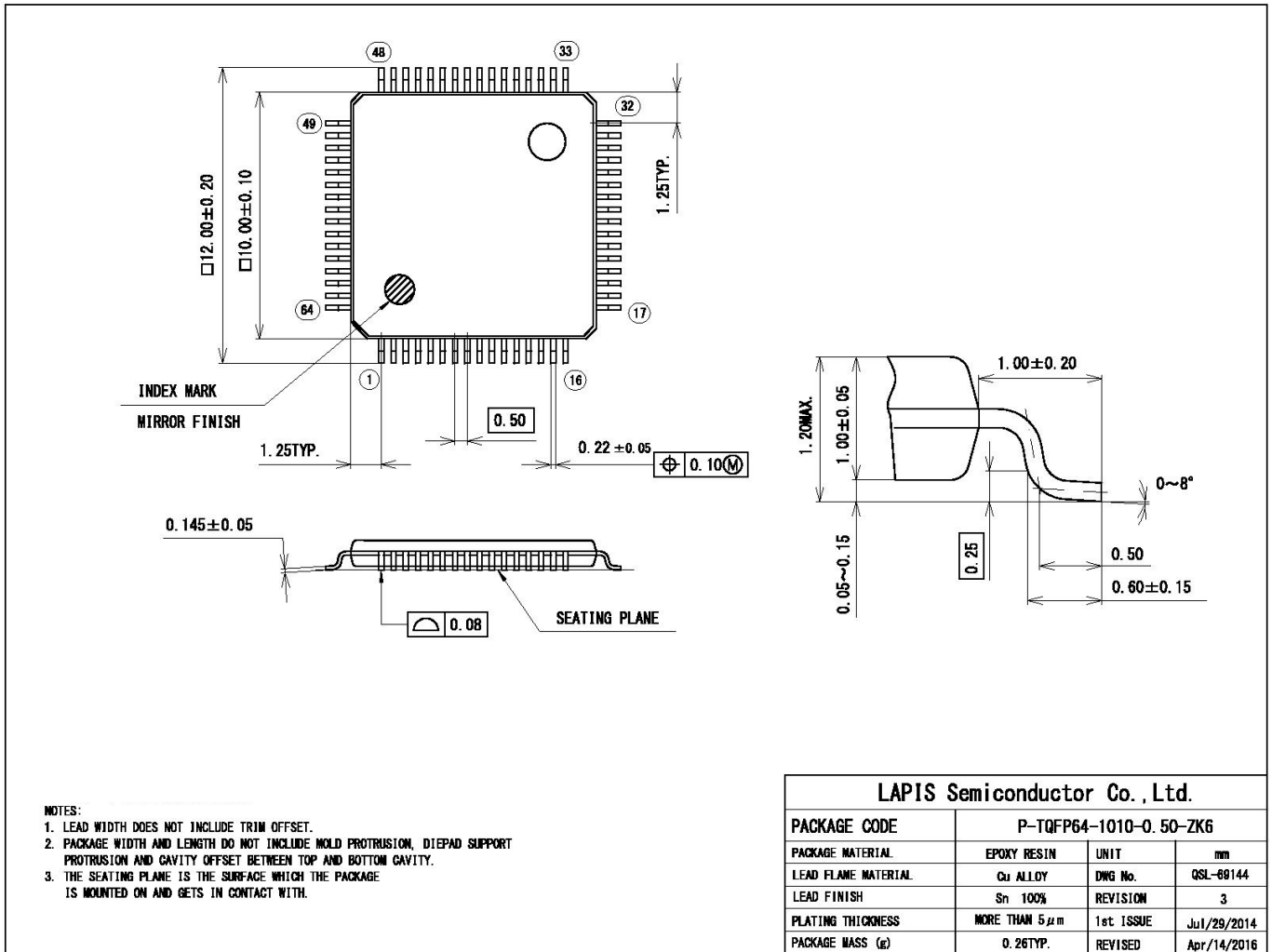


(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64pin TQFP Package

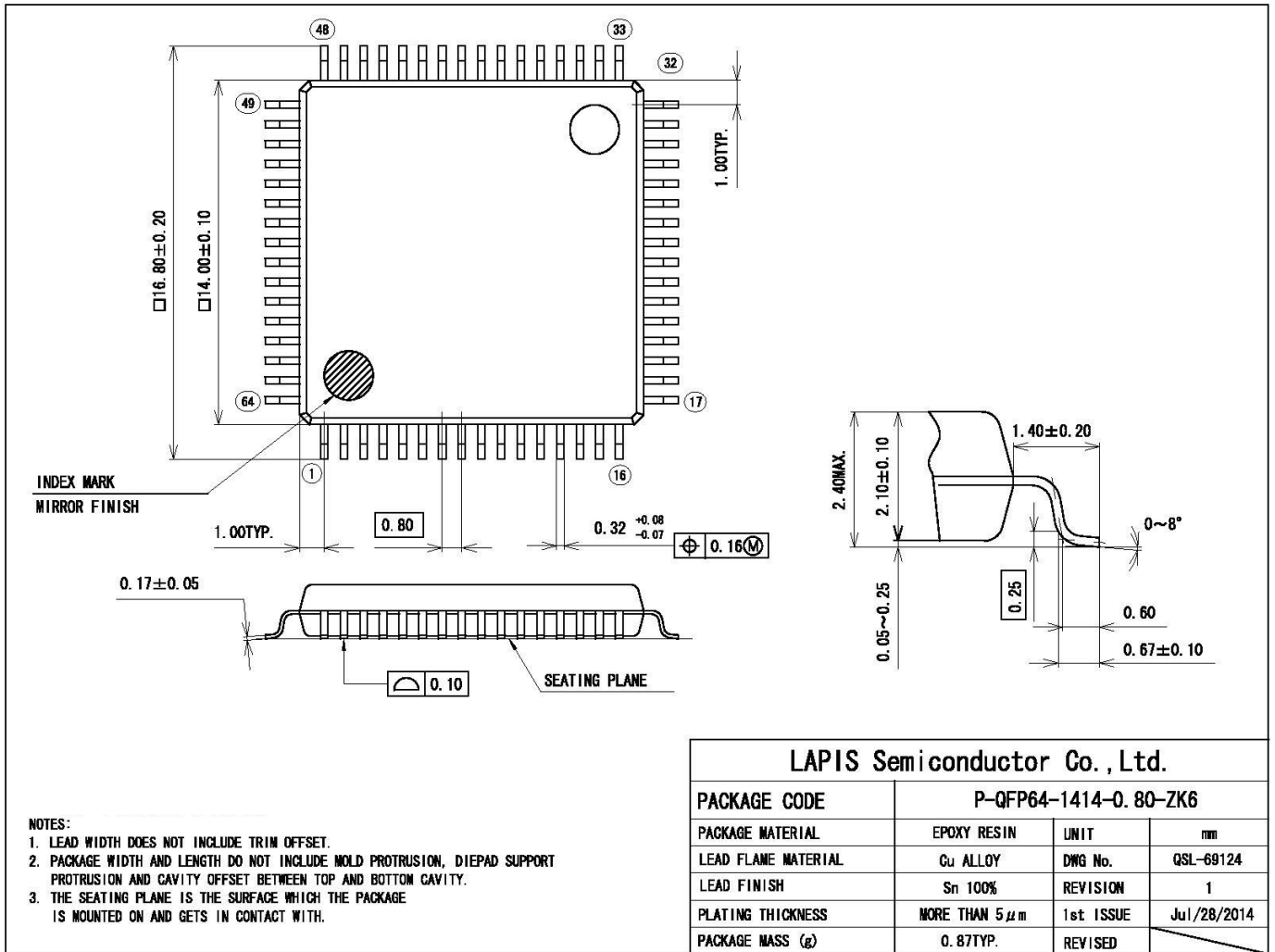


(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64pin QFP Package

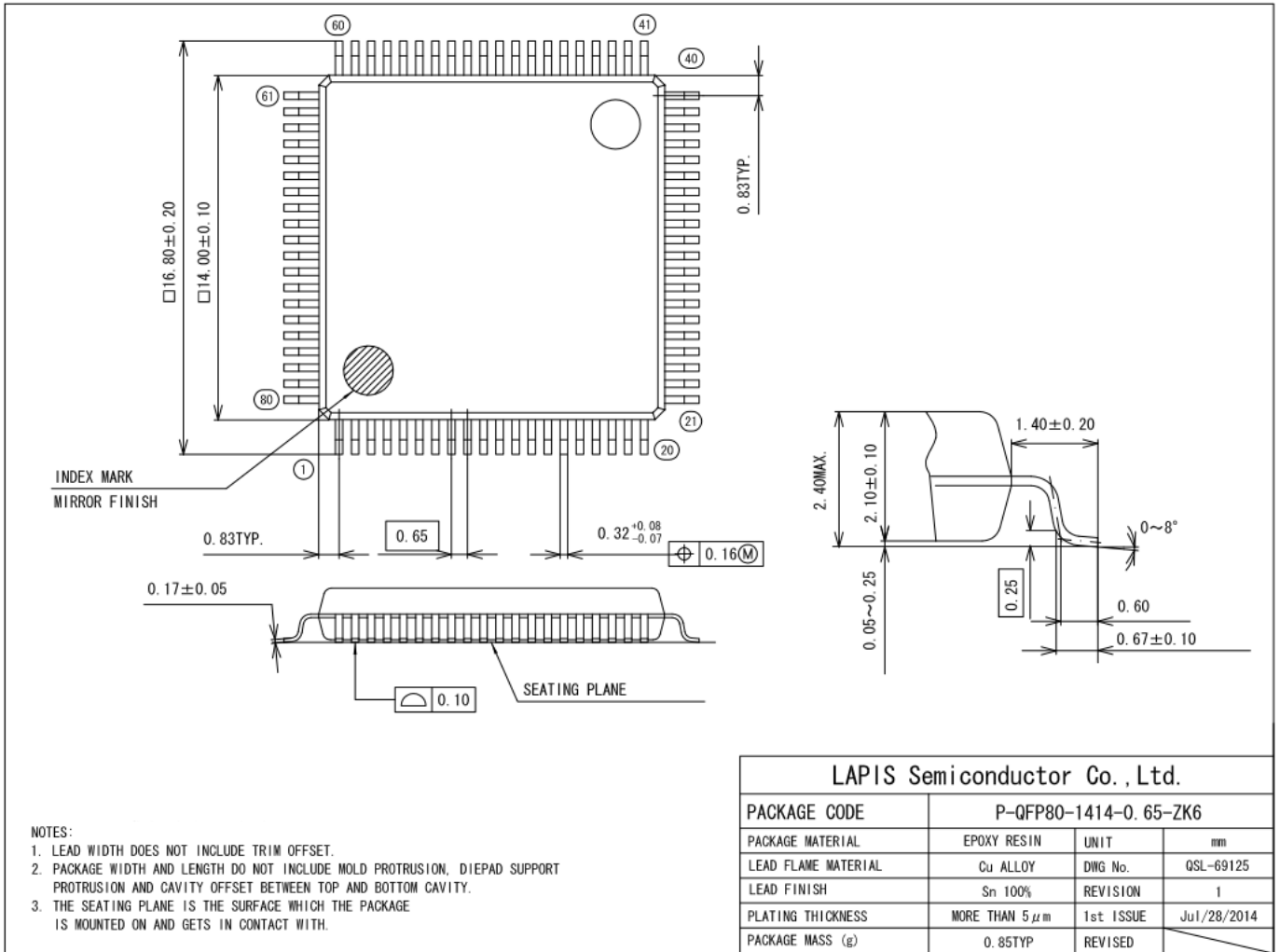


(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

80pin QFP Package

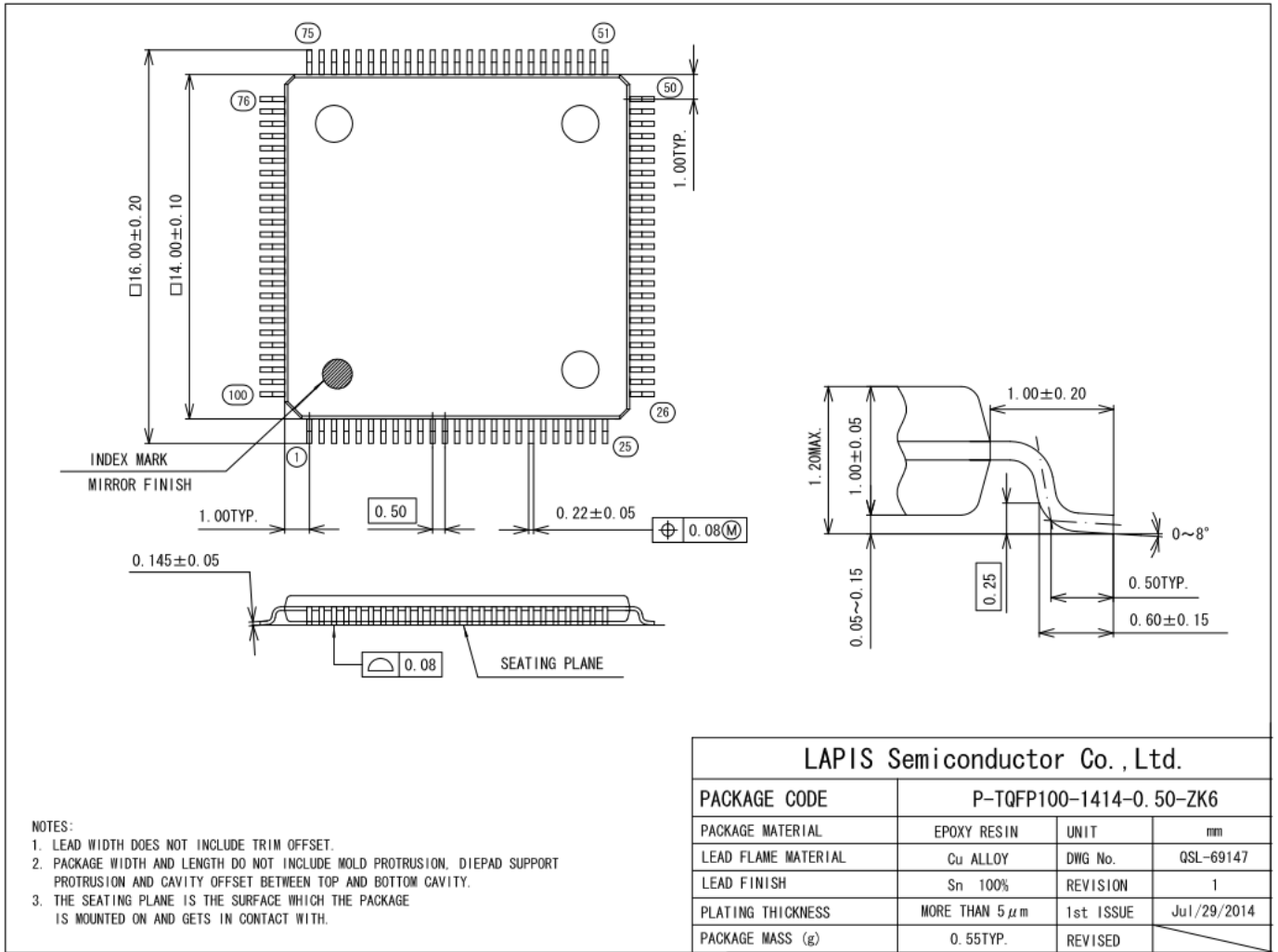


(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

100pin TQFP Package

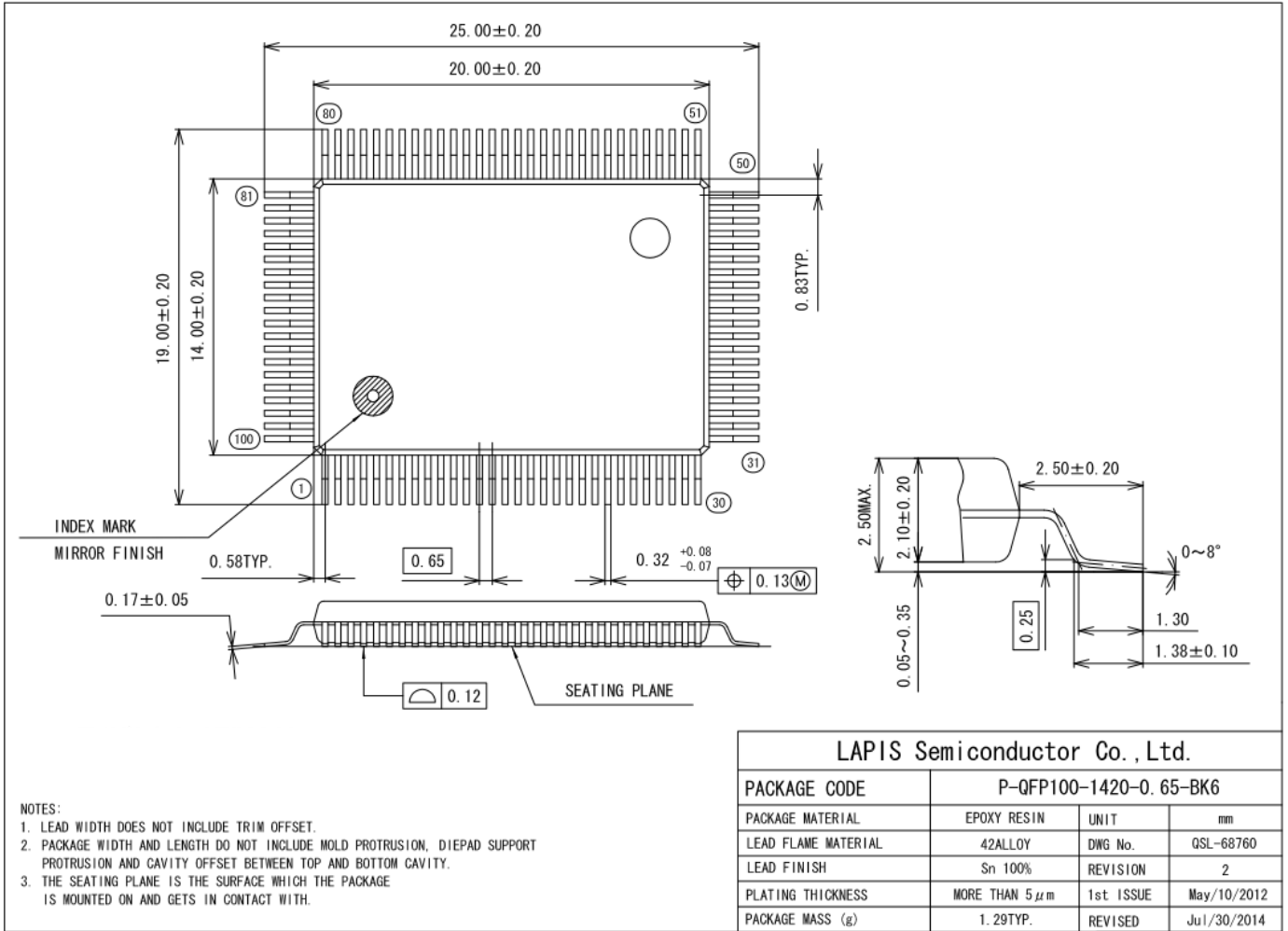


(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

100pin QFP Package



(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

| Document No. | Date | Page | | Description |
|----------------|--------------|------------------|-----------------|--|
| | | Previous Edition | Current Edition | |
| FEDL62Q1500-01 | Dec 17, 2018 | - | - | 1 st Revision. |
| FEDL62Q1500-02 | Jan 9, 2019 | 1 | 1 | Changed the products under developing (Table 1 ML62Q1500 Group Product List) |
| | | 26 | 26 | Deleted "(TBD)" of Current Consumption 1 |
| FEDL62Q1500-03 | May 15, 2019 | 1 | 1 | Changed the products under developing (Table 1 ML62Q1500 Group Product List) |
| | | 28 | 28 | Updated Current Consumption 3 |
| | | 32 | 32 | Added comment "*6" to the IOHL. |
| | | 52 | 52 | Updated 16MHz Characteristics graphs |
| | | 53,55 | 53,55 | Updated 24MHz Characteristics graphs |
| | | - | 56,57 | Added 16MHz and 24MHz Characteristics graphs |
| FEDL62Q1500-04 | May 31, 2019 | 3,4 | 3,4 | Updated the descriptions of DMA and Functional Timer. |
| | | 25 | 25 | Changed I _{OUTH} (total) and I _{OUTL} (total) of Absolute Maximum Ratings to 180mA from 150mA. |
| | | 32 | 32 | Corrected comment of the IOHLs. |
| FEDL62Q1500-05 | Mar 19, 2020 | 24 | 24 | Changed termination of unused pins |
| | | 25 | 25 | Added parameter "Operating temperature(Chip-Junction)" in Recommended Operating Conditions |
| | | 25 | — | Removed the section "Operation Confirmed Crystal Unit(32.768kHz)". This section is mentioned in Applications Note; "Operation-confirmed oscillator for ML62Q1000 series". |
| | | — | 26 | Added thermal characteristics section |
| | | 40 | 41 | Added comments and notes to the reset characteristics |
| | | 40 | 42 | Revised overall of "Power On Reset" section as "Slope of Power supply and Power On Reset" section. The major revisions are Added definitions of Power on rising/falling slope, Power on voltage, CPU operation start time, and added Note. |
| | | * | * | Corrected typo |
| FEDL62Q1500-06 | Jul 15, 2020 | 4,8,9 | 4,8,9 | Changed comment for UART. |
| | | 23 | 23 | Corrected pin name of Buzzer and description of SA-ADC in Table 4. |
| | | 41 | 41 | Corrected comment in waveform of P00/TEST0. |

Notes

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[HD64F3337SF16V](#) [MB90F428GCPF-GSE1](#) [MB90F342ESPMC-G-JNE1](#) [MB90022PF-GS-358E1](#) [MB96F395RWAPMC-GSE2](#)
[MB96395RSAPMC-GS-110E2](#) [MB90F883CSPMC-GE1](#) [S912ZVHY64F1CLL](#) [S912ZVHY64F1VLQ](#) [ST10F280](#) [MB96F338RSAPMCR-GK5E2](#) [CY90096PF-G-002-BND-ERE1](#) [ML62Q1569-NNNGAZ0AX](#) [ML62Q1739-NNNGAZ0AX](#) [ML62Q1749-NNNGAZ0AX](#)
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