

4V Drive Nch + Pch MOSFET

QS8M13

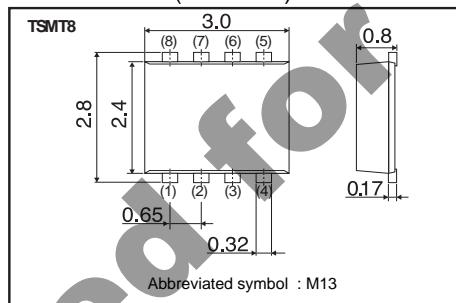
● Structure

Silicon N-channel MOSFET/
Silicon P-channel MOSFET

● Features

- 1) Low on-resistance.
- 2) High power package(TSMT8).
- 3) Low voltage drive(4V drive).

● Dimensions (Unit : mm)



● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	TCR
QS8M13	Basic ordering unit (pieces)	3000

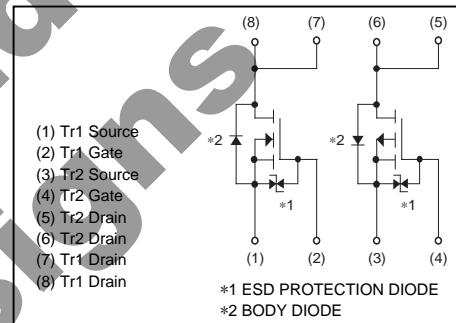
● Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Limits		Unit
		Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage	V_{DSS}	30	-30	V
Gate-source voltage	V_{GSS}	± 20	± 20	V
Drain current	Continuous	I_D	± 6	A
	Pulsed	I_{DP}	± 18	A
Source current (Body Diode)	Continuous	I_s	1.0	A
	Pulsed	I_{sp}	18	A
Power dissipation	P_D	1.5		W / TOTAL
		1.25		W / ELEMENT
Channel temperature	T_{ch}	150		$^\circ\text{C}$
Range of storage temperature	T_{stg}	-55 to +150		$^\circ\text{C}$

*1 $P_w \leq 10\mu\text{s}$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board.

● Inner circuit



● Electrical characteristics (Ta = 25°C)

<Tr1(Nch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	-	-	±10	µA	V _{GS} =±20V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	30	-	-	V	I _D =1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	-	-	1	µA	V _{DS} =30V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	1.0	-	2.5	V	V _{DS} =10V, I _D =1mA
Static drain-source on-state resistance	R _{DS(on)} *		-	20	28	I _D =6A, V _{GS} =10V
			-	25	35	I _D =6A, V _{GS} =4.5V
				28	39	I _D =6A, V _{GS} =4.0V
Forward transfer admittance	Y _{fs} *	3.0	-	-	S	V _{DS} =10V, I _D =6A
Input capacitance	C _{iss}	-	390	-	pF	V _{DS} =10V
Output capacitance	C _{oss}	-	150	-	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	-	70	-	pF	f=1MHz
Turn-on delay time	t _{d(on)*}	-	8	-	ns	I _D =3A, V _{DD} =15V
Rise time	t _r *	-	40	-	ns	V _{GS} =10V
Turn-off delay time	t _{d(off)*}	-	35	-	ns	R _L =5Ω
Fall time	t _f *	-	7	-	ns	R _G =10Ω
Total gate charge	Q _g *	-	5.5	-	nC	I _D =6A, V _{DD} =15V
Gate-source charge	Q _{gs} *	-	1.5	-	nC	V _{GS} =5V
Gate-drain charge	Q _{gd} *	-	2.1	-	nC	

*Pulsed

● Body diode characteristics (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V _{SD} *	-	-	1.2	V	I _s =6A, V _{GS} =0V

*Pulsed

● Electrical characteristics (Ta = 25°C)

<Tr2(Pch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	-	-	±10	µA	V _{GS} =±20V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	-30	-	-	V	I _D =-1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}		-	-1	µA	V _{DS} =-30V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	-1.0	-	-2.5	V	V _{DS} =-10V, I _D =-1mA
Static drain-source on-state resistance	R _{DS(on)} *		-	28	39	I _D =-5A, V _{GS} =-10V
			-	40	56	mΩ I _D =-2.5A, V _{GS} =-4.5V
			-	45	63	I _D =-2.5A, V _{GS} =-4.0V
Forward transfer admittance	Y _{fs} *	3	-	-	S	V _{DS} =-10V, I _D =-5A
Input capacitance	C _{iss}	-	1100	-	pF	V _{DS} =-10V
Output capacitance	C _{oss}	-	150	-	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	-	130	-	pF	f=1MHz
Turn-on delay time	t _{d(on)*}	-	9	-	ns	I _D =-2.5A, V _{DD} =-15V
Rise time	t _r *	-	40	-	ns	V _{GS} =-10V
Turn-off delay time	t _{d(off)*}	-	90	-	ns	R _L =6Ω
Fall time	t _f *	-	55	-	ns	R _G =10Ω
Total gate charge	Q _g *	-	10	-	nC	I _D =-5A, V _{DD} =-15V
Gate-source charge	Q _{gs} *	-	3.6	-	nC	V _{GS} =-5V
Gate-drain charge	Q _{gd} *	-	3.0	-	nC	

*Pulsed

● Body diode characteristics (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V _{SD} *	-	-	-1.2	V	I _s =-5A, V _{GS} =0V

*Pulsed

● Electrical characteristic curves ($T_a=25^\circ\text{C}$)

⟨Tr.1(Nch)⟩

Fig.1 Typical Output Characteristics (I)

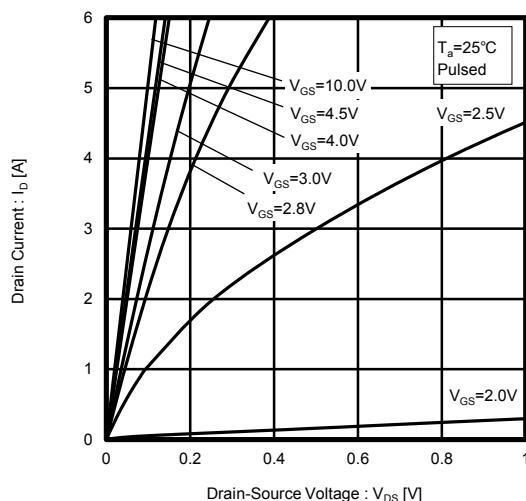


Fig.2 Typical Output Characteristics (II)

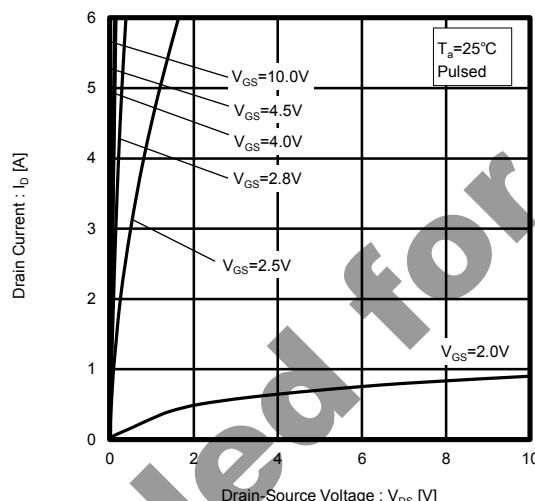


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

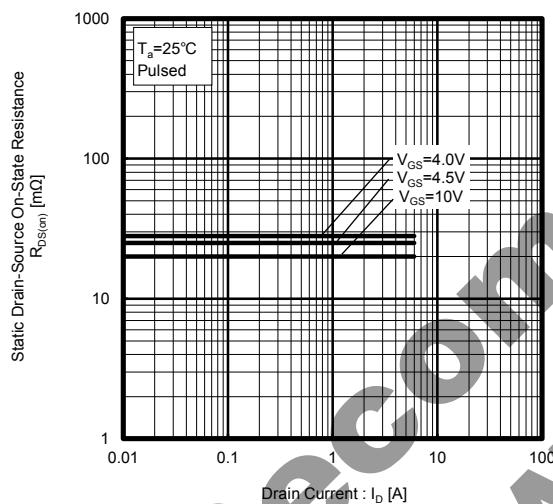


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

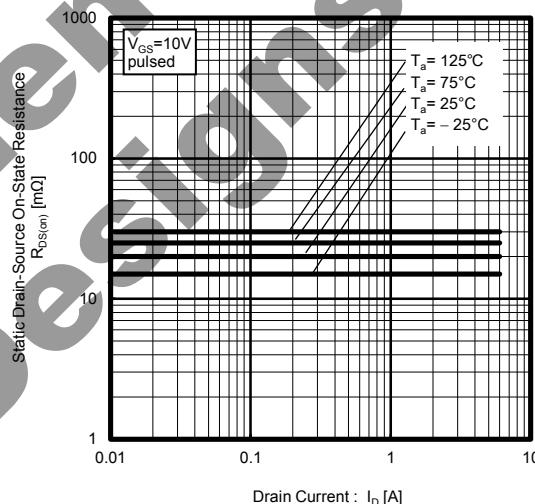


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

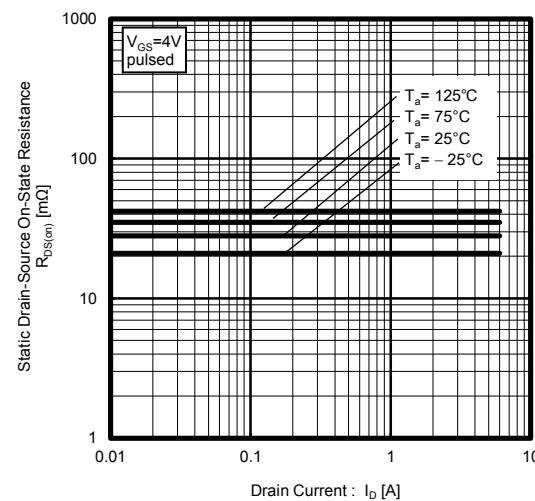
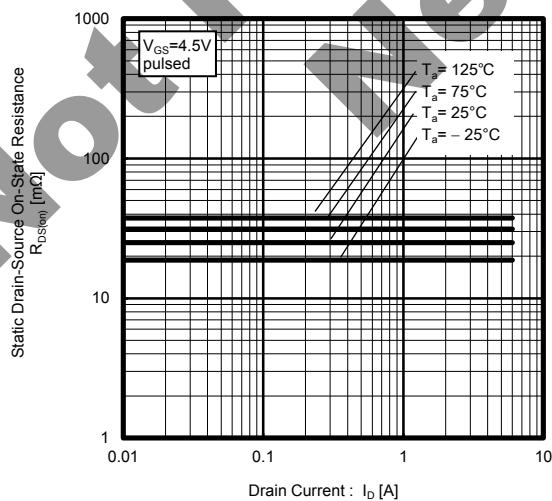


Fig.7 Forward Transfer Admittance vs. Drain Current

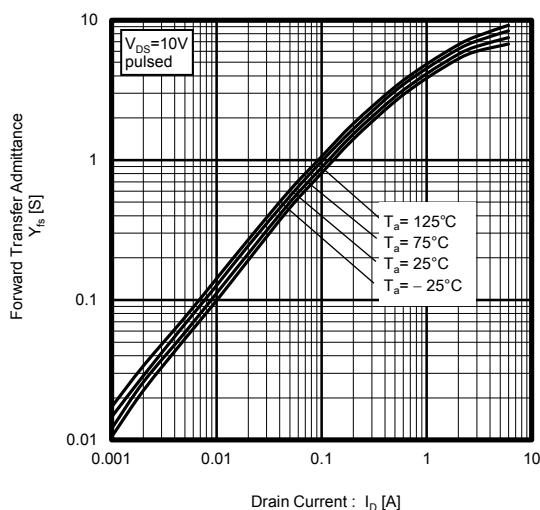


Fig.8 Typical Transfer Characteristics

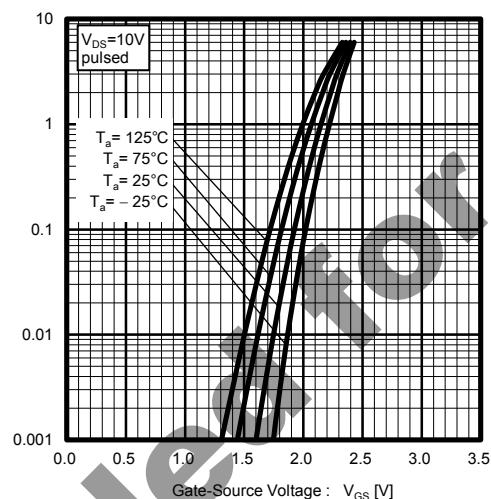


Fig.9 Source Current vs. Source-Drain Voltage

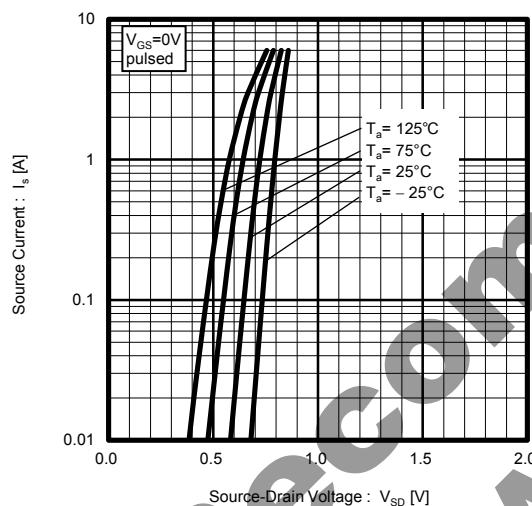


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

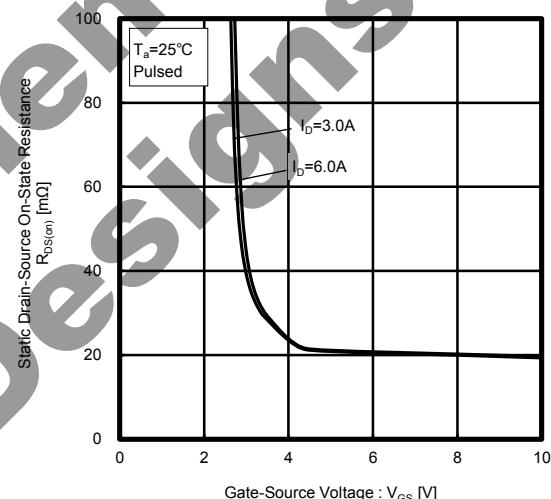


Fig.11 Switching Characteristics

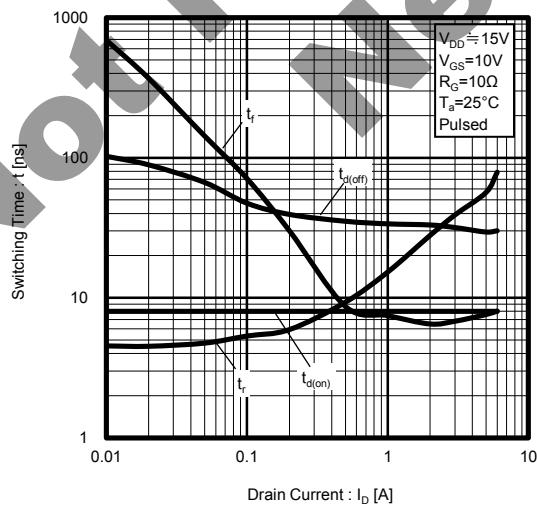


Fig.12 Dynamic Input Characteristics

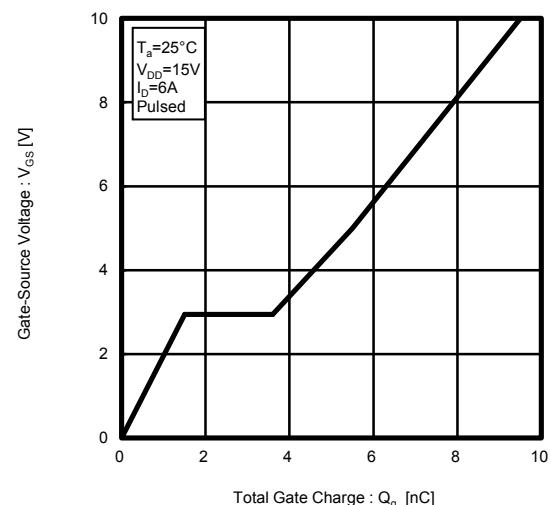


Fig.13 Typical Capacitance vs. Drain-Source Voltage

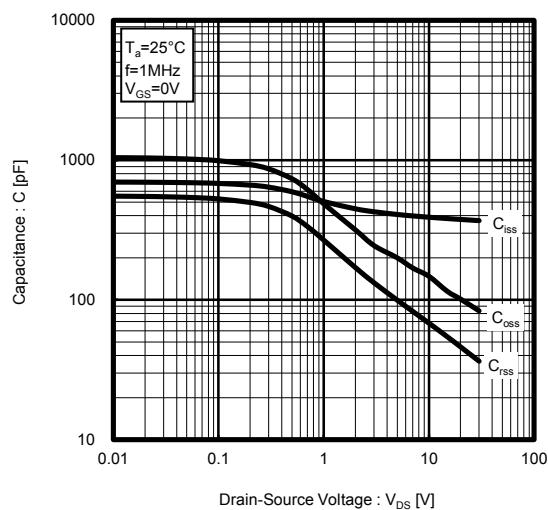


Fig.14 Maximum Safe Operating Area

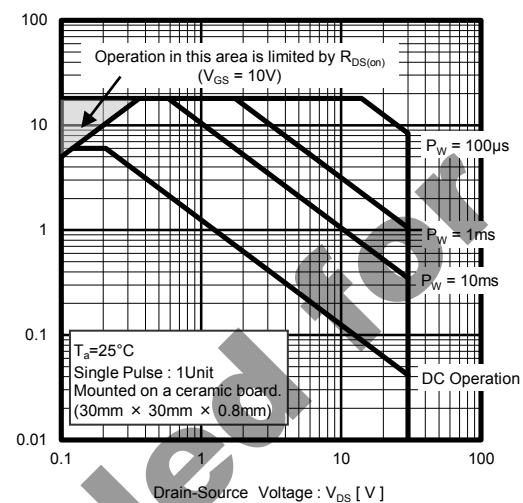
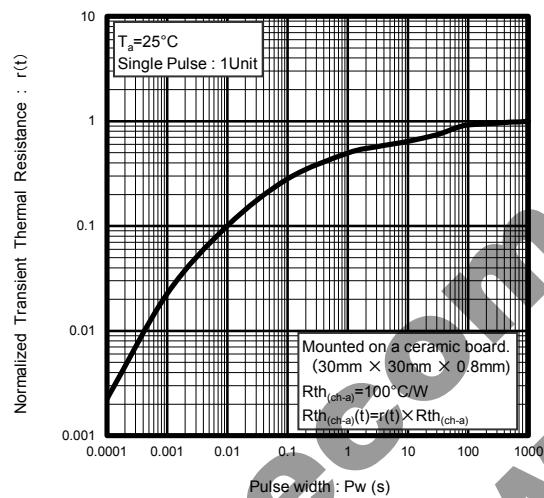


Fig.15 Normalized Transient Thermal Resistance v.s. Pulse Width



**Not Recommended
New Designs**

$\langle \text{Tr.2(Pch)} \rangle$

Fig.1 Typical Output Characteristics (I)

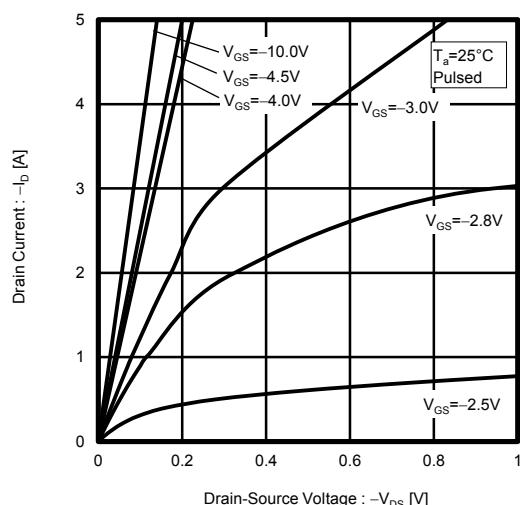


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

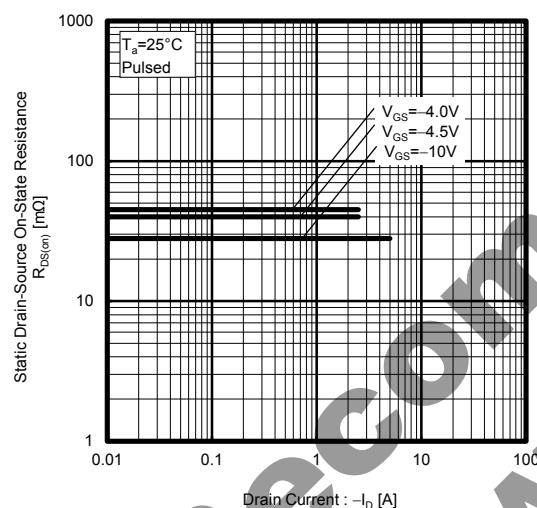


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

Fig.2 Typical Output Characteristics (II)

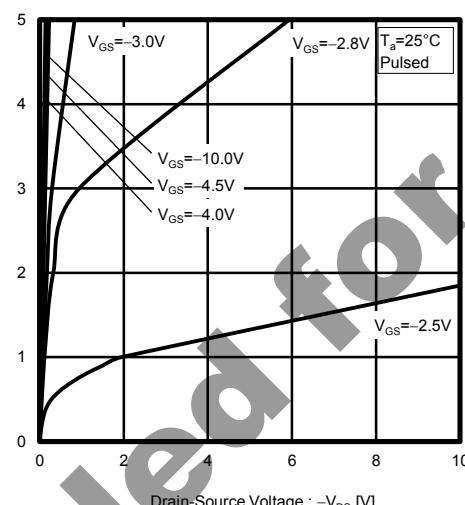


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

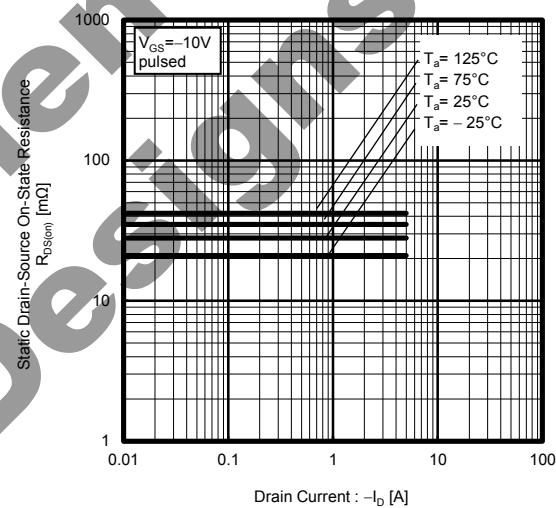


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

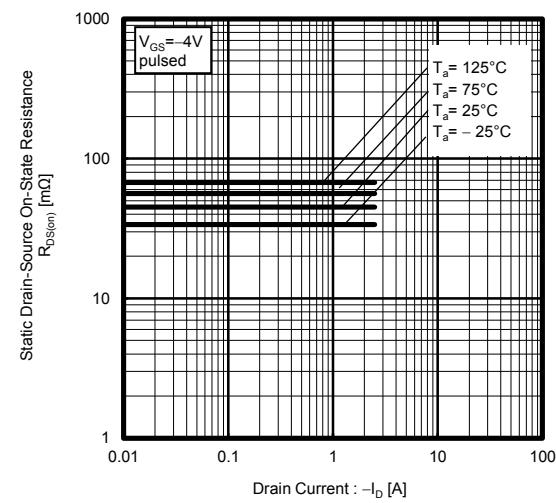
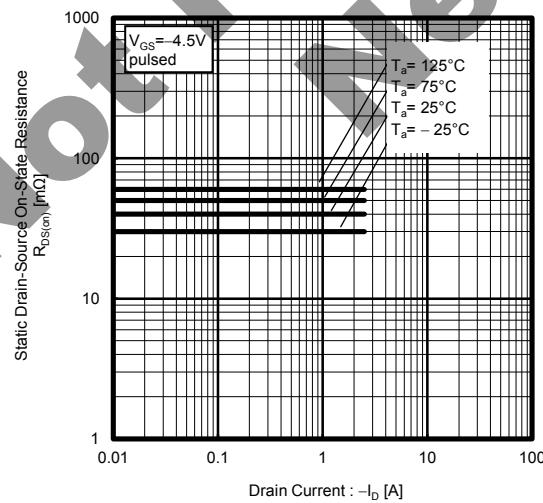


Fig.7 Forward Transfer Admittance vs. Drain Current

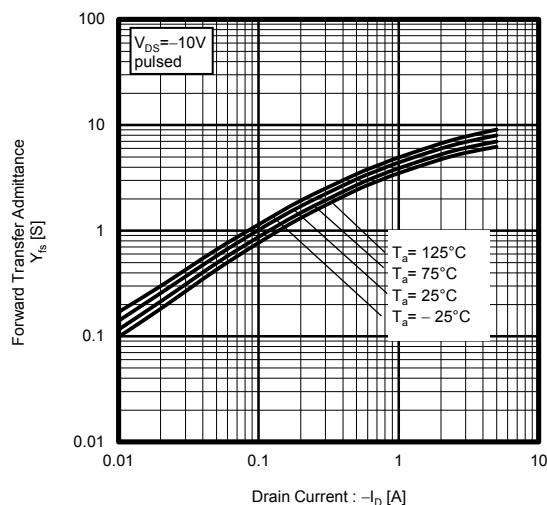


Fig.8 Typical Transfer Characteristics

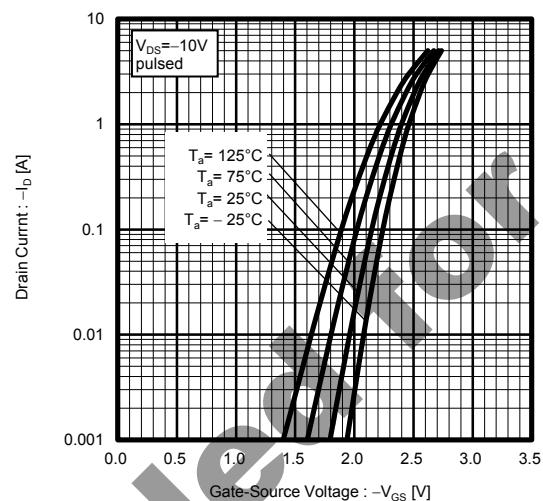


Fig.9 Source Current vs. Source-Drain Voltage

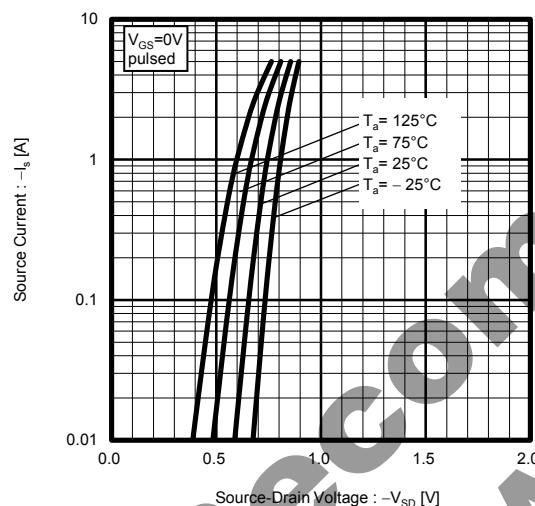


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

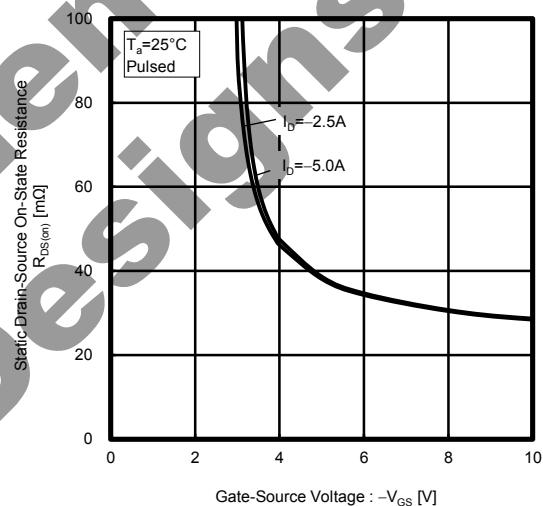


Fig.11 Switching Characteristics

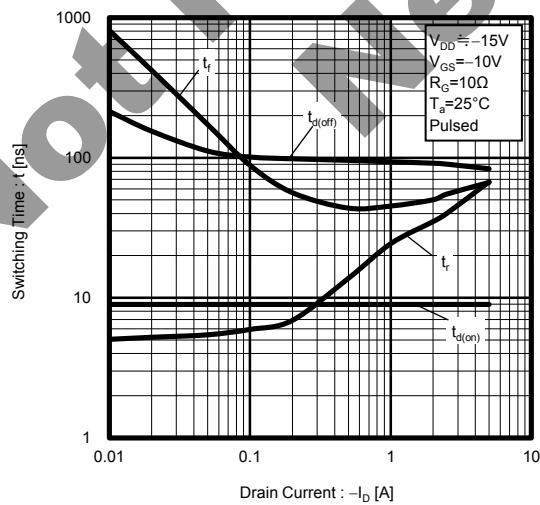


Fig.12 Dynamic Input Characteristics

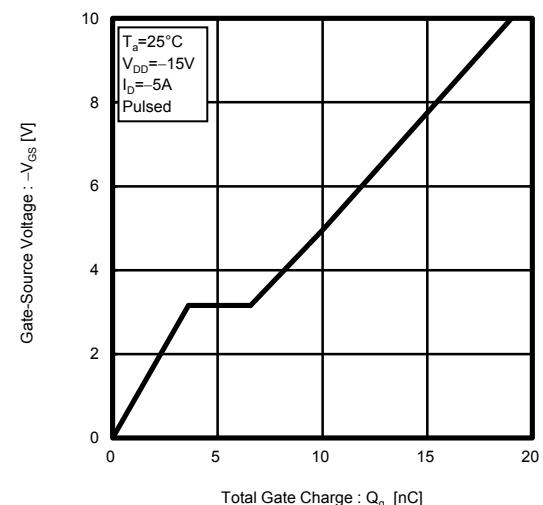


Fig.13 Typical Capacitance vs. Drain-Source Voltage

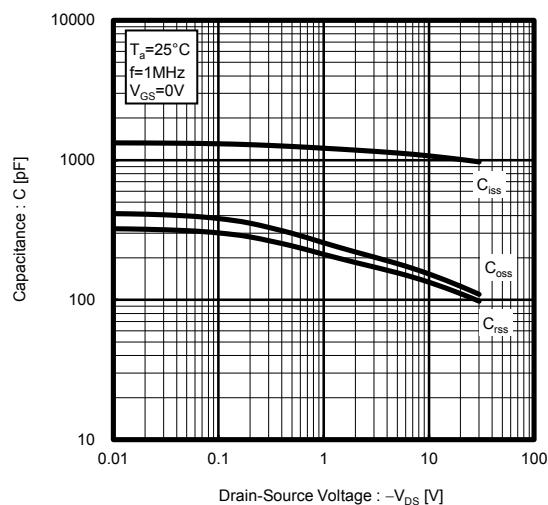


Fig.14 Maximum Safe Operating Area

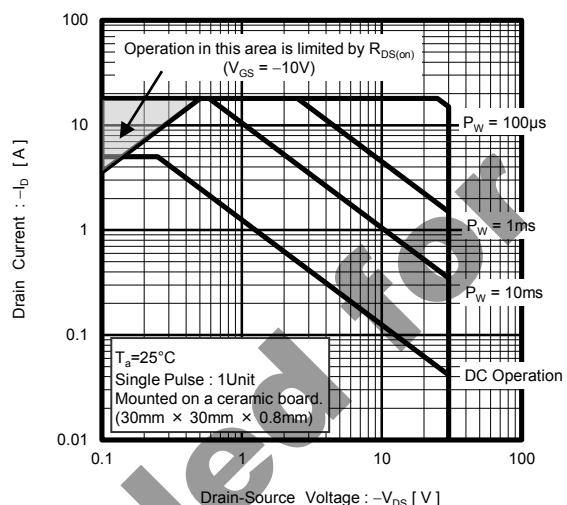
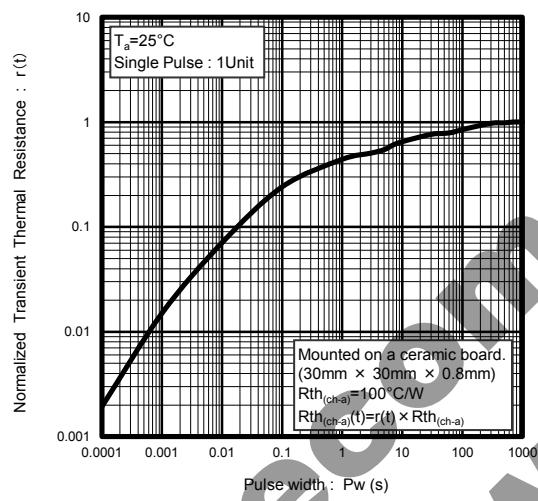


Fig.15 Normalized Transient Thermal Resistance v.s. Pulse Width



Not Recommended
New Designs

● Measurement circuits

<Tr1(Nch)>

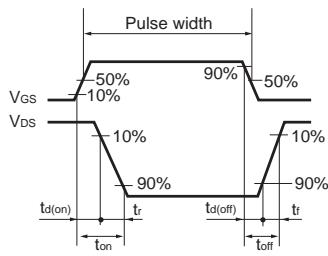
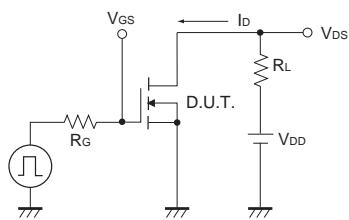


Fig.1-1 Switching Time Measurement Circuit

Fig.1-2 Switching Waveforms

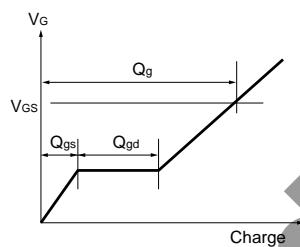
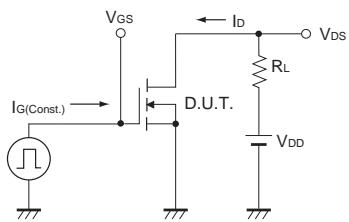


Fig.2-1 Gate Charge Measurement Circuit

Fig.2-2 Gate Charge Waveform

<Tr2(Pch)>

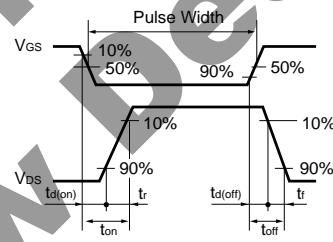
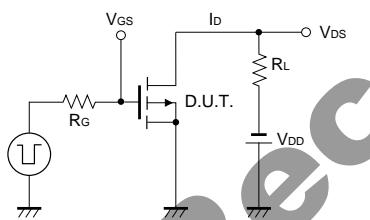


Fig.1-1 Switching Time Measurement Circuit

Fig.1-2 Switching Waveforms

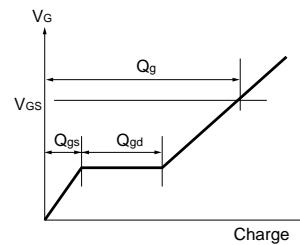
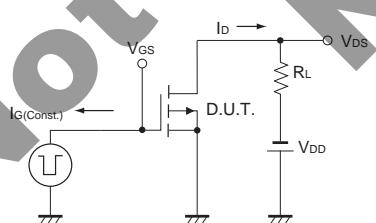


Fig.2-1 Gate Charge Measurement Circuit

Fig.2-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Notes

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