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LAPIS Technology Co., Ltd.
October 1, 2020

RB-S22Q53xTB48

User's Manual

Issue Date: March 26, 2020

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1. Overview

This instruction manual is for the RB-S22Q53xTB48 which is the ML22Q532/ML22Q533/ML22Q535 reference board.

Combining the board with a Sound Device Control Board 3 (hereinafter referred to as "SDCB3") enables the following functions to be implemented:

- Voice playback by ML22Q532/ML22Q533/ML22Q535.
- Writing voice data into ML22Q532/ML22Q533/ML22Q535.

2. Operational notes

The following describes the precautions to follow when handling the RB-S22Q53xTB48.

- Turn off the power when attaching the RB-S22Q53xTB48 to the SDCB3.
- Turn off the power when loading devices into the RB-S22Q53xTB48. Be sure to orient the device correctly. Pin 1 direction is toward the lower left side when the lid is opened. The Figure 1 shows the setting directions of devices.
- The ML22Q532/ML22Q533/ML22Q535 supply voltages are 2.7 to 3.6V / 3.3 to 5.5V. Use the RB-S22Q53xTB48 with a power supply voltage of 3.0V.
- RB-S22Q53xTB48 is a device used only by experts in R&D facilities for research and development purposes. RB-S22Q53xTB48 is not intended to be used in mass-produced products or parts thereof.
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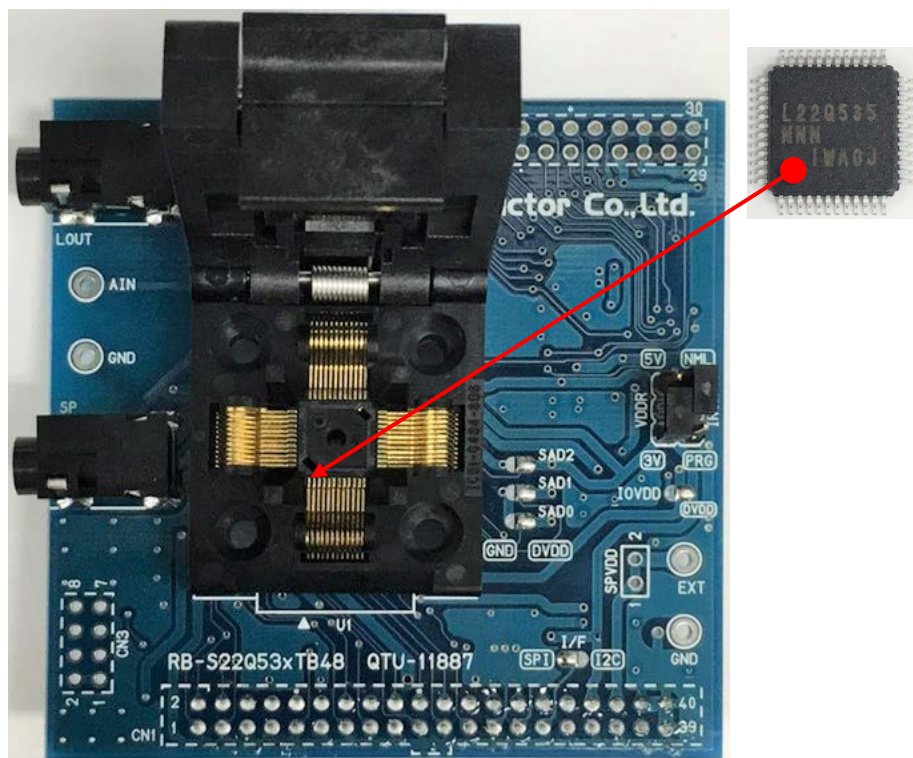


Figure 1 Outline Diagram

3. Specification

3.1. Jumper Pin Setting

Table 1 shows the RB-S22Q53xTB48 jumper pin settings.

Table 1

Jumper Pin Name	Setting
VDDR	Fixed on the 3V side
IRON	Fixed on the NML side

3.2. PCB layout

Figure 2 shows the RB-S22Q53xTB48 PCB layout.

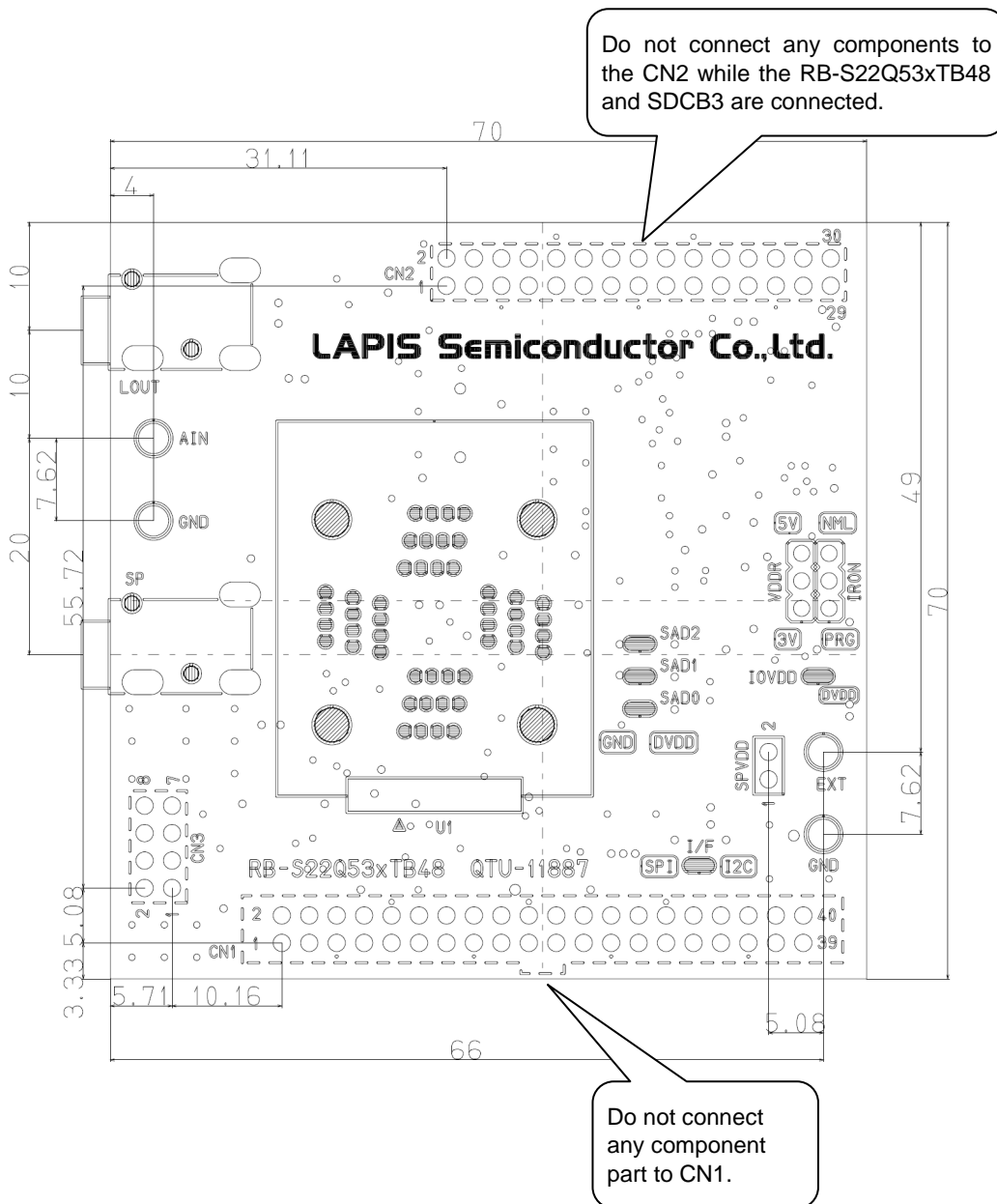
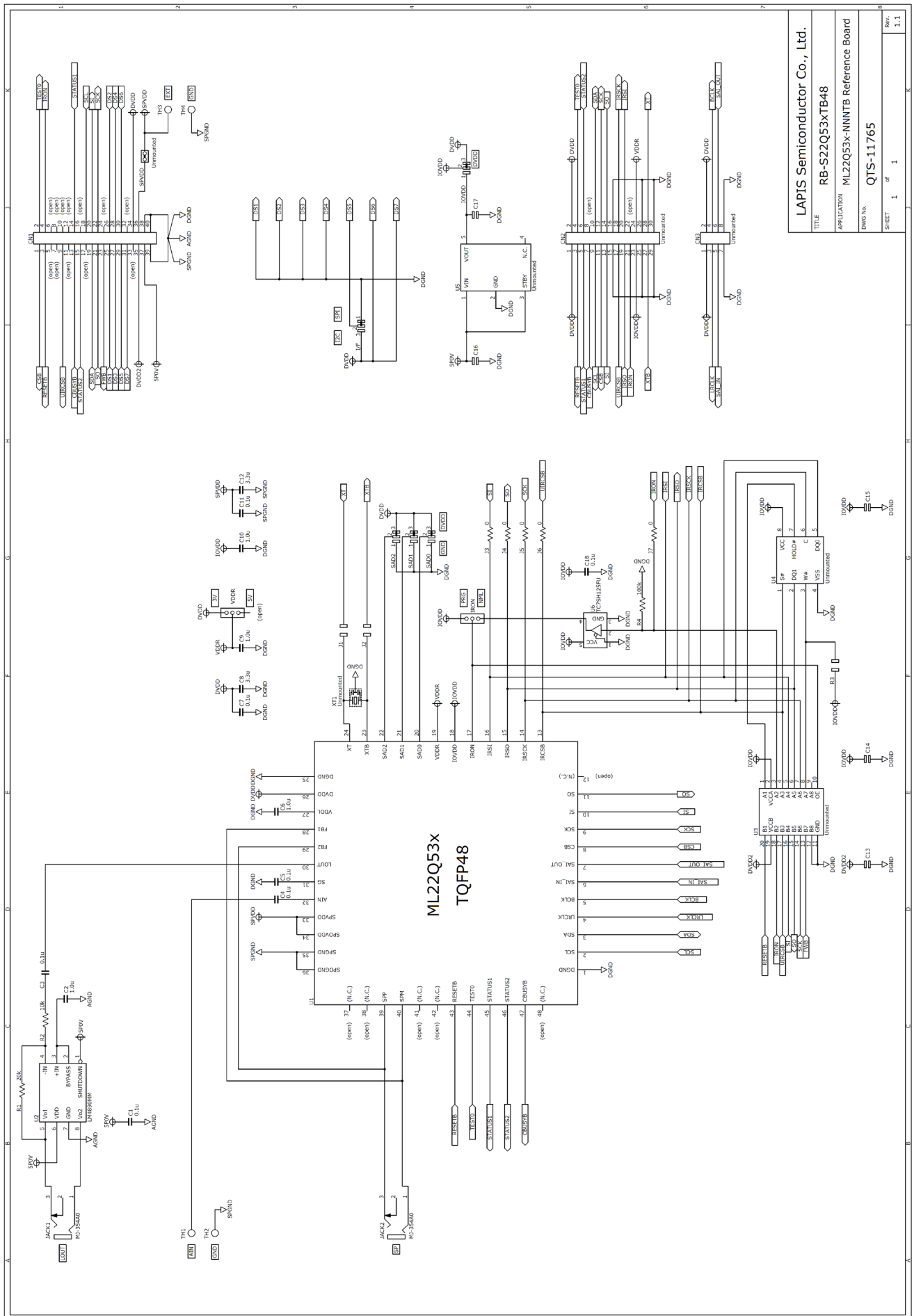


Figure 2 PCB layout

3.3. BOM list, Schematic

	Parts Number	Symbol	Contents	Qty.	Vendor
1	QTU-11887	RB-S22Q53xTB48	PCB	1	LAPIS Semiconductor Co., Ltd.
2	CGA3E2X7R1E104K080AA	C1,C3,C4,C5, C7,C11	Ceramic Capacitor 0.1 μ F/25V X7R	6	TDK Corporation
3	CGA3E1X7R1C105K080AC	C2,C6,C9,C10, C18	Ceramic Capacitor 1.0 μ F/16V X7R	5	TDK Corporation
4	C1608X5R1C335K080AC	C8,C12	Ceramic Capacitor 3.3 μ F/16V X5R	2	TDK Corporation
5	HIF3FB-40DA-2.54DSA(71)	CN1	40pin Receptacle	1	Hirose Electric Co., Ltd.
6	A2-3PA-2.54DSA	IRON,VDDR	3pin Pin Header	2	Hirose Electric Co., Ltd.
7	-	I/F,IOVDD	Select pad	2	-
8	MCR03EZPJ000	J3,J4,J5,J6,J7	Resistor 0 Ω	5	Rohm Co., Ltd.
9	MJ-354A0	JACK1,JACK2	2-Conductor Miniature Jack	2	MARUSHIN ELECTRIC MFG. CO., LTD.
10	MCR03EZPJ203	R1	Resistor 20k Ω \pm 5%	1	Rohm Co., Ltd.
11	MCR03EZPJ103	R2	Resistor 10k Ω \pm 5%	1	Rohm Co., Ltd.
12	MCR03EZPJ104	R4	Resistor 100k Ω \pm 5%	1	Rohm Co., Ltd.
13	-	SAD0,SAD1,SAD2	Select pad	3	-
14	IC51-806.A106725-001	U1	TQFP P0.50 48P Socket	1	YAMAICHI ELECTRONICS Co., Ltd.
15	LM4890MM/NOPB	U2	Audio Power Amplifier	1	Texas Instruments Incorporated
16	TC7SH125FU	U6	Bus Buffer with 3-State Output	1	Toshiba Corporation
17	HIF3GA-2.54SP	-	Short Pin	2	Hirose Electric Co., Ltd.
18	-	C13,C14,C15,C16, C17	1608	5	-
19	-	CN2	Unmounted	1	-
20	-	CN3	Unmounted	1	-
21	-	J1,J2	Unmounted	2	-
22	-	SPVDD	Unmounted	1	-
23	-	R3	Unmounted	1	-
24	-	TH1,TH2,TH3,TH4	Unmounted	4	-
25	-	U3	Unmounted	1	-
26	-	U4	Unmounted	1	-
27	-	U5	Unmounted	1	-
28	-	XT1	Unmounted	1	-



LAPIS Semiconductor Co., Ltd.	
RB-S22Q53xTB48	
APPLICATION ML22Q53x-MNNTB Reference Board	
DWG No.	QTS-11765
SHEET	1 of 1
Rev.	1.1

3.4. CN1

CN1 is a 40-pin connector that is used to connect to the SDCB3.

3.5. CN2

CN2 is a 30-pin connector to which ML22Q532/ML22Q533/ML22Q535 terminals are connected.

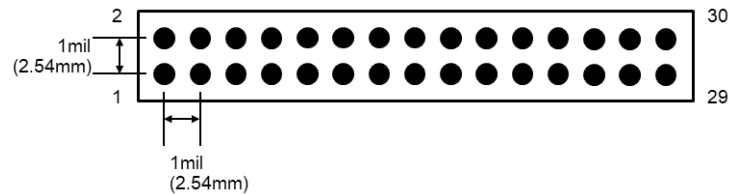


Figure 3 CN2 connectors hole pattern

Table 2 CN2 connector pin connections

CN2 Pin No	Connect LSI	LSI Pin No	LSI Pin Name	
1	VDD (3V)	ML22Q532/ML22Q533/ML22Q535	26	DVDD
2	VDD (3V)	ML22Q532/ML22Q533/ML22Q535	26	DVDD
3	I/O	ML22Q532/ML22Q533/ML22Q535	43	RESETB
4	I/O	ML22Q532/ML22Q533/ML22Q535	44	TEST0
5	I/O	ML22Q532/ML22Q533/ML22Q535	45	STATUS1
6	I/O	ML22Q532/ML22Q533/ML22Q535	46	STATUS2
7	I/O	ML22Q532/ML22Q533/ML22Q535	47	CBUSYB
8	I/O	-	-	-
9	I/O	ML22Q532/ML22Q533/ML22Q535	2	SCL
10	I/O	ML22Q532/ML22Q533/ML22Q535	3	SDA
11	I/O	ML22Q532/ML22Q533/ML22Q535	8	CSB
12	I/O	ML22Q532/ML22Q533/ML22Q535	9	SCK
13	I/O	ML22Q532/ML22Q533/ML22Q535	10	SI
14	I/O	ML22Q532/ML22Q533/ML22Q535	11	SO
15	GND	ML22Q532/ML22Q533/ML22Q535	1, 25	DGND
16	GND	ML22Q532/ML22Q533/ML22Q535	1, 25	DGND
17	I/O	ML22Q532/ML22Q533/ML22Q535	13	IRCSB
18	I/O	ML22Q532/ML22Q533/ML22Q535	14	IRSCK
19	I/O	ML22Q532/ML22Q533/ML22Q535	15	IRSO
20	I/O	ML22Q532/ML22Q533/ML22Q535	16	IRSI
21	I/O	ML22Q532/ML22Q533/ML22Q535	17	IRON
22	I/O	-	-	-
23	IOVDD	ML22Q532/ML22Q533/ML22Q535	18	IOVDD
24	VDDR	ML22Q532/ML22Q533/ML22Q535	19	VDDR
25	GND	ML22Q532/ML22Q533/ML22Q535	1, 25	DGND
26	GND	ML22Q532/ML22Q533/ML22Q535	1, 25	DGND
27	I/O	ML22Q532/ML22Q533/ML22Q535	23	XTB
28	I/O	ML22Q532/ML22Q533/ML22Q535	24	XT
29	GND	ML22Q532/ML22Q533/ML22Q535	1, 25	DGND
30	GND	ML22Q532/ML22Q533/ML22Q535	1, 25	DGND

3.6. CN3

The CN3 is an 8-pin connector to which the ML22Q532/ML22Q533/ML22Q535 serial audio interface terminals are connected.

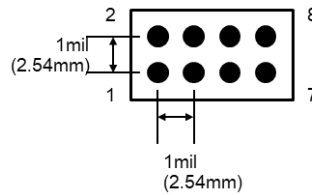


Figure 4 CN3 connectors hole pattern

Table 3 CN3 connector pin connections

CN3 Pin No	Connect LSI	LSI Pin No	LSI Pin Name
1	VDD (3V)	ML22Q532/ML22Q533/ML22Q535	26 DVDD
2	VDD (3V)	ML22Q532/ML22Q533/ML22Q535	26 DVDD
3	I/O	ML22Q532/ML22Q533/ML22Q535	4 LRCLK
4	I/O	ML22Q532/ML22Q533/ML22Q535	5 BCLK
5	I/O	ML22Q532/ML22Q533/ML22Q535	6 SAI_IN
6	I/O	ML22Q532/ML22Q533/ML22Q535	7 SAI_OUT
7	GND	ML22Q532/ML22Q533/ML22Q535	1, 25 DGND
8	GND	ML22Q532/ML22Q533/ML22Q535	1, 25 DGND

3.7. LOUT jack

LOUT is a jack to which the ML22Q532/ML22Q533/ML22Q535 line-amp outputs are connected via a speaker amplifier.

3.8. SP jack

SP is the jack to which ML22Q532/ML22Q533/ML22Q535 speaker amplifier outputs are connected.

3.9. AIN, GND terminal

This terminal is connected to the ML22Q532/ML22Q533/ML22Q535 speaker amplifier input terminal. Input a speaker amplifier input signal between the AIN pin and GND pin.

3.10. Ceramic resonator, External Clock

Ceramic resonator can be mounted on a XT1. Table 4 table shows the ceramic resonators used.

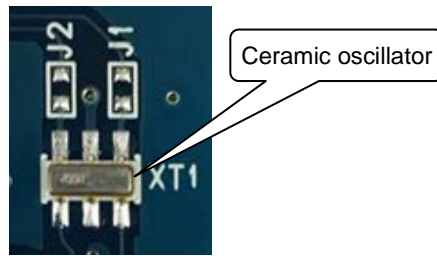


Figure 5 Ceramic resonator

Table 4 Ceramic resonator

Vendor	Frequency[Hz]	Parts Number
Murata Manufacturing Co., Ltd.	4M	CSTCR4M00G55B-R0
Murata Manufacturing Co., Ltd.	4.096M	CSTCR4M09G55B-R0

External clocks can be entered from the CN2's 28 pins. Connect between J1 terminals.

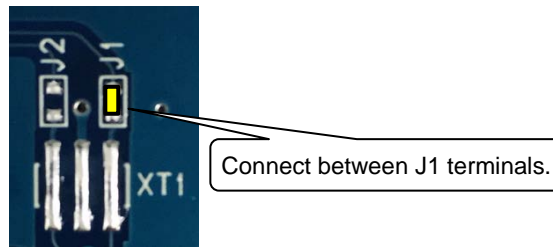


Figure 6 External clock

Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEBL22Q53xRB-01	October 31, 2019	–	–	First edition.
FEBL22Q53xRB-03	March 26, 2020	3	3	3.3. BOM list, Schematic

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