

RS1P600BH

Nch 100V 60A Power MOSFET

V _{DSS}	100V
R _{DS(on)} (Max.)	8.8mΩ
I _D	±60A
P_D	35W

Features

- 1) Low on resistance
- 2) Small Surface Mount Package
- 3) Pb-free plating; RoHS compliant
- 4) Halogen free
- 5) 100% Rg and UIS tested

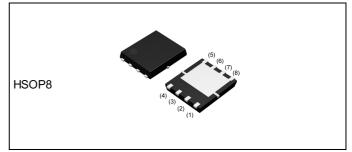
Application

Primary side switch

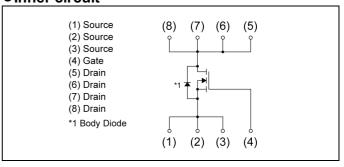
Moter drives

DC/DC converter

Outline



●Inner circuit



Packaging specifications

	ing opcomoducino	
	Packing	Embossed Tape
	Reel size (mm)	330
Type	Tape width (mm)	12
	Quantity (pcs)	2500
	Taping code	TB1
	Marking	RS1P600BH

● **Absolute maximum ratings** (T_a = 25°C ,unless otherwise specified)

Parameter	Symbol	Value	Unit	
Drain - Source voltage	V_{DSS}	100	V	
Continuous dunin suument	T _c = 25°C	I _D *1	±60	А
Continuous drain current	T _a = 25°C	I _D	±18	Α
Pulsed drain current	I _{DP} *2	±72	Α	
Gate - Source voltage	V_{GSS}	±20	V	
Avalanche current, single pulse		I _{AS} *3	18	Α
Avalanche energy, single pulse		E _{AS} *3	26	mJ
Dawar diagination		P _D *1	35	W
Power dissipation		P _D *4	3.0	W
Junction temperature	T _j	150	°C	
Operating junction and storage te	T _{stg}	-55 to +150	°C	

●Thermal resistance

Dorameter	Curah al	Values			1.1-:4
Parameter	Symbol	Min.	Тур.	Max.	Unit
Thermal resistance, junction - case	R _{thJC} *1	-	-	3.5	°C/W
Thermal resistance, junction - ambient	R _{thJA} *4	-	-	41.7	°C/W

● Electrical characteristics (T_a = 25°C)

Davanastan	Cymaele ed	Conditions	Values			Lleit	
Parameter	Symbol Conditions		Min.	Тур.	Max.	Unit	
Drain - Source breakdown voltage	V _{(BR)DSS}	$V_{GS} = 0V$, $I_D = 1mA$	100	-	-	V	
Breakdown voltage temperature coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_{j}}$	I _D = 1mA referenced to 25°C	-	62.3	-	mV/°C	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100V, V _{GS} = 0V	-	-	5	μA	
Gate - Source leakage current	I _{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	1	1	±500	nA	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1mA$	2.0	-	4.0	V	
Gate threshold voltage temperature coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_j}$	I _D = 1mA referenced to 25°C	-	-4.5	-	mV/°C	
Static drain - source	D *5	V _{GS} = 10V, I _D = 18A	-	6.7	8.8		
on - state resistance	R _{DS(on)} *5	V _{GS} = 6V, I _D = 18A	-	8.6	12.9	mΩ	
Gate resistance	R_G	-	0.6	1.2	3.6	Ω	
Forward Transfer Admittance	Y _{fs} *5	V _{DS} = 5V, I _D = 18A	16	-	-	S	

^{*1}T_c =25°C, Limited only by maximum temperature allowed.

^{*2} Pw ≤ 10µs, Duty cycle ≤ 1%

^{*3} L \simeq 0.1mH, V_{DD} = 50V, R_G = 25 Ω , Starting T_j = 25 $^{\circ}$ C Fig.3-1,3-2

^{*4} Mounted on a Cu board (40×40×0.8mm)

^{*5} Pulsed

● Electrical characteristics (T_a = 25°C)

Dorameter	Symbol	Conditions		Unit		
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Input capacitance	C _{iss}	V _{GS} = 0V	*1020	2040	*4080	
Output capacitance	C _{oss}	V _{DS} = 50V	*195	390	*780	pF
Reverse transfer capacitance	C _{rss}	f = 1MHz	*9	18	*36	
Turn - on delay time	t _{d(on)} *5	V _{DD} ≈ 50V,V _{GS} = 10V	-	26	-	
Rise time	t r*5	I _D = 9A	-	30	-	no
Turn - off delay time	t _{d(off)} *5	$R_L \simeq 5.5\Omega$	_	46	-	ns
Fall time	t _f *5	$R_G = 10\Omega$	-	23	-	

^{*:} Guarantee of Design

● Gate charge characteristics (T_a = 25°C)

Darameter	Symbol	Canditions		Values			Unit
Parameter	Symbol Conditions		Oris	Min.	Тур.	Max.	Offic
Total gate charge	O *5		V _{GS} = 10V	*16.0	32.0	*64.0	
Total gate charge	Q_g^{*5}	$V_{DD} \simeq 50V$		*10.5	21.0	*42.0	»C
Gate - Source charge	Q _{gs} *5	I _D = 18A	V _{GS} = 6V	*3.6	7.2	*14.4	nC
Gate - Drain charge	Q _{gd} *5			*4.1	8.3	*16.6	

^{*:} Guarantee of Design

● Body diode electrical characteristics (Source-Drain) (T_a = 25°C)

Darameter	Cumbal	Conditions		Values	Unit	
Parameter	Symbol	symbol Conditions		Тур.	Max.	Offic
Continuous forward current	I _S	T = 25°C	1	-	2.5	Α
Pulse forward current	I _{SP} *2	T _a = 25°C	-	-	72	Α
Forward voltage	V _{SD} *5	$V_{GS} = 0V, I_S = 2.5A$	-	-	1.2	V
Reverse recovery time	t _{rr} *5	I _S = 18A, V _{GS} =0V	-	63	-	ns
Reverse recovery charge	Q _{rr} *5	di/dt = 100A/μs	-	120	-	nC

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Fig.1 Power Dissipation Derating Curve

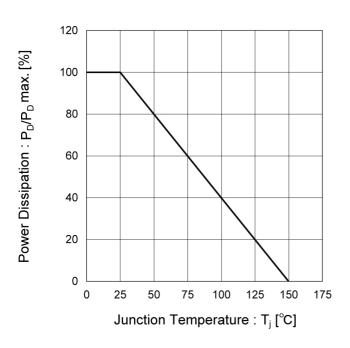
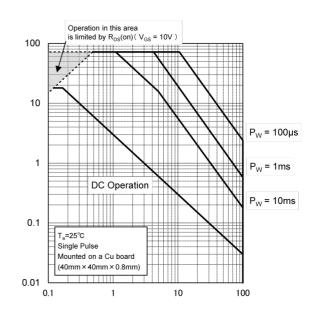


Fig.2 Maximum Safe Operating Area



Drain Current : I_D [A]

Drain - Source Voltage : V_{DS} [V]

Fig.3 Normalized Transient Thermal Resistance vs. Pulse Width

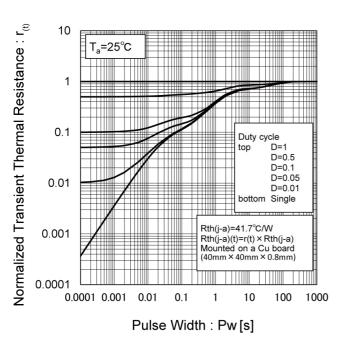


Fig.4 Single Pulse Maximum Power Dissipation

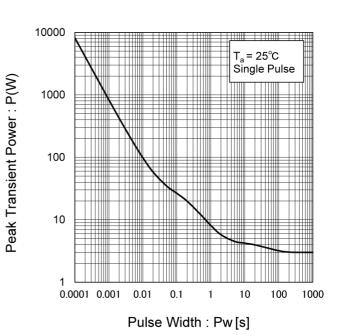


Fig.5 Typical Output Characteristics(I)

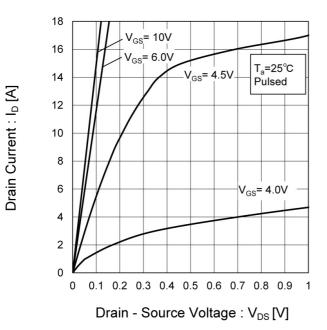
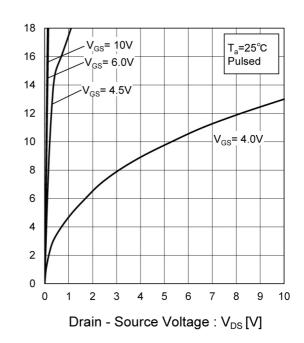


Fig.6 Typical Output Characteristics(II)



Drain Current : I_D [A]

Fig.7 Breakdown Voltage vs.
Junction Temperature

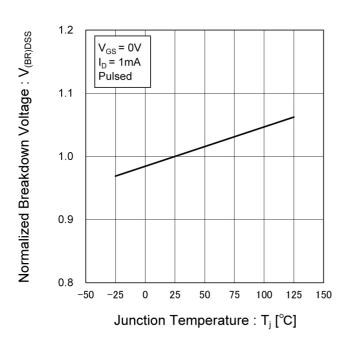


Fig.8 Typical Transfer Characteristics

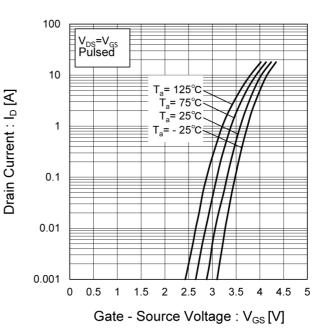


Fig.9 Gate Threshold Voltage vs.
Junction Temperature

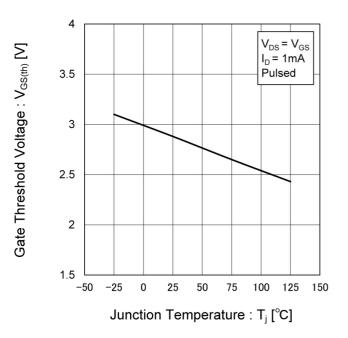


Fig.10 Forward Transfer Admittance vs.
Drain Current

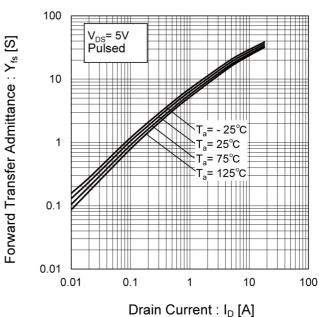


Fig.11 Drain Current Derating Curve

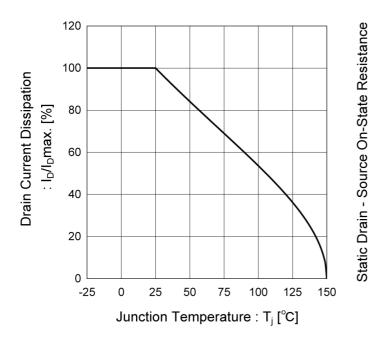


Fig.12 Static Drain - Source On - State Resistance vs. Gate Source Voltage

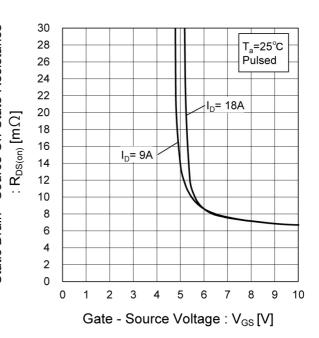


Fig.13 Static Drain - Source On - State Resistance vs. Junction Temperature

Static Drain - Source On-State Resistance 19 V_{GS} = 10V 18 Pulsed 17 16 15 14 13 12 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}\left[\mathsf{m}\Omega
ight]$ 11 10 9 8 7 6 I_D = 18A 5 4 3 2 1 0 -50 -25 0 25 50 75 100 125 150 Junction Temperature : T_j [°C]

Fig.14 Static Drain - Source On - State
Resistance vs. Drain Current (I)

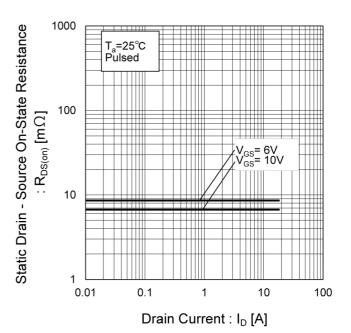


Fig.15 Static Drain - Source On - State Resistance vs. Drain Current (II)

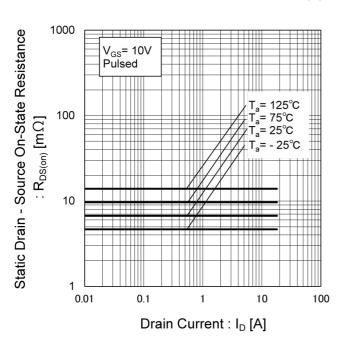


Fig.16 Static Drain - Source On - State Resistance vs. Drain Current (III)

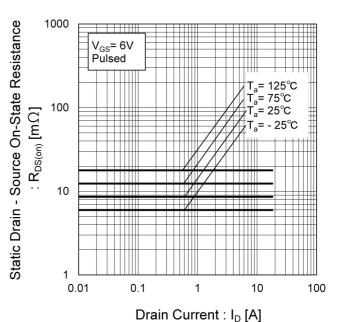


Fig.17 Typical Capacitances vs.

Drain - Source Voltage

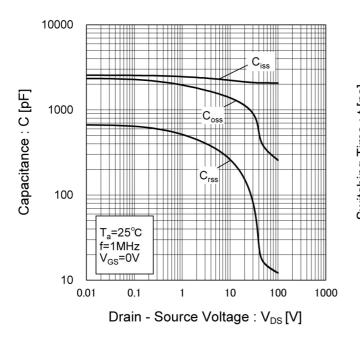


Fig.18 Switching Characteristics

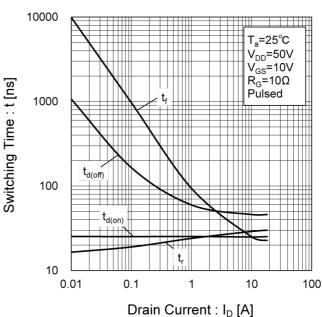


Fig.19 Typical Gate Charge

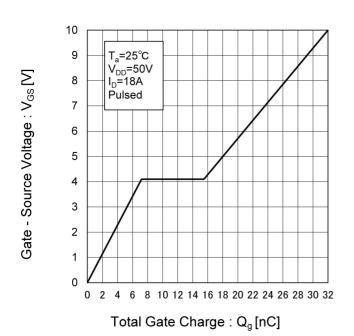
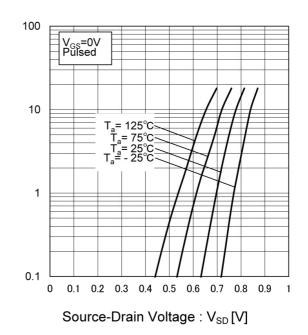


Fig.20 Source Current vs.

Source Drain Voltage



Source Current : Is [A]

Measurement circuits

Fig.1-1 Switching Time Measurement Circuit

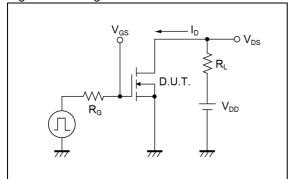


Fig.1-2 Switching Waveforms

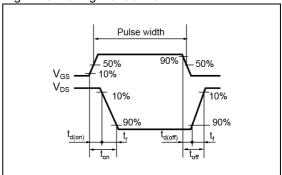


Fig.2-1 Gate Charge Measurement Circuit

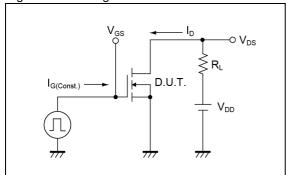


Fig.2-2 Gate Charge Waveform

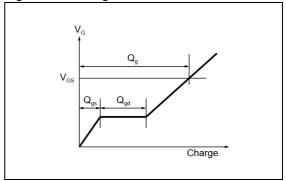


Fig.3-1 Avalanche Measurement Circuit

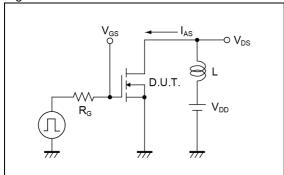
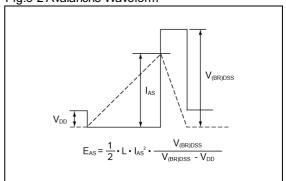


Fig.3-2 Avalanche Waveform

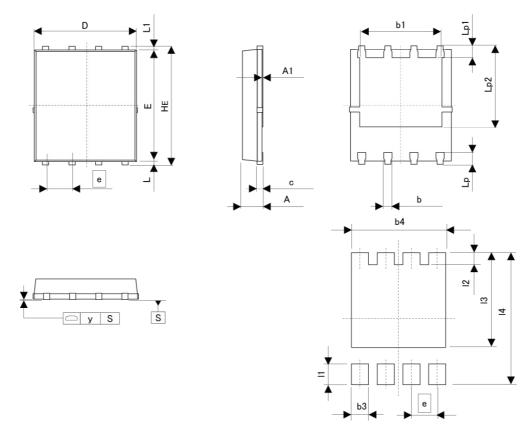


Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Dimensions

HSOP8 (TB1)



Pattern of terminal position areas [Not a recommended pattern of soldering pads]

DIM	MILIME	ETERS	INC	HES
DIIVI	MIN	MAX	MIN	MAX
Α	0.90	1.10	0.035	0.043
A1	0.00	0.05	0.000	0.002
b	0.33	0.42	0.013	0.017
b1	3.61	3.96	0.142	0.156
С	0.20	0.30	0.008	0.012
D	4.80	5.00	0.189	0.197
E	5.70	5.80	0.224	0.228
е	1.	27	0.0)50
HE	5.90	6.10	0.232	0.240
L	0.06	0.20	0.002	0.008
L1	0.06	0.20	0.002	0.008
Lp	0.51	0.71	0.020	0.028
Lp1	0.41	0.61	0.016	0.024
Lp2	3.79	4.39	0.149	0.173

DIM	MILIME	TERS	INC	HES
DIIVI	MIN	MAX	MIN	MAX
b3	-	0.68	-	0.027
b4	1	4.06	-	0.160
I1	-	0.81	-	0.032
12	•	0.71	-	0.028
13	•	4.49	ī	0.177
14	-	6.20	-	0.244

Dimension in mm/inches



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 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- 1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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- 1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
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Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

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- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- Even under ROHM recommended storage condition, solderability of products out of recommended storage time period
 may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is
 exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Notice-PGA-E Rev.004

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