

# 4V Drive Nch MOSFET

## RSD200N05

### ●Structure

Silicon N-channel MOSFET

### ●Features

- 1) Low on-resistance.
- 2) Fast switching speed.
- 3) Drive circuits can be simple.
- 4) Parallel use is easy.

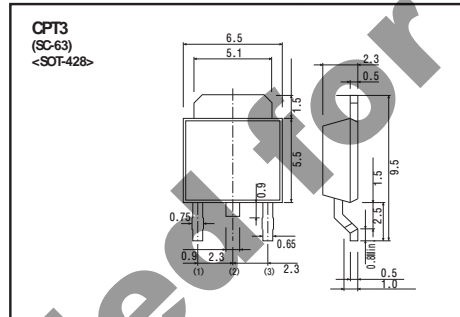
### ●Application

Switching

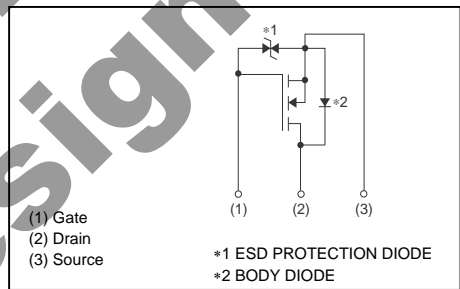
### ●Packaging specifications

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	2500
RSD200N05		○

### ●Dimensions (Unit : mm)



### ●Inner circuit



### ●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Drain-source voltage	$V_{DSS}$	45	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	Continuous	$I_D$	$\pm 20$ A
	Pulsed	$I_{DP}$ *1	$\pm 40$ A
Source current (Body Diode)	Continuous	$I_S$	16 A
	Pulsed	$I_{SP}$ *1	40 A
Power dissipation	$P_D$ *2	20	W
Channel temperature	$T_{ch}$	150	°C
Range of storage temperature	$T_{stg}$	-55 to +150	°C

\*1  $P_W \leq 10 \mu s$ , Duty cycle  $\leq 1\%$

\*2  $T_c = 25^\circ C$

### ●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to Case	$R_{th(ch-c)}$ *	6.25	°C / W

\*  $T_c = 25^\circ C$

●Electrical characteristics (T<sub>a</sub> = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	-	-	±10	μA	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	45	-	-	V	I <sub>D</sub> =1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> =45V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	1.0	-	2.5	V	V <sub>DS</sub> =10V, I <sub>D</sub> =1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	-	20	28	mΩ	I <sub>D</sub> =20A, V <sub>GS</sub> =10V
		-	25	35		I <sub>D</sub> =20A, V <sub>GS</sub> =4.5V
		-	28	40		I <sub>D</sub> =20A, V <sub>GS</sub> =4.0V
Forward transfer admittance	Y <sub>fs</sub>  *	10	-	-	S	I <sub>D</sub> =20A, V <sub>DS</sub> =10V
Input capacitance	C <sub>iss</sub>	-	950	-	pF	V <sub>DS</sub> =10V
Output capacitance	C <sub>oss</sub>	-	250	-	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	-	120	-	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	-	10	-	ns	I <sub>D</sub> =10A, V <sub>DD</sub> =25V
Rise time	t <sub>r</sub> *	-	20	-	ns	V <sub>GS</sub> =10V
Turn-off delay time	t <sub>d(off)</sub> *	-	50	-	ns	R <sub>L</sub> =2.5Ω
Fall time	t <sub>f</sub> *	-	20	-	ns	R <sub>G</sub> =10Ω
Total gate charge	Q <sub>g</sub> *	-	12	-	nC	V <sub>DD</sub> =25V
Gate-source charge	Q <sub>gs</sub> *	-	3.5	-	nC	I <sub>D</sub> =20A,
Gate-drain charge	Q <sub>gd</sub> *	-	4.0	-	nC	V <sub>GS</sub> =5V

\*Pulsed

●Body diode characteristics (Source-Drain) (T<sub>a</sub> = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V <sub>SD</sub> *	-	-	1.2	V	I <sub>s</sub> =20A, V <sub>GS</sub> =0V

\*Pulsed

●Electrical characteristic curves (Ta=25°C)

Fig.1 Typical Output Characteristics ( I )

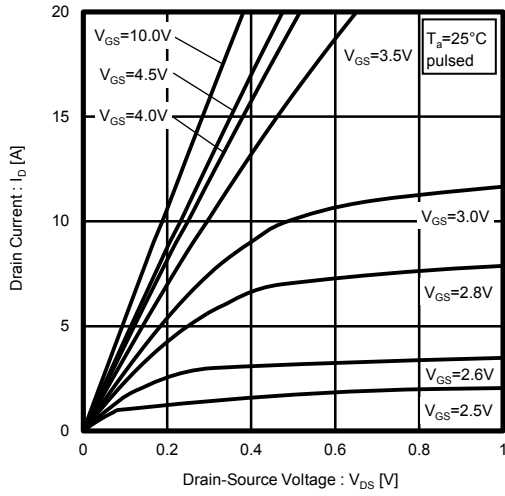


Fig.2 Typical Output Characteristics ( II )

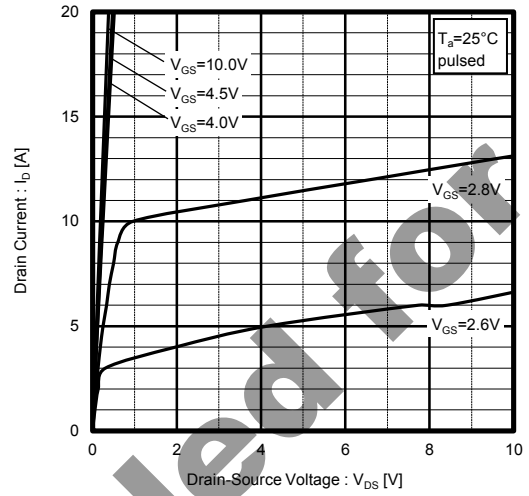


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

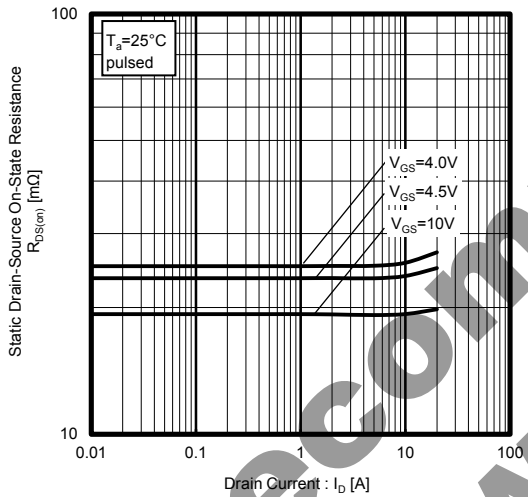


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

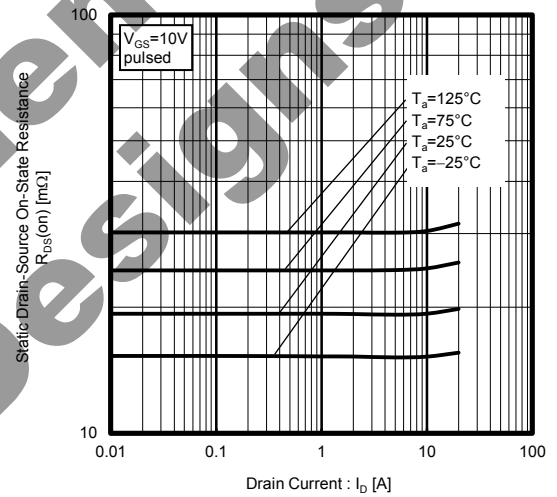


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

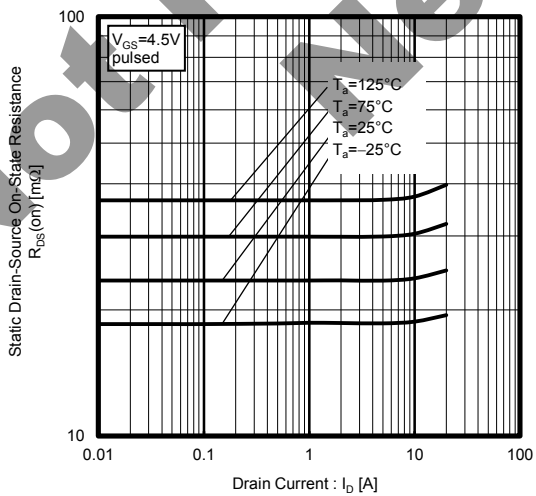


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

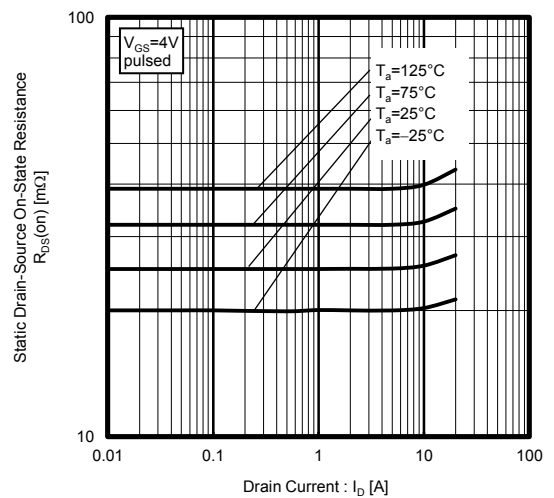


Fig.7 Forward Transfer Admittance vs. Drain Current

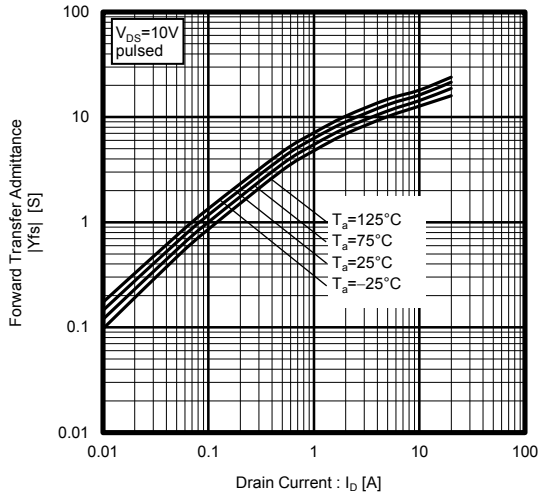


Fig.8 Typical Transfer Characteristics

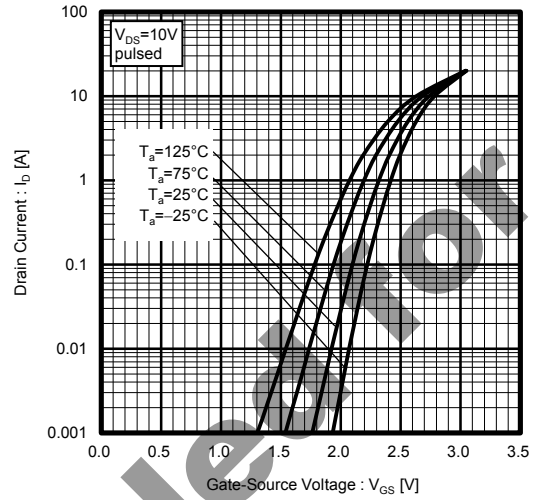


Fig.9 Source Current vs. Source-Drain Voltage

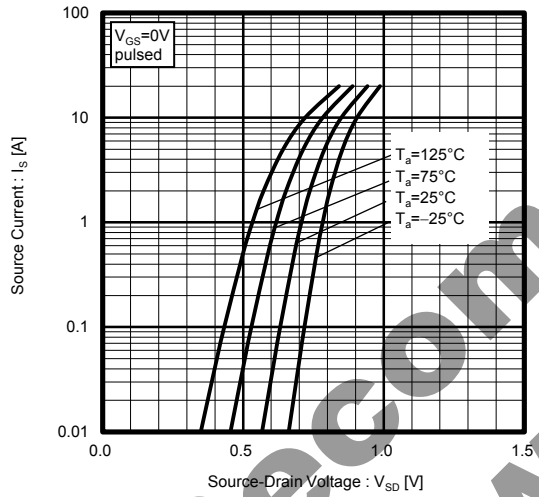


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

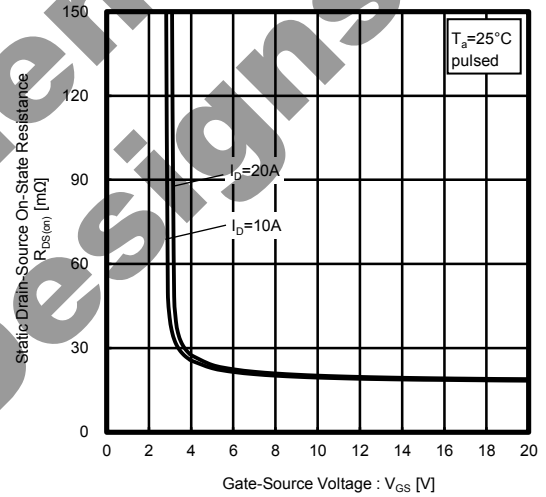


Fig.11 Switching Characteristics

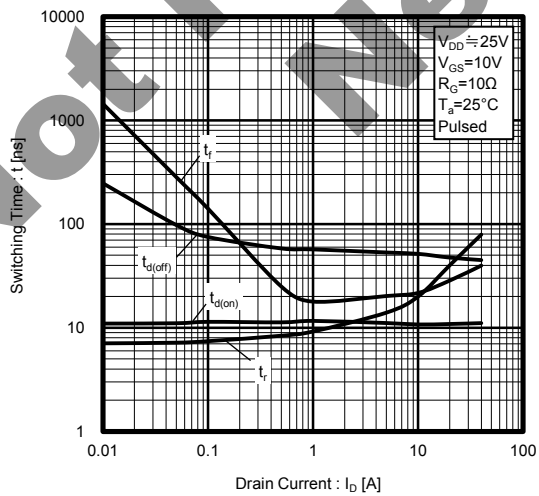


Fig.12 Dynamic Input Characteristics

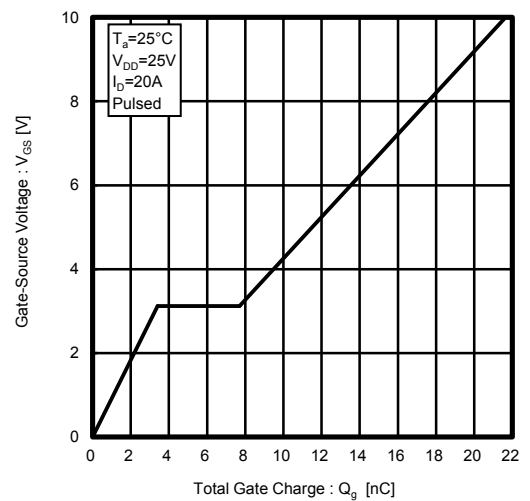


Fig.13 Typical Capacitance vs. Drain-Source Voltage

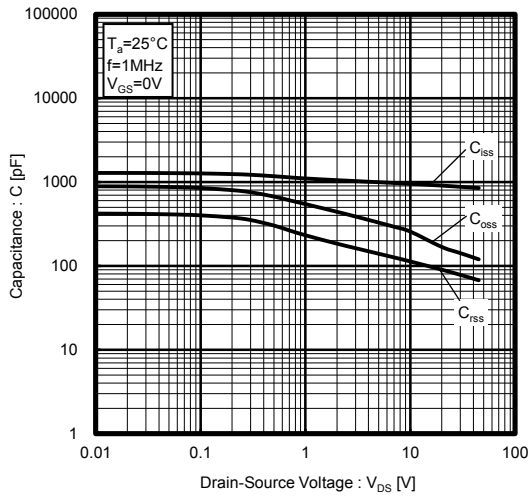


Fig.14 Maximum Safe Operating Area

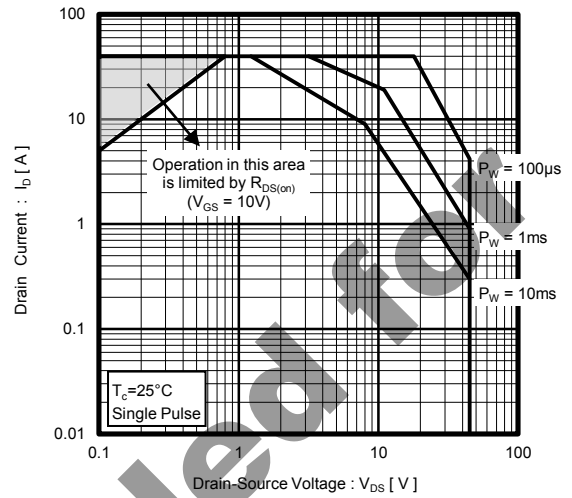
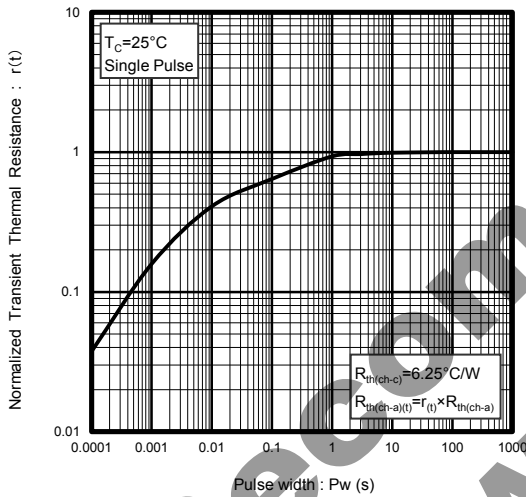


Fig.15 Normalized Transient Thermal Resistance v.s. Pulse Width



Not Recommended for New Designs

● Measurement circuits

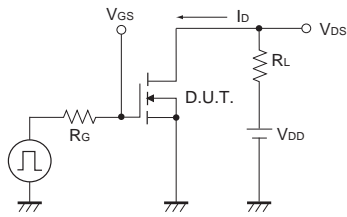


Fig.1-1 Switching Time Measurement Circuit

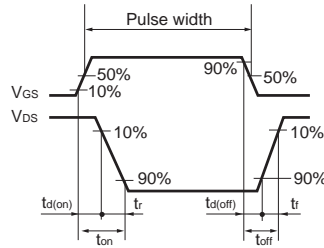


Fig.1-2 Switching Waveforms

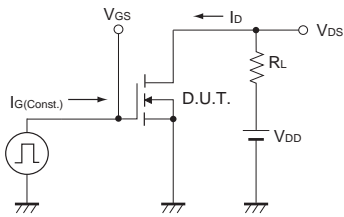


Fig.2-1 Gate Charge Measurement Circuit

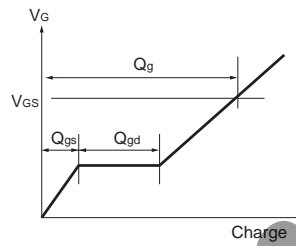


Fig.2-2 Gate Charge Waveform

Not Recommended for New Designs

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