1.5V Drive Pch MOSFET

RW1A025AP

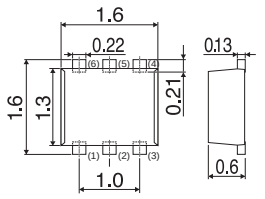
● Structure
Silicon P-channel MOSFET

● Features
1) Low On-resistance.
2) Small high power package.
3) Low voltage drive.(1.5V)

● Application
Switching

● Dimensions (Unit : mm)

WEMT6

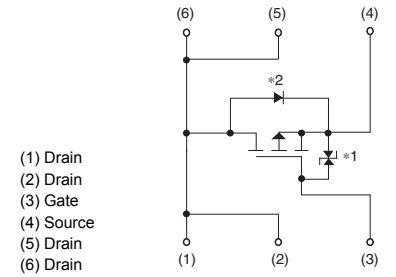


Abbreviated symbol : SD

● Packaging specifications

Type	Package	Taping
	Code	T2CR
	Basic ordering unit (pieces)	8000
RW1A025AP		O

● Inner circuit



*1 ESD PROTECTION DIODE
*2 BODY DIODE

● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	−12	V
Gate-source voltage		V_{GSS}	0 to −8	V
Drain current	Continuous	I_D	±2.5	A
	Pulsed	I_{DP} *1	±7.5	A
Source current (Body Diode)	Continuous	I_S	−0.5	A
	Pulsed	I_{SP} *1	−7.5	A
Power dissipation		P_D *2	0.7	W
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	−55 to +150	°C

*1 Pw≤10μs, Duty cycle≤1%

*2 Mounted on a ceramic board.

● Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to Ambient	Rth (ch-a)*	179	°C / W

*Mounted on a ceramic board.

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● **Electrical characteristics** (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	−10	μA	V_{GS}=−8V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	−12	-	-	V	I_D=−1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	-	-	−10	μA	V_{DS}=−12V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	−0.3	-	−1.0	V	V_{DS}=−6V, I_D=−1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	-	44	62	mΩ	I_D=−2.5A, V_{GS}=−4.5V
		-	55	77		I_D=−1.2A, V_{GS}=−2.5V
		-	75	110		I_D=−1.2A, V_{GS}=−1.8V
		-	90	180		I_D=−0.5A, V_{GS}=−1.5V
Forward transfer admittance	$\|Y_{fs}\|$*	3.5	-	-	S	I_D=−2.5A, V_{DS}=−6V
Input capacitance	C_{iss}	-	2000	-	pF	V_{DS}=−6V
Output capacitance	C_{oss}	-	130	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	120	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$*	-	11	-	ns	I_D=−1.2A, V_{DD}≒−6V
Rise time	t_r *	-	40	-	ns	V_{GS}=−4.5V
Turn-off delay time	$t_{d(off)}$*	-	160	-	ns	R_L=5Ω
Fall time	t_f *	-	60	-	ns	R_G=10Ω
Total gate charge	Q_g*	-	16	-	nC	I_D=−2.5A
Gate-source charge	Q_{gs}*	-	2.4	-	nC	V_{DD}≒−6V
Gate-drain charge	Q_{gd}*	-	2.2	-	nC	V_{GS}=−4.5V

*Pulsed

●**Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}*	-	-	−1.2	V	I_s=−2.5A, V_{GS}=0V

*Pulsed

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●Electrical characteristic curves (Ta=25°C)

Fig.1 Typical output characteristics(Ⅰ)

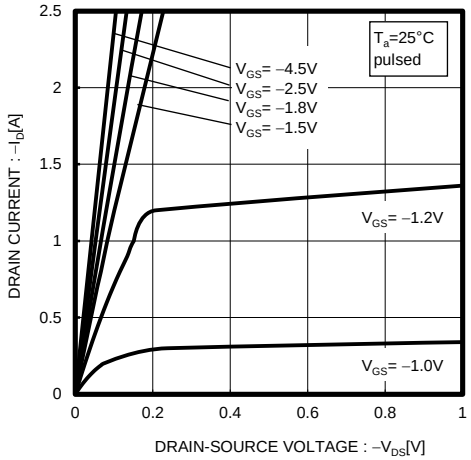

Fig.2 Typical output characteristics(Ⅱ)

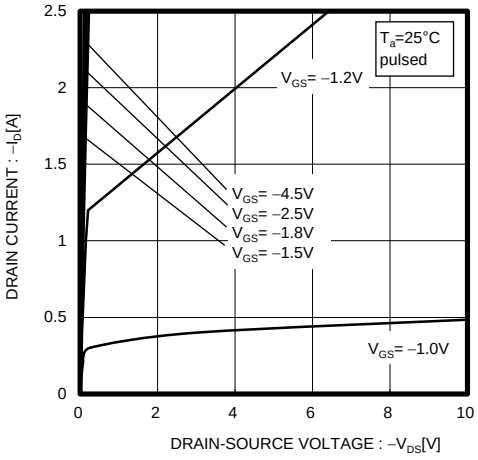

Fig.3 Typical Transfer Characteristics

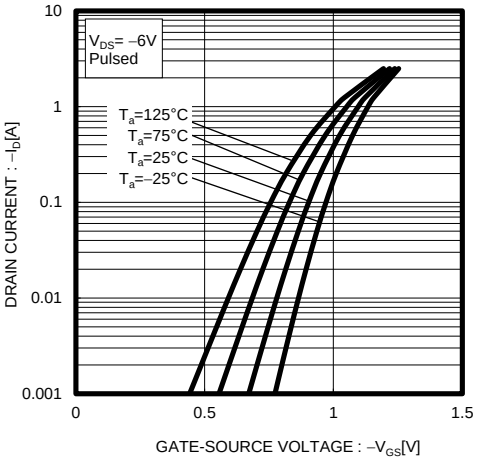

Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

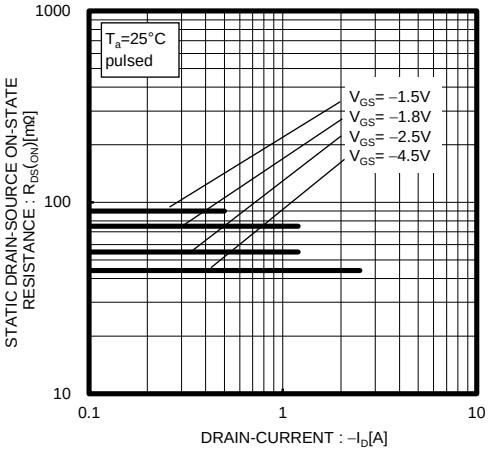

Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

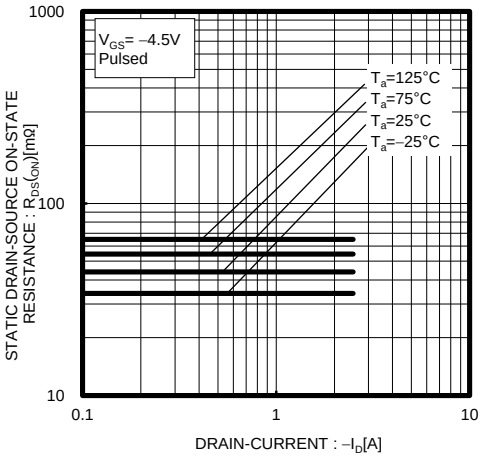

Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

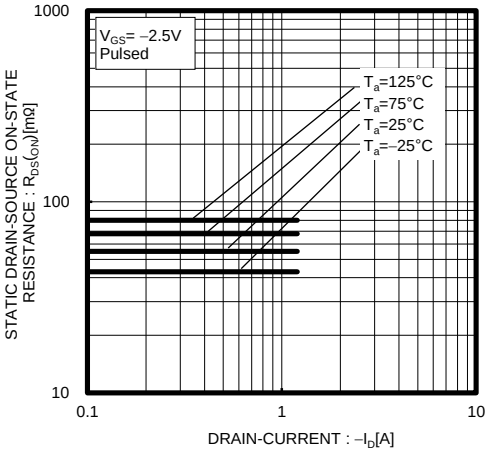

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Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

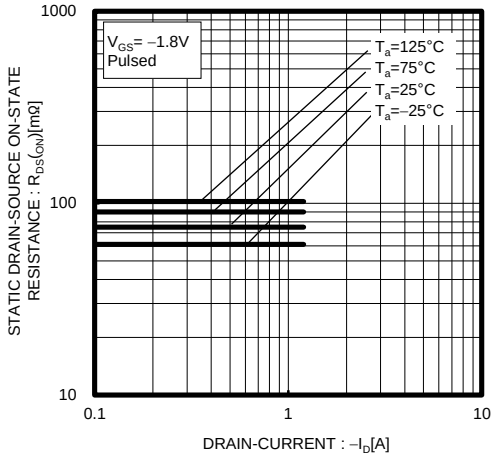

Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(Ⅴ)

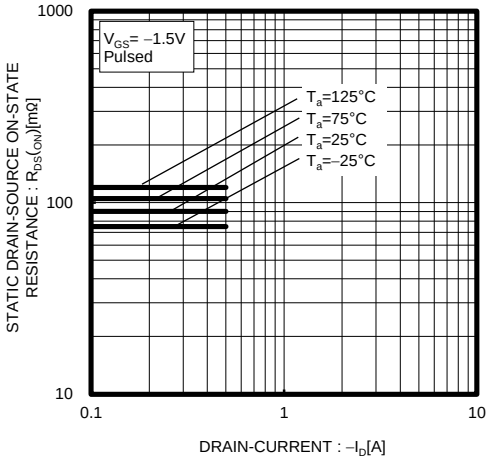

Fig.9 Forward Transfer Admittance vs. Drain Current

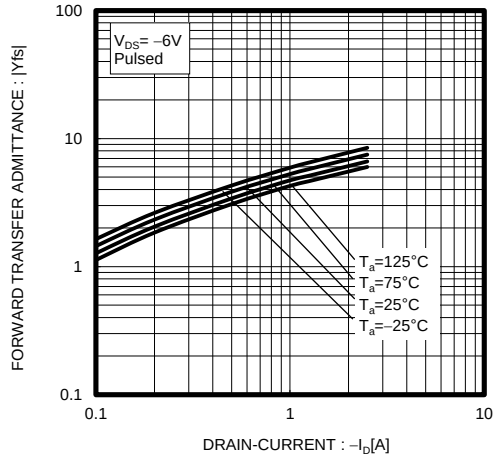

Fig.10 Reverse Drain Current vs. Sourse-Drain Voltage

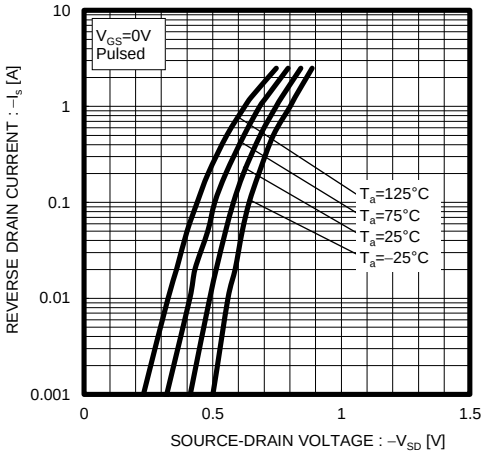

Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

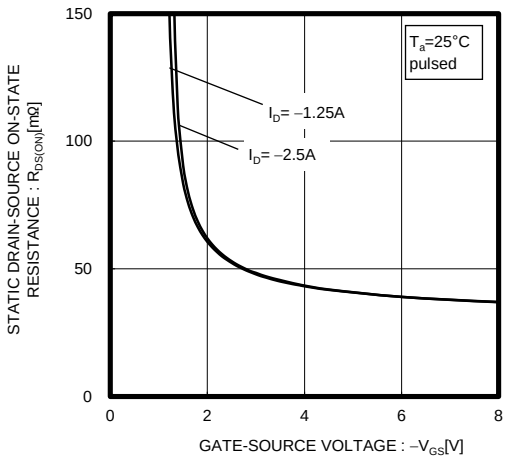

Fig.12 Switching Characteristics

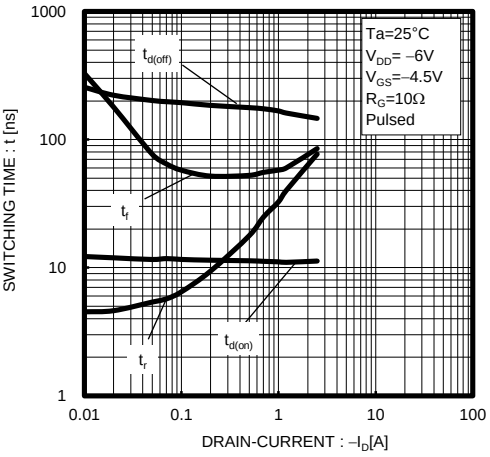

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Fig.12 Dynamic Input Characteristics

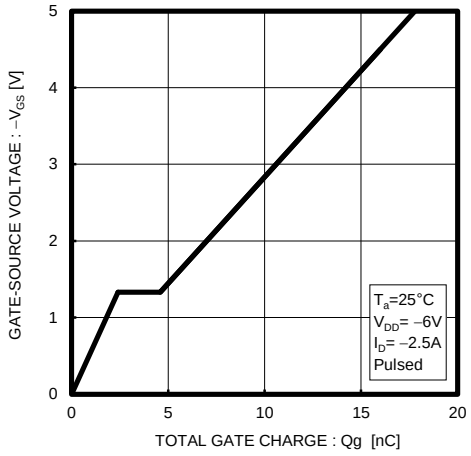
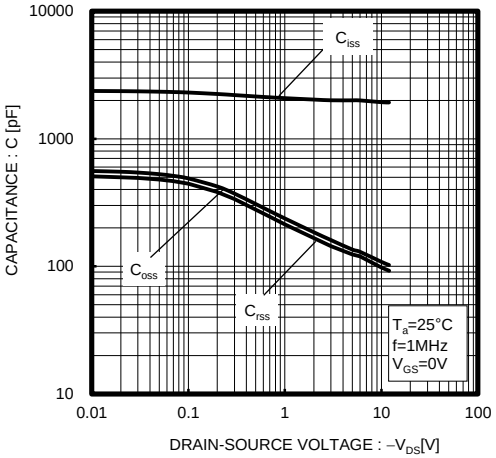


Fig.13 Typical Capacitance vs. Drain-Source Voltage



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● **Measurement circuits**

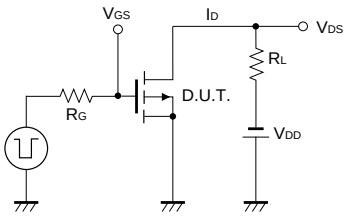

Fig.1-1 Switching Time Measurement Circuit

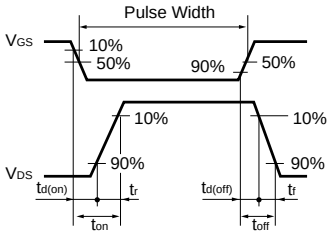

Fig.1-2 Switching Waveforms

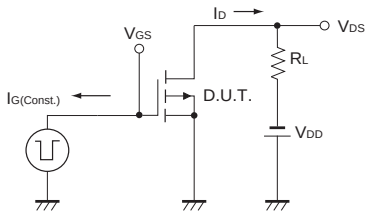

Fig.2-1 Gate Charge Measurement Circuit

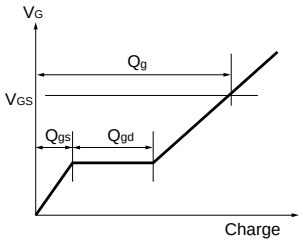

Fig.2-2 Gate Charge Waveform

● **Notice**

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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