4V Drive Nch+Nch MOS FET

SM6K2

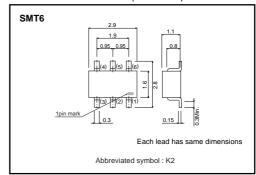
Structure

Silicon N-channel MOSFET transistor

●Features

- 1) Two RHU002N06 chips in a SMT package.
- 2) Mounting possible with SMT3 automatic mounting machines.
- 3) Transistor elements are independent, eliminating mutual interference.
- 4) Mounting cost and area can be cut in half.

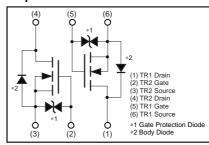
●External dimensions (Unit : mm)



Packaging specifications

	Package	Taping
	Code	T110
Туре	Basic ordering unit (pieces)	3000
SM6K2		0

●Equivalent circuit



A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use.
Use the protection circuit when fixed voltages are exceeded.

● Absolute maximum ratings (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit
Drain-source voltage		VDSS	60	V
Gate-source voltage		Vgss	±20	V
Desir success	Continuous	ΙD	200	mA
Drain current	Pulsed	IDP *1	800	mA
Drain reverse current	Continuous	Idr	200	mA
	Pulsed	IDRP *1	800	mA
Total power dissipation		Pp *2	300	mW / TOTAL
		FD	200	mW / ELEMENT
Channel temperature		Tch	150	°C
Storage temperature		Tstg	-55 to +150	°C

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Pth/oh.o*	416.7	°C/W/TOTAL
Charmer to ambient	Rth(ch-a)	625	°C / W / ELEMENT

^{*} With each pin mounted on the recommended lands



^{*1} Pw≤10µs, Duty cycle≤1% *2 With each pin mounted on the recommended lands

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Conditions	
Gate leakage current	Igss	-	-	±10	μΑ	Vgs=±20V, Vps=0V	
Drain-source breakdown voltage	V (BR) DSS	60	_	-	V	In=1mA, Vgs=0V	
Drain cutoff current	IDSS	_	_	1	μΑ	V _{DS} =60V, V _{GS} =0V	
Gate threshold voltage	VGS (th)	1	_	2.5	V	V _{DS} =10V, I _D =1mA	
Drain-source on-state resistance	_ *	-	1.7	2.4	0	In=200mA, Vgs=10V	
	RDS (on)	_	2.8	4.0	Ω	In=200mA, Vgs=4V	
Forward transfer admittance	I Yfs I *	0.1	_	-	S	V _{DS} =10V, I _D =200mA	
Input capacitance	Ciss	-	15	-	pF	Vps=10V	
Output capacitance	Coss	-	8	-	pF	V _{GS} =0V f=1MHz	
Reverse transfer capacitance	Crss	-	4	-	pF		
Turn-on delay time	td (on) *	-	6	-	ns	I _D =100mA, V _{DD} ≒30V V _{GS} =10V	
Rise time	tr *	-	5	-	ns		
Turn-off delay time	td (off) *	-	12	_	ns	RL=300Ω	
Fall time	t _f *	-	95	_	ns	$R_G = 10\Omega$	
Total gate charge	Qg *	_	2.2	4.4	nC	V _{DD} ≒30V	
Gate-source charge	Q _{gs} *	-	0.6	-	nC	Vgs=10V Ip=200mA	
Gate-drain charge	Q _{gd} *	_	0.3	_	nC		

^{*} Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward voltage	V _{SD}	_	-	1.2	V	I _S =200mA, V _{GS} =0V

Electrical characteristic curves

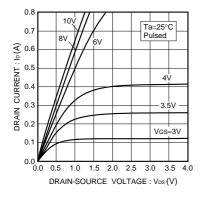


Fig.1 Typical output characteristics

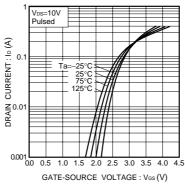


Fig.2 Typical transfer characteristics

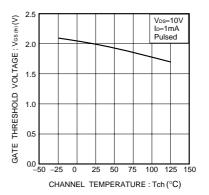


Fig.3 Gate threshold voltage vs. channel temperature

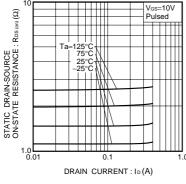


Fig.4 Static drain-source on-State resistance vs. drain current (I)

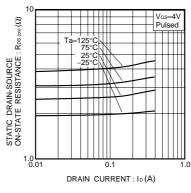


Fig.5 Static drain-source on-state resistance vs. drain current (II)

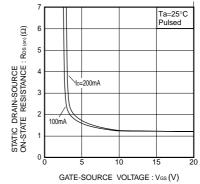


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

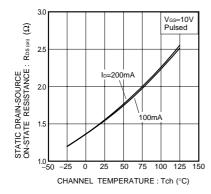


Fig.7 Static drain-source on-state resistance vs. channel temperature

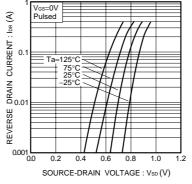


Fig.8 Reverse drain current vs. source-drain voltage (I)

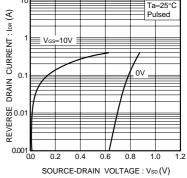


Fig.9 Reverse drain current vs. source-drain voltage (II)

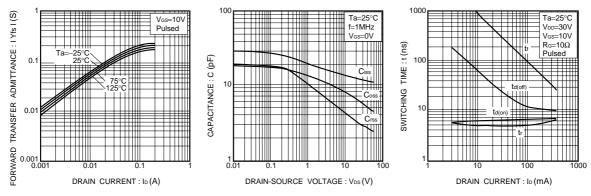


Fig.10 Forward transfer admittance vs. drain current

Fig.11 Typical capacitance vs. drain-source voltage

Fig.12 Switching characteristics

•Switching characteristics measurement circuit

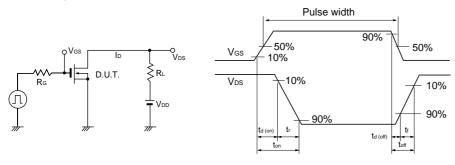


Fig.13 Switching time test circuit

Fig.14 Switching time waveforms

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