

# 4V Drive Nch+Pch MOSFET

## SP8M4

●Structure

Silicon N-channel / P-channel MOSFET

●Features

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (SOP8).

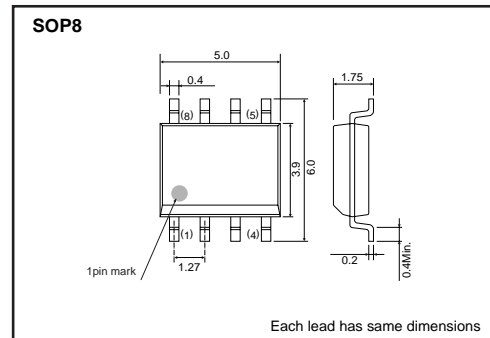
●Application

Power switching, DC / DC converter.

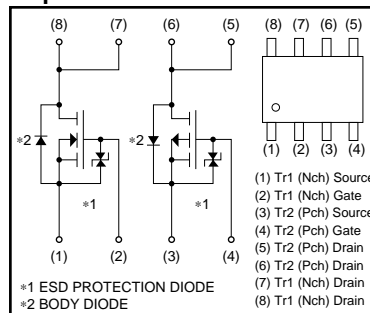
●Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8M4		○

●Dimensions (Unit : mm)



●Equivalent circuit



\*1 ESD PROTECTION DIODE  
 \*2 BODY DIODE  
 (1) Tr1 (Nch) Source  
 (2) Tr1 (Nch) Gate  
 (3) Tr2 (Pch) Source  
 (4) Tr2 (Pch) Gate  
 (5) Tr2 (Pch) Drain  
 (6) Tr2 (Pch) Drain  
 (7) Tr1 (Nch) Drain  
 (8) Tr1 (Nch) Drain

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit	
		Nchannel	Pchannel		
Drain-source voltage	V <sub>DSS</sub>	30	-30	V	
Gate-source voltage	V <sub>GSS</sub>	±20	±20	V	
Drain current	Continuous	I <sub>D</sub>	±9.0	±7.0	A
	Pulsed	I <sub>DP</sub> *1	±36	±28	A
Source current (Body diode)	Continuous	I <sub>S</sub>	1.6	-1.6	A
	Pulsed	I <sub>SP</sub> *1	36	-28	A
Total power dissipation	P <sub>D</sub> *2	2		W	
Channel temperature	T <sub>ch</sub>	150		°C	
Storage temperature	T <sub>stg</sub>	-55 to +150		°C	

\*1 P<sub>w</sub>≤10μs, Duty cycle≤1%  
 \*2 MOUNTED ON A CERAMIC BOARD.

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	R <sub>th (ch-a)*</sub>	62.5	°C / W

\*MOUNTED ON A CERAMIC BOARD.

## Transistors

## N-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	–	–	±10	μA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	30	–	–	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	$I_{DSS}$	–	–	1	μA	$V_{DS}=30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	–	2.5	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	12	18	mΩ	$I_D=9.0A, V_{GS}=10V$
		–	16	24		$I_D=9.0A, V_{GS}=4.5V$
		–	17	25		$I_D=9.0A, V_{GS}=4V$
Forward transfer admittance	$ Y_{fs} $ *	7.0	–	–	S	$I_D=9.0A, V_{DS}=10V$
Input capacitance	$C_{iss}$	–	1190	–	pF	$V_{DS}=10V$
Output capacitance	$C_{oss}$	–	340	–	pF	$V_{GS}=0V$
Reverse transfer capacitance	$C_{rss}$	–	190	–	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	10	–	ns	$I_D=4.5A, V_{DD}\doteq 15V$
Rise time	$t_r$ *	–	15	–	ns	$V_{GS}=10V$
Turn-off delay time	$t_{d(off)}$ *	–	55	–	ns	$R_L=3.33\Omega$
Fall time	$t_f$ *	–	22	–	ns	$R_G=10\Omega$
Total gate charge	$Q_g$ *	–	15	–	nC	$V_{DD}\doteq 15V$
Gate-source charge	$Q_{gs}$ *	–	3.0	–	nC	$V_{GS}=5V$
Gate-drain charge	$Q_{gd}$ *	–	6.1	–	nC	$I_D=9.0A$

\*Pulsed

## ●Body diode characteristics (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	$V_{SD}$ *	–	–	1.2	V	$I_S=6.4A, V_{GS}=0V$

\*Pulsed

## Transistors

## P-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	±10	μA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	–30	–	–	V	I <sub>D</sub> = –1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	–1	μA	V <sub>DS</sub> = –30V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	–1.0	–	–2.5	V	V <sub>DS</sub> = –10V, I <sub>D</sub> = –1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	20	28	mΩ	I <sub>D</sub> = –7.0A, V <sub>GS</sub> = –10V
		–	25	35		I <sub>D</sub> = –3.5A, V <sub>GS</sub> = –4.5V
		–	30	42		I <sub>D</sub> = –3.5A, V <sub>GS</sub> = –4.0V
Forward transfer admittance	Y <sub>fs</sub>   *	6.0	–	–	S	I <sub>D</sub> = –3.5A, V <sub>DS</sub> = –10V
Input capacitance	C <sub>iss</sub>	–	2600	–	pF	V <sub>DS</sub> = –10V
Output capacitance	C <sub>oss</sub>	–	450	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	350	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	20	–	ns	I <sub>D</sub> = –3.5A, V <sub>DD</sub> ≐ –15V
Rise time	t <sub>r</sub> *	–	50	–	ns	V <sub>GS</sub> = –10V
Turn-off delay time	t <sub>d(off)</sub> *	–	110	–	ns	R <sub>L</sub> =4.29Ω
Fall time	t <sub>f</sub> *	–	70	–	ns	R <sub>G</sub> =10Ω
Total gate charge	Q <sub>g</sub> *	–	25	–	nC	V <sub>DD</sub> ≐ –15V
Gate-source charge	Q <sub>gs</sub> *	–	5.5	–	nC	V <sub>GS</sub> = –5V
Gate-drain charge	Q <sub>gd</sub> *	–	10	–	nC	I <sub>D</sub> = –7.0A

\*Pulsed

## ●Body diode characteristics (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub>	–	–	–1.2	V	I <sub>S</sub> = –1.6A, V <sub>GS</sub> =0V

Transistors

N-ch

●Electrical characteristic curves

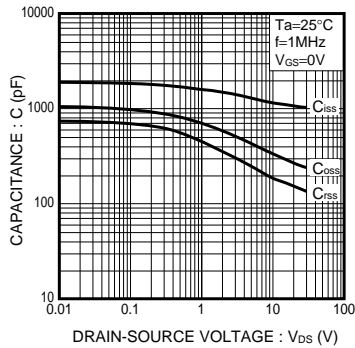


Fig.1 Typical Capacitance vs. Drain-Source Voltage

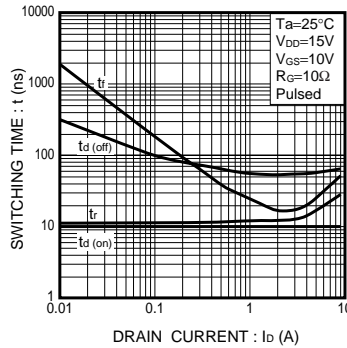


Fig.2 Switching Characteristics

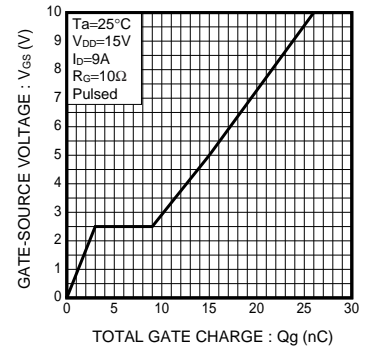


Fig.3 Dynamic Input Characteristics

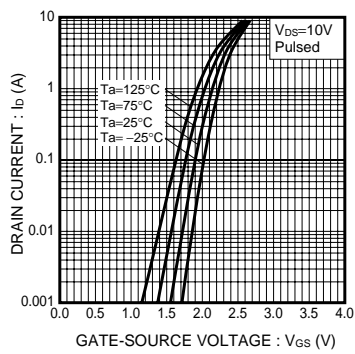


Fig.4 Typical Transfer Characteristics

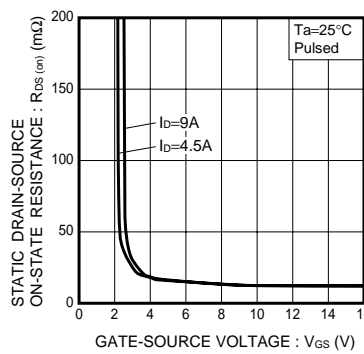


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

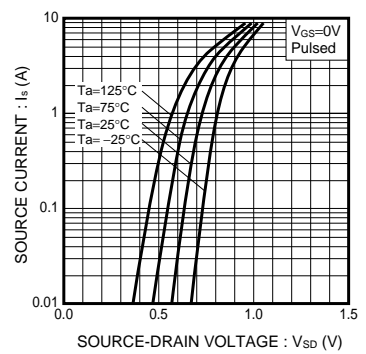


Fig.6 Source Current vs. Source-Drain Voltage

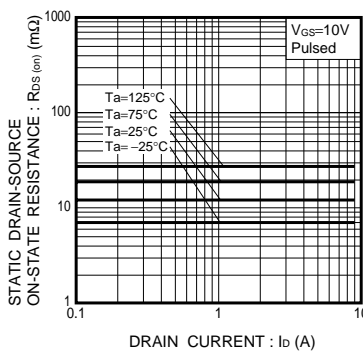


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

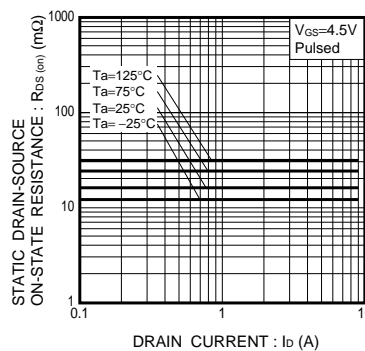


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

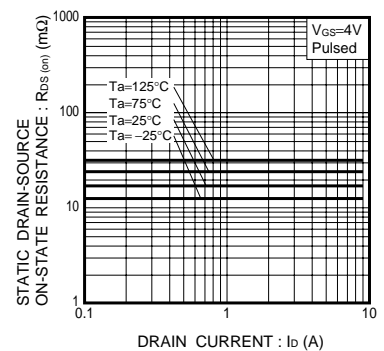


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Transistors

P-ch

●Electrical characteristic curves

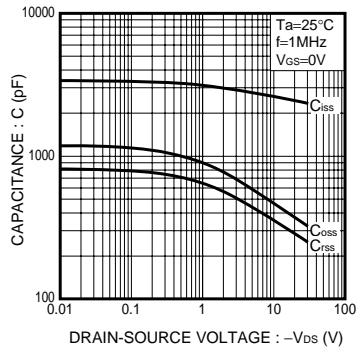


Fig.1 Typical Capacitance vs. Drain-Source Voltage

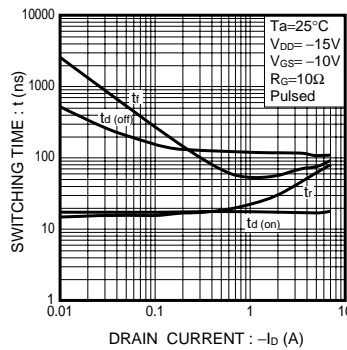


Fig.2 Switching Characteristics

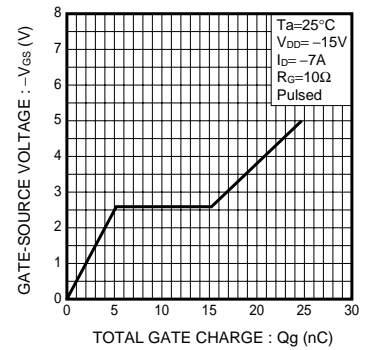


Fig.3 Dynamic Input Characteristics

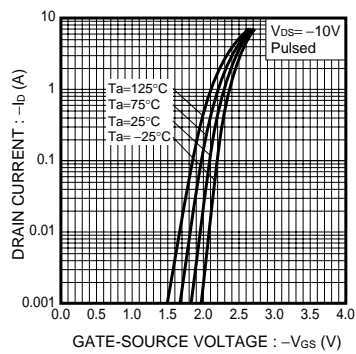


Fig.4 Typical Transfer Characteristics

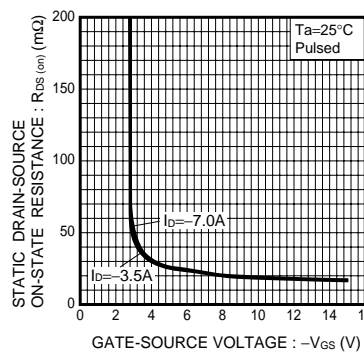


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

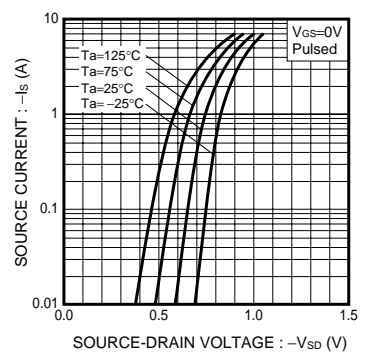


Fig.6 Source Current vs. Source-Drain Voltage

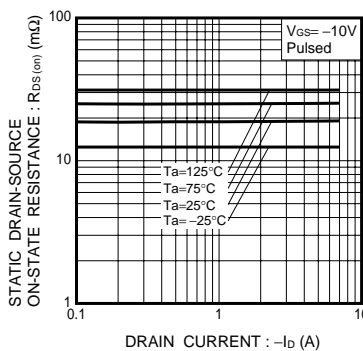


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

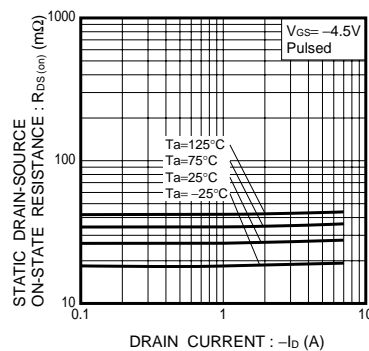


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

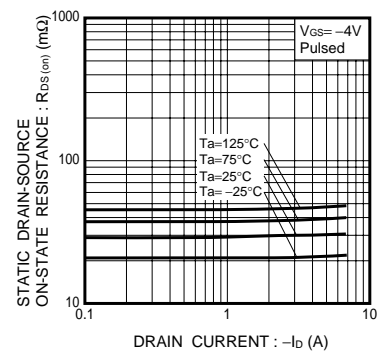


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

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