

4V Drive Nch + Nch MOSFET

TT8K11

Structure

Silicon N-channel MOSFET

Features

- 1) Low on-resistance.
- 2) Low voltage drive(4V drive).
- 3) Small surface mount package(TSST8).

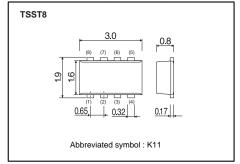
Application

Switching

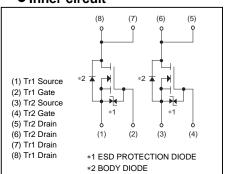
Packaging specifications

	Package	Taping
Type	Code	TCR
	Basic ordering unit (pieces)	3000
TT8K11		0

• Dimensions (Unit : mm)



• Inner circuit



● Absolute maximum ratings (Ta = 25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I _D	±3	А
	Pulsed	I _{DP} *1	±12	Α
Source current (Body Diode)	Continuous	l _s	0.8	Α
	Pulsed	I _{sp} *1	12	Α
Power dissipation		P _D *2	1.25	W / TOTAL
		·Б	1.0	W / ELEMENT
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	-55 to +150	°C

^{*1} Pw≤10µs, Duty cycle≤1%

• Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to Ambient	Rth (ch-a)*	100	°C / W/ TOTAL
	Kill (Cll-a)	125	°C / W/ ELEMENT

^{*}Mounted on a ceramic board.

^{*2} Mounted on a ceramic board.

● Electrical characteristics (Ta = 25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	$V_{GS}=\pm20V$, $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	٧	I _D =1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	1	-	1	μA	V_{DS} =30V, V_{GS} =0V
Gate threshold voltage	V _{GS (th)}	1.0	-	2.5	٧	V_{DS} =10V, I_{D} =1A
		1	51	71		$I_D=3A$, $V_{GS}=10V$
Static drain-source on-state resistance	R _{DS (on)}	1	67	94	mΩ	$I_D = 3A, V_{GS} = 4.5V$
		1	78	109		$I_D=3A$, $V_{GS}=4V$
Forward transfer admittance	IY _{fs} I*	2.0	-	-	S	V_{DS} =10V, I_{D} =3A
Input capacitance	C _{iss}	1	140	-	pF	V _{DS} =10V
Output capacitance	C _{oss}	1	55	-	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	1	28	-	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	-	5	-	ns	V _{DD} ≒15V, I _D =1.5A
Rise time	t _r *	1	13	-	ns	V _{GS} =4.5V
Turn-off delay time	t _{d(off)} *	1	20	-	ns	$R_L=10\Omega$
Fall time	t _f *	1	3	-	ns	$R_G=10\Omega$
Total gate charge	Q _g *	-	2.5	-	nC	V _{DD} ≒15V, I _D =3A
Gate-source charge	Q _{gs} *	-	0.8	-	nC	V _{GS} =5V
Gate-drain charge	Q _{gd} *	-	0.6	-	nC	

^{*}Pulsed

●Body diode characteristics (Source-Drain)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward Voltage	V _{SD} *	-	-	1.2	V	I _s =3A, V _{GS} =0V

^{*}Pulsed

●Electrical characteristic curves (Ta=25°C)

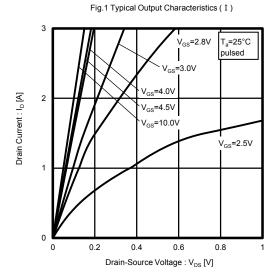


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

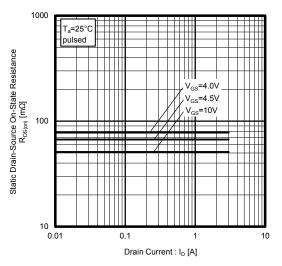


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

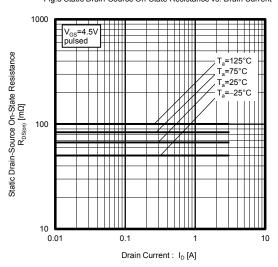


Fig.2 Typical Output Characteristics (II)

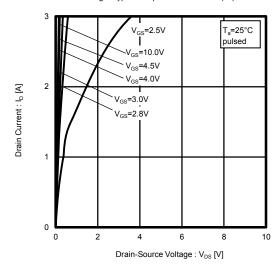


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

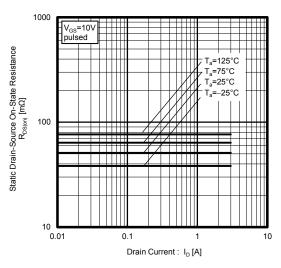


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

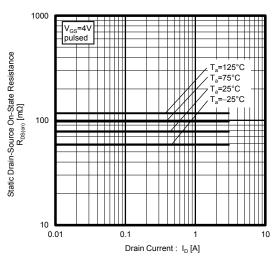


Fig.7 Forward Transfer Admittance vs. Drain Current

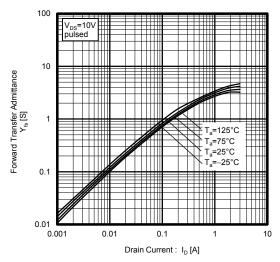


Fig.9 Source Current vs. Source-Drain Voltage

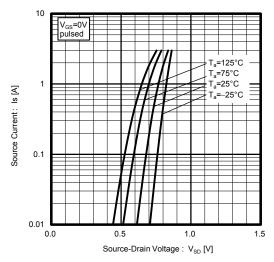


Fig.11 Switching Characteristics

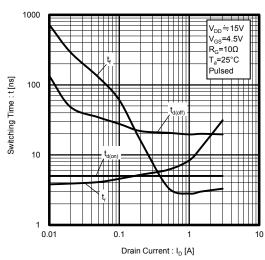


Fig.8 Typical Transfer Characteristics

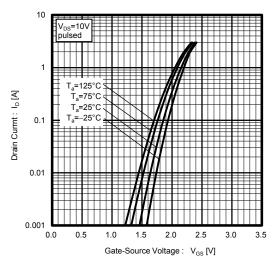


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

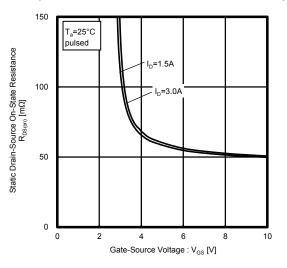


Fig.12 Dynamic Input Characteristics

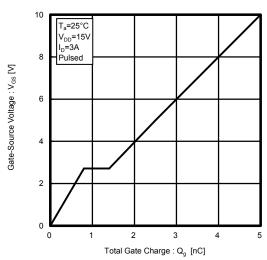


Fig.13 Typical Capacitance vs. Drain-Source Voltage

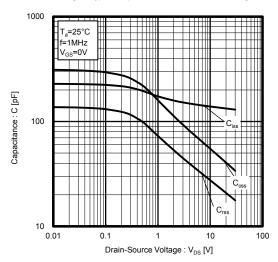


Fig.15 Normalized Transient Thermal Resistance v.s. Pulse Width

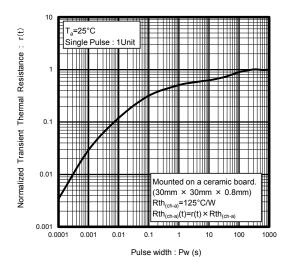
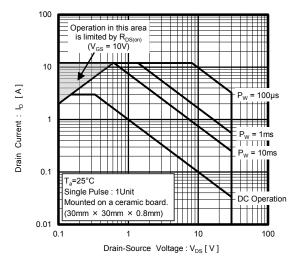


Fig.14 Maximum Safe Operating Area



Measurement circuits

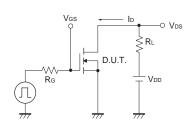


Fig.1-1 Switching Time Measurement Circuit

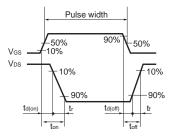


Fig.1-2 Switching Waveforms

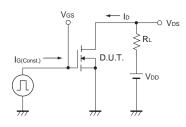


Fig.2-1 Gate Charge Measurement Circuit

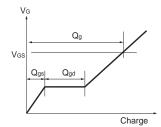


Fig.2-2 Gate Charge Waveform

Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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