

# UT6JE5

## -100V Pch+Pch Power MOSFET

V <sub>DSS</sub>	-100V
R <sub>DS(on)</sub> (Max.)	840mΩ
I <sub>D</sub>	±1.0A
P <sub>D</sub>	2.0W

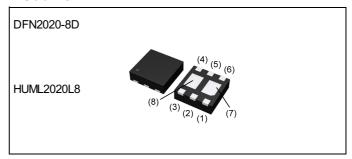
#### Features

- 1) Low on resistance
- 2) Small surface mount package
- 3) Pb-free plating; RoHS compliant
- 4) Halogen Free

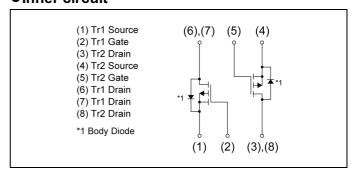
## Application

Switching

## Outline



## ●Inner circuit



## Packaging specifications

	Packing	Embossed Tape
	Reel size (mm)	180
Type	Tape width (mm)	8
	Quantity (pcs)	3000
	Taping code	TCR
	Marking	JE5

## ● **Absolute maximum ratings** (T<sub>a</sub> = 25°C ,unless otherwise specified) < Tr1 and Tr2>

Parameter	Symbol	Value	Unit
Drain - Source voltage	$V_{DSS}$	-100	V
Continuous drain current	I <sub>D</sub>	±1.0	А
Pulsed drain current	I <sub>DP</sub> *1	±4.0	А
Gate - Source voltage	$V_{GSS}$	±20	V
Power dissipation (total)	P <sub>D</sub> *2	2.0	W
Junction temperature	T <sub>j</sub>	150	°C
Operating junction and storage temperature range	T <sub>stg</sub>	-55 to +150	°C

## ●Thermal resistance

Parameter	Symbol	Values			Linit
Parameter	Symbol	Min.	Тур.	Max.	Unit
Thermal resistance, junction - ambient	R <sub>thJA</sub> *2	1	-	62.5	°C/W

## ● Electrical characteristics (T<sub>a</sub> = 25°C) < Tr1 and Tr2>

Davamatav	Cymah ol	Conditions		Values			
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit	
Drain - Source breakdown voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0V, I_D = -1mA$		-	-	V	
Breakdown voltage	ΔV <sub>(BR)DSS</sub>	I <sub>D</sub> = -1mA		-68		mV/°C	
temperature coefficient	ΔT <sub>j</sub>	referenced to 25°C	-	-00	-	IIIV/ C	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -100V, V <sub>GS</sub> = 0V		-	-1	μA	
Gate - Source leakage current	I <sub>GSS</sub>	$V_{DS} = 0V$ , $V_{GS} = \pm 20V$	-	-	±100	nA	
Gate threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -1 \text{mA}$	-1.0	-	-2.5	V	
Gate threshold voltage	$\Delta V_{GS(th)}$	I <sub>D</sub> = -1mA		3.7		V/°C	
temperature coefficient	$\Delta T_{j}$	referenced to 25°C	-	3.1	-	V/C	
Static drain - source	D *3	$V_{GS} = -10V, I_D = -1A$	-	650	840	mΩ	
on - state resistance	R <sub>DS(on)</sub> *3	$V_{GS} = -4.5V, I_D = -1A$	-	690	900	11122	
Gate resistance	$R_{G}$	f=1MHz, open drain	-	15	-	Ω	
Forward Transfer Admittance	Y <sub>fs</sub>  *3	$V_{DS} = -5V, I_{D} = -1A$	1.3	-	-	S	

<sup>\*1</sup> Pw  $\leq$  10µs, Duty cycle  $\leq$  1%

<sup>\*2</sup> Mounted on a Cu board (40×40×0.8mm)

<sup>\*3</sup> Pulsed

## ● Electrical characteristics (T<sub>a</sub> = 25°C) < Tr1 and Tr2>

Daramatar	Cymahal	Conditions	Values			Unit	
Parameter	Symbol Conditions -		Min.	Тур.	Max.	Unit	
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V	-	90	-		
Output capacitance	C <sub>oss</sub>	V <sub>DS</sub> = -50V	-	12	-	pF	
Reverse transfer capacitance	C <sub>rss</sub>	f = 1MHz	-	11	-		
Turn - on delay time	t <sub>d(on)</sub> *3	$V_{DD} \simeq -50V, V_{GS} = -10V$	-	6.3	-		
Rise time	t <sub>r</sub> *3	I <sub>D</sub> = -0.5A	-	5.4	-		
Turn - off delay time	t <sub>d(off)</sub> *3	R <sub>L</sub> = 100Ω	-	31.0	-	ns	
Fall time	t <sub>f</sub> *3	$R_G = 10\Omega$	-	25.0	-		

# ● Gate charge characteristics (T<sub>a</sub> = 25°C) < Tr1 and Tr2>

Darameter	Cumbal	Conditions -		Values			1 1:4
Parameter	Symbol			Min.	Тур.	Max.	Unit
Total mate above	O *3		V <sub>GS</sub> = -10V	-	6.7	-	
Total gate charge	$Q_g^{*3}$	V <sub>DD</sub> ≃ -50V I <sub>D</sub> = -1A		-	3.7	-	0
Gate - Source charge	Q <sub>gs</sub> *3		V <sub>GS</sub> = -4.5V	-	1.2	-	nC
Gate - Drain charge	Q <sub>gd</sub> *3			-	1.5	-	

## ● Body diode electrical characteristics (Source-Drain) (T<sub>a</sub> = 25°C)

## <Tr1 and Tr2>

Parameter	Symbol	Conditions	Values			Unit	
Farameter	Symbol	Conditions	Min.	Тур.	Max.	Offic	
Continuous forward current	I <sub>S</sub>	T <sub>a</sub> = 25°C	-	-	-1.67	^	
Pulse forward current	I <sub>SP</sub> *1	1 <sub>a</sub> – 25 C	-	-	-4.0	A	
Forward voltage	V <sub>SD</sub> *3	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1.67A	-	-	-1.2	V	
Reverse recovery time	t <sub>rr</sub> *3	I <sub>S</sub> = -1A, V <sub>GS</sub> = 0V	-	22	-	ns	
Reverse recovery charge	Q <sub>rr</sub> *3	di/dt = 100A/μs	-	53	-	nC	

Fig.1 Power Dissipation Derating Curve

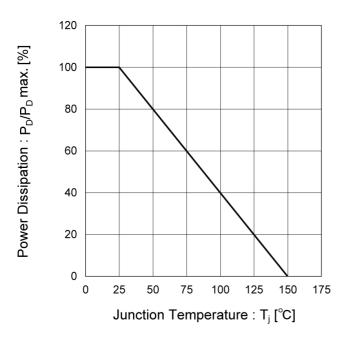
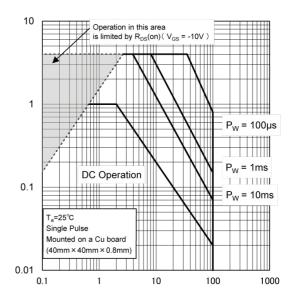


Fig.2 Maximum Safe Operating Area



Drain Current : -l<sub>D</sub> [A]

Drain - Source Voltage : -V<sub>DS</sub> [V]

Fig.3 Normalized Transient Thermal Resistance vs. Pulse Width

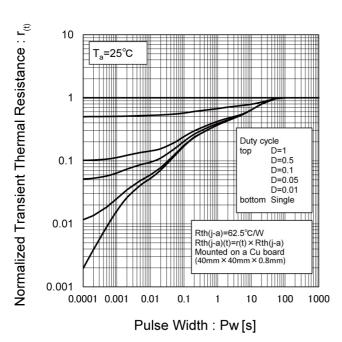


Fig.4 Single Pulse Maximum Power Dissipation

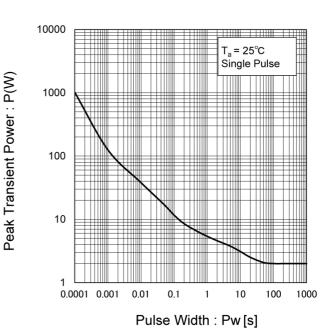


Fig.5 Typical Output Characteristics(I)

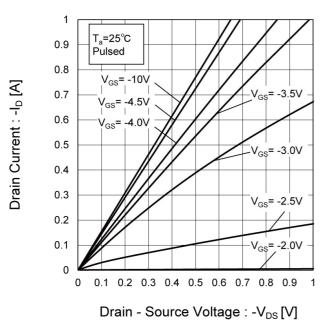


Fig.6 Typical Output Characteristics(II)

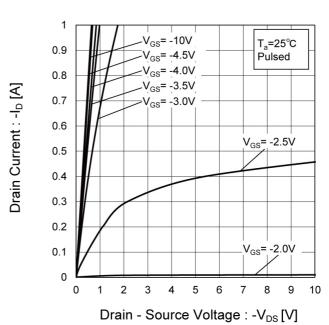


Fig.7 Normalized Breakdown Voltage vs. Junction Temperature

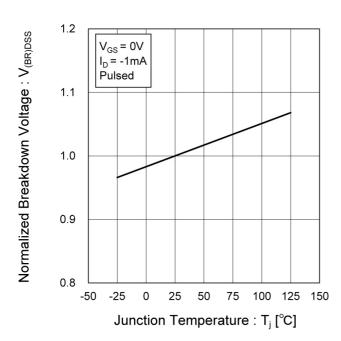


Fig.8 Typical Transfer Characteristics

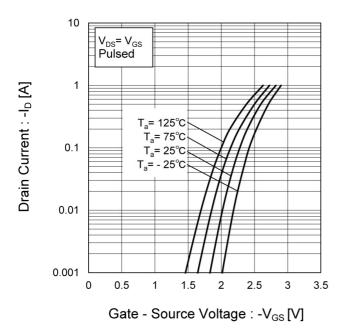


Fig.9 Gate Threshold Voltage vs.
Junction Temperature



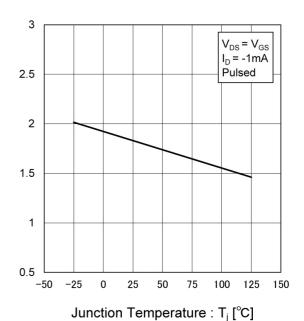


Fig.10 Forward Transfer Admittance vs.
Drain Current

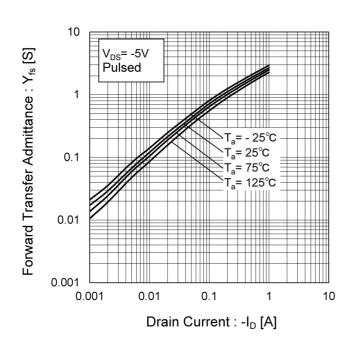


Fig.11 Drain Current Derating Curve

120 100 **Drain Current Dissipation** 80 : I<sub>D</sub>/I<sub>D</sub>max. [%] 60 40 20 0 -25 0 25 50 75 100 125 150 Junction Temperature : T<sub>j</sub> [°C]

Fig.12 Static Drain - Source On - State Resistance vs. Gate Source Voltage

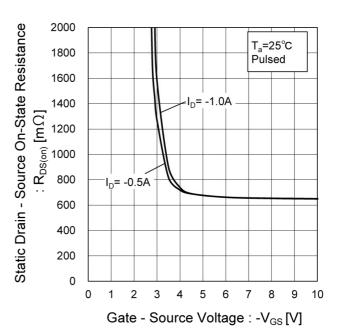
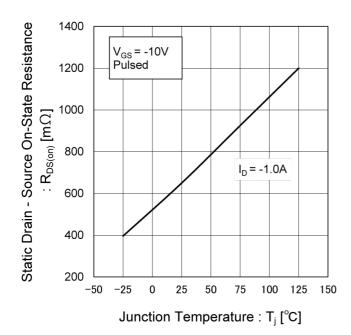


Fig.13 Static Drain - Source On - State Resistance vs. Junction Temperature



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Fig.14 Static Drain - Source On - State
Resistance vs. Drain Current (I)

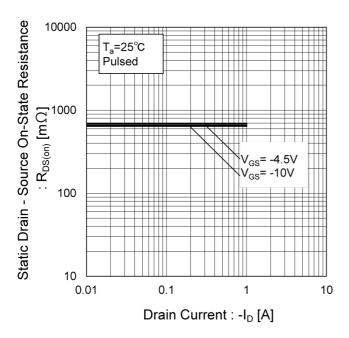


Fig.15 Static Drain - Source On - State Resistance vs. Drain Current (II)

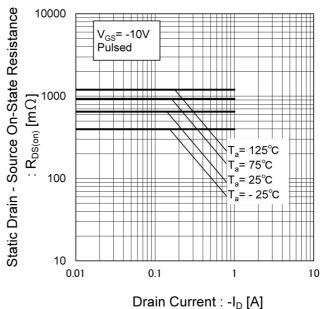


Fig.16 Static Drain - Source On - State Resistance vs. Drain Current (III)

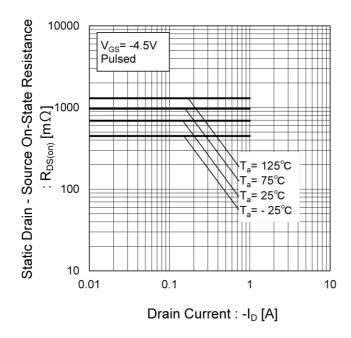


Fig.17 Typical Capacitances vs.

Drain - Source Voltage

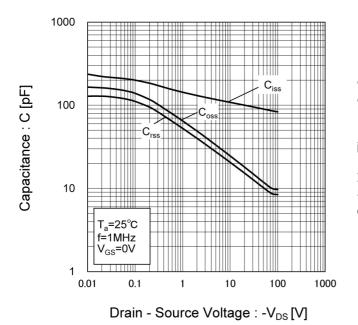


Fig.18 Switching Characteristics

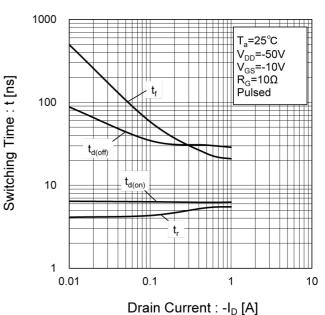


Fig.19 Typical Gate Charge

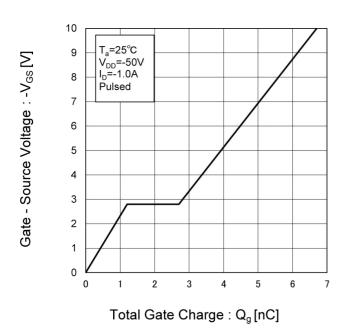
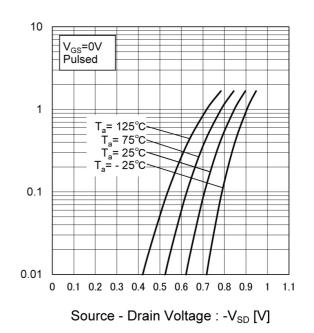


Fig.20 Source Current vs.
Source Drain Voltage



Source Current : -I<sub>s</sub> [A]

## • Measurement circuits < It is the same for the Tr1 and Tr2>

Fig.1-1 Switching Time Measurement Circuit

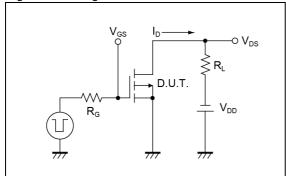


Fig.2-1 Gate Charge Measurement Circuit

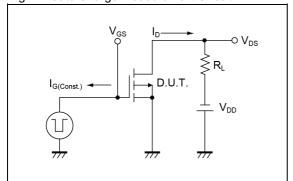


Fig.1-2 Switching Waveforms

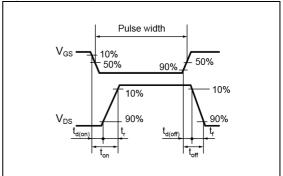
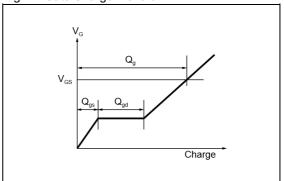


Fig.2-2 Gate Charge Waveform

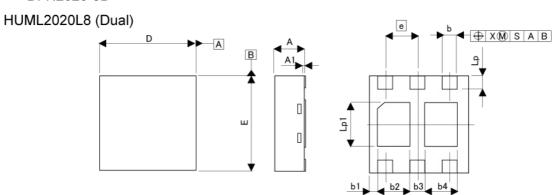


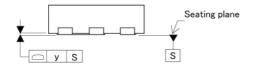
## Notice

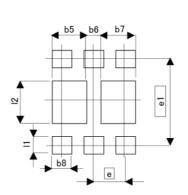
This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

## Dimensions

#### DFN2020-8D







Pattern of terminal position areas [Not a pattern of soldering pads]

DIM	MILIME	TERS	INC	HES
DIIVI	MIN	MAX	MIN	MAX
Α	0.55	0.65	0.022	0.026
A1	0.00	0.05	0.000	0.002
b	0.25	0.35	0.010	0.014
b1	0.	25	0.0	)10
b2	0.60	0.70	0.024	0.028
b3	0	.3	0.0	)12
b4	0.60	0.70	0.024	0.028
D	1.90	2.10	0.075	0.083
E	1.90	2.10	0.075	0.083
е	0.	65	0.0	)26
Lp	0.225	0.325	0.009	0.013
Lp1	0.80	1.00	0.031	0.039
х	-	0.10	-	0.004
у	-	0.10	»-	0.004

DIM	MILIME	TERS	INCHES	
DIIVI	MIN	MAX	MIN	MAX
b5	-	0.70	( <b>-</b>	0.028
b6	0.20	0.30	0.008	0.012
b7	-	0.70	(-	0.028
b8	-	0.45	-	0.018
e1	1.7	725	0.0	)68
I1	-	0.425	1.5	0.017
12	-	1.00	1-	0.039

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Dimension in mm/inches



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  - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
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- 4. The Products are not subject to radiation-proof design.
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- 7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
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  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
- Even under ROHM recommended storage condition, solderability of products out of recommended storage time period
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  exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
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EVK-001 RB-D62Q1722GA64 RB-D62Q1747TB100