

Thyristor Surge Suppressors

P0060~P3500SA_B_C Serie

Description

P0060~P3500SA_B_C Series are low capacitance devices designed to protect broadband equipment such as VOIP, DSL modems and DSLAMs from damaging overvoltage transients.

The series provides a surface mount solution that enables equipment to comply with global regulatory standards while limiting the impact to broadband signals.



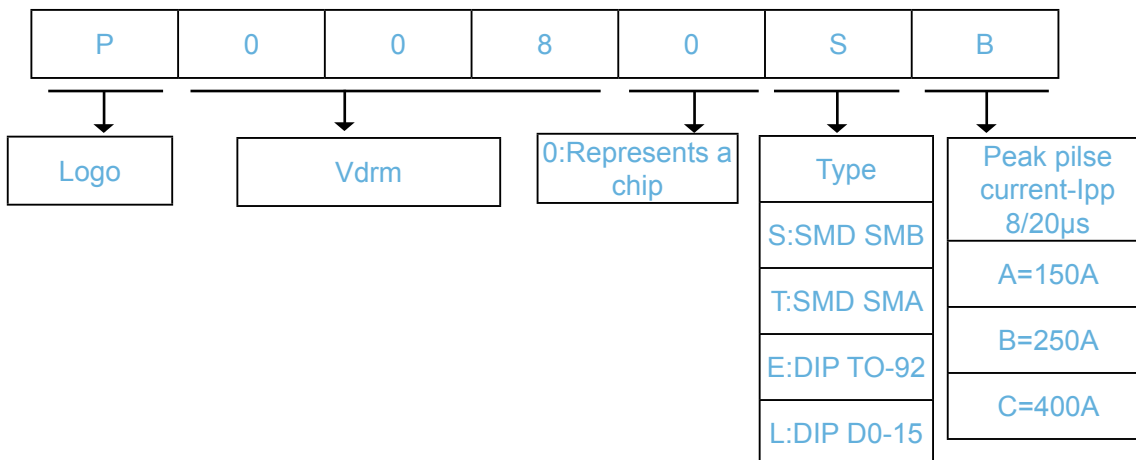
Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade with use
- Fails short circuit when surged in excess of ratings
- Low Capacitance

Applicable Global Standards

- TIA-968-A
- ITU K.20/21 Enhanced level*
- ITU K.20/21 Basic Level
- GR 1089 Inter building*
- GR 1089 Inter building
- IEC 6100-4-5
- YD/T 1082
- YD/T 993
- YD/T 950

Product Name



Electrical Characteristics (@ TA = 25 °C Unless Otherwise Noted)

Type Number	V _{DRM}	I _{DRM}	V _{BO}	I _H	I _S	I _T	V _T	C _J		Package Dimensions inch(mm)
	V	μA	V	MA	MA	A	V	pF _{Min}	pF _{Max}	
P0080SA	6	5	25	50	800	2.2	4	25	150	<p style="text-align: center;">SMB/DO-214AA</p>
P0080SB	6	5	25	50	800	2.2	4	25	150	
P0080SC	6	5	25	50	800	2.2	4	35	260	
P0300SA	25	5	40	50	800	2.2	4	15	140	
P0300SB	25	5	40	50	800	2.2	4	15	140	
P0300SC	25	5	40	50	800	2.2	4	25	250	
P0640SA	58	5	77	150	800	2.2	4	40	60	
P0640SB	58	5	77	150	800	2.2	4	40	60	
P0640SC	58	5	77	150	800	2.2	4	55	155	
P0720SA	65	5	88	150	800	2.2	4	35	60	
P0720SB	65	5	88	150	800	2.2	4	35	75	
P0720SC	65	5	88	150	800	2.2	4	50	150	
P0900SA	75	5	98	150	800	2.2	4	35	55	
P0900SB	75	5	98	150	800	2.2	4	35	70	
P0900SC	75	5	98	150	800	2.2	4	45	140	
P1100SA	90	5	130	150	800	2.2	4	30	50	
P1100SB	90	5	130	150	800	2.2	4	30	70	
P1100SC	90	5	130	150	800	2.2	4	45	115	
P1300SA	120	5	160	150	800	2.2	4	25	45	
P1300SB	120	5	160	150	800	2.2	4	25	60	
P1300SC	120	5	160	150	800	2.2	4	40	105	
P1500SA	140	5	180	150	800	2.2	4	25	40	
P1500SB	140	5	180	150	800	2.2	4	25	55	
P1500SC	140	5	180	150	800	2.2	4	35	95	
P1800SA	170	5	220	150	800	2.2	4	25	35	
P1800SB	170	5	220	150	800	2.2	4	25	50	
P1800SC	170	5	220	150	800	2.2	4	35	90	
P2300SA	190	5	260	150	800	2.2	4	25	35	
P2300SB	190	5	260	150	800	2.2	4	25	50	
P2300SC	190	5	260	150	800	2.2	4	30	80	
P2600SA	220	5	300	150	800	2.2	4	20	35	
P2600SB	220	5	300	150	800	2.2	4	20	45	
P2600SC	220	5	300	150	800	2.2	4	30	80	
P3100SA	275	5	350	150	800	2.2	4	20	35	
P3100SB	275	5	350	150	800	2.2	4	20	45	
P3100SC	275	5	350	150	800	2.2	4	30	70	
P3500SA	320	5	400	150	800	2.2	4	20	35	
P3500SB	320	5	400	150	800	2.2	4	20	40	
P3500SC	320	5	400	150	800	2.2	4	25	65	

Notes:
 - Absolute maximum ratings measured at TA= 25°C (unless otherwise noted).
 - Devices are bi-directional.

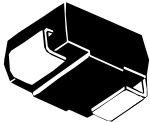
SERIES	Peak Pulse Current-I _{pp} (A)				
	2/10μs	8/20μs	10/160μs	10/560μs	10/1000μs
A	200	150	100	60	50
B	250	250	150	100	80
C	500	400	200	120	100

Surge Ratings

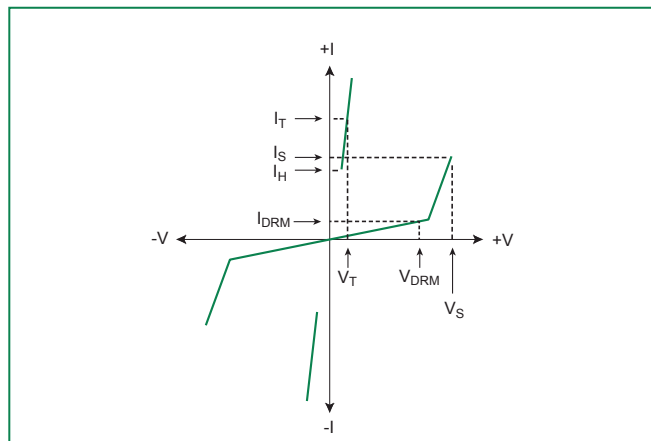
Series	I_{PP}					I_{TSM} 50/60 Hz	di/dt
	2x10 μs	8x20 μs	10x160 μs	10x560 μs	10x1000 μs		
	A min	A min	A min	A min	A min	A min	A/ μs max
A	150	150	90	50	45	20	500
B	250	250	150	100	80	30	500
C	500	400	200	150	100	50	500

Notes:
 1 Current waveform in μs - Peak pulse current rating (I_{pp}) is repetitive and guaranteed for the life of the product.
 2 Voltage waveform in μs - I_{pp} ratings applicable over temperature range of $-40^{\circ}C$ to $+85^{\circ}C$
 - The device must initially be in thermal equilibrium with $-40^{\circ}C \leq T_J \leq +150^{\circ}C$

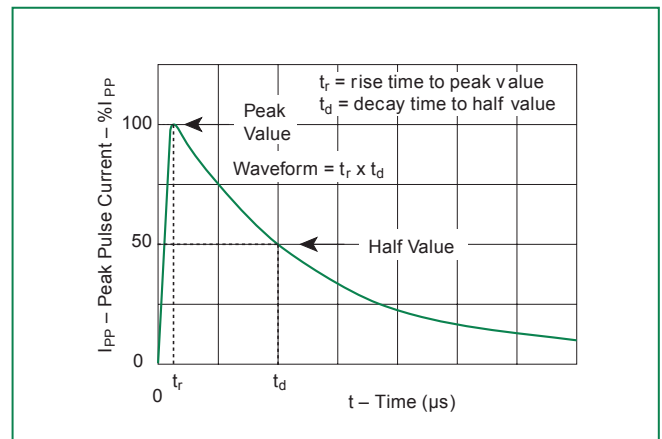
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
 DO-214AA	T_J	Operating Junction Temperature Range	-40 to +150	$^{\circ}C$
	T_S	Storage Temperature Range	-65 to +150	$^{\circ}C$
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	$^{\circ}C/W$

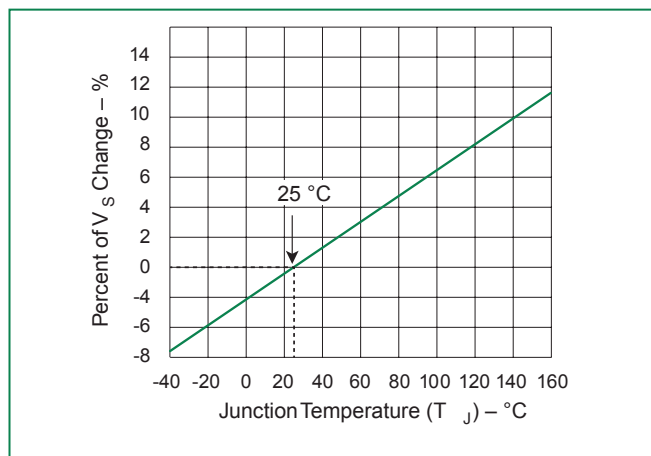
V-I Characteristics



$t_r \times t_d$ Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

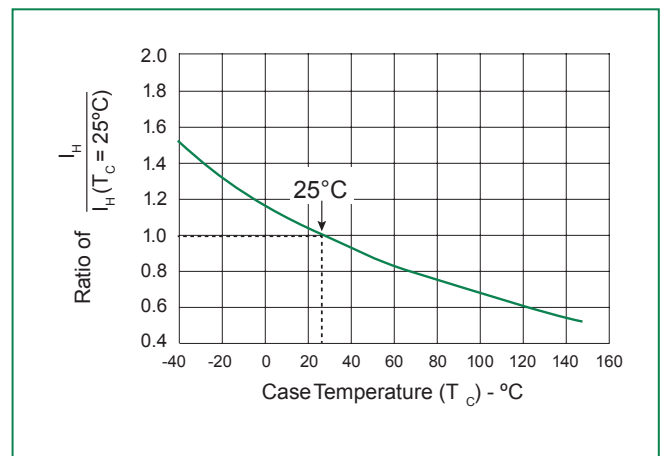
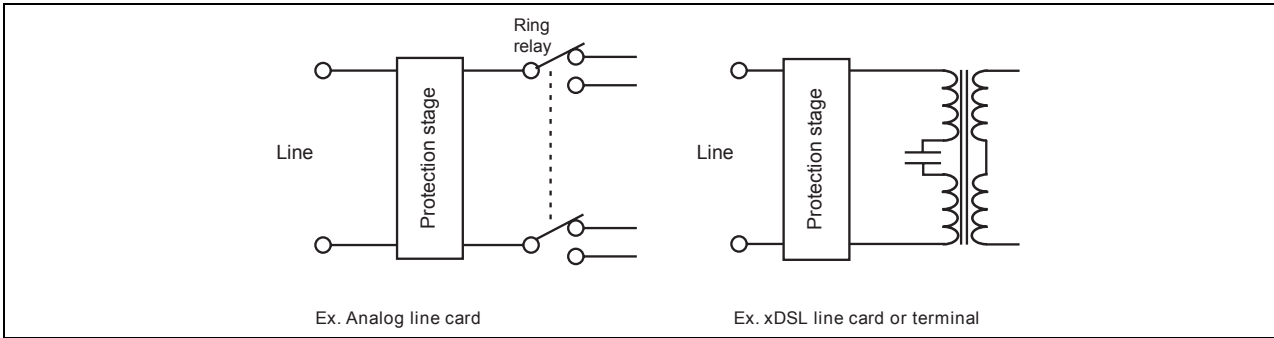


Figure 1.E examples of protection stages for line cards



In such a stage, parallel function is assumed by one or several Trisil, and is used to protect against short duration surge (lightning). During this kind of surges the Trisil limits the voltage across the device to be protected at its break over value and then fires. The fuse assumes the series function, and is used to protect the module against long duration or very high current mains disturbances (50/60Hz). It acts by safe circuit opening. Lightning surge and mains disturbance surges are defined by standards like GR1089, FCC part 68, ITU-T K20.

Figure 2. Typical circuits

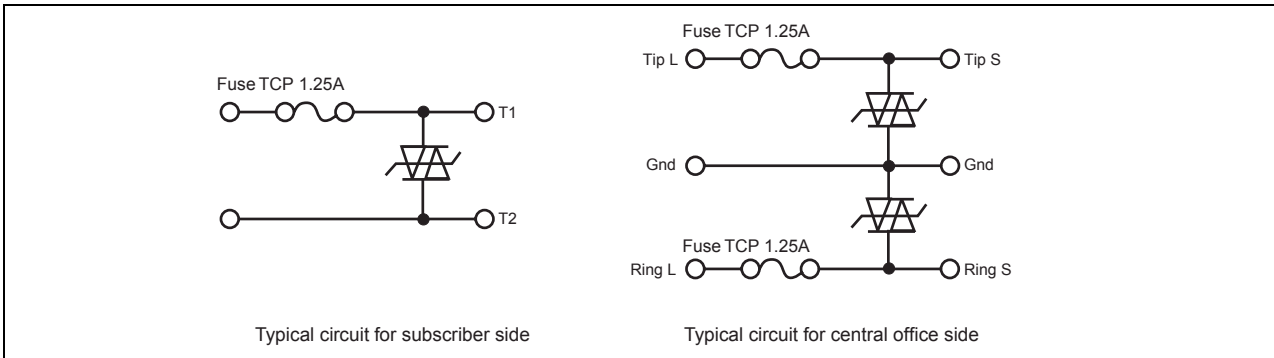


Figure 3.T test circuit 1 for Dynamic I_{BO} and V_{BO} parameters

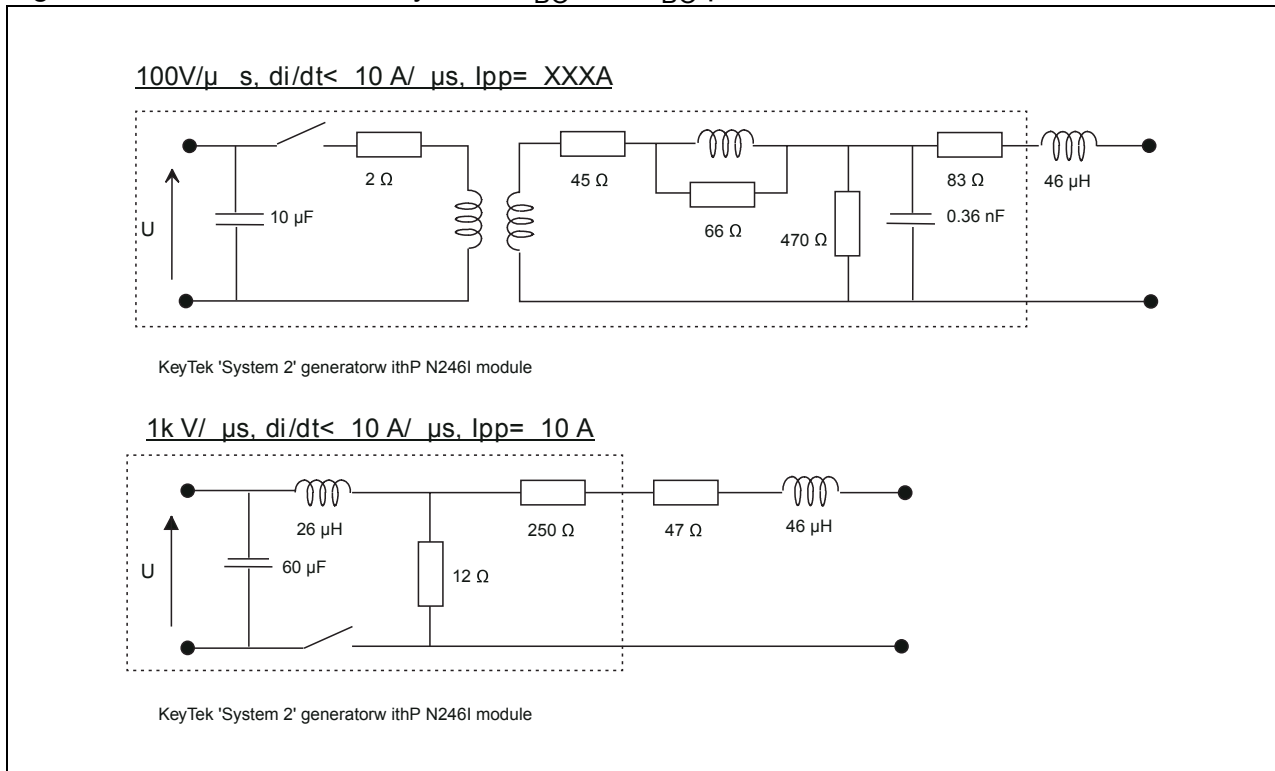


Figure 5. Test circuit 3 for dynamic I_H parameter

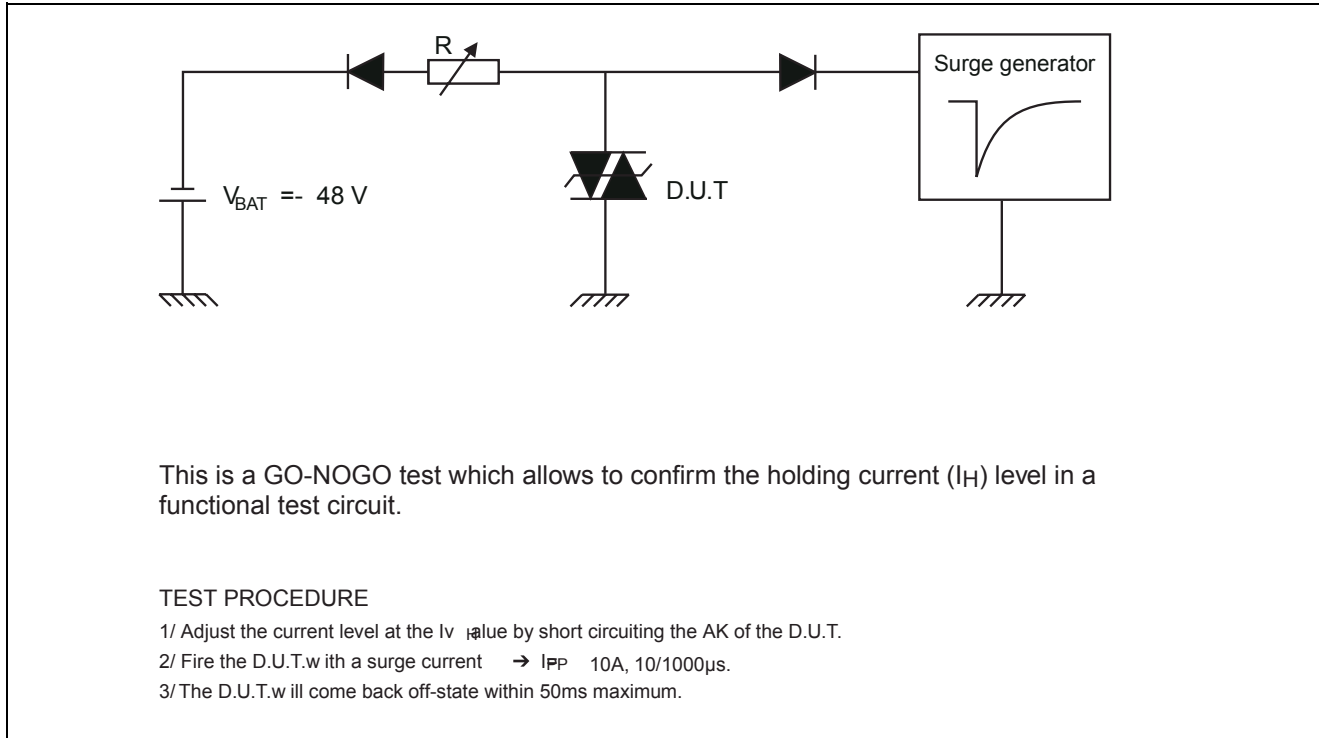
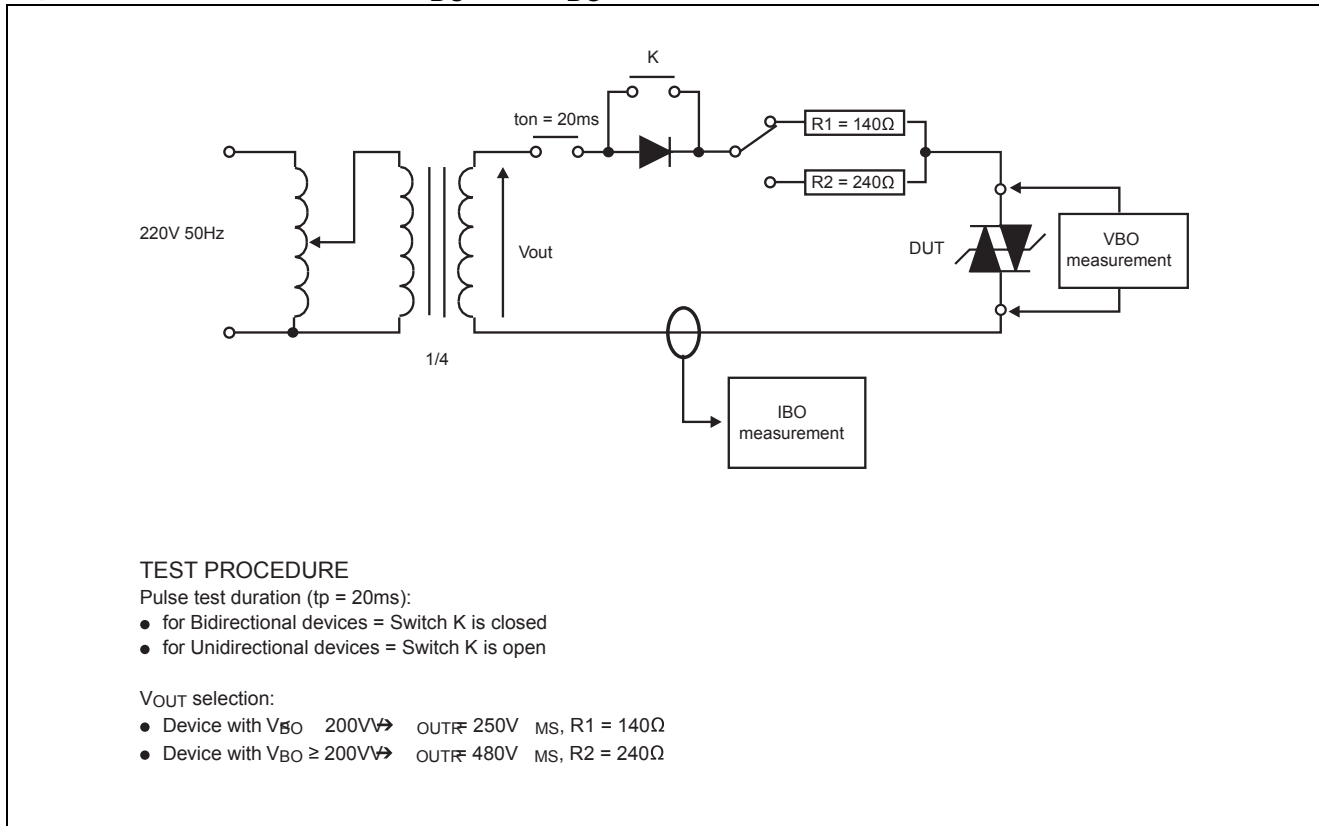
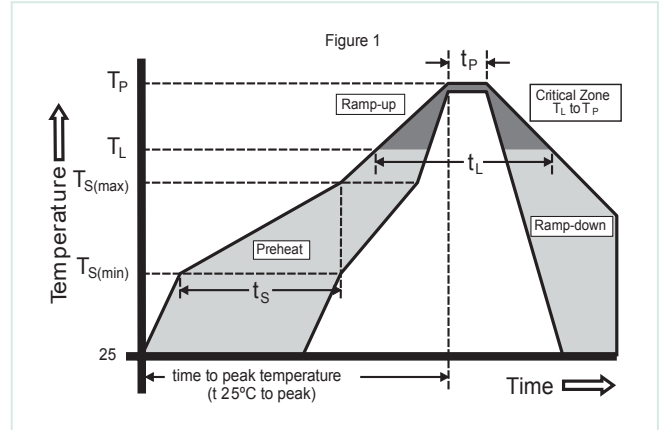


Figure 4. Test circuit 2 for I_{BO} and V_{BO} parameters



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	- Temperature Min ($T_{s(min)}$)	+150°C
	- Temperature Max ($T_{s(max)}$)	+200°C
	- Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	- Temperature (T_L) (Liquidus)	+217°C
	- Temperature (t_L)	60-150 secs.
Peak Temp (T_p)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_p)		8 min. Max.
Do not exceed		+260°C



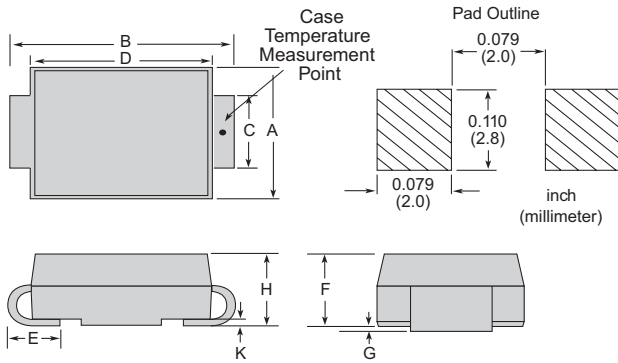
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification 94V-0

Environmental Specifications

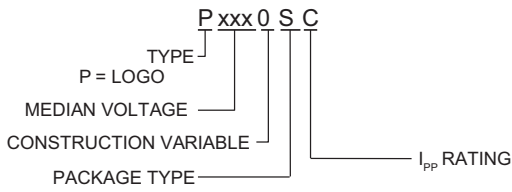
High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Dimensions — DO-214AA

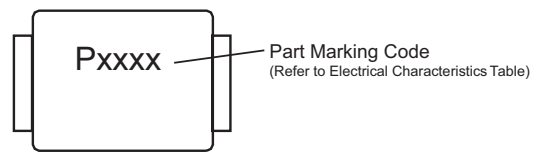


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.130	0.156	3.30	3.95
B	0.201	0.220	5.10	5.60
C	0.077	0.087	1.95	2.20
D	0.159	0.181	4.05	4.60
E	0.030	0.063	0.75	1.60
F	0.075	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.077	0.104	1.95	2.65
K	0.006	0.016	0.15	0.41

Part Numbering



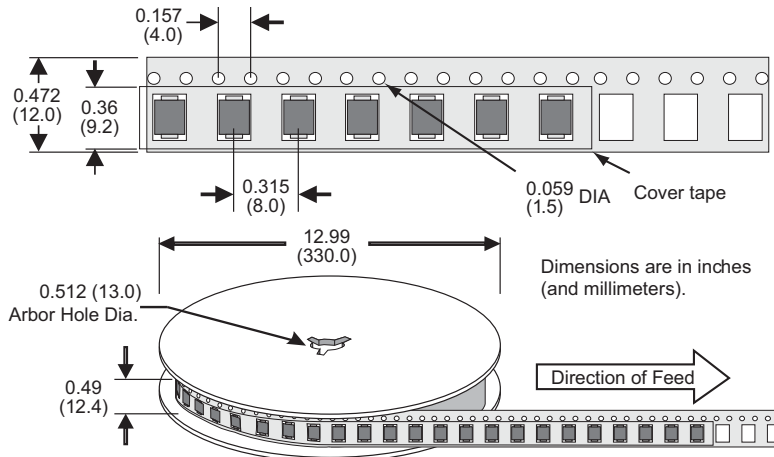
Part Marking



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
S	DO-214AA Tape & Reel Pack	2500	N/A	EIA-481-D

Tape and Reel Specification — DO-214AA



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